Modelling, characterisation and application of GaN switching devices

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Symbol	Meaning
A	Area
A_c	Transformer core cross section area
ACR	Inductor alternating current resistance
B	Magnetic flux density
BW	Bandwidth
c	Speed of light in free space
C_A	Converter output capacitance of any leading leg switch
C_{A1}	Transistor T_{A1} output capacitance
C_{A2}	Transistor T_{A2} output capacitance
C_B	Converter output capacitance of any lagging leg switch
C_{B1}	Transistor T_{B1} output capacitance
C_{B2}	Transistor T_{B2} output capacitance
C_D	Diode capacitance
$C_{DS\text{-}GaN}$	GaN HEMT drain to source capacitance
$C_{DS\text{-}Si}$	Si MOSFET drain to source capacitance
$C_{DS\text{-}Si(TR)}$	Time related Si MOSFET drain to source capacitance
$C_{GD\text{-}GaN}$	GaN HEMT gate to drain capacitance
$C_{GD\text{-}Si}$	Si MOSFET gate to drain capacitance
$C_{GD\text{-}Si(TR)}$	Si MOSFET time related gate to drain capacitance
$C_{GS\text{-}GaN}$	GaN HEMT gate to source capacitance
$C_{GS\text{-}Si}$	Si MOSFET gate to source capacitance
$C_{iss\text{-}Si}$	Si MOSFET input capacitance
C_o	Converter output filter capacitance

C_{oss}	Transistor output capacitance at a particular drain to source voltage
$C_{oss(TR)}$	Time related transistor output capacitance
$C_{oss\text{-}GaN}$	GaN HEMT output capacitance
$C_{oss\text{-}Si}$	Si MOSFET output capacitance
C_{rect}	Rectifier diode capacitance at a specific reverse voltage
$C_{(TR)}$	Time related capacitance
DCR	Inductor direct current resistance
D_{IL}	Diode induced switching loss
$E_{D\text{-}GaN}$	Energy dissipated in the channel of the GaN HEMT
$E_{D\text{-}Si}$	Energy dissipated in the channel of the Si MOSFET
E_{ff}	Efficiency
E_{off}	Transistor switching energy loss during turn-off
$E_{off\text{-}3}$	Energy loss during turn-off stage 3
E_{on}	Transistor switching energy loss during turn-on
$E_{on\text{-}2}$	Energy loss during turn-on stage 2
$E_{on\text{-}3}$	Energy loss during turn-on stage 3
$E_{on\text{-}4}$	Energy loss during turn-on stage 4.
ESR	Capacitor equivalent series resistor
$E_{S\text{-}GaN}$	Energy stored in the output capacitance of the GaN HEMT
$E_{S\text{-}Si}$	Energy stored in the output capacitance of the Si MOSFET
E_T	Transistor total switching energy loss
f	Small signal evaluation frequency
f_s	Switching frequency
g	Transistor transconductance
$g_{m\text{-}GaN}$	GaN HEMT transconductance
$g_{m\text{-}Si}$	Si MOSFET transconductance

$i_{cascode}(t)$	Instantaneous cascode device current that can be measured
i_{CA1}	Capacitor C_{A1} current
i_{CA2}	Capacitor C_{A2} current
$i_{CDmax\text{-}off}$	Maximum diode reverse current during turn-off
$i_{CDmax\text{-}on}$	Maximum diode reverse current during turn-on
$i_{CDS\text{-}GaN}(t)$	Instantaneous GaN HEMT drain to source capacitance current
$i_{CDS\text{-}Si}(t)$	Instantaneous Si MOSFET drain to source capacitance current
$i_{CD}(t)$	Instantaneous diode capacitance reverse current
$i_{CGD\text{-}GaN}(t)$	Instantaneous GaN HEMT gate to drain capacitance current
$i_{CGD\text{-}Si}(t)$	Instantaneous Si MOSFET gate to drain capacitance current
$i_{CGS\text{-}Si}(t)$	Instantaneous Si MOSFET gate to source capacitance current
i_{Dmax}	Switch maximum drain current
$i_D(t)$	Instantaneous switch drain current
$i_{D\text{-}GaNmax}$	Maximum GaN HEMT channel current
$i_{D\text{-}GaN}(t)$	Instantaneous GaN HEMT channel current
$i_{D\text{-}Simax}$	Maximum Si MOSFET channel current
$i_{D\text{-}Si}(t)$	Instantaneous Si MOSFET channel current
$i_G(t)$	Instantaneous gate current
i_{LO}	Instantaneous converter output filter inductor current
$i_{S\text{-}Si}$	Si MOSFET source current
$I_{D\text{-}ON}$	Transistor on-state current
I_F	Diode forward current
I_i	Converter input current
I_L	Double pulse tester evaluation current
I_{LO}	Output inductor current at the overlap instant

I_{mag}	Transformer magnetising current
I_o	Average value or DC component of a converter output voltage
I_p	Transformer primary current
I_{prim}	Output current reflected to the primary winding
I_R	Transistor reverse conduction current
I_{SEC}	Secondary winding current
I_{ss}	Current switching speed
k	Steinmetz equation constant
l	Length
L_D	Cascode device drain parasitic inductance
L_G	Cascode device gate parasitic inductance
L_{int1}	Cascode device parasitic inductance common to the GaN HEMT and the Si MOSFET power loops
L_{int2}	Cascode device GaN HEMT gate parasitic inductance
L_{int3}	Cascode device parasitic inductance common to the GaN power loop and the Si MOSFET control and power loops
L_k	Transformer primary leakage inductance
L_o	Converter output filter inductance
$L_{powerloop}$	Power loop inductance
L_{prim}	Transformer primary self-inductance
L_S	Cascode device common source parasitic inductance
N	Transformer turns ratio, 1:N
N_P	Number of turns of the transformer primary winding
p_{off}	Instantaneous power during turn-off
p_{on}	Instantaneous power during turn-on
P_c	Output filter capacitor power dissipation
P_{clamp}	Clamp circuit power dissipation

P_{cv}	Transformer core loss per volume unit
P_{Diode}	Rectifier diode conduction power loss
$P_{Diode\text{-}SW}$	Rectifier diodes switching loss
P_{driver}	Transistor driver power loss
P_i	Converter input power
P_L	Filter inductor power loss
P_o	Converter output power
P_{QC}	Transistor conduction power loss
P_T	Converter total power loss
P_{TC}	Transformer core power loss
Q	Inductor quality factor
Q_{GD}	Transistor gate to drain charge
Q_{rr}	Diode reverse recovery charge
R_{AC}	Windings' AC resistance
R_{clamp}	Clamp circuit resistance
R_{DC}	Transformer windings' DC resistance
$R_{DS\text{-}ON}$	Transistor on-state resistance
R_G	Gate resistor
R_L	Load resistance
t_{PD}	Propagation delay time
t_r	Rise time
$t_{1\text{-}OFF}$	$S_{1\text{-}OFF}$ end time
$t_{1\text{-}ON}$	$S_{1\text{-}ON}$ end time
$t_{2\text{-}OFF}$	$S_{2\text{-}OFF}$ end time
$t_{2\text{-}ON}$	$S_{2\text{-}ON}$ end time
$t_{3\text{-}OFF}$	$S_{3\text{-}OFF}$ end time
$t_{3\text{-}ON}$	$S_{3\text{-}ON}$ end time

T	Switching period
T_D	Dead time
T_j	Junction temperature
T_{OL}	Overlap period
T_{res}	Duration of the resonant transition in the converter leading leg
v_{A2}	Bottom side leading leg transistor drain to source voltage
v_{B2}	Bottom side lagging leg transistor drain to source voltage
$v_{DS}(t)$	Switch drain to source voltage
$v_{DS\text{-}cascode}(t)$	Instantaneous cascode device drain to source voltage that can be measured
$v_{DS\text{-}GaN}(t)$	Instantaneous GaN HEMT drain to source voltage
$v_{DS\text{-}GaN}\ (t_{3\text{-}OFF})$	GaN HEMT drain-source voltage at the end of $S_{3\text{-}OFF}$
$v_{DS\text{-}Simax}$	Maximum Si MOSFET drain to source voltage
$v_{DS\text{-}Si}(t)$	Instantaneous Si MOSFET drain to source voltage
$v_{DS\text{-}Si}\ (t_{2\text{-}OFF})$	Si MOSFET drain to source voltage at the end of $S_{2\text{-}OFF}$
$v_{DS\text{-}Si}\ (t_{2\text{-}ON})$	Si MOSFET drain to source voltage at the end of $S_{2\text{-}ON}$
$v_{DS\text{-}Si}\ (t_{3\text{-}OFF})$	Si MOSFET drain to source voltage at the end of $S_{3\text{-}OFF}$
$v_{DS\text{-}Si}\ (t_{3\text{-}ON})$	Si MOSFET drain to source voltage at the end of $S_{3\text{-}ON}$
$v_D(t)$	Instantaneous diode reverse voltage
v_F	Velocity factor
$v_{GD\text{-}GaN}(t)$	Instantaneous GaN HEMT gate to drain voltage
$v_{GD\text{-}Si}(t)$	Instantaneous Si MOSFET gate to drain voltage
$v_{GSH}(t)$	Top side switch gate to source voltage
$v_{GSL}(t)$	Bottom side switch gate to source voltage
$v_{GS}(t)$	Switch gate to source voltage
$v_{GS\text{-}GaN}\ (t)$	Instantaneous GaN HEMT gate to source voltage
$v_{GS\text{-}Si}\ (t)$	Instantaneous Si MOSFET gate to source voltage

$v_{GS\text{-}Si}\,(t_{1\text{-}OFF})$	Si MOSFET gate to source voltage at the end of $S_{1\text{-}OFF}$
$v_{GS\text{-}Si}\,(t_{1\text{-}ON})$	Si MOSFET gate to source voltage at the end of $S_{1\text{-}ON}$
$v_{GS\text{-}Si}\,(t_{2\text{-}OFF})$	Si MOSFET gate to source voltage at the end of $S_{2\text{-}OFF}$
$v_{GS\text{-}Si}\,(t_{2\text{-}ON})$	Si MOSFET gate to source voltage at the end of $S_{2\text{-}ON}$
$v_{GS\text{-}Si}\,(t_{3\text{-}OFF})$	Si MOSFET gate to source voltage at the end of $S_{3\text{-}OFF}$
$v_{GS\text{-}Si}\,(t_{3\text{-}ON})$	Si MOSFET gate to source voltage at the end of $S_{3\text{-}ON}$
v_{Lk}	Leakage inductance voltage drop
V_A	Bottom side leading leg transistor drain to source voltage
V_{AB}	Difference between v_{A2} and v_{B2} or between V_A and V_B
V_B	Bottom side lagging leg transistor drain to source voltage
V_{clamp}	Clamp circuit voltage
V_{DD}	Gate driver positive voltage
$V_{DS\text{-}GaN}(s)$	GaN HEMT drain to source voltage in the Laplace domain
$V_{DS\text{-}OFF}$	Transistor off-state voltage
$V_{DS\text{-}Si}(s)$	Si MOSFET drain to source voltage in the Laplace domain
V_F	Diode forward voltage
$V_{GS\text{-}Si}\,(s)$	Si MOSFET gate to source voltage in the Laplace domain
V_i	Average value or DC component of a converter or test circuit input voltage
V_{LS}	Voltage drop due to circuit stray inductance
V_o	Average value or DC component of a converter output voltage
V_R	Diode reverse voltage
V_{rect}	Rectifier voltage
V_{SEC}	Secondary winding voltage
$V_{TH\text{-}GaN}$	Threshold voltage of the GaN HEMT in a cascode device
$V_{TH\text{-}Si}$	Threshold voltage of the Si MOSFET in a cascode device
$Z_{DS\text{-}Si}$	Si MOSFET drain to source impedance

$Z_{GD\text{-}Si}$	Si MOSFET gate to drain impedance
$Z_{GS\text{-}Si}$	Si MOSFET gate to source impedance
α	Steinmetz equation constant
β	Steinmetz equation constant
δ	Shift delay control variable
ΔI_{Lo}	Output inductor ripple current
ΔV_o	Output voltage ripple
ε	Skin depth
ω	Angular frequency

List of abbreviations

Abbreviation	Meaning
2DEG	Two Dimensional Electron Gas
ACFP	Anode Connected Field Plates
APEC	Applied Power Electronics Conference
CVR	Current Viewing Resistor
DBC	Direct Bound Copper
DPT	Double Pulse Tester
DUT	Device Under Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistor
EV	Electric Vehicle
GIT	Gate Injection Transistor
HCSMU	High Current Source/Measure Unit
HEMT	High Electron Mobility Transistor
HEV	Hybrid Electric Vehicle
HVSMU	High Voltage Source/Measure Unit
IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
JFET	Junction Field Effect Transistor
LED	Light-Emitting Diode
LiDAR	Light Detection and Ranging
L-FER	Lateral Field-Effect Rectifier
MEA	More Electric Aircraft
MIS	Metal Insulator Semiconductor

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PFC	Power Factor Correction
PQFN	Power Quad Flat No-leads
PTH	Plated-Through Hole
PV	Photo-Voltaic
PWM	Pulse Width Modulation
RF	Radio Frequency
SBD	Schottky Barrier Diode
SJ	Super Junction
SMD	Surface Mount Device
TV	Television
UPS	Uninterruptible Power Supply
ZVS	Zero Voltage Switching

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Abstract

The recent application of semiconductor materials, such as GaN, to power electronics has led to the development of a new generation of devices, which promise lower losses, higher operating frequencies and reductions in equipment size.

The aim of this research is to study the capabilities of emerging GaN power devices, to understand their advantages, drawbacks, the challenges of their implementation and their potential impact on the performance of power converters.

The thesis starts by presenting the development of a simple model for the switching transients of a GaN cascode device under inductive load conditions. The model enables accurate predictions to be made of the switching losses and provides an understanding of the switching process and associated energy flows within the device. The model predictions are validated through experimental measurements. The model reveals the suitability of the cascode device to soft-switching converter topologies.

Two GaN cascode transistors are characterised through experimental measurement of their switching parameters (switching speed and switching loss). The study confirms the limited effect of the driver voltage and gate resistance on the turn-off switching process of a cascode device.

The performance of the GaN cascode devices is compared against state-of-the-art super junction Si transistors. The results confirm the feasibility of applying the GaN cascode devices in half and full-bridge circuits.

Finally, GaN cascode transistors are used to implement a 270V – 28V, 1.5kW, 1 MHz phase-shifted full-bridge isolated converter demonstrating the use of the devices in soft-switching converters. Compared with a 100 kHz silicon counterpart, the magnetic component weight is reduced by 69% whilst achieving a similar efficiency of 91%.

Declaration

No portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

Copyright statement

Dedication

To my wife, for her unconditional love and support during these years and for being my inspiration.

To my mother, father, and sister, for their belief, patience and unquestionable support.

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Chapter 1: Introduction

1.1 Background

Global warming has become a major concern in recent years. The effects of climate change are visible and are resulting in societies taking action to reduce CO_2 emissions. The general consensus is that to limit the temperature rise to 2°C above pre-industrial levels, the CO_2 emissions with respect to 2008 need to be cut by half by 2050, [1]. Developed countries are targeting even higher reductions, for example, the United Kingdom is targeting 80%, [2].

In 2012, electricity and heating were the source of 42% of global CO_2 emissions whilst transport was responsible for 23%, [3]. Reductions in these areas would result in significant reductions overall since they represent 65% of the total emissions.

The global demand for energy is continuously growing; forecasts indicate that electricity generation will grow from 20.2 trillion kWh in 2010 to 39 trillion kWh by 2040, [4], close to an 100% increase. Clean energy sources must meet this additional demand and replace part of the current demand if CO_2 emissions are to be reduced. Solar and wind energies are very promising options to replace fossil fuel generation, but the costs of these technologies need to decrease if they are to be widely used.

Transport, the second largest generator of CO_2 emissions is another great opportunity area. Hybrid and full electric cars have become available in the last years, however they are also more expensive than their conventional counterparts limiting their adoption. Meanwhile, the aerospace sector is implementing the concept of the more electric aircraft (MEA) where pneumatic, mechanical and hydraulic systems are replaced by electrical systems to increase efficiency as well as reducing maintenance costs.

Power electronic converters are a fundamental part of all these developments. A DC-DC converter and an inverter are needed to interface a photo-voltaic (PV) array with the AC electrical grid, [5, 6], whilst rectifiers and inverters are required as part of the systems to convert the energy produced by wind turbines into the AC electrical grid, [7]. Hybrid and fully electric vehicles require power converters to transform the energy from the DC energy source such as a battery or fuel cell to the

AC motor, whilst AC-DC converters are used to charge the battery from the electrical grid in the case of plug-in vehicles. In addition, power converters are needed to supply the multiple auxiliary loads such as climate control, actuators, driver information, security and entertainment systems.

Similarly, multiple power converters are employed within MEA systems to interface generators with load equipment, [8].

To enable this range of new applications, power electronic converters need to be more efficient, compact, reliable and cheaper. Furthermore, power converters are not just in new technologies, they can be found in almost every electrical device such as laptops, cell phones, appliances, motors, pumps, heaters, lighting, servers, and industrial applications. Improvements in power converters will result in energy savings in these applications as well.

Silicon switching devices have been the overwhelming power device technology in recent decades, with the metal-oxide-semiconductor field-effect transistor (MOSFET) being the key device for lower power, higher frequency applications.

Si MOSFET technology has gradually improved as reflected in its figures of merit. The main figures of merit that are used to compare different technologies are the on-state resistance normalised to a unit of area ($R_{DS\text{-}ON}*A$) and the gate to drain charge normalised to the on-state resistance ($R_{DS\text{-}ON}*Q_{GD}$), [9], Q_{GD} charging and discharging processes determine the voltage switching time which is the main factor impacting the switching losses of an unipolar power device, [10]. The first figure of merit gives an indication of how the conduction losses compare between technologies whilst the second gives an indication of the potential difference in switching loss.

Each technology has a limit in the minimum $R_{DS\text{-}ON} * A$ (called the specific on-resistance) that can be achieved for a specific breakdown voltage, for example, the limit is around 50mΩ*cm^2 at 600V for silicon. Current Si devices are very close to the limit, [11-13].

New developments such as the super junction Si MOSFET have pushed the performance of Si devices beyond the theoretical limit by introducing

three-dimensional structures which use the chip area more effectively at higher cost, [11].

New materials such as SiC and GaN are emerging as alternatives to Si potentially allowing significant improvements to the figure of merit of switching devices. Thanks to their wider band-gap energy, it is possible to fabricate smaller devices for a particular breakdown voltage with similar or smaller on-state resistance compared with Si devices. The reduction of size is accompanied by reductions in charge improving the $R_{DS\text{-}ON} * Q_{GD}$ figure of merit and suggesting lower device switching losses for a given on-state resistance. Figure 1.1 presents the theoretical one-dimensional limit for Si and the new wide band-gap materials, [14].

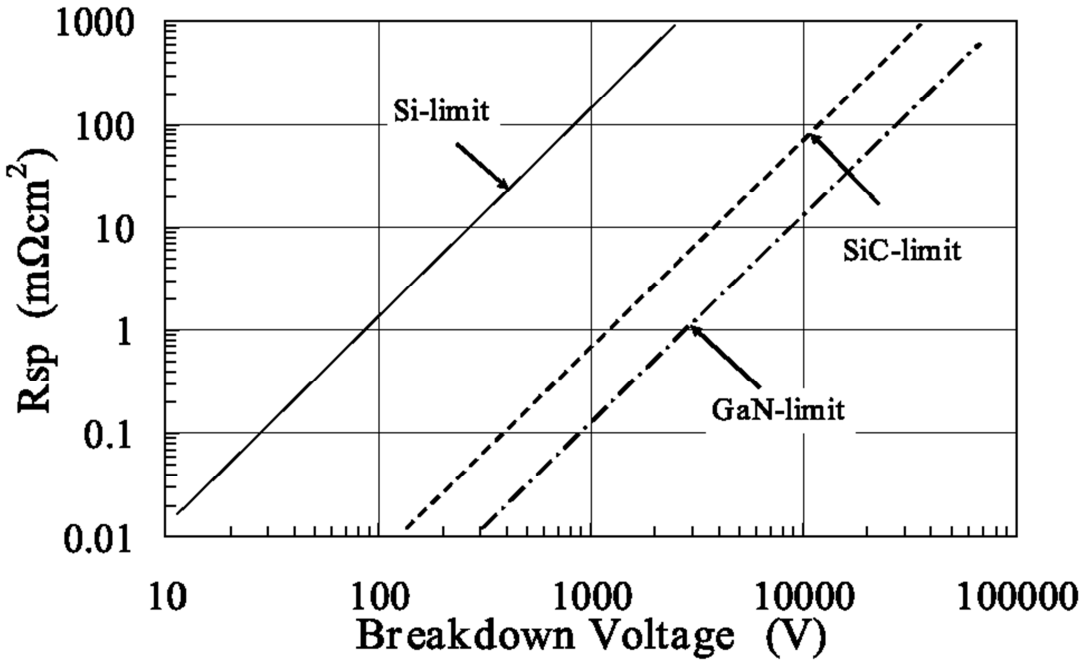


Figure 1.1: Specific on-resistance versus breakdown voltage one-dimensional limit for Si, SiC and GaN, [14]

GaN presents the lowest theoretical value of specific on-resistance and indicates the possibility of reaching the best figure of merit. The reduction of switching losses allows the switching frequency to be increased, reducing the size of magnetic devices and output filters and resulting in a smaller and cheaper system.

1.2 Scope

This research work focuses on GaN devices rated around 600V for converter applications between 200V and 400V. GaN devices in this operating range were in early development at the beginning of this research, prototype samples were barely available and only in cascode configuration, therefore, this work has investigated cascode switching devices.

1.3 Research objectives

The objectives of this research are:

1. To develop a simple analytical model of the cascode switching transients which provides an understanding of the switching processes, and forms a basis for converter design including the estimation of turn-off/on switching losses.

2. To characterise the switching behaviours of emerging GaN devices in terms of switching speed, energy losses and their relation with operating and driving parameters. To compare the results against state-of-the-art Si devices.

3. To identify applications and topologies that best exploit the characteristics of GaN devices and to quantify the performance gains through the development of a demonstrator.

1.4 Significance of the work

Although other work presents analytical models of the switching transients of cascode GaN devices, these are very complex or very simple. The model developed here allows the derivation of time domain equations for the main electrical variables of the circuit in a simple way without significantly sacrificing accuracy. Plots of the switching transients are easily generated using the time domain equations and the energy losses can be tracked in either of the two devices forming the cascode configuration, allowing a better understanding of the switching process.

Practical results of GaN devices have been presented in other publications. However, much of this work considers an elementary switching cell formed by the test device

and a SiC diode. This work extends the study to consider two GaN cascode devices in an inverter leg configuration which is a key part of half and full-bridge converter topologies. This work demonstrates the viability of operating the devices in this mode and the simple model can be used to estimate losses.

Energy loss results for two different GaN cascode devices are presented allowing comparison of characteristics and the identification of common features such as the insensitivity of the turn-off energy losses to the drive circuit voltage and the gate resistor.

The application of the GaN devices in a soft-switching DC-DC power converter for the aerospace sector highlights the benefits of this technology to increase the switching frequency. It was increased ten times with respect to the typical Si-based solution at similar efficiency (>91%). This allowed a reduction of 58% in volume and 69% of weight in the transformer, whilst a reduction of 94% in volume and 84% in weight is achieved for the output filter inductor with respect to its Si-based counterpart.

1.5 Thesis structure

The thesis is divided in six chapters.

Chapter 1 presents the introduction of the research frame work, its scope and objectives.

Chapter 2 presents the literature review. GaN material characteristics are compared against Si and SiC. The devices that are fabricated using GaN are summarised. Previous characterisation work is analysed. The challenges posed by GaN devices and the proposed solutions are described. Finally, the potential application of the devices is explored and the GaN-based converter demonstrations are summarised.

Chapter 3 introduces the development of a simple analytical model. It presents the switching transients divided into four stages. The equivalent circuits and derivation of equations for each stage are shown. The simple model is validated using experimental measurements and later used to analyse the effect of different driving conditions in the switching waveforms. The Chapter concludes with an analysis of how the switching energy loss is distributed between the devices of the cascode.

Chapter 4 presents the practical testing of GaN devices. The study focuses on cascode devices. Transphorm and GaN Systems parts are evaluated along with a SiC diode and in an inverter leg configuration under inductive load conditions. The effects of operating and driving conditions are presented and discussed. The results of the Transphorm device are compared against state-of-the-art super junction Si MOSFETs at different operating conditions.

Chapter 5 shows the design of a 1MHz, 1.5kW and 270V – 28V phase-shifted full-bridge isolated converter using GaN cascode devices. The performance benefits of using GaN devices are quantified and discussed.

Chapter 6 presents the conclusions of the research work, its contributions and identifies further research opportunities.

Chapter 2: Literature review

2.1 Introduction

The objective of this Chapter is to review the development of GaN technology in power electronics. First, the characteristics of wide bandgap materials are presented. GaN and SiC technologies are discussed next and the advantages of GaN are identified. GaN diodes and switches are reviewed including their internal structures and characterisation results; special attention is given to the cascode connection. One of the main obstacles of GaN technology, the current collapse or dynamic $R_{DS\text{-}ON}$ phenomenon, is reviewed in detail. The potential application fields of GaN devices along with some performance results are shown. Driving, thermal and instrumentation aspects of GaN devices and applications are also discussed.

2.2 Wide band-gap materials

SiC and GaN materials are the most promising alternatives to Si in the near term. The main characteristics of these materials are presented in Table 2.1 (extracted from [11]) to illustrate their advantages.

Table 2.1: Silicon, silicon carbide and gallium nitride characteristics, [11]

Property	Si	4H-SiC	GaN
Band-gap energy (eV)	1.12	3.26	3.39
Intrinsic carrier concentration (cm^{-3})	1.4×10^{10}	8.2×10^{-9}	1.9×10^{-10}
Critical Field (MV/cm)	0.23	2.2	3.3
Electron mobility ($cm^2/(Vs)$)	1400	950	1500
Thermal conductivity (W/(cm K))	1.5	3.8	1.3

The band-gap energy is the energy required to move an electron from the valence band to the conduction band. If the band-gap is higher, a thinner layer or shorter length of material is required to support a particular breakdown voltage. Of the three materials, GaN presents the highest band-gap energy value, 4% higher than 4H-SiC and both are around three times higher than Si. This allows the fabrication of devices that exceed the Si limit as shown in Figure 1.1. In addition, the higher band-gap energy allows higher temperature operation, [15, 16]. The materials could operate at

such high temperature that the maximum temperature of a device would be set by the packaging and the formation of contacts rather than the material itself, [15].

The much lower intrinsic carrier concentration in SiC and GaN suggests that devices made from these materials would have smaller leakage current, [11].

The critical field which is proportional to the band-gap energy determines the breakdown voltage of a device indicating that SiC and GaN devices of a particular material thickness can support a larger voltage than a silicon device.

The electron mobility within the material is related to its conduction resistance. GaN presents the highest electron mobility while SiC presents the poorest.

Finally, SiC has the highest thermal conductivity, almost three times that of GaN, which has the lowest value (slightly smaller than Si). This property potentially allows SiC devices to operate at higher ambient temperatures and current densities when compared against the other two materials for the same power loss.

Therefore both wide band-gap materials offer the possibility of building smaller devices at a specific breakdown voltage when compared against silicon. The slightly higher bandgap energy and superior electron mobility of GaN in comparison with SiC indicates the potential of the material for power device applications. The superior electron mobility of GaN is enhanced by the two dimensional electron gas (2DEG) that is formed at the interface between GaN and aluminium gallium nitride (AlGaN) materials, and represents one of the main advantages of GaN against SiC since smaller conduction losses are obtained at higher electron mobility.

On the other hand, SiC offers the possibility of operating at higher temperatures when compared with GaN because of its superior thermal conductivity.

2.3 Application of wide band-gap materials in power devices

SiC is the more mature wide band-gap technology for power devices. Schottky barrier diodes (SBDs) in the range of 600V-1200V have been commercially available for some years and 1700V SBDs are being offered by Wolfspeed, [17]. In contrast, transistors have become generally available in the last two to three years.

On the other hand, GaN is widely used in lighting and lately in the radio frequency (RF) area but its application for high voltage power devices is relatively new. At higher voltages (around 1200V and above) vertical structures, where the current flows through the device including the substrate, are needed and the structure requires the substrate to be made of the same base material, [18]. The high defects' density of GaN substrates has prevented the development of GaN vertical devices. In contrast, SiC substrates are significantly cheaper and have significantly higher quality than GaN ones, [19], leading to the development of SiC devices in this voltage range, [18].

Various different substrates have been used to grow GaN layers overcoming the issues of GaN as a substrate, for example sapphire, Si and SiC. GaN on sapphire devices have been demonstrated but the poor thermal conductivity of sapphire limits the performance. GaN on Si devices have better thermal conductivity than sapphire and are significantly cheaper than the other substrate options, [19]. Lateral device structures (where all the terminals are in the same side of the device and the current flows close to the surface) are normally manufactured when using different substrates which can limit the achievable breakdown voltage of the devices. Although GaN on Si lateral devices up to 2200V have been demonstrated by removing the Si substrate, [20], most of the commercially available devices are rated around 600V and below.

GaN on Si devices have a significant cost advantage compared with SiC and the cost is predicted to approach Si levels. Some companies such as EPC are predicting that GaN on Si devices rated at 600V and below will become cheaper than their Si counterparts, [18], mainly due to the economies of scale with large size silicon wafers.

In addition, since GaN devices are physically smaller, more devices per wafer can be manufactured.

Si has the advantage of decades of development and power devices are fabricated in vertical structures in wafers of up to 300 mm, [21]. SiC is manufactured in wafers of 100mm of diameter and 150mm are being developed, [22]. GaN on Si normally uses wafers of 150 mm and the technology is quickly improving, 200mm wafers have recently been demonstrated, [23-25]. When GaN devices are built on Si wafers, Si

foundry infrastructure can be used with minimum modifications to the process reducing the manufacturing costs.

The $R_{DS\text{-}ON} * A$ figure of merit of GaN on Si devices is making its way towards the SiC limit, which is well beyond the physical limitations of Si, [24]. Furthermore, if the cost obstacle of GaN substrates is overcome and vertical GaN devices start to appear, the device performance could be far beyond the SiC limit as stated by Avogy research, [26].

2.4 GaN device manufacturers

A summary of the main GaN device designers and manufacturers is presented next.

Efficient Power Conversion

Efficient Power Conversion or EPC is based in the United States and it was the first company offering commercial GaN switches. EPC offers a wide variety of GaN on Si normally-off devices ranging from 30V – 450V, [27, 28] and a number of publications including three books, [29]. EPC focuses on products for applications in datacom/telecom, DC-DC converters, envelope tracking, wireless power, high radiation environments, light distancing and ranging (LiDAR), Class D audio and power inverters, [30].

GaN Systems

GaN Systems is a fab-less Canadian based company with offices in China, Germany, Japan and USA that currently is offering enhancement mode 650V GaN switches with drain currents of up to 60A and on-state resistances as low as 25mΩ, [31]. Three 100V GaN switches are also offered in two different packages with drain currents of up to 90A and on-state resistances as low as 7.4mΩ, [31]. The island structure of the devices is the basis of its products, [32]. Their first prototype developments included cascode devices that were used in this research. GaN Systems focuses on switch mode power supplies, uninterruptible power supplies (UPS) and motor control, solar and wind technologies, hybrid and electric vehicle battery control, health management systems and power factor correction, [33].

Infineon

The German company acquired International Rectifier in 2015 getting access to its GaN technology. International Rectifier had developed low voltage GaN cascode devices. In addition, Infineon has a partnership with Panasonic getting access to enhancement mode HEMTs in the 600V range. Infineon's target applications include telecom systems, servers, TV adapters and class-D audio amplifiers, [34].

NXP Semiconductors

The Dutch company has GaN HEMT products for the RF sector and is developing a GaN power switch technology based on cascode-connected HEMTs in the 600V range.

Panasonic

The Japanese corporation has developed the gate injection transistor (GIT), an enhancement mode switch in the 600V range. This new structure allows a significant improvement in the on-state resistance of the switches, [35]. Panasonic targets applications such as power supplies for hybrid and electric vehicles and PV inverters, [35].

Transphorm

Transphorm is based in California in the United States with also a strong presence in Asia. Transphorm offers 600V GaN cascode devices ranging from 9A up to 34A in TO-220 and power quad flat no-leads (PQFN) packages, [36]. Transphorm products were the main devices that were used in this research work. Motor drivers, solar energy, switch mode power supplies and inverters are some of the target applications of Transphorm products, [37].

Other commercial activities:

- **Avogy.** Working in the development of GaN on GaN vertical devices, [38].
- **Cambridge Electronics.** Offering four different GaN products rated at 200V and 650V, [39].
- **EXAGAN.** Developing 600V and 1200V GaN on Si transistors in 200mm wafers in partnership with Soitec and CEA-Leti, [40, 41].

- **Fujitsu.** Integrated its GaN business with Transphorm, [42].
- **MicroGaN**. Developing GaN on Si 600V switches and diodes, [43].
- **Powdec.** Developed 600V, 10A transistors, [44].
- **Qorvo.** Resulted from the merging of RFMD and Triquint and is developing 650V devices to be a drop-in replacement of current Si solutions, [45].
- **Sharp, GE, Sumitomo and Toshiba.** Investing in Transphorm GaN research, [46].
- **ST.** Developing GaN Schottky diodes in partnership with Velox Semiconductors, [47].

2.5 GaN devices

A brief survey of GaN diodes and switches is presented in this section.

2.5.1 Switches

A two-dimensional electron gas (2DEG) is created near the interface between GaN and AlGaN allowing the concentration of a large number of electrons with high mobility. The 2DEG phenomenon provides the basis for the high electron mobility transistor (HEMT) allowing the creation of switches with a very low on-resistance. The basic structure of a HEMT is shown in Figure 2.1, [48].

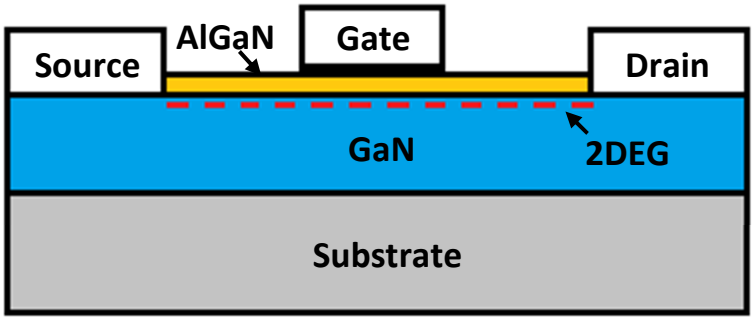


Figure 2.1: HEMT basic structure, [48]

A GaN surface is grown over a Si, Sapphire or SiC substrate. The GaN and AlGaN creates a 2DEG close to the interface of the materials. This 2DEG short circuits the drain and source terminals when no field is applied to the gate terminal. To deplete the electrons a negative voltage with respect to the drain and source terminals needs to be applied to the gate terminal. As can be observed, the resultant device is normally-on or depletion mode. This kind of device is undesirable in most power

applications for safety reasons; a short-circuit in the power converter may arise during start-up or when a drive circuit fault occurs. Normally-off or enhancement mode devices are preferred.

To produce the normally-off behaviour, various solutions have been proposed. Initially, the most common solution was to connect the depletion mode HEMT in a cascode arrangement with a low voltage Si MOSFET, this configuration will be discussed in detail in section 2.7. Single normally-off devices can be generated by implementing a recessed-gate structure, [49], where the gate is recessed on a thinner AlGaN material under the gate performing a selective reduction of the 2DEG as shown in Figure 2.2. The aluminium nitride (AlN) buffer layer is used to smooth the transition between GaN and substrate materials because of their lattice mismatch and thermal expansion coefficient difference.

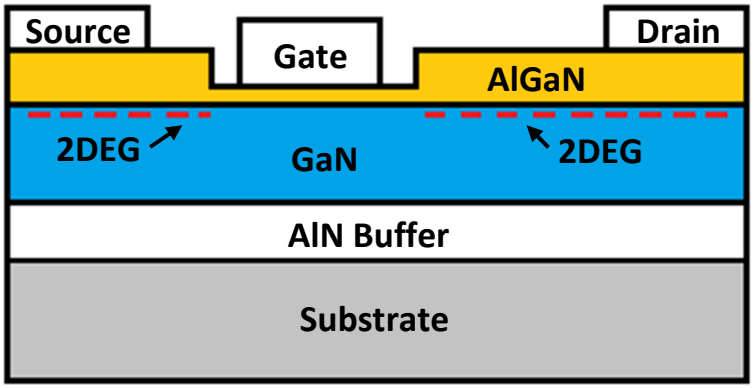


Figure 2.2: Basic structure of a HEMT with recessed gate, [49]

Another solution is to use a fluoride-based plasma treatment where fluoride ions are added to the GaN/AlGaN interface, [50]. The negative charge of the ions shifts the threshold voltage of the device in the positive direction generating normally-off devices. A combination of fluorine doping and a recessed gate was proposed in [51] to improve the behaviour. Adding a cap layer of InGaN beneath the gate has also proved to be effective to generate enhancement mode devices by raising the conduction band, [52].

A pn junction gate structure has similar effects and allows a higher gate voltage than a Schottky barrier gate. This approach is reported in [53] where 3V can be applied to the gate of the HEMT without producing a significant increase in the gate leakage

current compared with 1V in a typical Schottky barrier gate HEMT; the device built was rated at low voltage on sapphire substrate.

An approach supported by Panasonic is the gate injection transistor (GIT). This normally-off device is implemented by growing a p-AlGaN layer below the gate forming a pn junction as shown in Figure 2.3, [54]. The resulting device raises the potential under the gate to generate a normally-off device. When the gate voltage is higher than the forward voltage of the pn junction, holes are injected into the channel increasing the electron density and by consequence the channel maximum current. Uemoto *et al* used this approach to generate a normally-off device with a threshold voltage of 1V, a maximum drain current of 200mA/mm, a maximum breakdown voltage of 600V and a maximum gate voltage of 6V in 2007, [54]. The device was built on silicon helping to reduce the cost. Recently, these devices were successfully manufactured on 200mm Si wafers, [24].

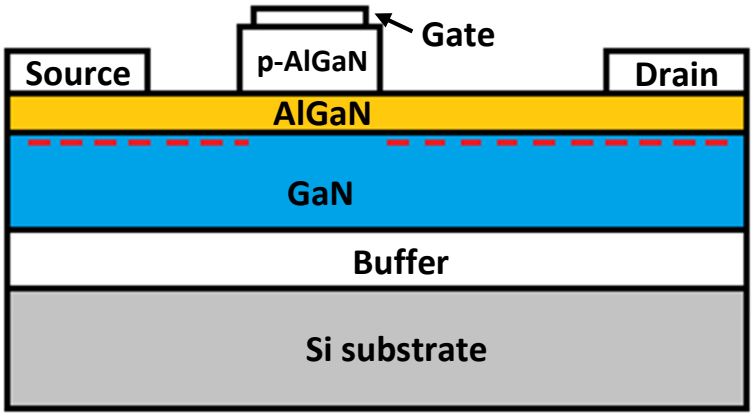


Figure 2.3: GIT structure, [54]

Previous methods have been effective to shift the threshold voltage to positive values. However, the values are very low (below 1V) reducing the immunity of the devices to electrical noise. In addition, the voltage that can be applied to the gate is also low if a Schottky structure is used in the gate.

A metal insulator semiconductor (MIS) gate structure is one of the solutions that has been proposed to increase the threshold voltage of the devices and the voltage that can be applied to the gate without having excessive gate leakage current. Combining the addition of cap layers beneath the gate, a gate recessed structure and a metal insulator semiconductor structure result in normally-off devices with high threshold

voltage and with a maximum drain current similar to normally-on devices. Kanamura *et al* in [55] presents an enhancement-mode MIS-HEMT by combining the recessed-gate technique and a triple cap layer to achieve a threshold voltage of 3V with a high current level and maximum breakdown voltage of 320V, the maximum drain current was 800mA/mm. Figure 2.4 presents the structure.

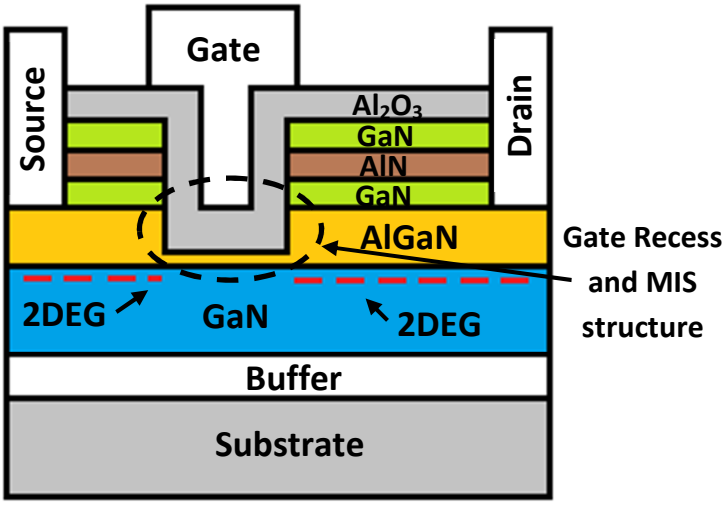


Figure 2.4: Cross sectional view of an AlGaN/GaN MIS-HEMT with a triple cap layer, a recessed-gate structure and high-k dielectrics, [55]

Oka *et al* in [56] succeeded in obtaining a device with even higher threshold voltage, 5.2V, getting a maximum drain current of over 200mA/mm and a maximum breakdown voltage of 400V. The drawback of the technique is an increase of the on-state resistance because of the disappearance of the 2DEG below the gate.

Some of the previous methods have created the possibility of fabricating enhancement-mode and depletion-mode devices on the same wafer allowing other driving and control stages to be integrated in a single GaN chip. For example, reference [57] presents a pulse width modulation (PWM) integrated circuit (IC) using GaN HEMTs which is able to operate at 1MHz and up to 250°C. The design can be monolithically integrated with a power switch dramatically reducing the parasitic elements in the gate loop and improving the transient behaviour, electromagnetic interference (EMI), energy consumption and reducing the voltage stress to the switching device's gate. This design still has to be optimised and it may reduce the flexibility to adjust the switching speed of the power device since the gate resistor is not accessible, but the driving voltage could be used instead.

2.5.2 Diodes

The development of GaN diodes lagged behind the development of the GaN switch partly because SiC Schottky barrier diodes have been established in the same market for some years and because of the technical difficulties of developing a part with good characteristics at low cost, [58].

The lack of cheap and high quality GaN substrates has forced the development of GaN diodes on different substrates such as Sapphire, SiC and Si, [19, 22]. The most common approach to implement Schottky diodes is the lateral structure, [22].

Although GaN on Sapphire devices, [59-62], and GaN on SiC devices, [63], have been demonstrated, silicon is the preferred substrate because of its better thermal conductivity and lower cost. However, it has been demonstrated that the lower defect density of GaN grown on either sapphire or SiC can produce devices with higher breakdown voltage. The basic structure for a lateral GaN Schottky barrier diode is presented in Figure 2.5.

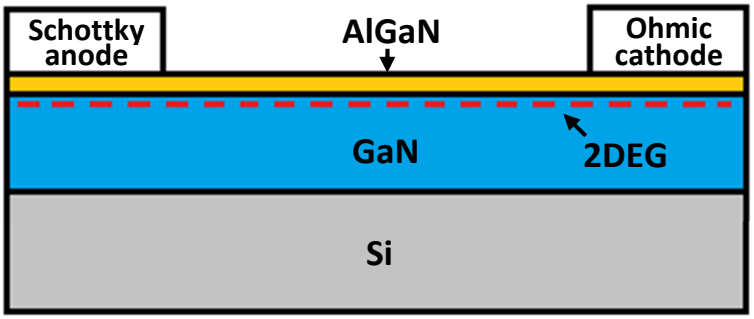


Figure 2.5: GaN Schottky barrier diode basic structure

The metal of the anode is chosen to create a Schottky junction with the AlGaN and a metal that creates an ohmic junction is used for the cathode. The Schottky barrier height will determine the voltage that needs to be applied to start the conduction of the diode.

The basic structure presents a high forward voltage and limited breakdown voltage. A buffer between the substrate and the GaN layer along with an AlGaN back barrier helps to reduce the leakage current and to increase by consequence the breakdown voltage as in [64, 65]. A GaN cap above the AlGaN layer can be also used for the same purpose, [64, 66-68]. A less common approach is to implement double metal contacts using nickel oxide as in [68]. The double contact reduces the leakage

current and increases the breakdown voltage by increasing the Schottky barrier height. However, it slightly increases the on-state voltage. Also, anode connected field plates (ACFP) are used to spread the electric field increasing the breakdown voltage significantly, [65, 69]. The highest breakdown voltage reported for lateral GaN on Si SBDs is 1.9kV and was achieved using two field plates, [70].

Various techniques have been proposed to reduce the on-state voltage of the Schottky diode. A combination of a Schottky contact with an ohmic region has shown a reduction of the on-state voltage, but increases the leakage current by several orders of magnitude, [71]. Yi-Wei *et al*, [67], showed that Si can be used to dope the material below the anode and the cathode, reducing the on-state voltage and increasing the breakdown voltage; the improvement is around 20% compared with a part without the doping. The anode recessed technique has been used successfully to reduce the on-state voltage of GaN SBDs as shown in [25, 65, 66, 72, 73]. A Schottky junction voltage as low as 0.5V has been achieved using this technique, [65]. Further improvements can be obtained if the recessed anode technique is combined with an ohmic mixed contact as demonstrated in [72] reaching an on-voltage of 0.37V.

Another approach to reduce the on-state voltage is the lateral field-effect rectifier (L-FER) reported in [74] where the rectifier is implemented by using the structure of a normally-off HEMT produced by fluorine plasma treatment. The gate and drain terminals are short-circuited and this way the on-state voltage is determined by the threshold voltage of the device and not by the Schottky barrier height. A device of 390V was built and its on-state voltage was 0.63V at 100A/cm^2, [74], however a drawback was an increased leakage current, which was attributed to the buffer. Since the L-FER structure is compatible with the manufacturing process of HEMTs; rectifiers and switches could be monolithically integrated.

Another structure that allows the integration of diode and HEMT structures is to generate a GaN SBD by electrically connecting the drain and source of the HEMT structure to generate the cathode and to create a Schottky junction in the gate terminal to generate the anode, [69].

Some of the techniques that have been used to increase the threshold voltage of GaN HEMTs have also proved to be useful to produce low on-state voltage and low

leakage current diodes. The MIS structure was successfully used in the recessed anode of a diode to generate a structure able to block up to 1.1kV, [73]. In addition, the manufacturing process is compatible with that of MIS-HEMTs, which would allow component integration, reducing parasitic elements and manufacturing cost. Also GaN SBDs in vertical structures have been developed and their figures of merit are comparable with the lateral structures, [75-78].

A benchmark plot of the different GaN SBDs' figures of merit is presented by Mingda *et al* in [70] and is presented in Figure 2.6 which shows that the GaN on Si lateral SBDs are approaching the GaN limit and are likely to move closer as the technology is developed. For example, Avogy have recently announced a 2600V vertical GaN p-n diode with a specific on-resistance of 2mΩ cm^2, [79], which is very close to the GaN limit.

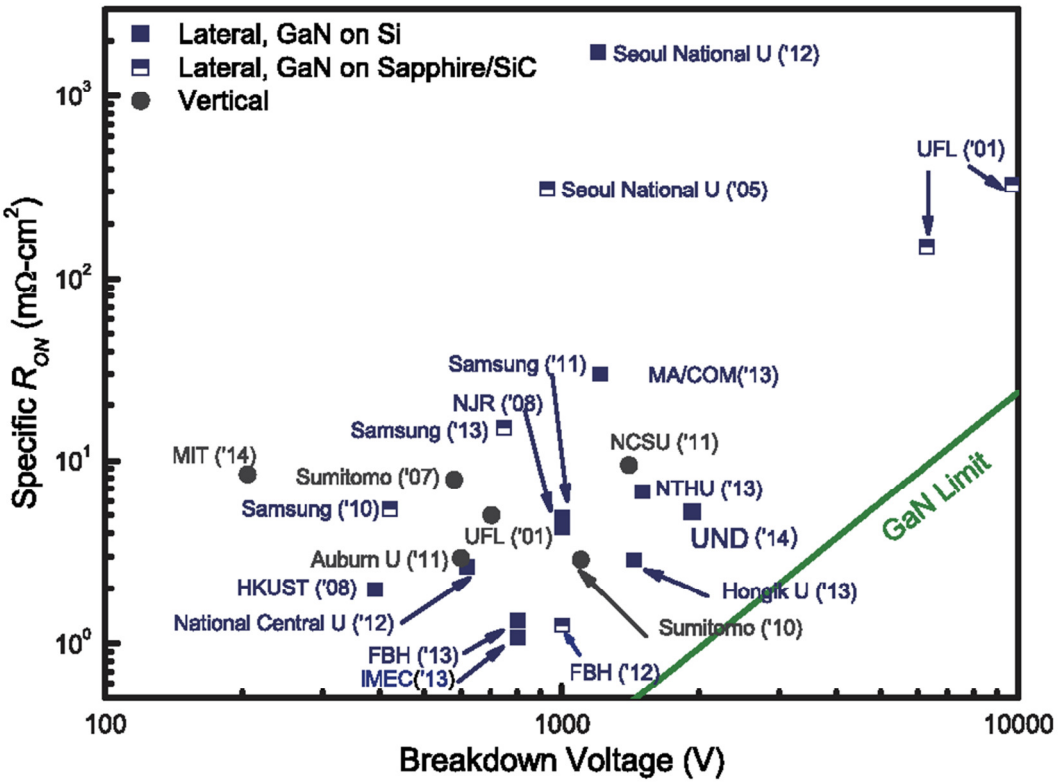


Figure 2.6: Benchmark plot of BV versus $R_{ON,SP}$ of GaN based unipolar power diodes, [70]

In 2014, Zhang *et al*, [80], demonstrated for the first time two GaN on Si vertical devices that can potentially combine the performance advantage of a vertical device and the low cost of using a Si substrate. The devices are a SBD and a p-n diode, rated at 205V and 300V, although, according to the authors, more research is

required to understand the leakage current mechanism which may enable an increase in breakdown voltage.

Another approach was introduced by Powdec, the idea is to build a vertical SBD using a Sapphire substrate; Sapphire allows GaN to be grown with lower defect density than when using Si substrates. Finally, the substrate is removed leaving just the Schottky diode and freeing the device of the poor thermal conductivity of the sapphire, [81].

2.6 Current collapse

Current collapse or dynamic on-resistance refers to the increase of GaN devices' on-resistance after a period of high-voltage stress during the off-state. In other words, the maximum current achievable at a particular on-state voltage is reduced. There is also a related reduction in the transconductance, [82].

This phenomenon has been one of the main obstacles in the development and adoption of GaN-based devices since it increases the conduction losses and compromises the reliability.

It has been reported that current collapse is mainly caused by electrons from the gate leakage current, [83-85], that are caught in traps on the AlGaN surface, generating a field that depletes the 2DEG of the AlGaN/GaN hetero-interface, and by consequence decreases the 2DEG density and increases the channel resistance, [83]. The electron trapping occurs mainly in the zone between the gate and the drain as this is an area of high electric field as demonstrated in [86].

Additional traps may be generated by high voltage stress as found by Jungwoo *et al*, [87]. They suggest that the high voltage stress creates strain over the AlGaN surface and above a critical value, through reverse piezoelectric effect, generates dislocations that increases the number of electron traps.

Other mechanisms that contribute to current collapse are the injection of hot electrons in the buffer, [85, 88], and the substrate, [83]. However, these effects are less significant because of the distance between the buffer or the substrate and the 2DEG layer.

Current collapse decreases over time when the device is in the on-state as the trapped electrons are released. The release process can have time constants of the order of seconds, [89].

Several solutions have been proposed to control or reduce current collapse. Passivation of the AlGaN surface has been used to reduce the number of traps and reduce current collapse, [85, 86, 88-90]. Also, Kawanago *et al*. in [91] found that using titanium nitride (TiN) as the material for the gate contact instead of the typical Ni has a positive impact on current collapse due to the TiN nitrogen concentration that can passivate the AlGaN surface.

The use of field plates help to spread the electric field and reduce the peak value of the field at the edges of the gate terminal, reducing the leakage current, have been shown to mitigate current collapse, [83, 92]. The field plates also have the effect of accelerating the release of trapped charges. Furthermore, Koudymov *et al* in [93] found that a semiconducting dielectric under the field plate is necessary to reduce current collapse.

Alternatively, a GaN/AlGaN/GaN structure has been shown to reduce current collapse but the leakage current is increased and the technique was not effective in protecting the device from damage induced by high electric fields, [82].

It has also been shown that a more conductive substrate helps to reduce current collapse, specifically a Si substrate showed significant improvement over sapphire, [94].

The electrical connection of the substrate also has a role in the mitigation of current collapse, for example higher current collapse has been measured on GaN HEMTs with the drain connected to the back side of the device, [95]. Similarly, GaN SBDs with the cathode connected to the substrate exhibit higher current collapse.

The understanding of current collapse has matured in the last few years to the extent that some suppliers such as Transphorm, have claimed that current collapse has been eliminated from their products, [96]. EPC has published reliability reports where there are no evident signs of current collapse, [97]. The challenge in the near future is to develop devices with current collapse suppression at increasingly higher rated voltage.

Standard techniques to measure and quantify current collapse are not well established, however the Keysight Technologies power device analyser / curve Tracer, B1505A, now offers a current collapse option, [98]. This equipment is able to measure the current collapse in GaN devices applying stress voltages of up to 3kV. The stress level, stress time and monitoring time after stress can be set. The diagram of the measurement is shown in Figure 2.7, [99]. During the off-state the high voltage source/measure unit (HVSMU) module applies a high voltage stress to the device under test (DUT) and the diode D_1 is reverse biased. Later, the DUT is turned-on and since the HVSMU module has very low output current capacity (few mA), the DUT drops the voltage of the HVSMU module. When the DUT voltage drops sufficiently the diode D_1 is forward biased and conducts the high current provided by the high current source/measure unit (HCSMU) module. The HVSMU module continues providing a low current value and acts as a current source. The drain voltage and the drain current are monitored and used to calculate the channel resistance of the DUT.

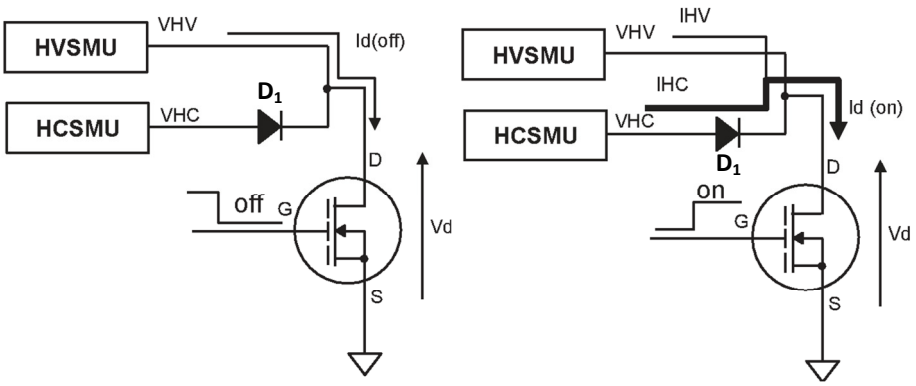


Figure 2.7: Test circuit diagram to measure current collapse used in B1505A, [99]

Although providing a very good solution for measuring current collapse, the B1505A has some limitations, the slew rate of the power supplies is quite slow (0.4V/μs), preventing the measurement of on-state resistance immediately after a representative rapid switching transient.

Other researchers have proposed more flexible methods to measure current collapse. Joh et al, [100], uses common DC measurement equipment. The method was able to detect current collapse but it was not possible to quantify the increase in on-state resistance in the short term, which is important in high-frequency applications.

A hard-switching Vienna boost converter was used to evaluate the dynamic $R_{DS\text{-}ON}$ in [101] using a Wilson current mirror to clamp the drain to source voltage of the DUT, allowing measurements to be made with good resolution. If the oscilloscope was directly attached to the DUT, it would be exposed to a high voltage in the off-state, making accurate measurement of the low on-state voltage a challenge. However, the proposed circuit suffers from low frequency oscillations affecting accuracy.

Bin et al, [102], presented an improved clamp circuit using only one Si transistor, three diodes, two resistors and a capacitor. The oscillations were significantly reduced and the clamp circuit was used to measure the on-state resistance of GaN HEMTs under soft and hard-switching conditions. The readings could be obtained after 2μs of applying the stress voltage.

Finally, [103], presented a clamp circuit using just the series connection of a clamp capacitor and an active switch synchronised with the DUT. The clamp circuit allowed high resolution measurement of the drain to source voltage. A soft-switching circuit was implemented to evaluate the current collapse under different stress levels.

Whilst measuring current collapse within a typical converter circuit, as in the last three examples, is relatively straightforward providing a voltage clamp is used to protect the oscilloscope, there may be some limitations with regard to the stress time and recovery time. There is therefore a need for a circuit that is similar to the Keysight system with reduced switching delays and more flexibility to set stress time, on-state time, resolution, stress voltage and operating current.

2.7 Cascode device

One solution to create a normally-off switch from GaN technology is the cascode connection. In this arrangement a depletion mode HEMT is connected in series with a low voltage normally-off Si device, Figure 2.8. The source of the GaN HEMT is connected to the drain of the Si MOSFET and the gate of the GaN HEMT is connected to the source of the Si MOSFET. The gate of the silicon device forms the control input to the cascode circuit, therefore the Si MOSFET controls the turn-off/on of the cascode, while the GaN HEMT blocks virtually all of the voltage.

The cascode connection was one of the first methods to produce a normally-off GaN switch and when this research project started, these were virtually the only parts available. Transphorm and GaN Systems cascode devices were used during the development of this research.

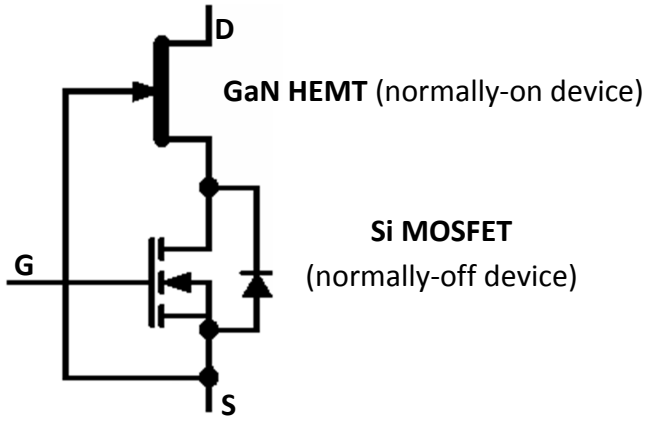


Figure 2.8: Cascode connection schematic

Recently, GaN Systems have released normally-off enhancement-mode HEMTs rated at up to 650V, 60A.

2.7.1 Operating modes

Forward conduction

When the gate to source voltage of the Si MOSFET ($v_{GS\text{-}Si}(t)$) exceeds the threshold voltage of the Si MOSFET ($V_{TH\text{-}Si}$), the channel of the Si MOSFET conducts and reduces almost to zero the gate to source voltage of the GaN HEMT ($v_{GS\text{-}GaN}(t)$) and by consequence its channel conducts. Both channels are then conducting the transistor on-state current $I_{D\text{-}ON}$ and the overall on-resistance of the cascode device is the addition of the individual channel resistances.

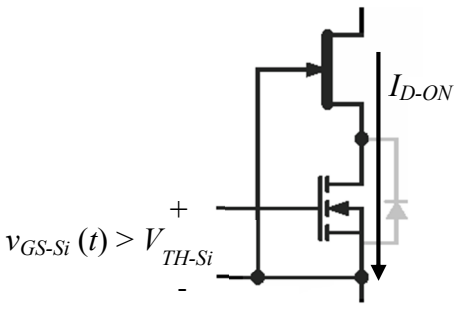


Figure 2.9: Cascode connection in forward conduction

Off state, $v_{GS\text{-}Si}(t) < V_{TH\text{-}Si}$ and $V_{DS\text{-}OFF} < -V_{TH\text{-}GaN}$

When $v_{GS\text{-}Si}(t)$ is smaller than $V_{TH\text{-}Si}$, the Si MOSFET channel is closed and blocks the applied off-state voltage $V_{DS\text{-}OFF}$. If $V_{DS\text{-}OFF}$ is smaller than $-V_{TH\text{-}GaN}$, the channel of the GaN HEMT will remain on and the GaN HEMT does not block voltage. In this case all the forward voltage applied across the switch is blocked by the Si MOSFET.

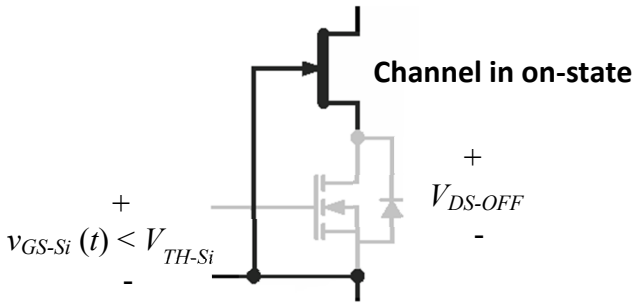


Figure 2.10: Cascode connection in off state, $V_{DS\text{-}OFF} < -V_{TH\text{-}GaN}$

Off state, $v_{GS\text{-}Si}(t) < V_{TH\text{-}Si}$ and $V_{DS\text{-}OFF} > -V_{TH\text{-}GaN}$

This state is similar to the previous one except that the forward voltage across the cascode is higher than $-V_{TH\text{-}GaN}$. The voltage blocked by each device is defined by the ratio of the GaN HEMT drain-source capacitance and the combination of the Si MOSFET output capacitance and the GaN HEMT gate-source capacitance. The capacitances ratio is designed in a way that the GaN HEMT blocks most the voltage limiting the voltage blocked by the Si MOSFET.

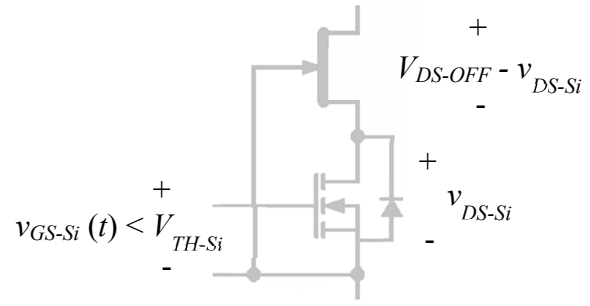


Figure 2.11: Cascode connection in off state, $V_{DS\text{-}OFF} > -V_{TH\text{-}GaN}$

Reverse conduction

When $v_{GS\text{-}Si}(t)$ is smaller than $V_{TH\text{-}Si}$ and the source terminal has a voltage higher than the drain terminal, the body diode of the Si MOSFET is forward biased and conducts. By consequence, the gate and source terminals of the GaN HEMT are at almost the same potential and the GaN HEMT channel conducts. Reverse conduction occurs through the body diode of the Si MOSFET and the channel of the GaN HEMT. The total voltage drop is the addition of the forward voltage of the body diode and the product of the operating current and channel resistance of the GaN HEMT. If the silicon gate were turned on, then reverse conduction would occur through the channels of both devices.

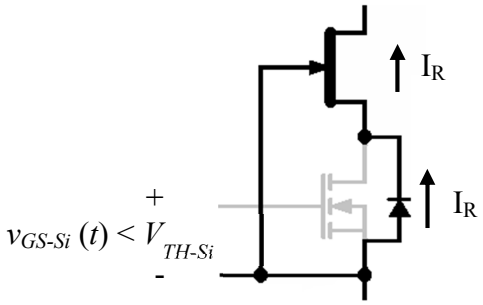


Figure 2.12: Cascode connection in reverse conduction

2.7.2 Cascode connection advantages and drawbacks

One of the advantages of the cascode is that standard silicon MOSFET driving techniques can be used, [104-106]. The threshold voltage is typically greater than 1.8V, [36, 106], providing decent noise immunity in the off-state, and the maximum gate-source voltage is around 20V, [36, 105] allowing the gate to be overdriven safely. In contrast enhancement-mode GaN devices can have threshold voltages ranging from 1V to 1.4V, [28, 31, 54] and maximum gate voltages of 7V, [28, 31].

A second advantage of the cascode is related to its turn-off loss. As will be discussed in Chapter 3, the turn-off loss is very small because of the interaction between devices, making it ideal for soft-switching applications where the turn-on losses are eliminated by zero voltage switching (ZVS) techniques [104, 107, 108].

An important characteristic of the cascode device is that the low voltage MOSFET body diode has very low reverse recovery charge (Q_{rr}), around 20 times lower, when compared against a Si MOSFET rated at high voltage, [109].

The main drawback of the cascode is related to the additional parasitic elements added by the interconnection of devices as described in [110] that may lead to delays and oscillations as modelled by Xiucheng et al, [108].

A second drawback is that the input capacitance of the cascode is from the Si MOSFET which is larger than that of a single GaN device of similar on-state resistance, [111].

2.7.3 Modelling

Detailed analysis of the cascode switching process is important to understand the interactions between the constituent devices and to provide a basis for optimising performance, drive circuit design and loss estimation.

Although the cascode configuration has been known for some time it is only recently that there has been high interest in its operation and design. With the emergence of SiC devices, the cascode configuration was considered as a solution to produce a normally-off switch from normally-on SiC JFETs. Rodriguez *et al*. described the different stages of the switching process of the cascode configuration and identified the equivalent circuit for the transitions in [104]. As in the model developed in this thesis, the parasitic inductance elements were neglected. The description of the turn-on transition is similar to the model developed in Chapter 3 of this work while the turn-off differs mainly during the transition of the current waveform. However, the equations of the main variables of the circuit were not derived since the intention of the author was just to describe the expected waveforms.

A simpler approach is presented in [112] by linearizing most of the waveforms. The approach considered all the parasitic capacitances of the circuit and the stray inductance between devices. The model succeeds in showing some of the general effects of the parameters on the switching performance, but the general waveforms do not show some of the main switching characteristics and interactions because of the assumptions and the complexity added by including the effect of the stray

inductance. The energy loss calculation has an error of less than 20% compared with simulation.

Xiucheng *et al*. developed the most complete model of the cascode configuration considering all the parasitic elements of the devices in [108] including both parasitic capacitance and inductance. The analysis divides the switching processes into stages and generates equivalent circuits for each. However, the high order of the equations makes it necessary to use specialised mathematical software to solve them. No time domain equations were derived from the model. The completeness of the model makes it a good candidate as the starting point for a simpler alternative.

Finally, SPICE models are accurate representations of the devices including all the parasitic effects. However, SPICE models may not be available and are specially designed for each device. The study of the effect of the cascode parameters in the interactions between devices using SPICE may be a challenge because of the complexity of editing the characteristics of a SPICE model. In addition, the complexity of the SPICE model may result in long simulation times.

A simpler model that allows quick and accurate energy loss predictions and that describes most of the cascode switching features is desirable to facilitate circuit design and evaluation of different transistor options.

2.8 Packaging

The small chip size of GaN transistors, the potentially high switching speeds and the sensitivity of the devices to over-voltage transients are creating a number of challenges with regard to device packaging.

The traditional through-hole package, such as that in Figure 2.13, has the advantage of high thermal capability and convenient handling/mounting. The main disadvantage relates to the high parasitic inductance of the leads. A study of the parasitic inductances of a TO-220 packaged cascode device, Figure 2.14, [110], found that L_{int3} is the most critical inductance because it is a common element for the gate loop of the Si MOSFET, the gate loop of the GaN HEMT and the power loop. It is followed by L_{int1} that is common to the GaN HEMT gate loop and the power loop and finally the source inductance that is common to the Si MOSFET gate loop and

the power loop. These inductances generate high amplitude oscillations and increase the switching times and energy losses.

Figure 2.13: GaN cascode device TO-220 through hole packaged, [113]

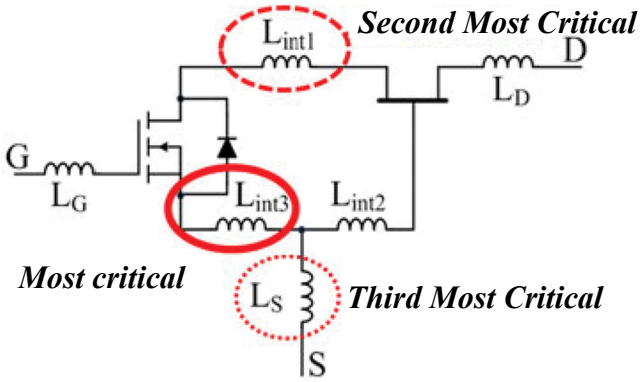


Figure 2.14: Critical parasitic inductances of the cascode configuration, [110]

As an alternative, the PQFN88 package, Figure 2.15, has a lower power capability and the thermal management is less flexible, but it has smaller parasitic inductance. The reduction of the parasitic inductance is mainly achieved by the lack of leads and because it is physically smaller. Its volume is almost one tenth of the through hole part and its pad size is 60% smaller than the D2PAK package, which is a SMD device with very similar dimensions to the TO-220, [114]. The PQFN package has a large dissipation tab that could be connected to either the drain or source terminals; Transphorm offers both versions. The drain tab version has an additional pad dedicated to the gate return, allowing the common inductance in the gate and power loops of the Si MOSFET to be minimised; L_S is zero for the package.

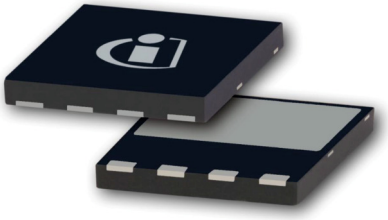


Figure 2.15: PQFN88 package, [114]

A new approach for virtually eliminating all the parasitic inductances which are common to more than one loop (L_{int1} and L_{int3}) is the stack die-structure, [115], Figure 2.16. L_{int3} is removed from the GaN HEMT gate loop by connecting the gate of the GaN HEMT directly to the Si MOSFET source. L_{int1} is eliminated by direct-soldering the drain of the Si MOSFET to the source of the GaN HEMT; the Si MOSFET is placed above the GaN HEMT for this purpose.

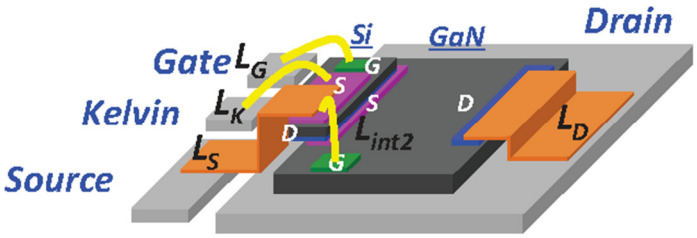


Figure 2.16: Package bonding diagram for the stack-die structure, [115]

The proposed structure significantly reduced the parasitic inductance of the cascode device, but at the expense of its thermal performance, [116]. A flip chip configuration and replacing the direct bond copper (DBC) aluminium oxide (Al_2O_3) substrate by an aluminium nitride (AlN) substrate results in improved thermal performance and maintains the benefits of the stack die-structure, [117].

Enhancement-mode single chip HEMTs can be packaged using more efficient solutions such as the approach implemented by EPC, Figure 2.17. The die of the device can be directly soldered to the printed circuit board (PCB) pads taking advantage of having all the pads on the same side of the die which results from the lateral structure, [118]. There are no wire bonds, resulting in a very low inductance and compact package.

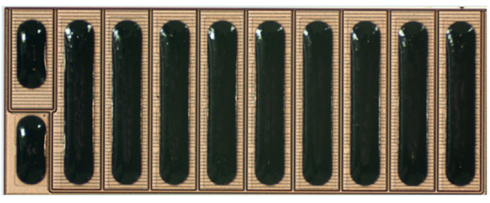


Figure 2.17: EPC enhancement mode GaN HEMT die, [119]

EPC claims that its third generation of devices can switch at more than 10MHz thanks to its improved package which includes a thicker gate pad and a dedicated gate return pad as shown in Figure 2.18, [118].

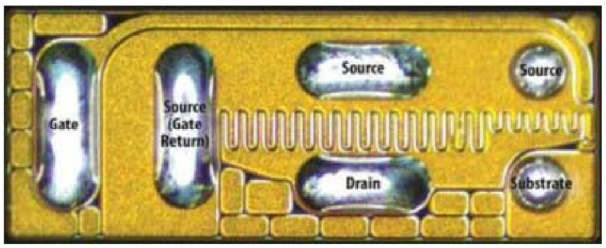


Figure 2.18: EPC third generation device, [118]

GaN Systems have also introduced a package without wire bonds for enhancement mode single chip high-voltage GaN HEMTs, [120]. The package uses a laminated structure where the connections are made by copper filled vias providing very low inductance paths as shown in Figure 2.19, [121].

The structure is used with the thermal pad on either the bottom or top side for improved thermal management.

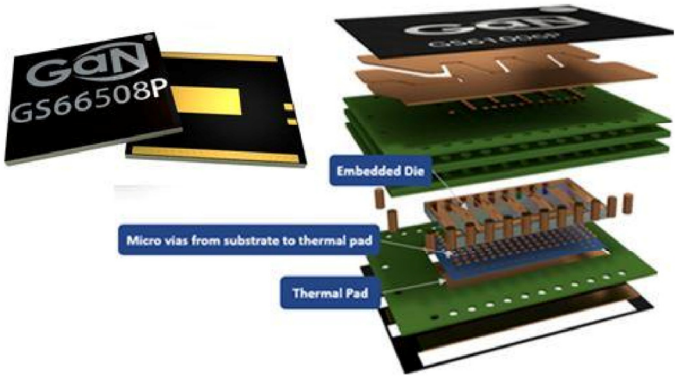


Figure 2.19: GaN Systems GaNPx package, [121]

2.9 Summary of GaN devices

Table 2.2 summarises the main parameters of the high voltage GaN diodes that have been reported whilst Table 2.3 lists the 600V transistors that are currently available.

Researchers report that the reverse recovery charge of the GaN devices is similar to their SiC equivalents, [59, 122, 123], or even lower, [124, 125] and that it is insensitive to temperature changes, [59, 122-124].

Table 2.2: Published GaN SBDs – summary of characteristics

Substrate	Breakdown Voltage (V)	I_{Fmax} (A)	V_F @ I_F	Q_{rr}	Organisation	Reference
SiC	600	2	1.6V @ 2A	5.57nC @ 300V, 2A	Technical University of Berlin	[122]
Si	600	9.2	1.1V @ 3A	10nC @ 300V, 5A	Schneider Electric (Transphorm devices)	[123]
Si	600	6	1.22V @ 3A	12nC @ 600V, 6A	Emcore Corporation	[124]
Si	600	18	0.94V @ 3A	-	Panasonic	[125]
Sapphire	747	6	1.2V @ 3A	19.7 nC @ 400V, 4A	Samsung Electronics	[59]

Table 2.3: Characteristics of main characterised GaN switches

Parameter / Device	GS66508	PGA26C09DV	TPH3006PD
Supplier	GaN Systems	Panasonic	Transphorm
Package	SMD	SMD/Through hole	Through hole
Structure	Single chip	Single chip	Cascode
Maximum breakdown voltage	650V	600V	600V
Maximum gate to source voltage	±10V	+11V (peak) +4.5V (static)	±18V
Maximum drain current at 25°C	30A	10A (SMD) / 15A (through hole)	17A
Threshold voltage at 25°C	1.6V	1.5V	1.8V
$R_{DS\text{-}ON}$ at 25°C	52mΩ	150mΩ (SMD) / 80mΩ (through hole)	150mΩ
Gate charge	6.5nC	10nC (through hole)	6.2nC

The on-state resistance of the transistors has a positive temperature coefficient, increasing by two to three as the temperature rises from 25°C to 150°C for the GaN Systems and Transphorm devices, but by 33% in the Panasonic device [123, 126, 127]. The threshold voltage of the parts is lower at higher temperature for all cases, [126-128]. Similarly, Jones *et al* reported that the transconductance of the GaN

Systems part decreases as the temperature increases having a negative effect on the turn-on loss, [127].

The switching losses of the devices are summarised in Table 2.4. The turn-off loss of all the devices is significantly smaller than the turn-on loss. The GaN Systems HEMT turn-on loss showed a positive temperature coefficient mainly at high current conditions, the reported energy loss increased 25% at 150°C with respect to the measurement at 25°C, the turn-off loss is not significantly affected by temperature, [127]. The through hole Panasonic part presents a similar behaviour, [5].

Table 2.4: Switching losses for GaN switches at: 400V, 10A, gate voltage = 8V and gate resistor = 0Ω for GS66508; 500V, 10A, gate voltage = 3.5V, turn-off gate resistor = 10 Ω and turn-on gate resistor = 33Ω for PGA26C09DV; 400V, 10A, gate voltage = 10V and gate resistor = 0Ω for TPH3006PD

Parameter / Device	**GS66508**	**PGA26C09DV**	**TPH3006PD**
Supplier	GaN Systems	Panasonic	Transphorm
Turn-off loss (μJ)	13	4	4
Turn-on loss (μJ)	28	30	23
Total loss (μJ)	41	34	27

Zhengyang *et al* compared the performance of the Transphorm cascode device against an equivalent Si super junction device finding that the turn-on loss of the Si MOSFET was almost four times the loss of the cascode device whilst the turn-off loss of the Si MOSFET was almost five times that measured in the GaN device at 15A, [110]. The higher non-linear output capacitance of the Si MOSFET contributed to higher loss in the super-junction device.

2.10 Driving GaN switches

The main challenges in driving enhancement mode GaN switches are related to their low threshold voltage, low gate to source breakdown voltage, and the oscillations induced by the high switching speed and the parasitic elements of the devices and layout, [129].

Normally-off devices such as the ones offered by EPC suffer from low threshold voltage and low gate to source breakdown voltage (around 6V). These characteristics make them especially sensitive to oscillations in the gate voltage. Operating the gate

close to 5V to get low enough drain to source resistance and with the breakdown just 1V above, presents a serious challenge. In addition, any noise in the driver signal during the off-state could trigger false turn-on compromising the integrity of the converter. Clamp circuits are recommended to avoid exceeding the maximum gate to source breakdown voltage along with dedicated gate drivers for GaN switches such as the LM5113 and LM5114 offered by Texas Instruments.

The cascode configuration provides a solution for the limited gate voltage of the GaN devices since the Si MOSFET gate to source breakdown voltage is ±18V for Transphorm devices. Driving these devices below 10V gives a comfortable margin for voltage oscillation without compromising the integrity of the part. Furthermore, adding series resistors, ferrite elements and snubber circuits have been proposed to reduce the magnitude of the gate voltage oscillations, but at the cost of increasing the switching losses, [130].

Cascode devices are also sensitive to false turn-on because of the high dV/dt of the drain to source voltage, which is a particular problem in inverter leg circuits, especially for the upper devices, careful layout design to minimise the stray inductance is recommended to reduce the risk of false turn-on, [129]. High dV/dt immunity is important for the drive circuit. Driving the gate with a negative voltage when turned-off is an additional solution, [131, 132].

The monolithic integration of drivers and power switches is an alternative solution to reduce the gate loop parasitic elements and by consequence the gate oscillations. Single packages including the driver and the power switch have been demonstrated in some of the latest publications, [133, 134].

Some authors have considered the energy efficiency of the driver and have developed resonant drivers to reduce the energy consumption by up to 50% by recycling part of the energy back to the driver power supply, [135, 136].

2.11 Thermal management

Heat removal from small SMD packages such as the PQFN88 is more challenging than in larger through hole packages since the main thermal path is through the printed circuit board (PCB) where it is soldered and only a small fraction of the heat

is dissipated from the device package to the air. The small size of the package that is the origin of the low parasitic inductance is the origin of thermal dissipation problems as well. The small dissipation area limits the heat that can be removed from the device.

The copper surface pad around the device in the same layer is often an insufficient thermal path for many applications. The typical solution is to place a heatsink on the layer opposite to the device and to interconnect both sides of the board using thermal vias, [137]. The copper thickness is also important because it affects the heat spreading along the board.

Insulated metal substrates such as T-Clad, [138], can be used as alternatives for better heat conduction from the device on the top layer to the heatsink underneath. These substrates have a very thin insulating layer and a copper or aluminium base, providing a much higher thermal conductivity than FR4. Furthermore, the board may be easily mounted onto a separate heatsink. This solution is currently used in lighting applications, [139, 140]. The drawbacks are the increased cost, [140], and higher parasitic capacitance between the device and the heatsink, [137].

2.12 Instrumentation

The high switching speed of GaN devices (more than 50V/ns and 3A/ns) requires higher performance measurement equipment than is often used in power electronics, in particular with regard to bandwidth and techniques to minimise parasitic effects.

To measure switching edges of a few ns with reasonable accuracy, an oscilloscope bandwidth of 1GHz is likely to be needed. The relationship between rise time and bandwidth for a flat response oscilloscope and 3% of rise time measurement error may be estimated by equation (2.1), [141].

$$t_r\left(ns\right)=\frac{700}{BW\left(MHz\right)} \tag{2.1}$$

Similarly, (2.2) may estimate the relation for probes, [142].

$$t_r\left(ns\right)=\frac{350}{BW\left(MHz\right)} \tag{2.2}$$

Many passive voltage probes have a maximum bandwidth of 500MHz, with a small number rated at 1GHz such as the TPP1000 of Tektronix, [143]. To minimise the potential corruption of the measured signal, compact connections, such as the ground lead become important and special adaptors may be used such as the spring ground connection that is normally available with any probe.

High voltage differential probes, [144], provide measurement convenience but tend to have a limited bandwidth of around 100MHz. As an alternative, high voltage passive probes, [145], are likely to offer more accurate measurements for signals with peak values higher than 400V.

Current measurement is particularly challenging. The common oscilloscope clamp-on current probes, such as the ones offered by Teledyne LeCroy [146], are not invasive but must be placed around the current path. The large size of the probe represents a problem since the power loop size would need to be increased, increasing the stray inductance and the oscillations. In addition, current probe bandwidths are limited to around 100MHz. This kind of probe is therefore not suitable for characterising high-speed switching devices but could be used for measurement of converter input and output currents.

The current transformers such as the ones offered by Pearson Electronics, [147], represents a more attractive option since they are more compact than the current probes and also provide galvanic isolation. The bandwidth is around 200MHz and could be used to characterise devices with special arrangements such as in [148]. The disadvantage is that it must be placed around the current path, the bandwidth is not as high as other options and it can't detect DC.

The Rogowski coils ([149]), have the advantage of being easier to place around the current path, for example some can be placed around the legs of a TO-220 package. The main drawback is that their bandwidth is limited to 30MHz and they can't measure DC signals.

Finally, current shunts such as the ones offered by T&M Research, [150], monitor the current by measuring the voltage in a coaxial low-value resistor with a bandwidth of up to 2GHz. The drawbacks are that it can't be used continuously due to its power dissipation limits, it needs to be connected in series in the circuit path and it does not

provide galvanic isolation. Although it adds some series inductance to the circuit, it has been demonstrated that it doesn't significantly affect power measurements when characterising power devices and provides one of the best measurement options, [151]. Most publications use current shunts to characterise high-speed switching devices.

2.13 Applications

The first commercially available GaN devices were developed by EPC, these single chip enhancement mode devices were rated at low voltage (≤200V) targeting low voltage DC power supplies for computers and other electronics, [152]. Later, 600V GaN switches appeared expanding the applications to grid connected circuits, motor drives, hybrid and electric vehicles and aerospace systems.

The first converter demonstrations using 600V GaN devices were DC/DC boost converters, [153, 154], due to the circuit's simple topology and wide use, for example in power factor correction (PFC) and PV circuits. These first prototypes demonstrated efficiencies above 95% switching at 1MHz, but with output power below 500W. The latest devices have allowed efficiencies in the region of 99% to be achieved, [123]. One of the highest efficiencies reported is 99.3%, [155], when switching at 100kHz and with an output power of 600W using GITs.

Figure 2.20 shows a single-phase PFC circuit in which a high purity sinusoidal current is drawn from the utility by appropriate control of transistor Q_1. Due to regulatory requirements, circuits such as this form the input stage of many items of power electronics equipment.

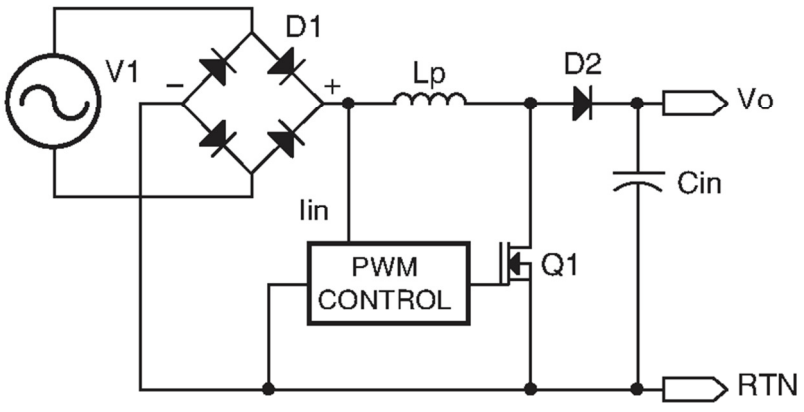


Figure 2.20: PFC circuit, [156]

Replacing Q_1 by a GaN transistor and D_2 by a SiC or GaN diode allows the operating frequency to be increased, not least due to the elimination of reverse recovery losses in D_2 if a Si diode were to be used, and results in a reduction in the size of L_p and the overall equipment. Zhehui *et al* compared a 300W, 1MHz, PFC circuit using GaN devices against a Si solution improving efficiency from 94% to 96.1% at 115VAC, [157]. Also, the increased frequency allowed an 80% reduction in the filter inductor size.

To increase the efficiency of PFC circuits, GaN devices have been used in bridgeless PFC topologies where the power path has only one diode. This operation was not feasible using Si devices because of the high switching losses resulting from the reverse recovery of the body diode, [158, 159]. A hard-switching totem-pole bridgeless PFC operating at 50kHz reached a peak efficiency of 99% at 400W using Transphorm GaN cascode switches, [158].

The frequency of the circuit may be extended to the MHz range by operating with the inductor current at the discontinuous mode boundary due to the reduced switching losses while maintaining high efficiency and reducing the size of the output and EMI filter, [159, 160]. For example, Zhengyang et al reported a system operating at 1MHz with a peak efficiency of 98.8% at 450W and a reduction of 75% in the EMI filter size against a 100kHz circuit, [159]. The main challenges of high frequency operation are related to the control, [159], and the high losses in the output filter inductor, [160].

A typical PV system is shown in Figure 2.21 and includes a boost converter circuit followed by an inverter.

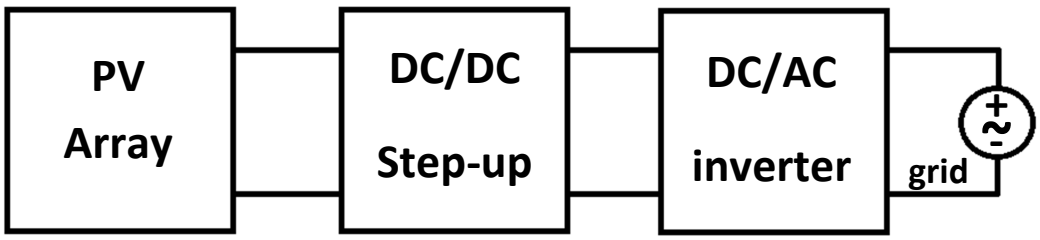


Figure 2.21: PV system diagram

Both the step-up converter and the inverter could take advantage of GaN devices and achieve efficiency improvements, reducing the cost of the solar energy by delivering

more power for the same number of panels. Also the reduced losses with GaN devices would reduce the heatsink requirements which is one of the main contributors to the cost of the system, [161]. An improvement of 1% in the efficiency of a GaN-based micro-inverter against an equivalent Si-based system at 200W and switching at 84kHz is reported in [161]. As the inverter efficiency of the Si circuit is above 97% the reduction in energy losses with GaN devices is around one third.

The GaN-based inverter circuit can also be applied to the control of motors as demonstrated in [24] where a 1.5kW three-phase half-bridge motor driver achieved 99.3% efficiency at rated power compared with 98.8% for an equivalent IGBT-based inverter, a reduction of 42% in energy losses.

The modelling and testing of GaN cascode devices in buck converters in hard/soft switching have demonstrated that these devices yield particularly high reductions in loss when operated in soft-switching, [108, 110, 162]. The efficiency of a 380V-200V, 1.2kW, 500 kHz, soft switching converter was reported to be 98.8% at rated power whilst the estimated efficiency for an equivalent super junction Si MOSFET converter was 97.7%. The GaN cascode device operating in soft-switching allowed a reduction of 48% in the converter loss, [110].

Circuits such as the half-bridge LLC resonant converter for medium power (below 500W) can take advantage of the characteristics of the GaN cascode devices achieving high efficiency at high-switching frequency. Efficiency improvements of at least 0.5% at full load in a 300W, 1MHz, LLC converter compared with a Si equivalent are reported in [128, 162]; the efficiency of the GaN converter is around 96% in both cases. These circuits are used in applications such as servers, TVs and LED lighting, [128].

Uninterruptible power supplies are another potential application of GaN devices in the 600V range at powers up to few kilowatts. These systems are becoming increasingly common to provide emergency power to critical loads such as computer servers during brown outs or complete failure of the utility. They consist of several converters which charge the battery when the utility is healthy and then convert the battery energy back to AC for the critical loads in the event of a utility failure. A demonstration presented in [123] showed that the implementation of a 500W UPS using GaN devices instead Si ones allowed the switching frequency to be increased

from 25kHz to 200kHz increasing the efficiency of the power supply by at least three percentage points in battery mode and at least six percentage points in online mode and reducing the cost by 6.8% as a result of smaller magnetic and filter devices. In addition, the converter size is reduced and the heatsink requirements are less severe.

GaN devices have also been identified as a potentially important technology for the automotive industry, particularly in hybrid electric vehicles (HEVs) and electric vehicles (EVs). Figure 2.22 presents a diagram showing some of the main functional blocks where GaN may be applied, [163].

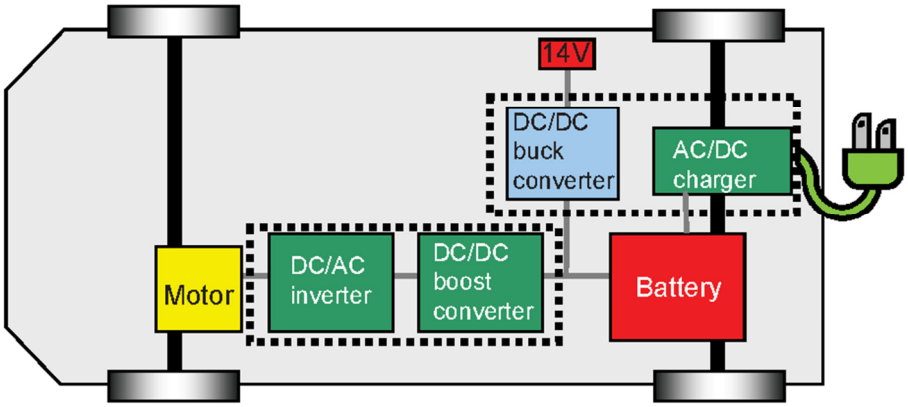


Figure 2.22: EV automotive systems, [163]

A grid connection is shown for battery charging, the battery voltage is typically 200-300V, [163]. A DC/DC converter is used to step-down the battery voltage to 14V for the accessories. The battery voltage is also boosted to supply energy to the 650V traction motor, [164].

Apart from the improved efficiency and higher operating frequency, GaN devices could contribute to one of the biggest architecture challenges in hybrid vehicles that is the unification of the cooling systems, [165]; currently two systems are used, one for the engine (typically 95°C) and another for the power electronics and traction machine (typically 60°C), [166]. The use of GaN devices operating at higher temperatures than used for Si could enable the use of higher temperature coolant for the power electronics and a single integrated on-board cooling system. However, this will require significant advances in the voltage and current capability of GaN devices and in the temperature capability of currently used packaging technologies. In

addition, challenges in the operation of the traction machine at higher temperatures need to be overcome.

The vehicle applications where there are greater, near-term prospects of using GaN devices are the accessory converters and the battery charger. Typical battery voltages are within the devices capability and the requirement for many of the 14V systems is 3.3kW, [166]. A battery charger PFC circuit was demonstrated to operate at a peak efficiency of 99% at 100kHz and 98% at 300kHz with an output power higher than 3.3kW using Transphorm devices in [165]. In addition, new reliability data meeting automotive requirements is shown. Furthermore, low voltage GaN devices could be used in the multiple converters around the accessories and electronic modules in the vehicle increasing the efficiency and power density.

The aerospace sector represents another opportunity for the 600V GaN devices. The MEA concept is giving rise to new electrical architectures for aircraft where the main voltage levels are 230VAC, 270VDC and 28VDC, [8, 167]. The 230VAC systems are sometimes variable frequency and AC/AC converters are required for the loads that need a constant frequency supply, [8]. The 270V is generated from the 230VAC variable frequency bus, [8], and GaN devices could be used to convert from AC/DC and to drive motors supplied by 270V levels. The 28V DC could also be generated from the variable frequency AC bus, [8] or the 270VDC, [167], GaN devices could be a strong option to implement this AC/DC or DC/DC conversion. The main obstacle, as in the automotive sector, is likely to be the high current and voltage ratings required for these systems, [8]. The implementation of GaN devices could help to reduce the size and weight of the electric systems and their cooling systems.

2.14 Summary of literature review

Wide bandgap materials, especially GaN and SiC, have characteristics that make them ideal candidates to replace Si for power electronic applications. Current Si-based devices are reaching their theoretical limits and are restricting the improvements in power electronic converters.

Wide bandgap materials' characteristics allow the fabrication of devices with lower on-state resistance and lower switching losses, leading to power electronic

converters with increased efficiencies or increased switching frequencies, which enable size reduction and higher power density.

Although the properties of GaN are superior to SiC, excepting the thermal conductivity, the lack of low cost and low defect density native substrates has limited GaN devices to lateral structures. GaN on Si has been demonstrated to be a cost-effective solution and has resulted in the appearance of GaN devices at Si cost.

GaN HEMTs rated at 600V started to appear in 2012 as depletion mode devices, however normally-off devices are preferred in power electronic converters for safety. The cascode structure has been used as a simple solution to generate a normally-off device from a depletion mode GaN part. Some authors have presented models of the configuration but they are very complex or very simple. There is a need for a relatively simple model that incorporates the key features of a cascode device switching transient.

Recently, 600V normally-off devices have started to appear but suffer from low gate to source breakdown voltage and low threshold voltage. The introduction of commercial GaN diodes has lagged behind the switches, however 600V Schottky diodes have appeared recently offering similar performance to established SiC counterparts but potentially at Si cost.

One of the main concerns with GaN devices is the current collapse phenomenon, an increase in channel resistance after high-voltage stress during the off-state. Most of the measurement systems are at die level or device level and require high-cost specialised equipment. Alternative measurement systems using standard laboratory instruments and realised at circuit level are starting to appear.

GaN devices have been shown to have very high switching speed and very low switching loss. The cascode devices present very low turn-off loss which makes them ideal for soft-switching topologies. However, there are some gaps in the literature with regard to how the driver parameters affect the switching speed and switching energy loss in cascode devices and in inverter leg configurations. The high switching speed and small size of GaN devices have produced new challenges in packaging and thermal management.

GaN devices rated at 600V and below have been demonstrated mainly in inverters, motor drivers, UPS, PV systems and LLC converters at powers up to a few kilowatts bringing benefits in terms of efficiency and passive component size. As the voltage and current capability of the devices increase it is anticipated that they will have a high potential to transform the performance of power electronic converters in automotive and the aerospace sectors.

Chapter 3: Modelling of cascode switching transients

3.1 Introduction

This Chapter describes a simple analytical model of the cascode switching transients. The model provides a better understanding of the switching process within the cascode arrangement and predicts the switching energy losses. The turn-off and turn-on processes are divided into four stages, similar to [108] but providing simplicity by neglecting the stray inductance and considering the parasitic capacitances and transconductances as constant. An equivalent circuit and a set of equations are written and analytically solved for each stage, the high order of the equations in more complex models make impossible to solve the equations analytically. Time domain waveforms are generated for the main voltages and currents, providing insight into the circuit operation and allowing the analysis of energy losses. The model was presented at the Applied Power Electronics Conference (APEC) 2015, [107].

3.2 Circuit and assumptions

A double pulse tester (DPT) circuit was used as a basis for the model generation. This circuit features the device under test, an inductive load and a freewheeling diode as shown in Figure 3.1. The driver switches between zero and V_{DD}. The inductor value is assumed to be very high such that I_L can be considered constant during the switching transients. The power supply establishes the operating voltage V_i of the device. The cascode consists of a low voltage silicon power MOSFET and a high-voltage, normally-on GaN HEMT. The model considers the transconductances (defined as the ratio of a variation in drain current to a variation in gate voltage) of both devices, $g_{m\text{-}Si}$ and $g_{m\text{-}GaN}$, and the inter-terminal parasitic capacitances as constants. The stray inductance is neglected for simplicity.

The cascode drain to source voltage ($v_{DS\text{-}cascode}(t)$) is the addition of the individual drain to source voltages ($v_{DS\text{-}Si}(t)$ and $v_{DS\text{-}GaN}(t)$) and is the voltage that is measured. The individual drain to source voltages can't be measured since the common node of the devices is not normally accessible. The cascode device current ($i_{cascode}(t)$) is the current that flows from the main power supply and decoupling capacitor and can be

calculated by adding $i_{D\text{-}GaN}(t)$, $i_{CDS\text{-}GaN}(t)$ and $i_{CGD\text{-}GaN}(t)$. Similar to $v_{DS\text{-}cascode}(t)$, this current represents the only current that can usually be measured in the cascode arrangement since the other currents are not accessible. The CVR represents a current measurement element with a very low resistance and virtually zero inductance.

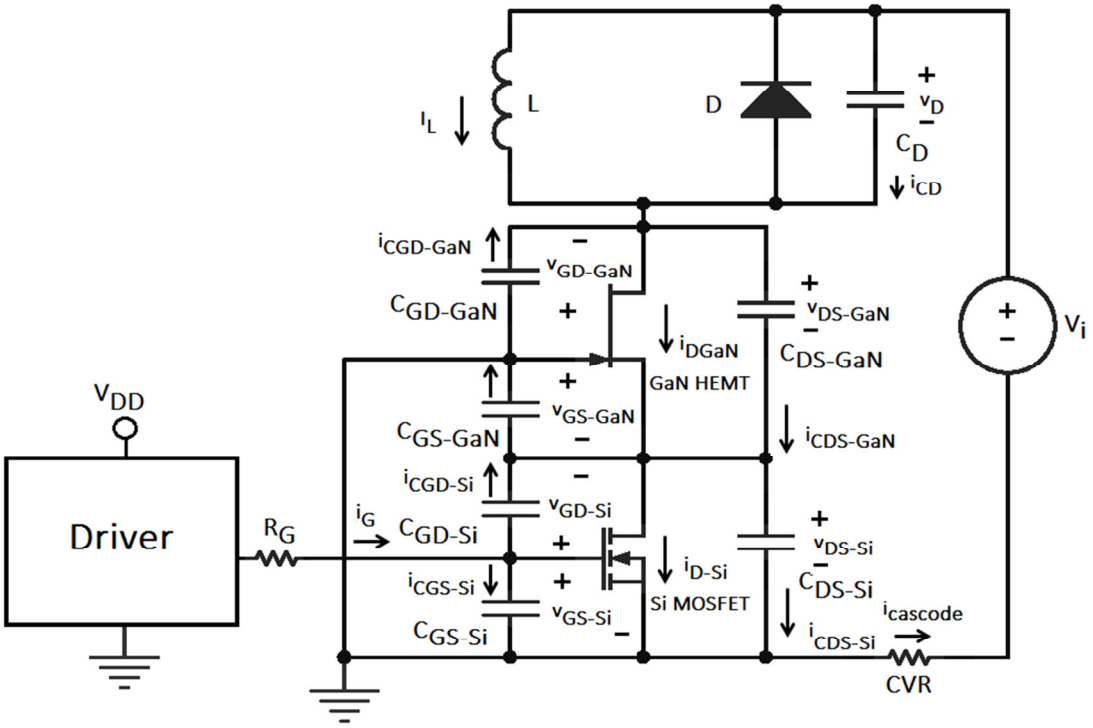


Figure 3.1: Switching circuit

3.3 Turn-off

The circuit is assumed to be under the following conditions before the turn-off process: the driver voltage is in the high state (V_{DD}), the freewheeling diode is blocking the input voltage (V_i) and the Si MOSFET and the GaN HEMT are in the conduction state. Therefore, both $v_{DS\text{-}GaN}$ and $v_{DS\text{-}Si}$ are close to zero volts and I_L is flowing through the channels of both devices.

Figure 3.2 presents the waveforms of the main variables during turn-off, [107].

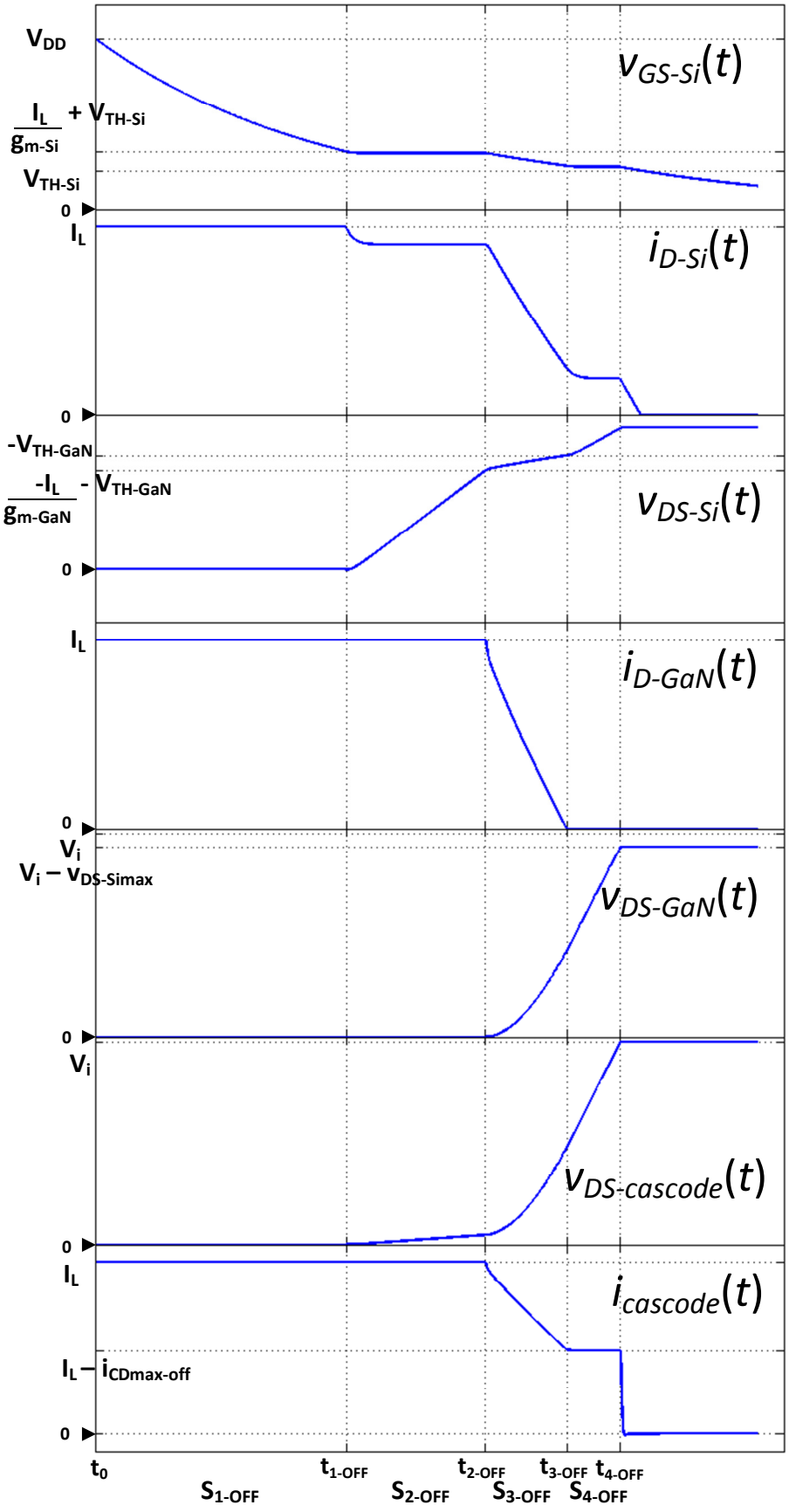


Figure 3.2: Turn-off model waveforms, [107]

3.3.1 $S_{1\text{-}OFF}$ – Si MOSFET input capacitance discharge

The driver voltage switches from V_{DD} to zero volts at the beginning of this stage discharging $C_{GS\text{-}Si}$ and $C_{GD\text{-}Si}$. By consequence, the gate to source voltage of the Si MOSFET decreases until it enters the saturation region and the following condition is met:

$$g_{m-Si}\left(v_{GS-Si}(t)-V_{TH-Si}\right)=I_L \tag{3.1}$$

where $V_{TH\text{-}Si}$ is the threshold voltage of the silicon MOSFET. All the other variables remain in the same state. Figure 3.3 presents the equivalent circuit during this stage.

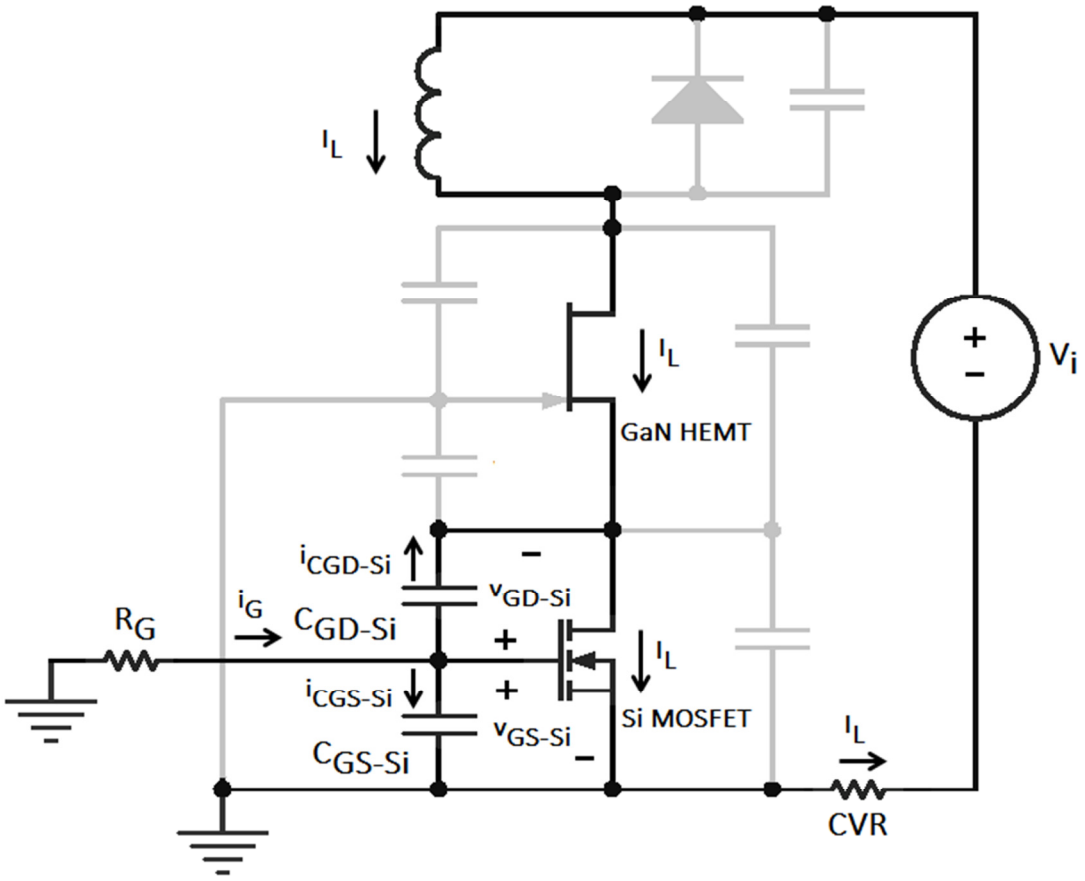


Figure 3.3: Turn-off $S_{1\text{-}OFF}$ circuit

Considering that $v_{DS\text{-}Si}(t)$ is virtually zero, $C_{GS\text{-}Si}$ and $C_{GD\text{-}Si}$ are effectively in parallel and form the input capacitance of the Si MOSFET ($C_{iss\text{-}Si}$). The following two equations can be written based on the gate current $i_G(t)$:

$$i_G(t)=-\frac{v_{GS-Si}(t)}{R_G} \tag{3.2}$$

$$i_G(t) = C_{iss-Si} \frac{dv_{GS-Si}(t)}{dt} \tag{3.3}$$

Equating (3.2) and (3.3) and solving for $v_{GS\text{-}Si}(t)$ with the initial condition $v_{GS\text{-}Si}(0) = V_{DD}$:

$$v_{GS-Si}(t) = V_{DD} e^{-\left(\frac{t}{R_G C_{iss-Si}}\right)} \tag{3.4}$$

The stage end time ($t_{1\text{-}OFF}$) can be obtained by equating (3.1) and (3.4) and solving for t, the resultant equation is:

$$t_{1-OFF} = -R_G C_{iss-Si} \ln\left(\frac{I_L + V_{TH-Si} g_{m-Si}}{V_{DD} g_{m-Si}}\right) \tag{3.5}$$

The gate to source voltage of the Si MOSFET at the end of the stage, $v_{GS\text{-}Si}(t_{1\text{-}OFF})$, is obtained by solving for $v_{GS\text{-}Si}(t)$ in (3.1):

$$v_{GS-Si}(t_{1-OFF}) = \frac{I_L}{g_{m-Si}} + V_{TH-Si} \tag{3.6}$$

There is no switching energy loss in either of the semiconductor devices since both remain in the conduction state.

3.3.2 $S_{2\text{-}OFF}$ – Si MOSFET output capacitance charge

The channel current of the Si MOSFET ($i_{D\text{-}Si}(t)$) starts to be restricted and the excess current charges the output capacitance of the Si MOSFET ($C_{GD\text{-}Si} + C_{DS\text{-}Si} + C_{GS\text{-}GaN}$) and $v_{DS\text{-}Si}(t)$ increases as a consequence.

The increase in $v_{DS\text{-}Si}(t)$ appears as a small voltage rise in the overall cascode drain to source voltage. All the other variables remain in the same state. Even though $i_{D\text{-}Si}(t)$ has changed, no change is reflected in the cascode current.

Figure 3.4 presents the equivalent circuit for this stage.

The channel current of the Si MOSFET is given by:

$$i_{D-Si}(t) = g_{m-Si}\left(v_{GS-Si}(t) - V_{TH-Si}\right) \tag{3.7}$$

Equation (3.2) is still valid for this stage. Since $v_{DS\text{-}Si}(t)$ is no longer zero, a new equation is written for the MOSFET gate node:

$$i_G(t) = C_{iss-Si}\frac{dv_{GS-Si}(t)}{dt} - C_{GD-Si}\frac{dv_{DS-Si}(t)}{dt} \tag{3.8}$$

Applying Kirchhoff's current law at the Si MOSFET drain node:

$$I_L = i_{D-Si}(t) + C_{oss-Si}\frac{dv_{DS-Si}(t)}{dt} - C_{GD-Si}\frac{dv_{GS-Si}(t)}{dt} \tag{3.9}$$

$C_{oss\text{-}Si}$ is the total effective output capacitance of the Si MOSFET including $C_{GD\text{-}Si}$, $C_{DS\text{-}Si}$ and $C_{GS\text{-}GaN}$. $C_{GS\text{-}GaN}$ is included since it is in parallel with $C_{DS\text{-}Si}$.

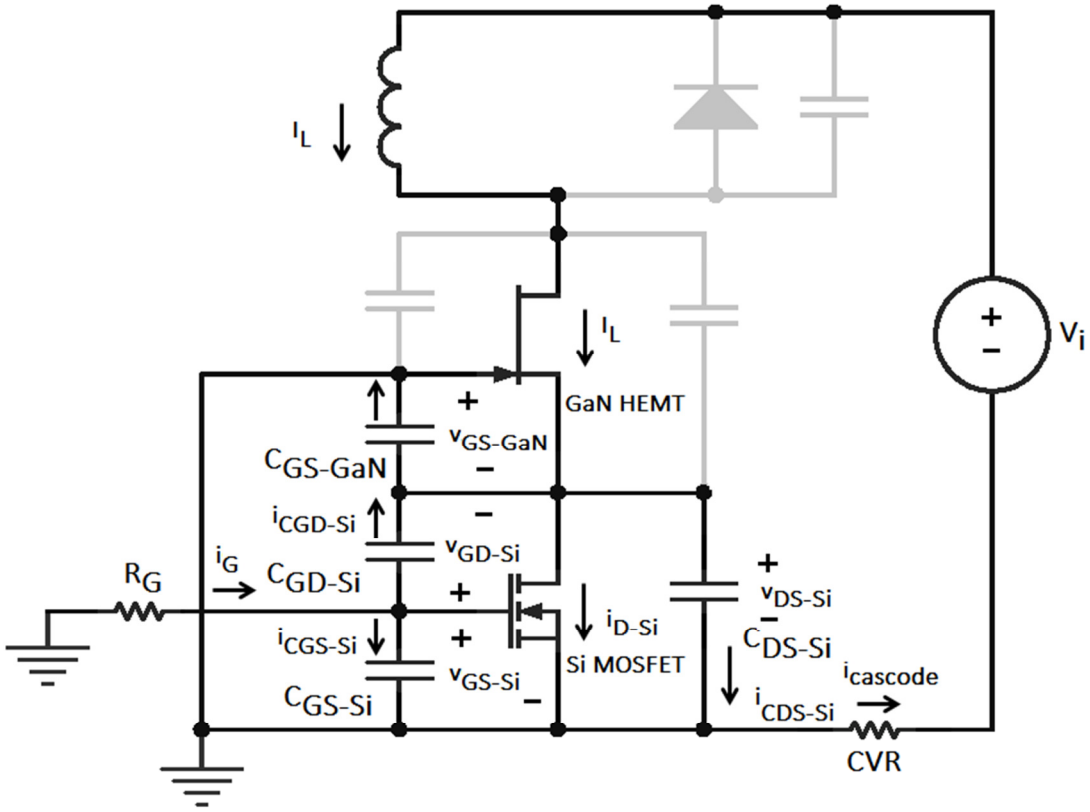


Figure 3.4: Turn-off $S_{2\text{-}OFF}$ circuit, $i_{D\text{-}Si}(t) > 0$

Equations (3.8) and (3.9) can be combined to eliminate $dv_{DS\text{-}Si}/dt$, and $i_{D\text{-}Si}$ and i_G may be eliminated using (3.7) and (3.2), allowing a solution for $v_{GS\text{-}Si}(t)$. The resultant equation is:

$$v_{GS-Si}(t) = \left(v_{GS-Si}(t_{1-OFF}) + k_{F202}\right)e^{-k_{F201}(t-t_{1-OFF})} - k_{F202} \tag{3.10}$$

The definition of the constants k_{F201} and k_{F202} can be found in the Appendix A. The constants $t_{1\text{-}OFF}$ and $v_{GS\text{-}Si}$ ($t_{1\text{-}OFF}$), defined in (3.5) and (3.6), represents the initial conditions of the stage.

The drain to source voltage of the Si MOSFET is obtained by substituting for the first derivative of $v_{GS\text{-}Si}$ in (3.8) using (3.10) and integrating, the final expression is:

$$v_{DS-Si}(t) = k_{F203}e^{-k_{F201}(t-t_{1-OFF})} + k_{F204}(t-t_{1-OFF}) - k_{F203} \tag{3.11}$$

The constants are defined in Appendix A.

This stage ends when the GaN transistor enters the linear region that is when the following condition is met:

$$g_{m-GaN}\left(-v_{DS-Si}(t) - V_{TH-GaN}\right) = I_L \tag{3.12}$$

$V_{TH\text{-}GaN}$ is the threshold voltage of the GaN HEMT.

The stage end time ($t_{2\text{-}OFF}$) may be determined by substituting for $v_{DS\text{-}Si}(t)$ in (3.12) using (3.11). However, the resulting equation can't be analytically solved. The value of $t_{2\text{-}OFF}$ may be obtained by using numerical methods. The value of $v_{GS\text{-}Si}$ at the end of the stage, $v_{GS\text{-}Si}(t_{2\text{-}OFF})$, is obtained by evaluating (3.10) for $t = t_{2\text{-}OFF}$. The value of $v_{DS\text{-}Si}$ at the end of the stage, $v_{DS\text{-}Si}(t_{2\text{-}OFF})$, is calculated from (3.12) for $t = t_{2\text{-}OFF}$.

If $v_{GS\text{-}Si}(t)$ drops below the threshold voltage $V_{TH\text{-}Si}$ before the end of this stage, then $i_{D\text{-}Si}(t)$ is equal to zero in (3.9) and the equations for $v_{GS\text{-}Si}(t)$ and $v_{DS\text{-}Si}(t)$ are as in (3.10) and (3.11) but with the constant definition changed as shown in Appendix A.

Switching losses will occur in the Si MOSFET if $v_{GS\text{-}Si}(t)$ has not decreased below the Si MOSFET threshold voltage. The switching loss can be obtained using:

$$E_{OFF-2} = \int_{t_{1-OFF}}^{t_{2-OFF}} v_{DS-Si}(t)\, i_{D-Si}(t)\, dt \tag{3.13}$$

The output capacitance of the Si MOSFET stores some energy as $v_{DS\text{-}Si}(t)$ increases. The energy obtained using $v_{DS\text{-}cascode}(t)$ and $i_{cascode}(t)$ during $S_{2\text{-}OFF}$ (as in a practical measurement) includes both the energy that is dissipated in the channel of the Si MOSFET and the energy that is stored in its output capacitance.

3.3.3 $S_{3\text{-}OFF}$ – GaN HEMT channel current fall

The gate to source voltage of the Si MOSFET continues decreasing, restricting its channel current even more. The excess current charges the output capacitance of the Si MOSFET and $v_{DS\text{-}Si}(t)$ continues rising. As $v_{DS\text{-}Si}(t)$ rises, the GaN HEMT current is restricted and the excess current charges the GaN HEMT output capacitance and $v_{DS\text{-}GaN}(t)$ increases.

The higher the restriction in $i_{D\text{-}Si}(t)$, the higher the current that charges the output capacitance of the Si MOSFET and the quicker $v_{DS\text{-}Si}(t)$ increases. For cases where R_G is very low, $v_{GS\text{-}Si}(t)$ decreases very quickly and $v_{DS\text{-}Si}(t)$ reaches $-V_{TH\text{-}GaN}$ in a very short period of time turning off the GaN HEMT channel before $v_{DS\text{-}GaN}(t)$ has risen significantly. The resulting power loss in the transistors will be very small when compared against a single device where the turn-off process involves the operating current commutating under high drain-to-source voltage conditions resulting in high instantaneous power losses. This is one of the main advantages of the cascode configuration. On the other hand, $i_{D\text{-}GaN}(t)$ commutates under high $v_{DS\text{-}GaN}(t)$ conditions when R_G has high values.

The increase in $v_{DS\text{-}GaN}(t)$ results in an equal, but opposite discharge of the freewheel diode capacitance C_D. The cascode drain to source voltage reflects the changes in $v_{DS\text{-}Si}(t)$ and $v_{DS\text{-}GaN}(t)$. The cascode current $i_{cascode}$ reflects the change in $i_{D\text{-}GaN}(t)$ but doesn't reach zero since there is current still flowing through the cascode device output capacitance.

The equivalent circuit is illustrated in Figure 3.5.

Equation (3.8) combined with (3.2) apply to this stage. The following equation can be written by applying Kirchhoff's current law to the drain of the GaN HEMT:

$$\left(C_{oss-GaN}+C_D\right)\frac{dv_{DS-GaN}\left(t\right)}{dt}+\left(C_{GD-GaN}+C_D\right)\frac{dv_{DS-Si}\left(t\right)}{dt}$$

$$+i_{D-GaN}\left(t\right)=I_L \tag{3.14}$$

where:

$$i_{D-GaN}=g_{m-GaN}\left(-v_{DS-Si}\left(t\right)-V_{TH-GaN}\right) \tag{3.15}$$

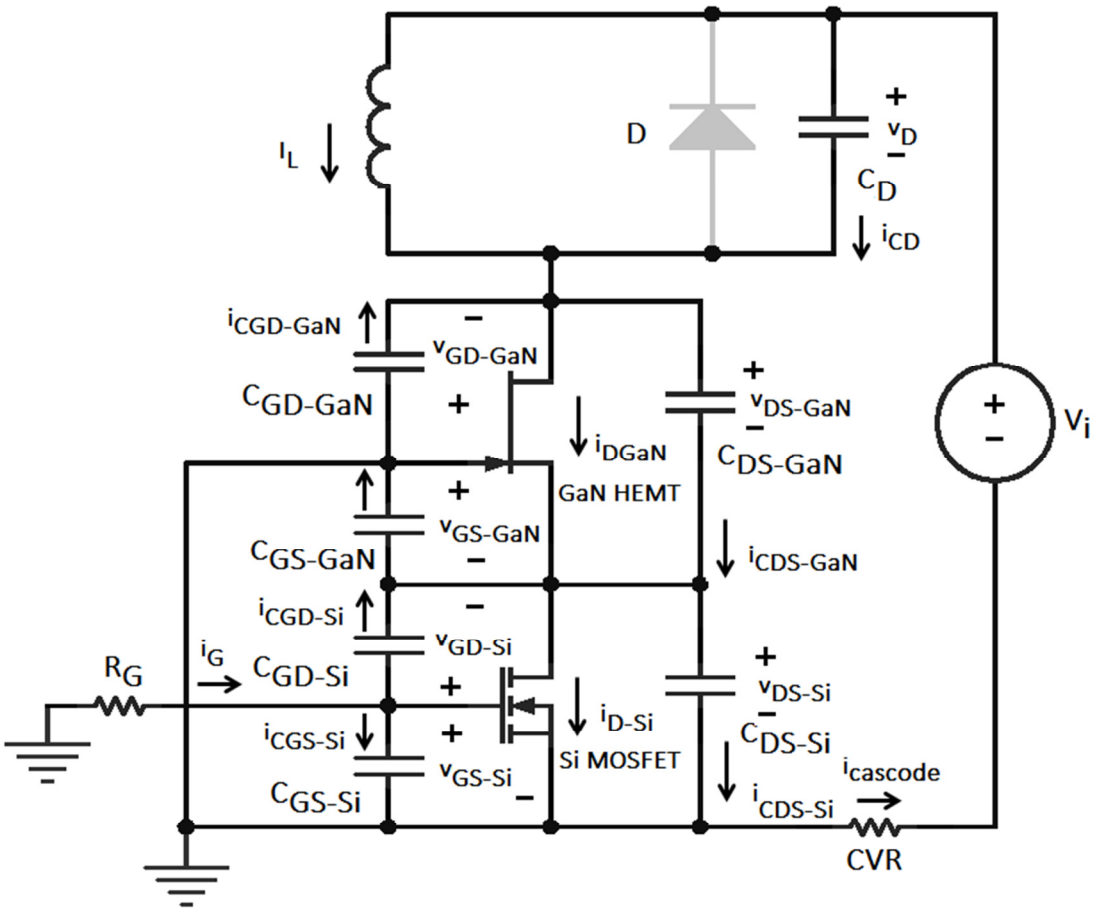


Figure 3.5: Turn-off $S_{3\text{-}OFF}$ circuit, $i_{D\text{-}Si}(t) > 0$

By applying Kirchhoff's current law to the drain of the Si MOSFET and using (3.15), the equation in (3.16) may be written.

$$C_{DS-GaN}\frac{dv_{DS-GaN}(t)}{dt} - C_{oss-Si}\frac{dv_{DS-Si}(t)}{dt} + C_{GD-Si}\frac{dv_{GS-Si}(t)}{dt}$$

$$-g_{m-GaN}v_{DS-Si}(t) - g_{m-Si}v_{GS-Si}(t) - g_{m-GaN}V_{TH-GaN} + g_{m-Si}V_{TH-Si} = 0 \quad (3.16)$$

To simplify the solution of the three differential equations with three variables, the combination of (3.8) and (3.2) is transformed to the Laplace domain and solved for $V_{GS\text{-}Si}(s)$, the resultant equations is:

$$V_{GS-Si}(s) = \frac{k_{F305}sV_{DS-Si}(s)}{s+k_{F307}} + \frac{k_{F306}}{s+k_{F307}} \quad (3.17)$$

Similarly, (3.14) is transformed to the Laplace domain and solved for $V_{DS\text{-}GaN}(s)$, the resultant expression is:

$$V_{DS-GaN}(s) = k_{F301}V_{DS-Si}(s) + \frac{k_{F302}V_{DS-Si}(s)}{s} + \frac{k_{F303}}{s^2} + \frac{k_{F304}}{s} \qquad (3.18)$$

Finally, (3.16) is transformed to the Laplace domain. The following equation is obtained:

$$C_{DS-GaN}sV_{DS-GaN}(s) - C_{oss-Si}\left(s + \frac{g_{m-GaN}}{C_{oss-Si}}\right)V_{DS-Si}(s)$$

$$+C_{GD-Si}\left(s - \frac{g_{m-Si}}{C_{GD-Si}}\right)V_{GS-Si}(s) + \frac{k_{F308}}{s} + k_{F309} = 0 \qquad (3.19)$$

where s is the Laplace operator and the constants are defined in the Appendix A. Equations (3.17) - (3.19) can be cross-substituted to eliminate two of the three variables, then reverse transformed to obtain the time domain expressions for the main voltages of the circuit. The following equation is obtained for $v_{DS\text{-}Si}(t)$:

$$v_{DS-Si}(t) = k_{F318} + k_{F319}e^{-k_{F312}(t-t_{2-OFF})} + k_{F320}e^{-k_{F313}(t-t_{2-OFF})} \qquad (3.20)$$

The gate to source voltage of the Si MOSFET is calculated from (3.17) substituting the Laplace transform of (3.20). The resultant time domain equation is:

$$v_{GS-Si}(t) = k_{F321}e^{-k_{F312}(t-t_{2-OFF})} + k_{F322}e^{-k_{F313}(t-t_{2-OFF})} + k_{F323}e^{-k_{F307}(t-t_{2-OFF})} \qquad (3.21)$$

The drain to source voltage of the GaN HEMT is obtained using (3.14) and substituting (3.20) and its first derivative, the resultant expression is:

$$v_{DS-GaN}(t) = -\frac{k_{F326}}{k_{F312}}\left(e^{-k_{F312}(t-t_{2-OFF})} - 1\right) - \frac{k_{F327}}{k_{F313}}\left(e^{-k_{F313}(t-t_{2-OFF})} - 1\right)$$

$$+\frac{k_{F325}}{k_{F324}}(t - t_{2-OFF}) + v_{DS-GaN}(t_{2-OFF}) \qquad (3.22)$$

The definition of the constants is presented in the Appendix A.

If $v_{GS\text{-}Si}(t)$ drops to the threshold voltage before the end of this stage, then $i_{D\text{-}Si}(t)$ is equal to zero and (3.16) changes to:

$$C_{DS-GaN}\frac{dv_{DS-GaN}(t)}{dt}-C_{oss-Si}\frac{dv_{DS-Si}(t)}{dt}+C_{GD-Si}\frac{dv_{GS-Si}(t)}{dt}$$

$$-g_{m-GaN}v_{DS-Si}(t)-g_{m-GaN}V_{TH-GaN}=0 \qquad (3.23)$$

The equations for $v_{GS\text{-}Si}$ (t), $v_{DS\text{-}Si}$ (t) and $v_{DS\text{-}GaN}$ (t) are given by (3.20) - (3.22) but with changes to the definition of the constants as shown in Appendix A.

This stage ends when $i_{D\text{-}GaN}$ (t) = 0. The end time of the stage, $t_{3\text{-}OFF}$, is obtained by substituting the stage ending condition in (3.15) for $t = t_{3\text{-}OFF}$, equating it with (3.20) and solving for $t_{3\text{-}OFF}$ by using a numerical method. The values of $v_{DS\text{-}Si}$, $v_{GS\text{-}Si}$ and $v_{DS\text{-}GaN}$ at the end of the stage ($v_{DS\text{-}Si}(t_{3\text{-}OFF})$, $v_{GS\text{-}Si}$ ($t_{3\text{-}OFF}$) and $v_{DS\text{-}GaN}(t_{3\text{-}OFF})$) are obtained by evaluating (3.20), (3.21) and (3.22) for $t = t_{3\text{-}OFF}$.

The main power losses in this stage occur when the GaN HEMT channel current reduces at the same time that $v_{DS\text{-}GaN}$(t) increases. This energy loss can be calculated as:

$$E_{off-3}=\int_{t_{2-OFF}}^{t_{3-OFF}} v_{DS-GaN}(t)\,i_{D-GaN}(t)\,dt \qquad (3.24)$$

Additional energy is dissipated in the Si MOSFET channel since its current is also switching simultaneously with a rising drain to source voltage. Evidently, some energy is stored in the output capacitance of both devices which form the cascode arrangement.

The energy data calculated using just $v_{DS\text{-}cascode}(t)$ and $i_{cascode}(t)$ includes the energy dissipated in both channels and the energy stored in the output capacitance of the cascode device.

3.3.4 $S_{4\text{-}OFF}$ – cascode drain-source voltage rise

After $i_{D\text{-}GaN}(t) = 0$, the entire I_L current charges the output capacitance of the GaN HEMT ($C_{oss\text{-}GaN}$), discharges the freewheel diode capacitance C_D, and $v_{DS\text{-}GaN}(t)$ increases. Similarly, the output capacitance of the Si MOSFET is charged and $v_{DS\text{-}Si}(t)$ keeps increasing. The voltage of the overall cascode arrangement increases until it reaches V_i. The current of the cascode device drops to zero instantaneously when $v_{DS\text{-}cascode} = V_i$ due to the absence of parasitic inductance that otherwise would limit the rate of current fall.

Figure 3.6 shows the equivalent circuit during this stage.

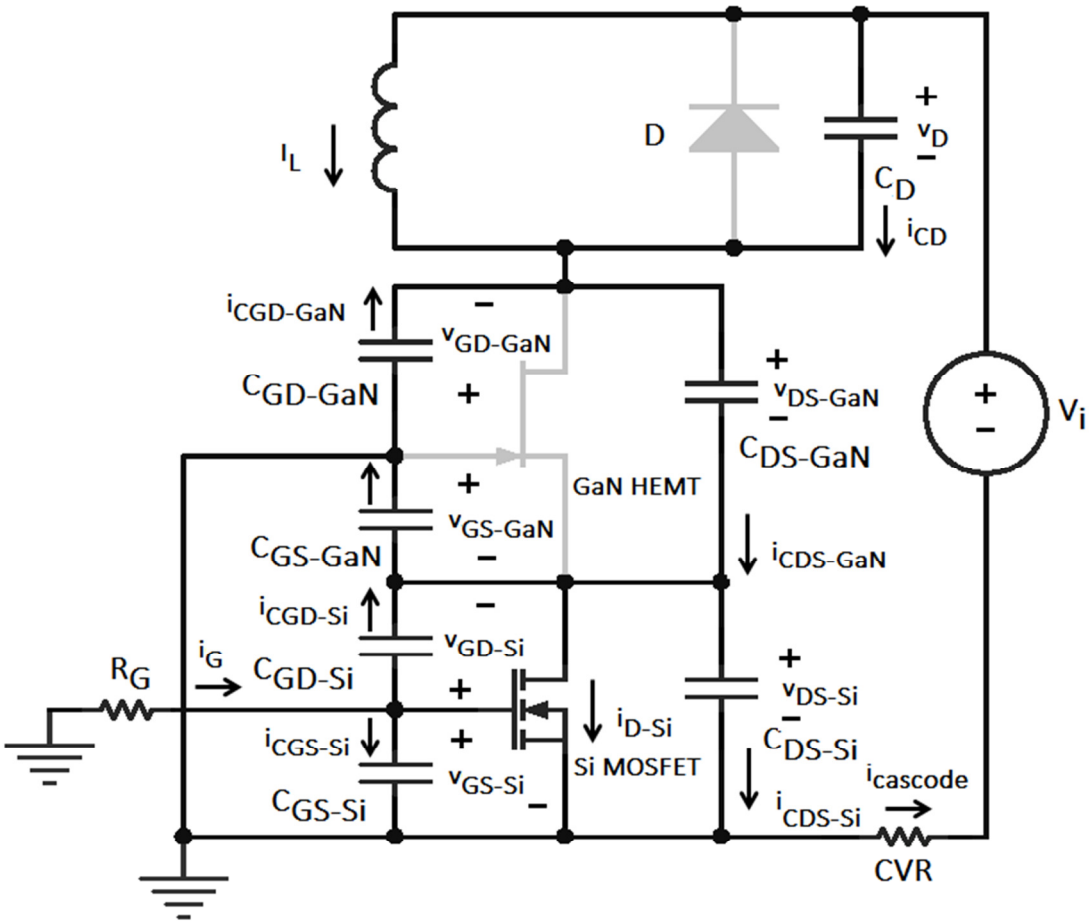


Figure 3.6: Turn-off $S_{4\text{-OFF}}$ circuit, $i_{D\text{-}Si}(t) > 0$

The combination of equations (3.8) and (3.2) is still valid for this stage. The following two equations can be written for the drain of the GaN HEMT and the drain of the Si MOSFET nodes:

$$\left(C_{oss-GaN}+C_D\right)\frac{dv_{DS-GaN}(t)}{dt}+\left(C_{GD-GaN}+C_D\right)\frac{dv_{DS-Si}(t)}{dt}=I_L \qquad (3.25)$$

$$C_{DS-GaN}\frac{dv_{DS-GaN}(t)}{dt}-C_{oss-Si}\frac{dv_{DS-Si}(t)}{dt}+C_{GD-Si}\frac{dv_{GS-Si}(t)}{dt}$$

$$-g_{m-Si}v_{GS-Si}(t)+g_{m-Si}V_{TH-Si}=0 \qquad (3.26)$$

To enable solution, the combination of equations (3.8) and (3.2) is transformed to the Laplace domain and solved for $V_{GS\text{-}Si}(s)$, the following equation is obtained:

$$V_{GS-Si}(s) = \frac{k_{F405} s V_{DS-Si}(s)}{s + k_{F407}} + \frac{k_{F406}}{s + k_{F407}} \tag{3.27}$$

Next, (3.25) is transformed to the Laplace domain and solved for $V_{DS\text{-}GaN}(s)$ obtaining:

$$V_{DS-GaN}(s) = k_{F401} V_{DS-Si}(s) + \frac{k_{F403}}{s^2} + \frac{k_{F404}}{s} \tag{3.28}$$

Equation (3.26) is finally transformed to the Laplace domain, the resultant equation is:

$$C_{DS-GaN} s V_{DS-GaN}(s) - C_{oss-Si} s V_{DS-Si}(s)$$

$$+ C_{GD-Si}\left(s - \frac{g_{m-Si}}{C_{GD-Si}}\right) V_{GS-Si}(s) + \frac{k_{F408}}{s} + k_{F409} = 0 \tag{3.29}$$

The constants are defined in Appendix A. The time domain expressions of $v_{DS\text{-}Si}(t)$ is obtained by cross-substitution between equations (3.27)-(3.29) and then inverse transformation back to the time domain. The drain-source voltage of the silicon MOSFET is obtained as:

$$v_{DS-Si}(t) = k_{F421} + k_{F422}\left(t - t_{3-OFF}\right) + k_{F423} e^{-k_{F412}\left(t - t_{3-OFF}\right)} \tag{3.30}$$

The drain to source voltage of the GaN HEMT can be obtained by substituting the first derivative of (3.30) into (3.25), the resultant expression is:

$$v_{DS-GaN}(t) = k_{F403}\left(t - t_{3-OFF}\right) + k_{F401}\left(v_{DS-Si}(t) - v_{DS-Si}\left(t_{3-OFF}\right)\right)$$

$$+ v_{DS-GaN}\left(t_{3-OFF}\right) \tag{3.31}$$

The gate to source voltage of the Si MOSFET can be calculated from (3.27) substituting the Laplace transform of (3.30). The time domain equation is:

$$v_{GS-Si}(t) = k_{F424} + k_{F425} e^{-k_{F407}\left(t - t_{3-OFF}\right)} + k_{F426} e^{-k_{F412}\left(t - t_{3-OFF}\right)} \tag{3.32}$$

If $v_{GS\text{-}Si}(t)$ drops below $V_{TH\text{-}Si}$ then $i_{D\text{-}Si}(t) = 0$. Equations (3.2), (3.8) and (3.25) are still valid but (3.26) changes to:

$$C_{DS-GaN} \frac{dv_{DS-GaN}}{dt} - C_{oss-Si} \frac{dv_{DS-Si}}{dt} + C_{GD-Si} \frac{dv_{GS-Si}}{dt} = 0 \tag{3.33}$$

Under these conditions the equations for $v_{GS\text{-}Si}$ (t), $v_{DS\text{-}Si}$ (t) and $v_{DS\text{-}GaN}$ (t) are as in (3.30) - (3.32) but the constant definitions change as shown in Appendix A.

This stage ends when $v_{DS\text{-}cascode}(t)$ is equal to V_i.

If $v_{GS\text{-}Si}(t)$ has not dropped below $V_{TH\text{-}Si}$ then there is a small power loss in the channel of the Si MOSFET. Otherwise, there is no switching loss during this stage; all the energy involved in this stage is stored in the output capacitance of the cascode arrangement.

3.4 Turn-on

The circuit is in the following conditions before the turn-on process: the driver voltage is in the low state (zero volts), both transistor channels are off and the inductor current flows through the freewheeling diode. The cascode voltage is approximately equal to V_i. Figure 3.7 shows the turn-on waveforms, [107].

3.4.1 $S_{1\text{-}ON}$ – Si MOSFET input capacitance charge

The driver voltage is switched from zero to V_{DD} at the beginning of this stage. The gate to source voltage of the Si MOSFET increases up to its threshold voltage charging the input capacitance of the Si MOSFET during this stage. All the other variables are unchanged. Figure 3.8 shows the equivalent circuit during this stage.

The following two equations can be written:

$$i_G(t)R_G + v_{GS-Si}(t) = V_{DD} \tag{3.34}$$

$$i_G(t) = C_{iss-Si}\frac{dv_{GS-Si}(t)}{dt} \tag{3.35}$$

Equating (3.34) and (3.35):

$$\frac{dv_{GS-Si}(t)}{dt} + \frac{v_{GS-Si}(t)}{R_G(C_{iss-Si})} = \frac{V_{DD}}{R_G(C_{iss-Si})} \tag{3.36}$$

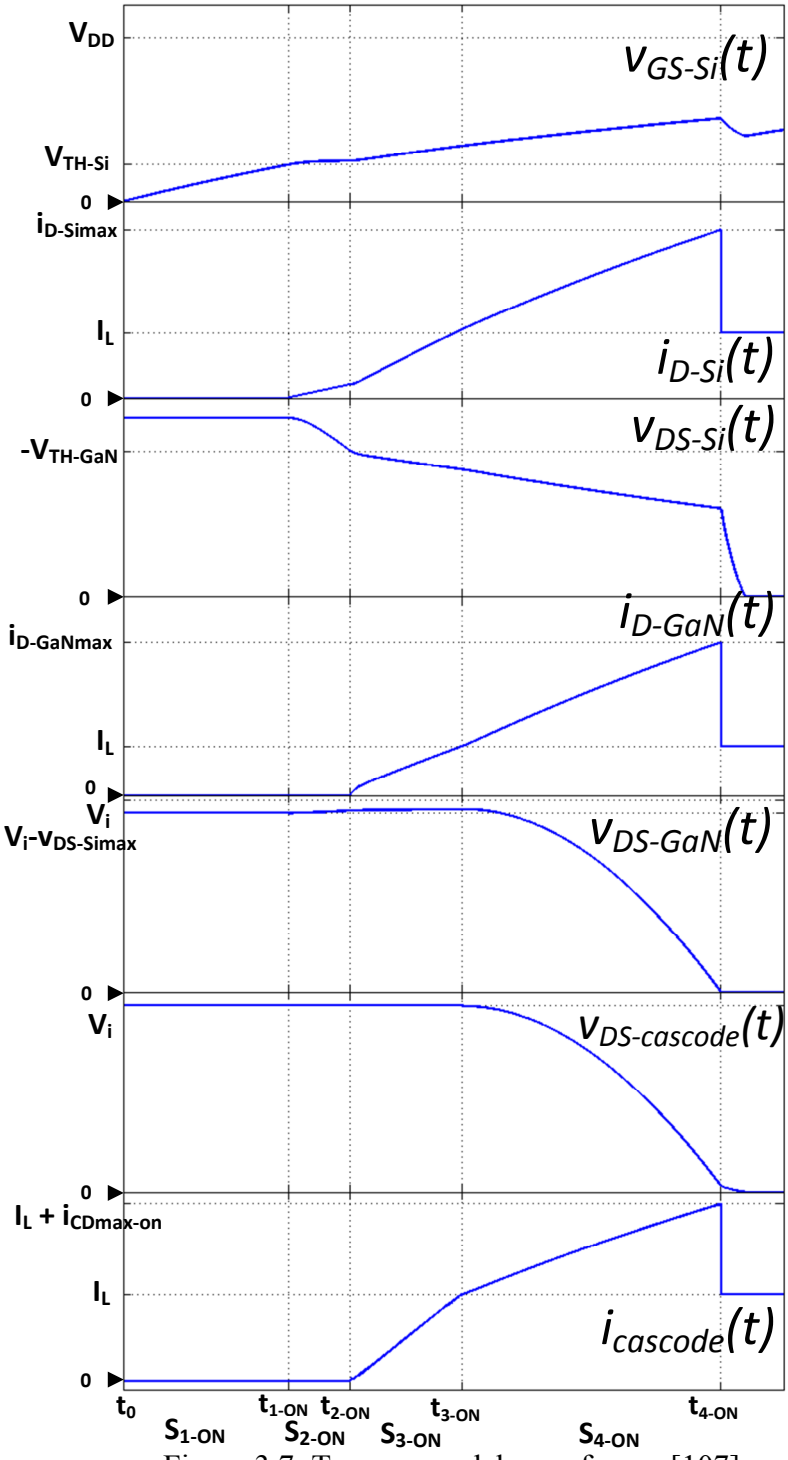


Figure 3.7: Turn-on model waveforms, [107]

Solving (3.36):

$$v_{GS-Si}(t) = V_{DD}\left(1 - e^{-\frac{t}{R_G C_{iss-Si}}}\right) \tag{3.37}$$

The gate to source voltage is the only variable changing and there is no switching loss since both channels are off.

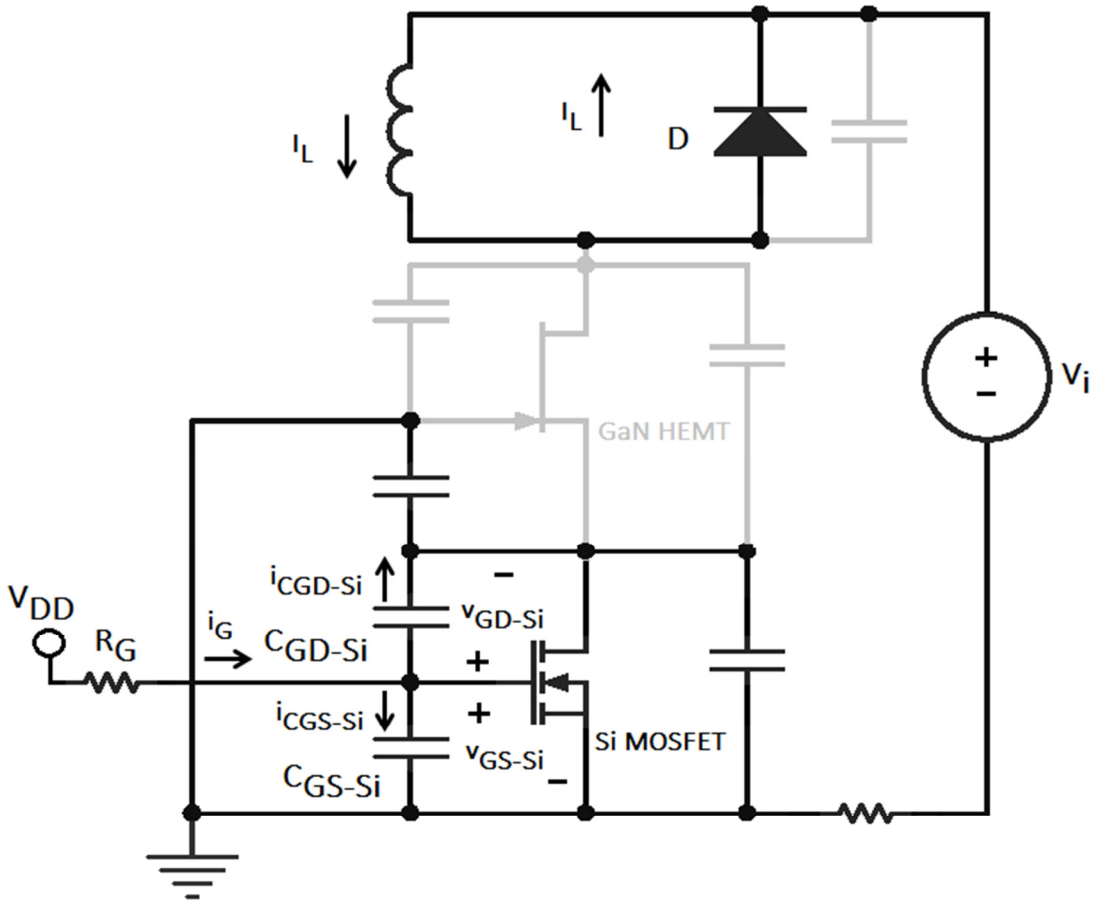


Figure 3.8: Turn-on $S_{1\text{-}ON}$ circuit

The stage ends when $v_{GS\text{-}Si} = V_{TH\text{-}Si}$. The stage end time, $t_{1\text{-}ON}$, is obtained using (3.37) and using the stage end condition for $t = t_{1\text{-}ON}$:

$$t_{1-ON} = R_G \left(C_{iss-Si}\right) \ln\left(\frac{V_{DD}}{V_{DD} - V_{TH-Si}}\right) \tag{3.38}$$

3.4.2 $S_{2\text{-}ON}$ – Si MOSFET output capacitance discharge

Once $v_{GS\text{-}Si}(t)$ exceeds the MOSFET threshold voltage $V_{TH\text{-}Si}$, the channel of the Si MOSFET starts to conduct. This current discharges the output capacitance of the Si MOSFET and $v_{DS\text{-}Si}(t)$ starts to decrease. The drain to source voltage of the GaN HEMT increases slightly as $v_{DS\text{-}Si}(t)$ decreases. The overall cascode drain to source voltage and cascode current remain unchanged.

Figure 3.9 shows the equivalent circuit during this stage.

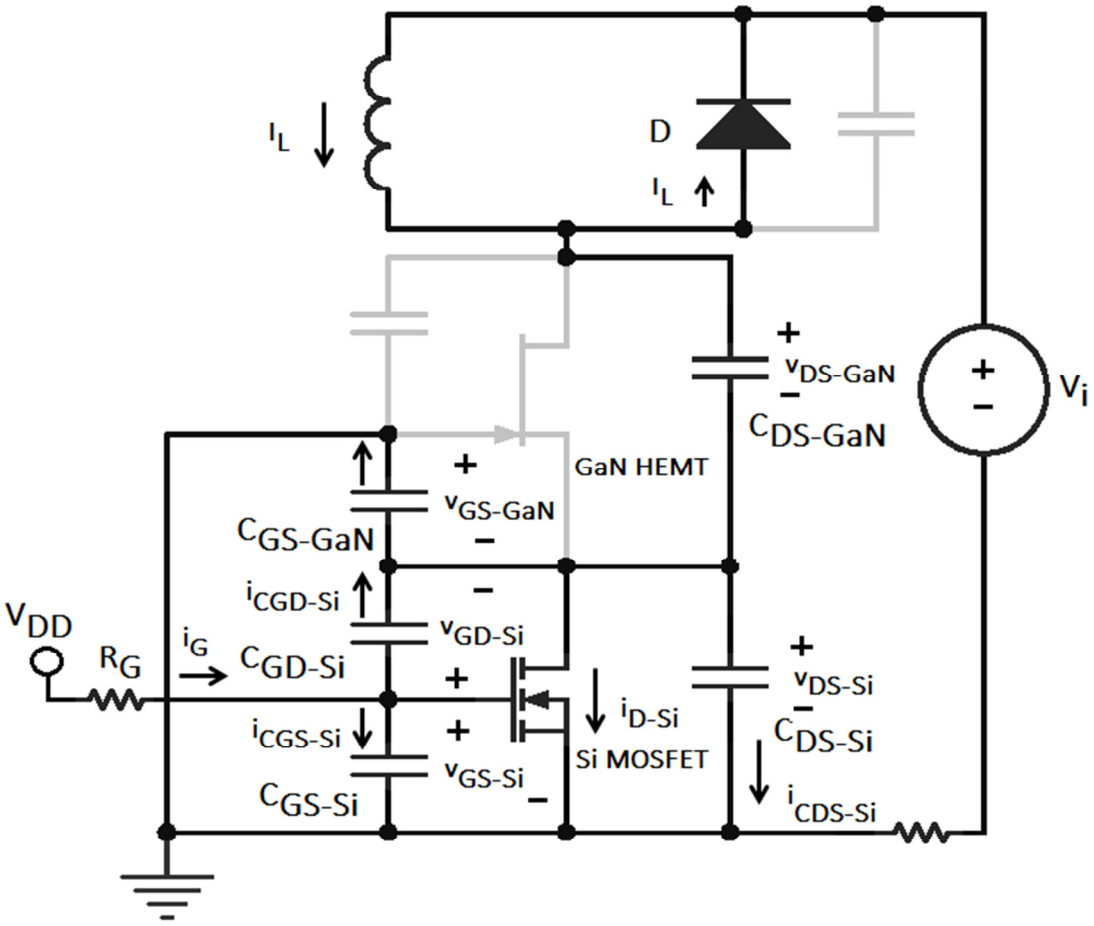


Figure 3.9: Turn-on $S_{2\text{-ON}}$ circuit

Similar to the analysis for stage 2 of the turn-off process ($S_{2\text{-OFF}}$) in section 3.3.2, the rate of change of MOSFET drain-source voltage may be related to the gate circuit conditions by equation (3.39).

$$\frac{dv_{DS-Si}(t)}{dt} = \frac{C_{iss-Si}}{C_{GD-Si}}\frac{dv_{GS-Si}(t)}{dt} + \frac{v_{GS-Si}(t)}{R_G C_{GD-Si}} - \frac{V_{DD}}{R_G C_{GD-Si}} \qquad (3.39)$$

Equation (3.7) describes the channel current of the Si MOSFET.

Applying Kirchhoff current law to the drain of the Si MOSFET results in:

$$g_{m-Si}\left(v_{GS-Si}(t) - V_{TH-Si}\right) = C_{GD-Si}\frac{dv_{GS-Si(t)}}{dt} - C_{oss-Si}\frac{dv_{DS-Si}(t)}{dt} \qquad (3.40)$$

where $C_{oss\text{-}Si}$ is as before the total effective output capacitance of the Si MOSFET and includes $C_{DS\text{-}Si}$, $C_{GD\text{-}Si}$ and $C_{GS\text{-}GaN}$.

Combining equations (3.39) and (3.40) to eliminate $dv_{DS\text{-}Si}/dt$ and solving for $v_{GS\text{-}Si}(t)$:

$$v_{GS-Si}(t) = \left(v_{GS-Si}(t_{1-ON}) + k_{N202}\right)e^{-k_{N201}\left(t-t_{1-ON}\right)} - k_{N202} \tag{3.41}$$

The expression for $v_{DS\text{-}Si}(t)$ can then be obtained by substituting (3.41) and its derivative back into (3.39):

$$v_{DS-Si}(t) = k_{N203}e^{-k_{N201}\left(t-t_{1-ON}\right)} + k_{N204}\left(t - t_{1-ON}\right) + v_{DS-Si}(t_{1-ON}) - k_{N203} \tag{3.42}$$

where $t_{1\text{-}ON}$ is defined in (3.38). The constants in equations (3.41) and (3.42) are defined in Appendix A.

This stage ends when $v_{DS\text{-}Si}(t) = -V_{TH\text{-}GaN}$. This condition is substituted into (3.42) and solved for t using numerical methods to obtain the stage end time, $t_{2\text{-}ON}$, this value is substituted into (3.41) and (3.42) to obtain $v_{GS\text{-}Si}(t_{2\text{-}ON})$ and $v_{DS\text{-}Si}(t_{2\text{-}ON})$ which are the final values of the variables and the initial conditions of the next stage.

Part of the energy stored in the output capacitance of the Si MOSFET is dissipated in the channel of the Si MOSFET during this stage. The energy can be calculated using:

$$E_{on-2} = \int_{t_{1-ON}}^{t_{2-ON}} v_{DS-Si}(t)\, i_{D-Si}(t)\, dt \tag{3.43}$$

3.4.3 $S_{3\text{-}ON}$ – GaN HEMT channel current rise

The gate to source voltage of the Si MOSFET continues increasing and $i_{D\text{-}Si}(t)$ increases further. As $i_{D\text{-}Si}(t)$ increases, $v_{DS\text{-}Si}(t)$ decreases and $v_{GS\text{-}GaN}(t)$ increases, resulting in a rising current through the channel of the GaN HEMT. The rate of rise of current is driven by the rate of change of $v_{DS\text{-}Si}(t)$. The inductor current is transferred from the freewheel diode to the cascode channel during this stage. The drain voltage of the GaN HEMT is assumed to remain constant for simplicity. The cascode overall voltage remains unchanged since any changes in $v_{DS\text{-}Si}(t)$ are compensated by an equal and opposite change in $v_{DS\text{-}GaN}(t)$. The cascode current is determined by the change in $i_{D\text{-}GaN}(t)$.

The inductor current is shared between the freewheeling diode and the channel of the GaN HEMT.

Figure 3.10 shows the equivalent circuit during this stage.

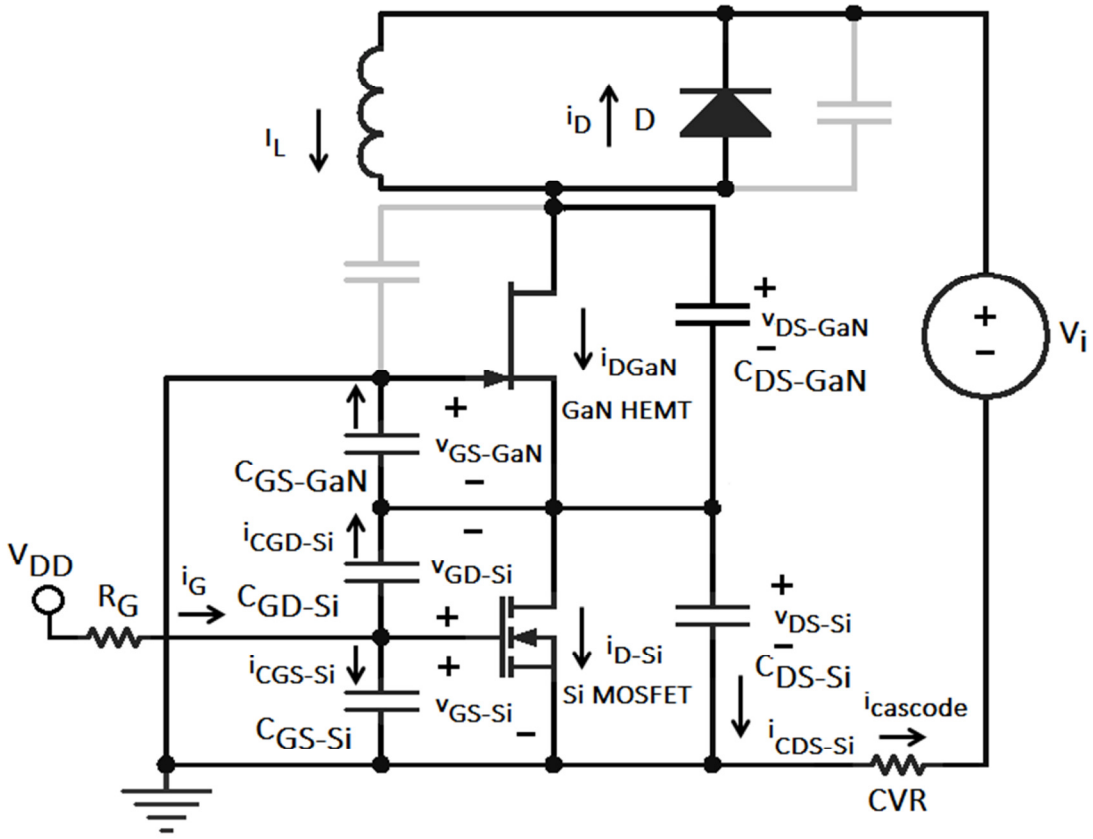


Figure 3.10: Turn-on $S_{3\text{-ON}}$ circuit

Equation (3.39) in turn-on stage $S_{2\text{-ON}}$, section 3.4.2 is still valid and in addition:

$$\frac{dv_{DS-Si}(t)}{dt}+\frac{dv_{DS-GaN}(t)}{dt}=0 \tag{3.44}$$

Applying Kirchhoff's current law at the drain of the Si MOSFET:

$$g_{m-Si}\left(v_{GS-Si}(t)-V_{TH-Si}\right)+C_{oss-Si}\frac{dv_{DS-Si}(t)}{dt}=C_{GD-Si}\frac{dv_{GS-Si}(t)}{dt}$$

$$+C_{DS-GaN}\frac{dv_{DS-GaN}(t)}{dt}+g_{m-GaN}\left(-v_{DS-Si}(t)-V_{TH-GaN}\right) \tag{3.45}$$

Equations (3.39), (3.44) and (3.45) form a set of three differential equations with three variables. By eliminating $v_{DS\text{-}GaN}$ by cross-substituting, then transforming into the Laplace domain, expressions in terms of $V_{GS\text{-}Si}(s)$ and $V_{DS\text{-}Si}(s)$ are obtained:

$$V_{GS-Si}(s)=\frac{k_{N306}s}{s+k_{N304}}V_{DS-Si}(s)+\frac{k_{N307}}{s\left(s+k_{N304}\right)}+\frac{k_{N308}}{s+k_{N304}} \tag{3.46}$$

$$\left(k_{N309}s + g_{m-GaN}\right)V_{DS-Si}\left(s\right) = \left(C_{DS-Si}s - g_{m-Si}\right)V_{GS-Si}\left(s\right) + \frac{k_{N310}}{s} + k_{N311} \quad (3.47)$$

The time domain expression for $v_{DS\text{-}Si}(t)$ is obtained by eliminating $v_{GS\text{-}Si}(t)$ between equations (3.46) and (3.47) and reverse transforming the expression:

$$v_{DS-Si}\left(t\right) = k_{N320} + k_{N321}e^{-k_{N315}\left(t-t_{2-ON}\right)} + k_{N322}e^{-k_{N316}\left(t-t_{2-ON}\right)} \quad (3.48)$$

The gate to source voltage of the Si MOSFET is then obtained using (3.46) and the Laplace transform of (3.48):

$$v_{GS-Si}\left(t\right) = k_{N323} + k_{N324}e^{-k_{N315}\left(t-t_{2-ON}\right)} + k_{N325}e^{-k_{N316}\left(t-t_{2-ON}\right)} + k_{N326}e^{-k_{N304}\left(t-t_{2-ON}\right)} \quad (3.49)$$

The definitions of the constants in equations (3.48) and (3.49) can be found in Appendix A.

This stage ends when $i_{D\text{-}GaN}(t)$ is equal to the inductor current I_L. The end time of the stage, $t_{3\text{-}ON}$, is determined by substituting the stage end condition ($i_{D\text{-}GaN}(t) = I_L$) and $v_{DS\text{-}Si}$ of (3.48) into (3.15) of section 3.3.3 and solving for t. The final values of $v_{GS\text{-}Si}$ and $v_{DS\text{-}Si}$ ($v_{GS\text{-}Si}(t_{3\text{-}ON})$ and $v_{DS\text{-}Si}(t_{3\text{-}ON})$) which are the initial conditions for the next stage are obtained by evaluating (3.48) and (3.49) for $t = t_{3\text{-}ON}$.

The power losses mainly occur in the channel of the GaN HEMT during the increase of its current under high voltage conditions, additional energy is dissipated in the channel of the Si MOSFET since $i_{D\text{-}Si}(t)$ rises as $v_{DS\text{-}Si}(t)$ decreases, but this energy is not as high as that in the channel of the GaN HEMT. The energy losses can be calculated using:

$$E_{on-3} = \int_{t_{2-ON}}^{t_{3-ON}} v_{DS-GaN}\left(t\right)i_{D-GaN}\left(t\right)dt + \int_{t_{2-ON}}^{t_{3-ON}} v_{DS-Si}\left(t\right)i_{D-Si}\left(t\right)dt \quad (3.50)$$

3.4.4 $S_{4\text{-}ON}$ – cascode drain-source voltage fall

Once the channel of the GaN HEMT is conducting the inductor current, its output capacitance starts to be discharged and $v_{DS\text{-}GaN}(t)$ decreases. As $v_{DS\text{-}GaN}(t)$ falls there will be a corresponding rise in the voltage of the freewheeling diode, charging its parasitic capacitance C_D. This current is added to the inductor current and appears as a current overshoot in the cascode current waveform. The change in both $v_{DS\text{-}Si}(t)$ and

$v_{DS\text{-}GaN}(t)$ is reflected in $v_{DS\text{-}cascode}(t)$. $C_{DS\text{-}GaN}$ and $C_{GD\text{-}GaN}$ are discharged directly into the channel of the GaN HEMT and this current is not part of $i_{cascode}(t)$. The same applies to the output capacitance of the Si MOSFET.

Figure 3.11 shows the equivalent circuit during this stage.

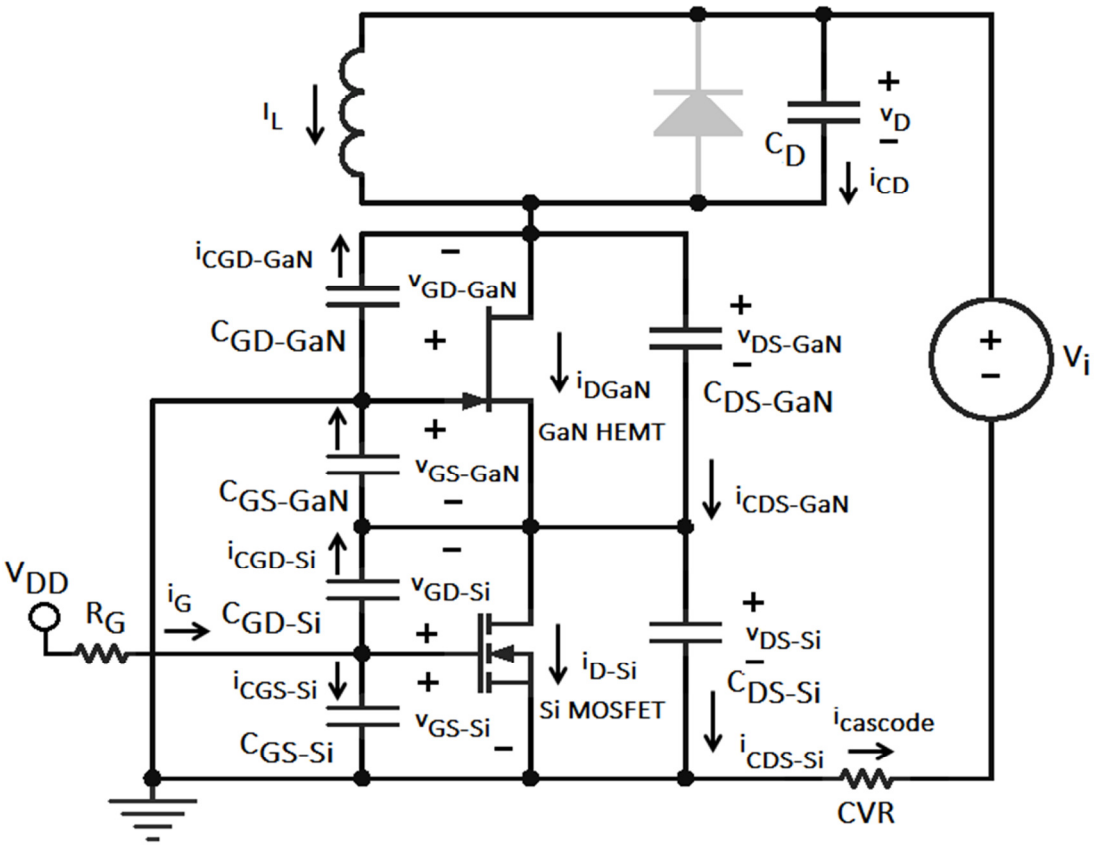


Figure 3.11: Turn-on $S_{4\text{-}ON}$ circuit

Applying Kirchhoff's current law at the drain of the GaN HEMT:

$$\left(C_{oss-GaN}+C_D\right)\frac{dv_{DS-GaN}(t)}{dt}=-\left(C_{GD-GaN}+C_D\right)\frac{dv_{DS-Si}(t)}{dt}+g_{m-GaN}v_{DS-Si}(t)$$

$$+g_{m-GaN}V_{TH-GaN}+I_L \qquad (3.51)$$

Equations (3.39) and (3.45) for the MOSFET are still valid for this stage. Transforming equations (3.39) and (3.51) into the Laplace domain and solving for $V_{GS\text{-}Si}(s)$ and $V_{DS\text{-}GaN}(s)$ respectively results in:

$$V_{GS-Si}(s)=\frac{k_{N406}s}{s+k_{N404}}V_{DS-Si}(s)+\frac{k_{N407}}{s\left(s+k_{N404}\right)}+\frac{k_{N408}}{s+k_{N404}} \qquad (3.52)$$

$$V_{DS-GaN}(s) = k_{N401}\frac{s+k_{N402}}{s}V_{DS-Si}(s) + \frac{k_{N403}}{s^2}$$

$$+\frac{v_{DS-GaN}(t_{3-ON}) - k_{N401}v_{DS-Si}(t_{3-ON})}{s} \quad (3.53)$$

Finally, transforming (3.45) into the Laplace domain:

$$(k_{N409}s + g_{m-GaN})V_{DS-Si}(s) = (C_{GD-Si}s - g_{m-Si})V_{GS-Si}(s)$$

$$+C_{DS-GaN}sV_{DS-GaN}(s) + \frac{k_{N410}}{s} + k_{N411} \quad (3.54)$$

Equations (3.52) and (3.53) are substituted into (3.54) and then reverse transformed to obtain the time domain expression of $v_{DS\text{-}Si}(t)$. The following equation is obtained for $v_{DS\text{-}Si}(t)$:

$$v_{DS-Si}(t) = k_{N420} + k_{N421}e^{-k_{N415}(t-t_{3-ON})} + k_{N422}e^{-k_{N416}(t-t_{3-ON})} \quad (3.55)$$

Next, $v_{GS\text{-}Si}$ can be obtained by substituting the Laplace transform of (3.55) into (3.52) and reverse transforming. The following equation is obtained.

$$v_{GS-Si}(t) = k_{N423} + k_{N424}e^{-k_{N415}(t-t_{3-ON})} + k_{N425}e^{-k_{N416}(t-t_{3-ON})}$$

$$+k_{N426}e^{k_{N404}(t-t_{3-ON})} \quad (3.56)$$

Similarly, $v_{DS\text{-}GaN}$ can be calculated by substituting the Laplace transform of (3.55) into (3.53) and reverse transforming. The obtained time domain expression is:

$$v_{DS-GaN}(t) = k_{N427} + k_{N428}(t-t_{3-ON}) + k_{N429}e^{-k_{N415}(t-t_{3-ON})}$$

$$+k_{N430}e^{-k_{N416}(t-t_{3-ON})} \quad (3.57)$$

This stage ends when $v_{DS\text{-}GaN}$ reaches its conduction value, ideally zero. After this, the remaining energy stored in the output capacitance of the Si MOSFET is discharged through its channel.

The main losses during this stage occur in the channel of the GaN HEMT since the drain to source voltage switches under high channel current conditions. Additional power loses are present in the channel of the Si MOSFET as $v_{DS\text{-}Si}$ decreases under high current conditions. The energy can be calculated with the following expression:

$$E_{on-4} = \int_{t_{3-ON}}^{t_{4-ON}} v_{DS-GaN}(t) i_{D-GaN}(t) dt + \int_{t_{3-ON}}^{t_{4-ON}} v_{DS-Si}(t) i_{D-Si}(t) dt \qquad (3.58)$$

The energy loss calculated using $v_{DS\text{-}cascode}(t)$ and $i_{cascode}(t)$ will be an under-estimate since it does not include the energy stored in the output capacitance of the cascode transistor.

3.5 MatLab implementation

MatLab was used to generate plots and to calculate the energy losses of the switching transients based in the developed simple model.

Two different MatLab scripts were developed for the implementation, one for the turn-off transient and another for the turn-on transient. Each script is divided into four different sections: parameters definition, stages definition, plots generation and energy losses summary.

Parameters definition

The time resolution of the calculations, operating and driver conditions and devices' parameters such as threshold voltage, transconductance and parasitic capacitances are defined in this section.

Stages definition

The switching transient stages are defined in this section. This section is divided into four different subsections, one per switching stage. Each subsection is implemented as described next.

First, the initial conditions and constants for the stage are defined. Next, the duration of each stage is calculated to generate the time arrays for the electrical variables and then the main current, voltage and power variables are calculated including the energy losses calculations as described in sections 3.3 and 3.4.

Plots generation

The plots of the main parameters of the switching transients are generated. Examples of the generated plots are presented in sections 3.6.2 and 3.6.3.

Energy losses summary

A summary of the different energy losses per stage is displayed in a text box and an example of the values provided is shown in section 3.7.

3.6 Model validation

A Transphorm TPH3006LD GaN cascode device rated at 600V, 17A (at T_j = 25°C) and $R_{DS\text{-}ON}$ = 0.15Ω (typical at T_j = 25°C) was used to validate the model. The following sections present a summary of how the model parameters were determined using the SPICE model of the device and the characteristics of the model accuracy.

The model provides a simple and accurate alternative to evaluate and compare devices when SPICE models are not available. The time of development of SPICE models can be long because of the complexity of accurately deriving all the parameters such as the parasitic inductances whilst the simple model parameters can be easily derived by the device manufacturers.

3.6.1 Model parameters

The parameters required to validate the simple model were derived from the SPICE model of the GaN cascode part provided by Transphorm. Practical measurement of the parameters was not possible since the two devices were in a single package. The individual cascode devices (the GaN HEMT and Si MOSFET) were split to determine their individual capacitance, transconductance and threshold voltage. The derivation of the different parameters is presented next.

Internal gate resistor

The SPICE model shows an internal 6Ω gate resistor connected to the gate terminal of the Si MOSFET. This value will be added to any external gate resistor.

Threshold voltages

The SPICE parameters of the Si MOSFET show that the threshold voltage of the Si MOSFET ($V_{TH\text{-}Si}$) is 2.25V whilst the threshold voltage of the GaN HEMT ($V_{TH\text{-}GaN}$) is -22V.

Transistors' capacitances and transconductance

The gate-source, gate-drain and drain-source capacitances ($C_{GS\text{-}Si}$, $C_{GD\text{-}Si}$ and $C_{DS\text{-}Si}$) were obtained by small signal AC analysis of the device at 1MHz. The devices' capacitance is frequency independent; 1 MHz was selected for being the test frequency typically specified in manufacturers' datasheets. $C_{GS\text{-}Si}$ and $C_{GD\text{-}Si}$ are obtained using the circuit shown in Figure 3.12, the DC power supply connected between drain and source sets the drain-source voltage and the power supply from gate to source injects a 0.5V, 1MHz AC signal for the capacitance evaluation. The gate-source impedance ($Z_{GS\text{-}Si}$) is calculated from the AC voltage and source current ($i_{S\text{-}Si}$) whilst the gate-drain impedance ($Z_{GD\text{-}Si}$) is calculated from the AC voltage and the drain current ($i_{D\text{-}Si}$).

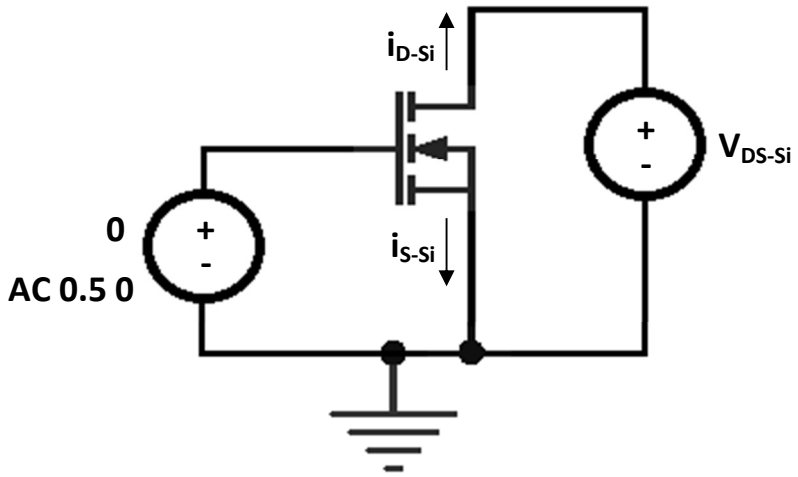


Figure 3.12: SPICE small signal AC analysis for input capacitance evaluation

The equivalent capacitances are then obtained using the following equations:

$$C_{GS-Si} = \frac{1}{2\pi f Z_{GS-Si}} \tag{3.59}$$

$$C_{GD-Si} = \frac{1}{2\pi f Z_{GD-Si}} \tag{3.60}$$

The drain-source capacitance ($C_{DS\text{-}Si}$) is obtained similarly but with a short-circuit between the gate and source and adding the AC signal in series with the power supply connected to the drain and source terminals as in Figure 3.13. The drain-source impedance ($Z_{DS\text{-}Si}$) is calculated from the AC voltage and the source current. The drain-source capacitance is then calculated as follows:

$$C_{DS-Si} = \frac{1}{2\pi f Z_{DS-Si}} \tag{3.61}$$

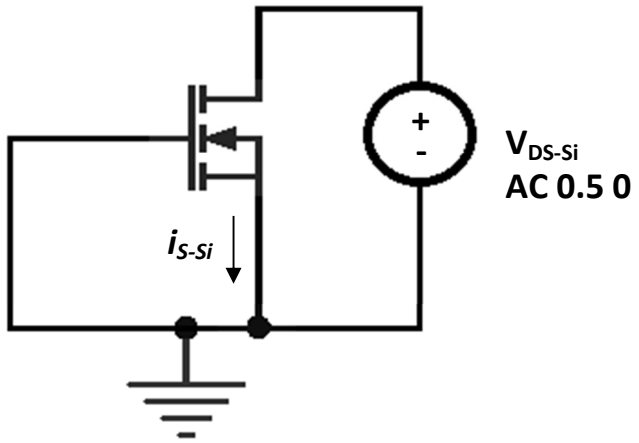


Figure 3.13: SPICE small signal AC analysis for output capacitance evaluation

The capacitances are determined at different drain-source voltages and plotted in Figure 3.14. $C_{GS\text{-}Si}$ is constant and equal to 685.5pF whilst $C_{GD\text{-}Si}$ and $C_{GS\text{-}Si}$ vary with $v_{DS\text{-}Si}$.

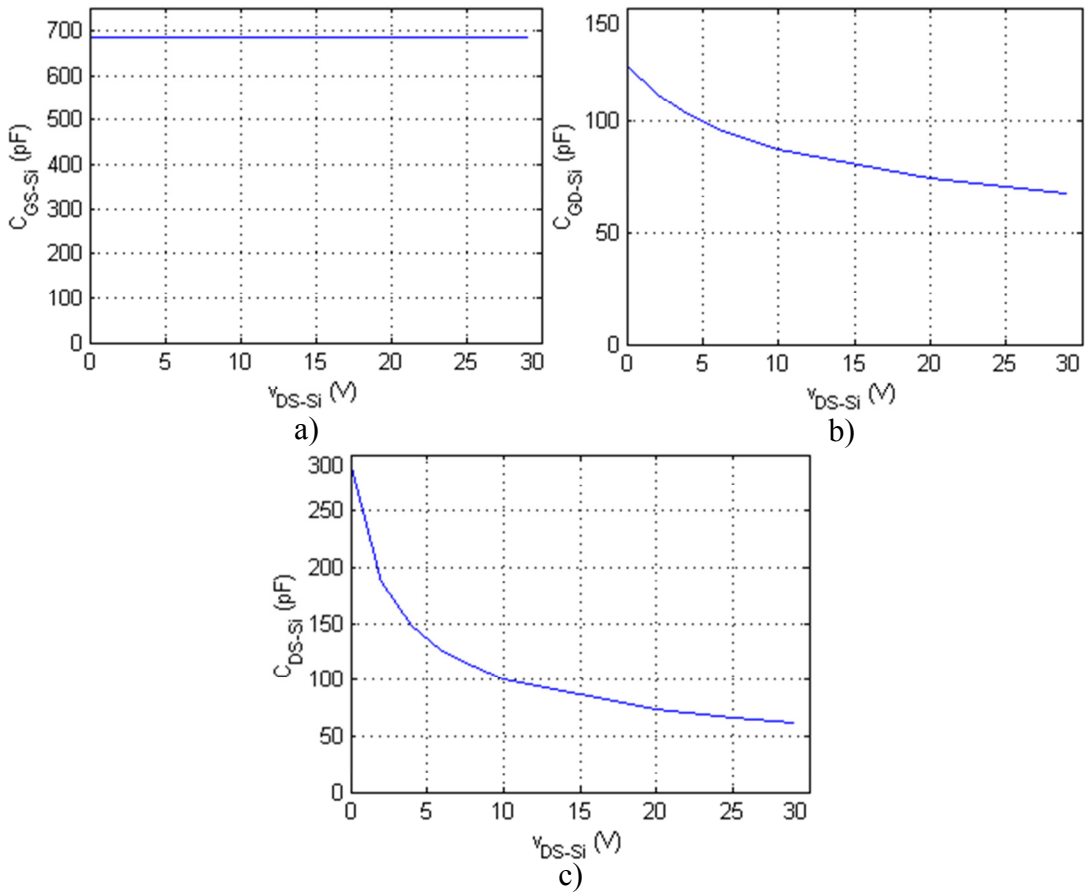


Figure 3.14: Si MOSFET capacitances: a) $C_{GS\text{-}Si}$ vs. $v_{DS\text{-}Si}$, b) $C_{GD\text{-}Si}$ vs. $v_{DS\text{-}Si}$ and c) $C_{DS\text{-}Si}$ vs. $v_{DS\text{-}Si}$

Constant capacitor values are determined for the model by determining equivalent capacitors which hold the same charge as the actual capacitors when charged to the same voltage. These are sometimes referred to as time-related equivalent capacitors and are determined as:

$$C_{(TR)} = \frac{\int_0^{V_i} C(V_{DS})\, dV_{DS}}{V_i} \tag{3.62}$$

The drain-source voltage of the Si MOSFET switches between zero and $-V_{TH\text{-}GaN}$, therefore, the equivalent capacitances ($C_{GD\text{-}Si(TR)}$ and $C_{DS\text{-}Si(TR)}$) are calculated at $-V_{TH\text{-}GaN}$ and presented in Table 3.1 along with the constant gate to source capacitance.

Table 3.1: Si MOSFET equivalent capacitances at $V_{DS\text{-}Si}$ = 22V

Capacitance	Value (pF)
$C_{GS\text{-}Si}$	685.5
$C_{GD\text{-}Si(TR)}$	89.5
$C_{DS\text{-}Si(TR)}$	115.9

A constant value was determined for the transconductance for a specific current I_L by taking the gradient of a straight line approximation to the i_D:v_{GS} characteristic as shown in Figure 3.15.

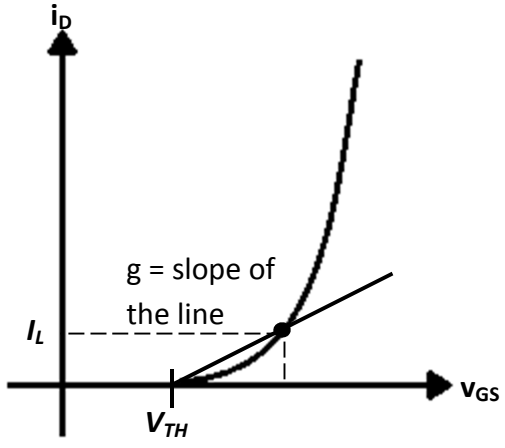


Figure 3.15: Equivalent constant transconductance approximation

This approximation was used since the transconductance value must represent the transistor current as it switches between zero and the forced on-state level of I_L.

By monitoring v_{GS} and i_D during inductive turn-on in SPICE, the equivalent constant transconductance values were determined for several on-state current values and are plotted in Figure 3.16.

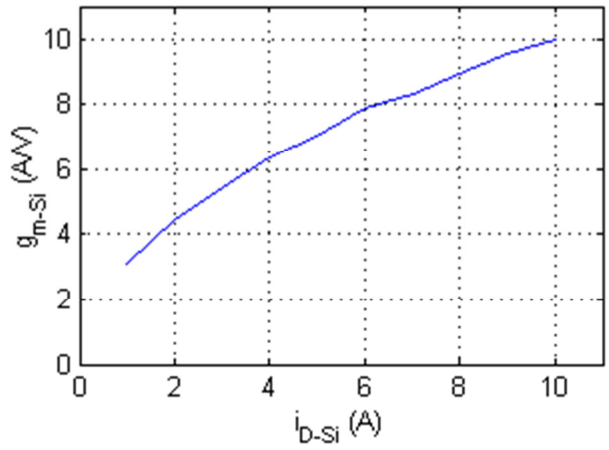


Figure 3.16: $g_{m\text{-}Si}$ vs. $i_{D\text{-}Si}$

The estimated parameters for the GaN HEMT were obtained in a similar way but with a reverse bias between gate and source to hold the device off for the estimation of the capacitances. The resultant capacitances are shown in Figure 3.17.

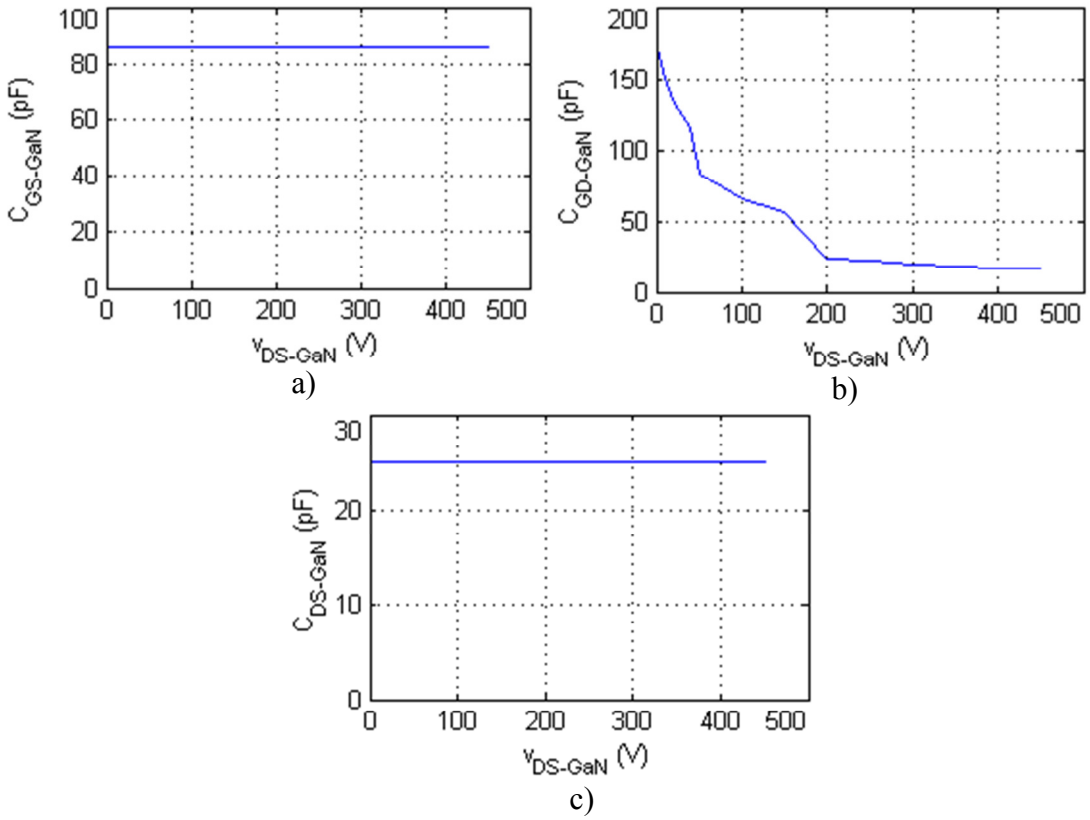


Figure 3.17: GaN HEMT capacitances: a) $C_{GS\text{-}GaN}$ vs. $v_{DS\text{-}GaN}$, b) $C_{GD\text{-}GaN}$ vs. $v_{DS\text{-}GaN}$ and c) $C_{DS\text{-}GaN}$ vs. $v_{DS\text{-}GaN}$

$C_{GS\text{-}GaN}$ and $C_{DS\text{-}GaN}$ are constant and equal to 85.8pF and 25pF respectively whilst $C_{GD\text{-}GaN}$ changes over the drain to source voltage of the GaN HEMT ($v_{DS\text{-}GaN}$). These values and the time related equivalent gate-drain capacitance of the GaN HEMT ($C_{GD\text{-}GaN(TR)}$) at 200V and 400V are summarised in Table 3.2.

Table 3.2: GaN HEMT equivalent capacitances

Capacitance	Value (pF)
$C_{GS\text{-}GaN}$	85.8
$C_{DS\text{-}GaN}$	25
$C_{GD\text{-}GaN(TR)}$ at $v_{DS\text{-}GaN}$ = 200V	76.4
$C_{GD\text{-}GaN(TR)}$ at $v_{DS\text{-}GaN}$ = 400V	48.3

The calculated transconductance for the GaN HEMT for different on-state current values is plotted in Figure 3.18.

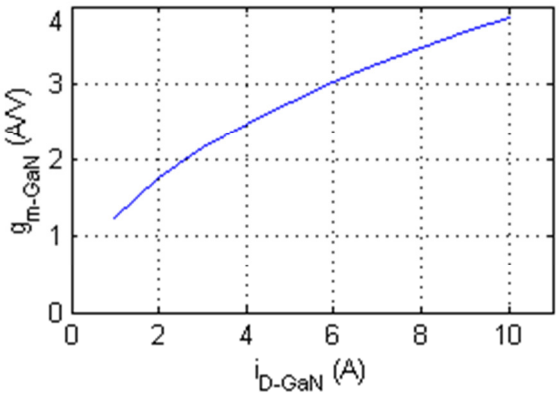


Figure 3.18: $g_{m\text{-}GaN}$ vs. $i_{D\text{-}GaN}$

Freewheel diode capacitance

A SCS210AJ SiC diode rated at 650V and 10A (at T_j = 137°C) was used as the freewheeling element. Its time related equivalent capacitance was calculated from the datasheet plot of capacitance against voltage and using (3.62). The values at reverse voltage (V_R) equal to 200V and 400V are shown in Table 3.3.

Table 3.3: Freewheeling SCS210AJ SiC diode time related equivalent capacitance at V_R = 200V and V_R = 400V

Capacitance	Value (pF)
$C_{D(TR)}$ @ V_R = 200V	73.1
$C_{D(TR)}$ @ V_R = 400V	56.7

The inductor capacitance (in parallel with the diode capacitance) was neglected since it is one order of magnitude smaller than the diode capacitance (<3pF).

Summary of parameters

Table 3.4 presents a summary of the parameters at different operating conditions that will be frequently used. Also, Table 3.5 presents a summary of the model parameter values that are insensitive to operating conditions.

Table 3.4: Model parameters at different conditions

Parameters	Conditions			
	200V, 5A	200V, 10A	400V, 5A	400V, 10A
$g_{m\text{-}Si}$	7.1 A/V	10 A/V	7.1 A/V	10 A/V
$g_{m\text{-}GaN}$	2.8 A/V	3.9 A/V	2.8A/V	3.9 A/V
$C_{GD\text{-}GaN}$	76.4pF	76.4 pF	48.3 pF	48.3 pF
C_D	73.1 pF	73.1 pF	56.7 pF	56.7 pF

Table 3.5: Constant model parameters

Parameter	Value
$V_{TH\text{-}Si}$	2.25V
$C_{GS\text{-}Si}$	685.5pF
$C_{GD\text{-}Si}$ ($v_{DS\text{-}Si}$ = 22V)	89.5pF
$C_{DS\text{-}Si}$ ($v_{DS\text{-}Si}$ = 22V)	115.9pF
$V_{TH\text{-}GaN}$	-22V
$C_{GS\text{-}GaN}$	85.8pF
$C_{DS\text{-}GaN}$ ($v_{DS\text{-}GaN}$ = 400V)	25pF

3.6.2 Model waveforms

The model waveforms are compared against practical measurements. Figure 3.19 shows the waveforms generated by the simple model and experimental

measurements at V_i = 400V, I_L = 10A, V_{DD} = 10V and R_G = 10Ω. The model parameters were obtained from Table 3.4 and Table 3.5 and Chapter 4 describes the practical system and measurement methods in detail.

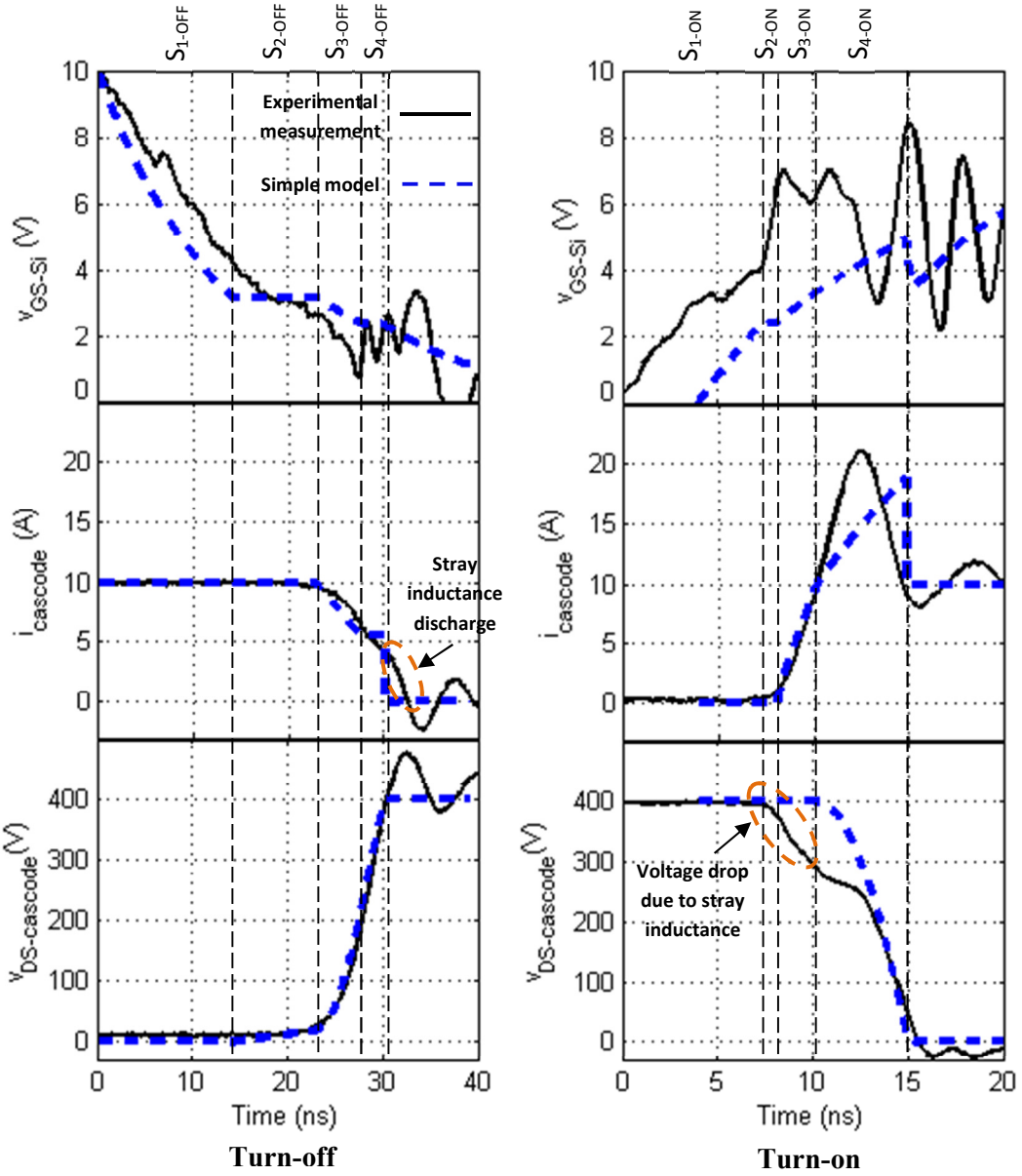


Figure 3.19: Simple model and practical measurements' waveforms at V_i = 400V, I_L = 10A, V_{DD} = 10V and R_G = 10Ω

Overshoots, undershoots and parasitic oscillations are observed in the experimental measurements. In contrast, we observe signals without oscillations in the model waveforms where the stray inductance was neglected.

Good agreement is observed in the $i_{cascode}$ and $v_{DS\text{-}cascode}$ waveforms but this is not the case for the $v_{GS\text{-}Si}$ waveforms where some time shift is observed. The main reason for

the gate-source voltage differences is that the practical measurement of $v_{GS\text{-}Si}$ includes the effects of the internal gate resistance (6Ω as reported in section 3.6.1) since the internal MOSFET gate node is inaccessible. Figure 3.20 illustrates the difference in the measurement point.

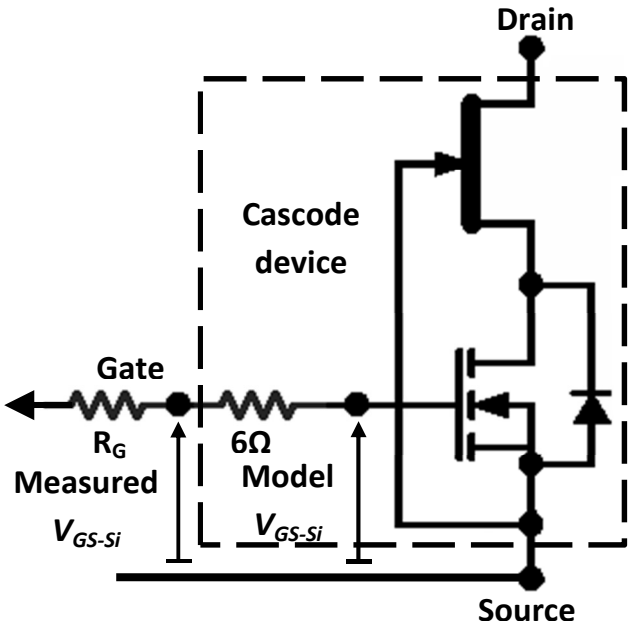


Figure 3.20: Gate-source voltage measurement points, model and experimental measurements

The cascode currents switch at a similar speed during $S_{3\text{-OFF}}$. After that, the channel of the GaN HEMT is closed and the output capacitance of the cascode device is charged linearly as seen in the model $v_{DS\text{-}cascode}$ waveform during $S_{4\text{-OFF}}$. The cascode current waveform looks constant because of the constant capacitance assumption whilst it decreases in the measurements since the freewheel diode capacitance increases and the cascode device output capacitance decreases as $v_{DS\text{-}cascode}$ rises transferring more I_L current from the cascode device to the freewheel diode. Once $S_{4\text{-OFF}}$ ends, the model cascode current switches instantaneously to zero, since the stray inductance was neglected, and the cascode drain-source voltage reaches the operating voltage. On the other hand, the practical measurement shows how the stray inductance is discharged and generates a voltage overshoot in the $v_{DS\text{-}cascode}$ waveform due to a parasitic resonance with the capacitances.

Despite the differences in the turn-off cascode current waveforms, the switching times are very close, the fall time of the current (transition from 90% to 10% of the operating level) is 6.3ns for the model and 7.1ns for the measurement, the simple model predicted time is only 12% lower than the measurement. In addition, the

model and measured $v_{DS\text{-}cascode}$ waveforms are almost identical; the rise time (transition from 10% to 90% of the operating level) predicted from the model is 5.2ns whilst it is 5.4ns in the practical measurements, less than 4% variation. The model succeeded to show the main features of the waveforms and to accurately predict the switching speeds of the cascode currents and drain-source voltages during turn-off.

Figure 3.21 shows a comparison of the instantaneous power during turn-off (p_{off}) and turn-on (p_{on}) between the simple model and the measured waveforms calculated by multiplying the $i_{cascode}$ and $v_{DS\text{-}cascode}$ waveforms. Very close agreement is observed during $S_{2\text{-}OFF}$ and $S_{3\text{-}OFF}$ because of the similarity of the waveforms during these stages. The model shows slightly higher dissipation during $S_{4\text{-}OFF}$ because of the constant capacitance assumption. After stage four, the practical measurement instantaneous power reflects the power released by the stray inductance. The turn-off energy predicted by the model is expected to be slightly lower than the measured one because of this additional energy and the longer transients caused by the stray inductance.

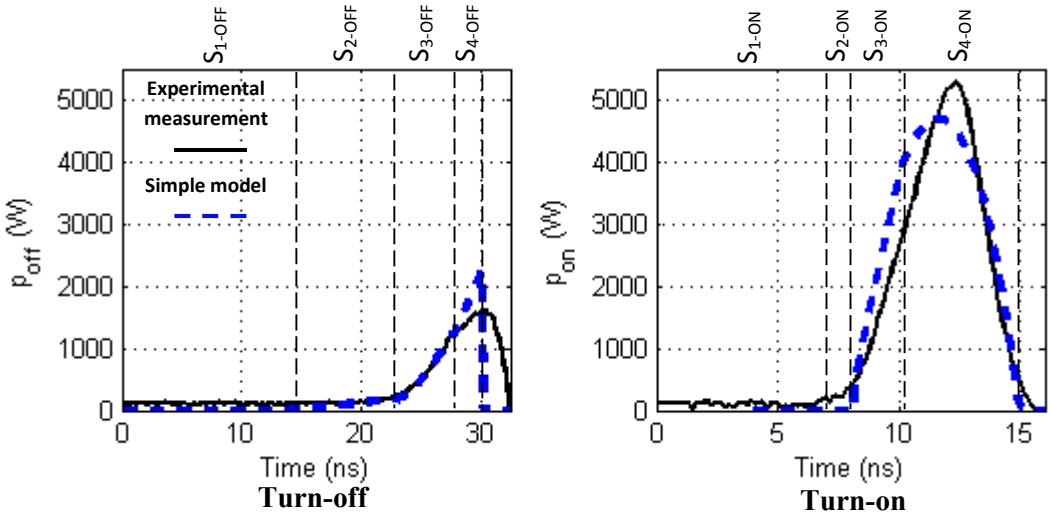


Figure 3.21: Instantaneous power during turn-off and turn-on switching transients, simple model vs. experimental measurements at V_i = 400V, I_L = 10A, V_{DD} = 10V and R_G = 10Ω

The cascode current turn-on transients show very close agreement during $S_{3\text{-}ON}$. The rise time predicted by the simple model is 1.8ns whilst it is 2ns for the experimental measurements, the simple model predicted rise time is 10% quicker than the measured one. The difference is attributed to the stray inductance and model

assumptions. The cascode voltage waveforms differ mainly because of the voltage drop generated by the power loop stray inductance when it is being charged by the switching cascode current in the practical measurements. The model cascode drain-source voltage remains constant during $S_{3\text{-}ON}$ and then starts to drop once $S_{4\text{-}ON}$ starts. The voltage drop also explains the difference in cascode voltage fall times. Once the cascode current reaches its maximum value in the experimental measurements, the effects of the stray inductance are less evident and the cascode drain-source voltage speeds are similar between the model and the measurements. Higher turn-on power dissipation is observed during $S_{3\text{-}ON}$ in the simple model than in the measurements as shown in Figure 3.21 and it is another consequence of the voltage drop in the experimental waveforms.

The freewheel diode reverse capacitive charge adds to the operating current and generates an overshoot in the cascode current waveforms as $v_{DS\text{-}cascode}$ switches to zero. Because of this additional current plus the discharge of the cascode output capacitance, the current switching speed decreases and remains constant until $v_{DS\text{-}cascode}$ is zero and then switches instantaneously to the operating current in the model. The step change is explained by the omission of the stray inductance. On the other hand, the measurements show a sinusoidal current overshoot due to the resonant interaction between the stray inductance and capacitances. The maximum amplitude of the overshoots is close, 21.1A and 18.9A for experimental measurement and the model respectively, the simple model prediction is less than 11% smaller when compared against measurements.

Although there are differences in the turn-on waveforms attributed to the stray inductance, the model shows the main features of the cascode turn-on switching transient and the instantaneous power waveforms are fairly close and have similar shapes as shown in Figure 3.21. Lower losses would be expected in the simple model predictions than in experimental measurements when very high cascode current switching speeds are achieved or the layout is not optimised, increasing the circuit stray inductance and its effects.

Both the model and the measurements show that the turn-on power dissipation is significantly higher during the turn-on switching transient than during the turn-off

switching transient. High voltage and high current conditions during switching and the charge added by the freewheel diode during turn-on explain the difference.

The simple model was used to predict the switching losses of the practical waveforms by integrating the instantaneous power plots of Figure 3.21. The calculations of the model indicate that the turn-off switching energy loss is 7.8μJ and the turn-on total loss is 21.8μJ resulting in a total switching loss of 29.6μJ. Similarly, the instantaneous power waveforms of the measurements are integrated during the switching intervals obtaining a turn-off switching loss of 9.7μJ and a turn-on switching loss of 20.4μJ and the total energy power loss is 30.1 μJ. The simple model losses were only 2% lower when compared against the practical measurements. The higher losses of the turn-on process partially compensated the lower losses observed during turn-off in the model predictions. The difference can be attributed to the stray inductance of the real circuit and the assumption of constant capacitance and transconductance values.

The simple model waveforms present many of the characteristics of the practical measurements and allow accurate energy loss calculations although simplifying assumptions were used. Further validation of the accuracy of the model predicting energy losses at different conditions is presented in Chapter 4.

3.6.3 Influence of driving parameters and operating conditions.

Gate resistor

The model was used to assess the effect of the gate resistor on the cascode waveforms. Figure 3.22 shows a comparison of the model switching waveforms at V_i = 400V, I_L = 10A , V_{DD} = 10V and R_G = 1Ω and 15Ω during turn-off.

The waveforms show that the entire turn-off process duration is increased from 14.5ns at R_G = 1Ω to 37.8ns at R_G = 15Ω. However, the duration of $S_{3\text{-OFF}}$ plus $S_{4\text{-OFF}}$ (when most of $i_{cascode}$ and $v_{DS\text{-}cascode}$ changes take place) increases only 2ns from 5.8ns at R_G = 1Ω to 7.8ns at R_G = 15Ω.

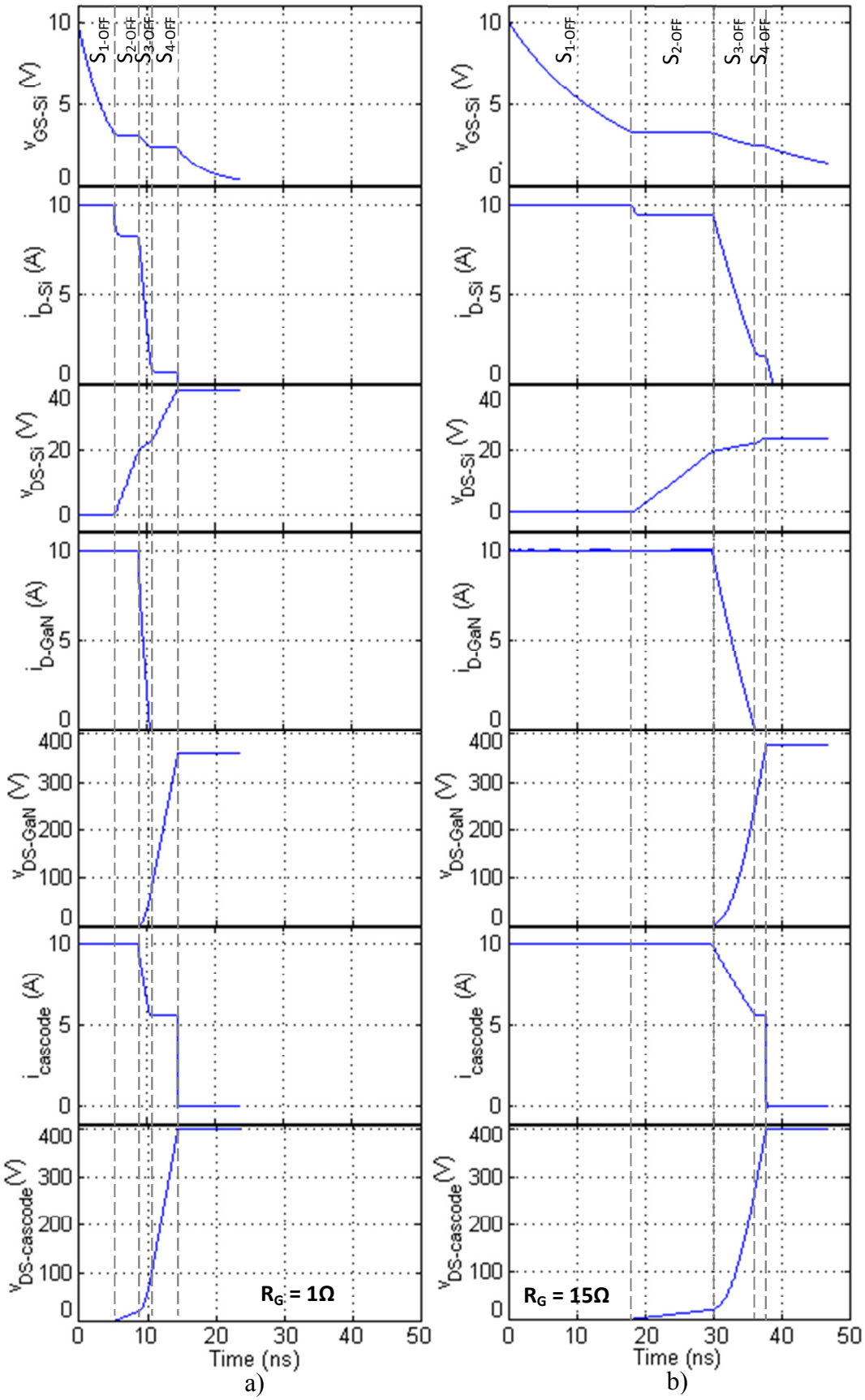


Figure 3.22: Model turn-off waveforms at V_i = 400V, I_L = 10A, V_{DD} = 10V: a) R_G = 1Ω and b) R_G = 15Ω

Although R_G doesn't influence the duration of the sum of $S_{3\text{-OFF}}$ and $S_{4\text{-OFF}}$ significantly, it does affect the individual stage lengths. $S_{3\text{-OFF}}$ is very short with the small R_G and increases with R_G whilst $S_{4\text{-OFF}}$ reduces with R_G. As a result the power loss in the GaN HEMT will be low with a small R_G since $i_{D\text{-}GaN}$ falls whilst $v_{DS\text{-}cascode}$ is low and the HEMT loss increases with R_G.

The switching speed of the GaN HEMT channel current is very high due to the cascode mechanism where the GaN HEMT gate-source voltage is driven by the Si MOSFET at a relatively constant current as reflected by relatively linear drain-source waveforms. The gate resistor influences the switching speed of the GaN HEMT current by slowing $v_{DS\text{-}Si}$ but it has lower influence on the charging speed of $v_{DS\text{-}GaN}$, which is mainly determined by the constant cascode current during $S_{4\text{-OFF}}$.

The predicted cascode current fall time and drain-source voltage rise time are shown and compared against experimental measurements (obtained from Figure 4.13 in the next Chapter) in Table 3.6.

Table 3.6: Model and experimental measurements' turn-off switching times at V_i = 400V, I_L = 10A, V_{DD} = 10V and R_G = 1Ω and R_G = 15Ω

Gate resistor	**Cascode current fall time (ns)**		**Drain-source voltage rise time (ns)**	
	Model	Measurement	Model	Measurement
R_G = 1Ω	5.5	7.1	4.4	4.9
R_G = 15Ω	6.7	7.3	5.7	5.7

Very close agreement between the model and the experimental measurements is observed at R_G = 15Ω, the drain-source voltage rise time is identical while the cascode current fall time is 9.2% smaller in the model than in the measurements. The difference is bigger at R_G = 1Ω, where the current transient predicted by the model is 22.6% quicker than measured. The difference is attributed to the higher influence of the stray inductance at higher switching speed (when R_G = 1Ω) and the simplifying assumptions of the model.

Both, the model and the experimental measurement show a small rise in the switching times as R_G is increased from 1Ω to 15Ω. As noted earlier in this section

the charging of the cascode output capacitance is the main process influencing the switching times and power losses during turn-off.

From Figure 3.22 we can observe that a longer $i_{cascode}$ plateau appears during $S_{4\text{-OFF}}$ at $R_G = 1\Omega$ than when $R_G = 15\Omega$. The presence of an $i_{cascode}$ plateau suggests a rapid GaN HEMT channel current transition and lower power dissipation during turn-off. The plateau presence with low gate resistor is confirmed by practical measurements as shown in Figure 3.23. The plateau level is the result of the current sharing between the freewheel diode and the cascode device whilst the cascode drain-source voltage is switching. The level in the measurements is 5.5A whilst it is 5.6A in the model as shown in Figure 3.22.

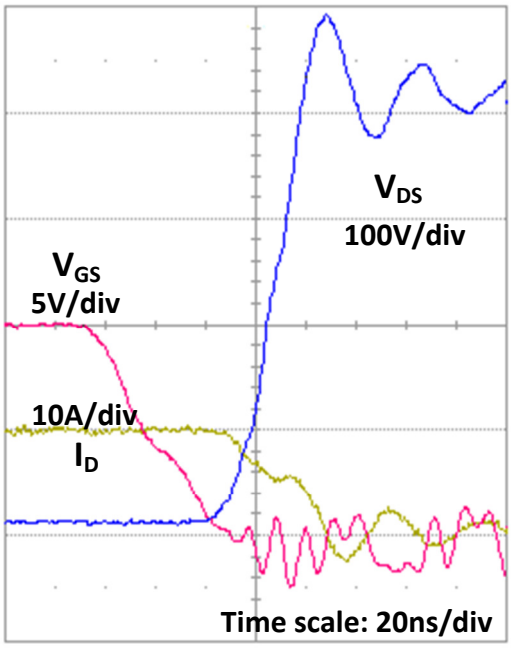


Figure 3.23: DPT experimental waveforms at $V_i = 400V$, $I_L = 10A$, $V_{DD} = 10V$ and $R_G = 1\Omega$, single Transphorm device along with a SiC diode

Figure 3.24 shows a comparison of the model turn-on waveforms at $R_G = 1\Omega$ and $R_G = 15\Omega$ at $V_i = 400V$, $I_L = 10A$ and $V_{DD} = 10V$. The waveforms show that the switching speed of the Si MOSFET gate-source voltage increases with a low gate resistor which in turn increases the switching speed of the other waveforms. Higher Si MOSFET gate-source switching speed opens the Si MOSFET channel quicker which in turn allows a quicker discharge of the output capacitance of the Si MOSFET. Then, the GaN HEMT gate-source voltage (which is in parallel with the Si MOSFET output capacitance) switches quicker, opening the channel of the GAN

HEMT faster and discharging the output capacitance of the GaN HEMT in a short time. Since the switching transients become extended with larger R_G, higher turn-on switching losses are expected.

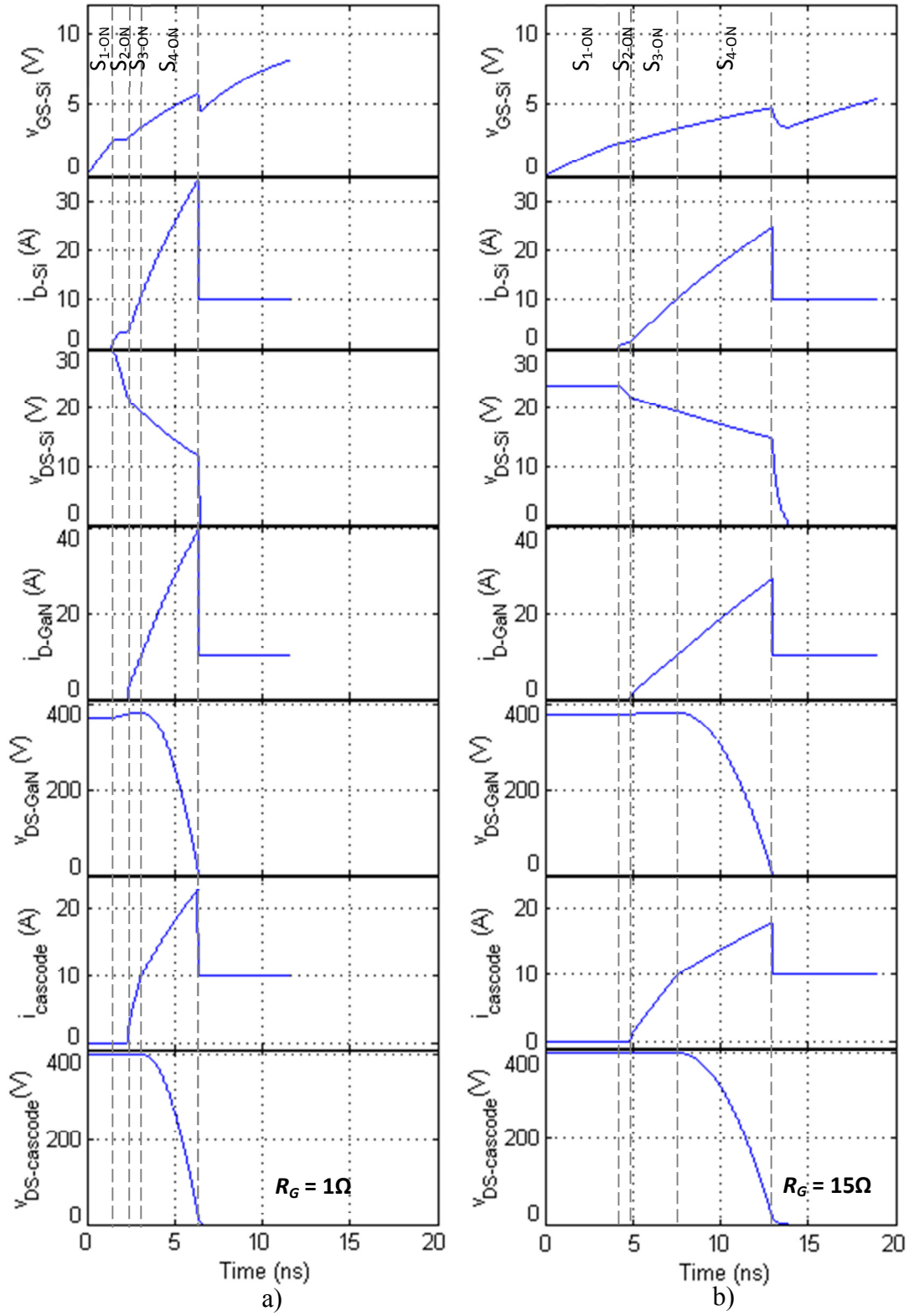


Figure 3.24: Model turn-on waveforms at V_i = 400V, I_L = 10A, V_{DD} = 10V: a) R_G = 1Ω and b) R_G = 15Ω

The waveforms show higher current in the channels of the Si MOSFET and GaN HEMT than in the overall cascode current, which is due to the internal discharge of the output capacitance of the devices through their channels.

As discussed in section 3.6.2, the experimental cascode drain-source voltage fall time differs significantly from the predicted value because of stray inductance. The cascode current rise time predicted by the model is 50% quicker than the experimental measurement, 0.7ns predicted against 1.4ns from measurements, as seen in Figure 4.13 in Chapter 4, the effect of the stray inductance at high switching speed conditions is the cause of this difference. When R_G = 15 Ω the model predicts a cascode current rise time of 2.3ns whilst the measurement is 2.8ns, 18% quicker. As the transitions are slower, better agreement is obtained between the model predictions and the experimental measurements.

Driver voltage

The waveforms of $S_{2\text{-OFF}}$, $S_{3\text{-OFF}}$ and $S_{4\text{-OFF}}$ are not sensitive to changes in the driver voltage. The initial conditions of $S_{2\text{-OFF}}$ are the same independent of the driver voltage and the same is true for the subsequent switching stages. The driver voltage only affects the duration of the $S_{1\text{-OFF}}$ stage as stated in equation (3.5), that is, it only affects the turn-off delay.

Figure 3.25 compares sample turn-on waveforms at different driver voltage, 6V and 10V, at V_i = 400V, I_L = 10A and R_G = 15Ω. The effect of a high driver voltage is similar to that of a low gate resistor. With higher driver voltage, the switching stages are shorter resulting in higher switching speed for both voltage and current waveforms. Therefore, lower turn-on switching losses are expected as the driver voltage is increased.

Whilst there are some errors in the predicted cascode drain-source voltage switching time because of stray inductance, the model accurately predicts the switching rise time of the cascode current. The model rise time at V_{DD} = 6V is 5.2ns and it is 2.3ns at V_{DD} = 10V. The measured cascode current rise times are 6.2ns at V_{DD} = 6V and 2.9ns at V_{DD} = 10V, the predicted current rise time is around 16% and 20% quicker.

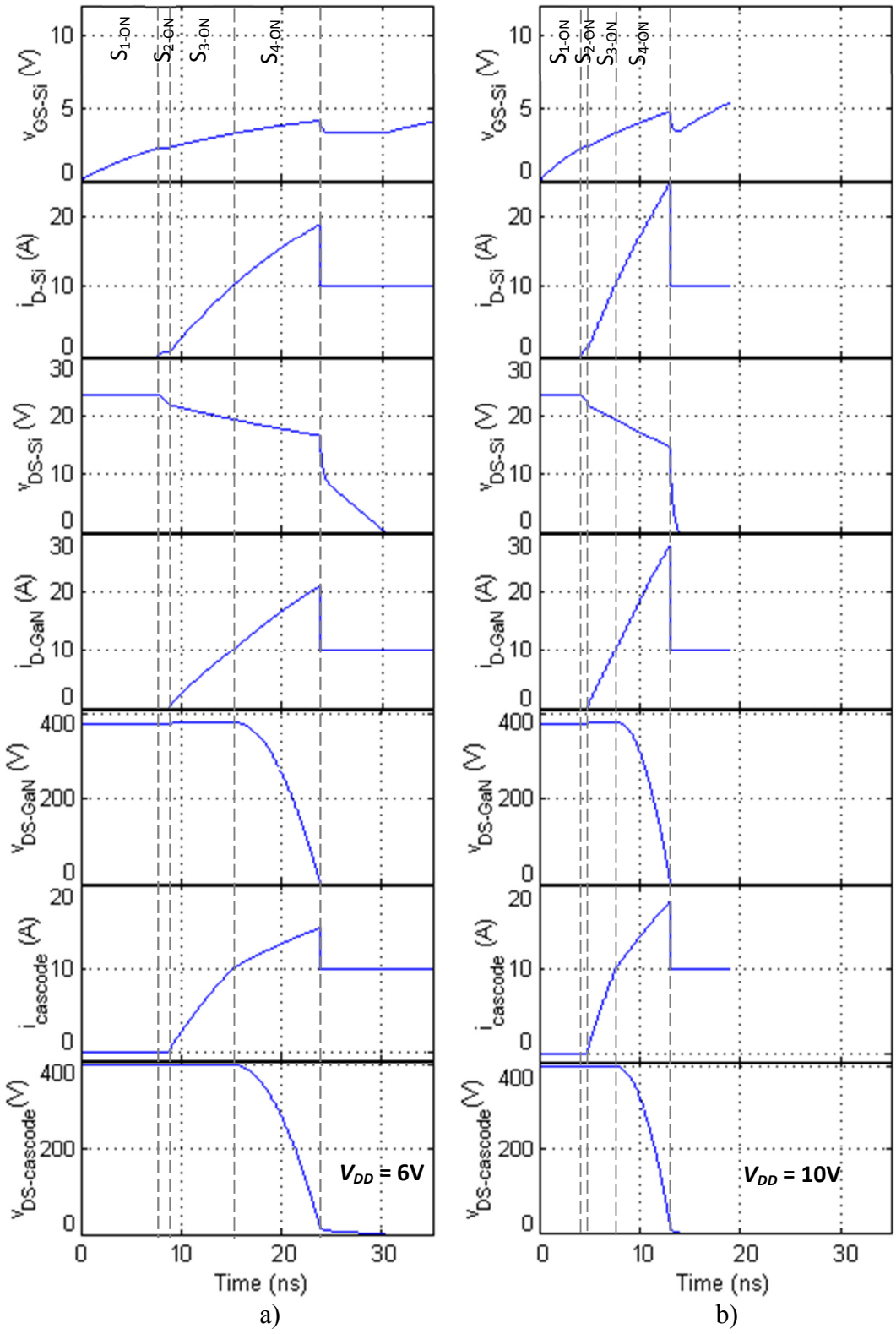


Figure 3.25: Model turn-on waveforms at V_i = 400V, I_L = 10A, R_G = 15Ω: a) V_{DD} = 6V and b) V_{DD} = 10V

3.7 Energy analysis

3.7.1 Measurable energy

The drain to source voltage of the cascode device and $i_{cascode}$ are usually the only measurable variables relating to the switching energy loss since the MOSFET drain is not normally accessible in a packaged cascode. Estimating, the energy losses by multiplying the total voltage and current then integrating will give slightly misleading results since the stored energy and dissipated energy will be included for the turn-off case. The dissipated energy can't be easily distinguished from the stored energy, and the measured turn-off loss will be overestimated. For example, Chapter 5 will introduce an electronic converter that uses zero voltage switching during turn-on to recover the energy stored during turn-off and the estimation of the turn-off energy loss will require distinguishing between stored and dissipated energies. In addition, the turn-on energy won't include the dissipation of the energy that is stored in the output capacitance of the cascode device. Therefore, the turn-on loss will be underestimated. However, the total switching energy ($E_{off} + E_{on}$) will be correct.

3.7.2 Energy losses distribution

The equations of the switching model in sections 3.3 and 3.4 can be used to calculate the energy losses and energy that is stored during any of the switching stages.

The equations were programmed in MATLAB and the parameters were based on Table 3.4 and Table 3.5 at V_i = 400V, I_L = 10A, V_{DD} = 10V and R_G = 10Ω. Figure 3.26 presents the results. $E_{D\text{-}Si}$ and $E_{D\text{-}GaN}$ are the energies that are dissipated in the Si and GaN devices, whilst $E_{S\text{-}Si}$ and $E_{S\text{-}GaN}$ are the energies stored in the device capacitances.

Most of the turn-off energy is stored in the output capacitance of the GaN HEMT (72%), whilst the Si MOSFET dissipates most of the total dissipated energy during turn-off (18%). All the turn-on energy is dissipated in the channels of the transistors, mostly in the GaN HEMT. The turn-on energy is much larger than the turn-off energy (2.8 times). The reason for this is the overshoot in transistor current at turn-on and that the device voltages tend to be higher during the current switching process.

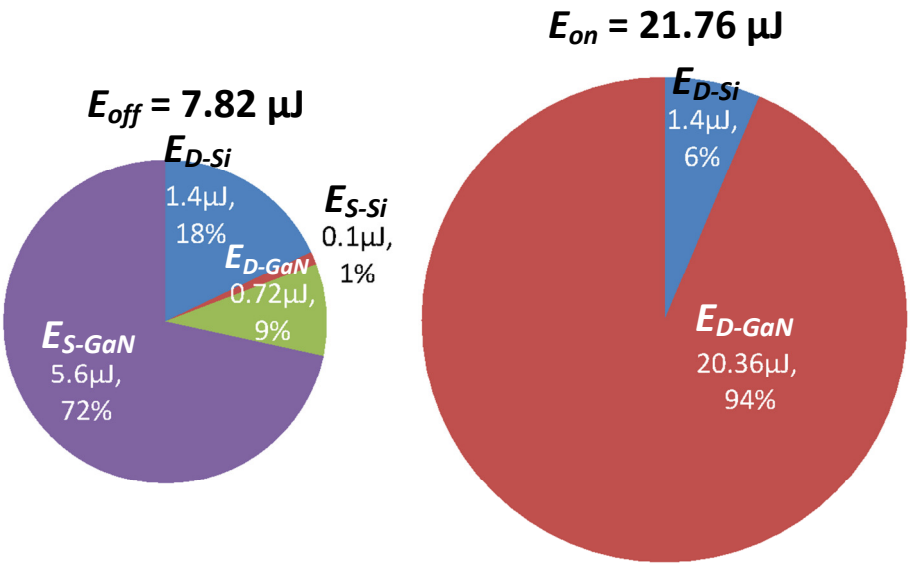


Figure 3.26: Turn-off and turn-on energy loss distribution for a Transphorm TPH3006LD. V_i = 400V, I_L = 10A, V_{DD} = 10V and R_G = 10Ω

Figure 3.27 presents the turn-off and turn-on energies per stage under the same sample conditions.

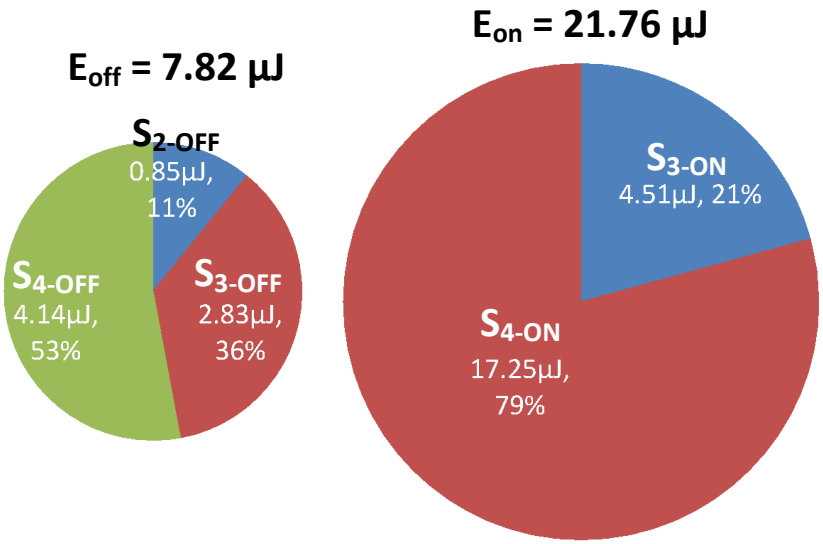


Figure 3.27: Turn-off and turn-on energy losses distribution per stage. V_i = 400V, I_L = 10A, V_{DD} = 10V and R_G = 10Ω.

The $S_{2\text{-}OFF}$ energy is totally related to the Si MOSFET, most of it is dissipated. The $S_{3\text{-}OFF}$ energy reflects the dissipation in both channels and some storage. The $S_{4\text{-}OFF}$ energy is largely stored in the capacitance of the GaN HEMT.

The low energy loss during turn-off makes the cascode device very attractive for soft-switching topologies where the turn-on loss is almost eliminated by the natural operation of the circuit.

3.8 Summary

This Chapter presented the development of a simple model of the switching transients for a cascode device under inductive load conditions. The model divides the switching transients into four different stages. The parasitic capacitances and the transconductances of both devices are considered as constant. The stray inductances are neglected.

Each stage is described in detail. Laplace and time domain expressions were derived for the main parameters of the circuit. These equations can be easily programmed in mathematical software to generate plots and energy loss calculations.

The model is validated using a Transphorm GaN cascode device rated at 600V, 17A (at T_j = 25°C) and $R_{DS\text{-}ON}$ = 0.15Ω (typical at T_j = 25°C). The selection of the model parameters is described. The model is compared against practical measurements, the model allowed accurate predictions of the current and drain-source voltage switching times. Greater differences between the model and experimental measurements were observed at higher switching speeds where the stray inductance becomes more dominant. The main features of the cascode waveforms are shown by the model. The predicted instantaneous power plots of the switching transients are similar to the measurements, allowing accurate predictions of the switching losses.

The model provides an accurate and simple alternative to more complex models for predicting switching times and switching energy losses. Complex models allow very accurate prediction of the switching waveforms and energy losses, such as [108], but adding complexity and increasing the computing time since numerical methods are required to solve the equations. In addition, the parasitic inductance elements are hard to be accurately predicted requiring significant effort.

The effects of the driving parameters are analysed showing that the value of the gate resistor has a relatively small effect on the turn-off process, but a larger effect at turn-on. A higher driver voltage also increases the turn-on switching speed.

The model is used to generate some sample results to analyse the energy distribution within the cascode configuration and between switching stages. The study concluded that most of the energy is dissipated in the GaN HEMT channel during turn-on and the most of the turn-off energy is stored in the output capacitance of the cascode devices.

Chapter 4: Practical testing of device switching performance

4.1 Introduction

This Chapter describes the practical testing of the switching characteristics of GaN cascode devices. The results provide insight into the detailed switching behaviour of the devices, the achievable switching speeds and the influence of circuit layout and driver parameters.

The Chapter starts with the description of the double-pulse test circuit that was used to measure the switching characteristics. After that, the Transphorm devices' measurements are presented in two configurations: a single device along with a SiC diode and two devices in an inverter leg configuration. The practical measurements are used to verify the accuracy of the model developed in Chapter 3 to predict switching energy losses. The body diode of the cascode arrangement is characterised and compared against a similarly rated SiC diode. The performance of the Transphorm devices is compared against a state-of-the-art super junction Si MOSFET.

4.2 Double pulse tester

4.2.1 Circuit description

A double pulse tester (DPT) is designed to measure the drain current and drain to source voltage of the device under test (DUT) during normal inductive turn-off and turn-on conditions over a range of voltages and currents. Figure 4.1 shows the DPT circuit. D is a freewheeling diode. The inductor L is used to establish the operating current and the current viewing resistor (CVR) is a non-inductive, co-axial current shunt used to measure the drain current of the DUT. The power supply is used to set the operating voltage V_i. The driver turns off/on the DUT by switching the gate between zero and V_{DD}.

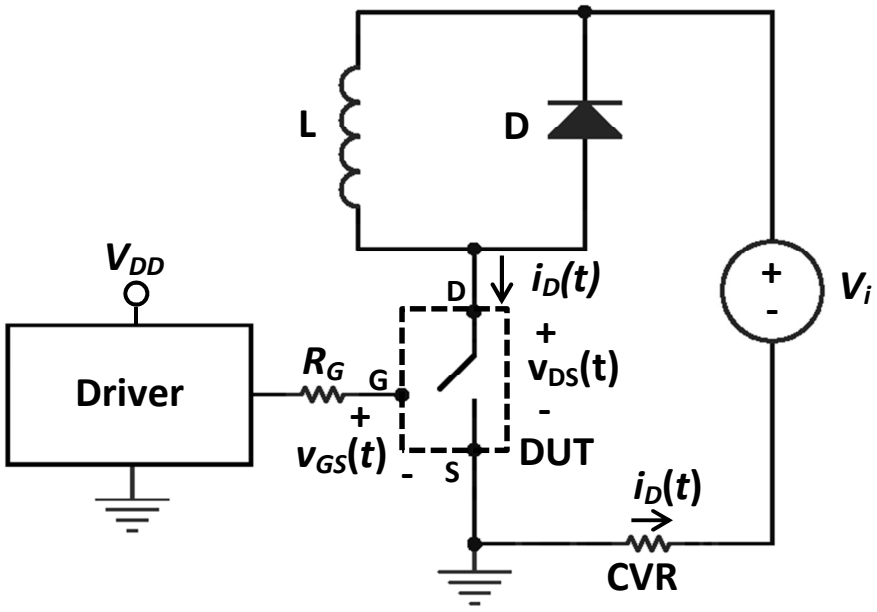


Figure 4.1: Double pulse tester circuit

Figure 4.2 presents the main waveforms of the DPT circuit. Two pulses are applied to the gate of the DUT. The first pulse of duration t_1 is used to establish a current I_L in the inductor L; since the DUT is turned on, $v_{DS}(t)$ is low. The freewheeling diode is blocking the input voltage.

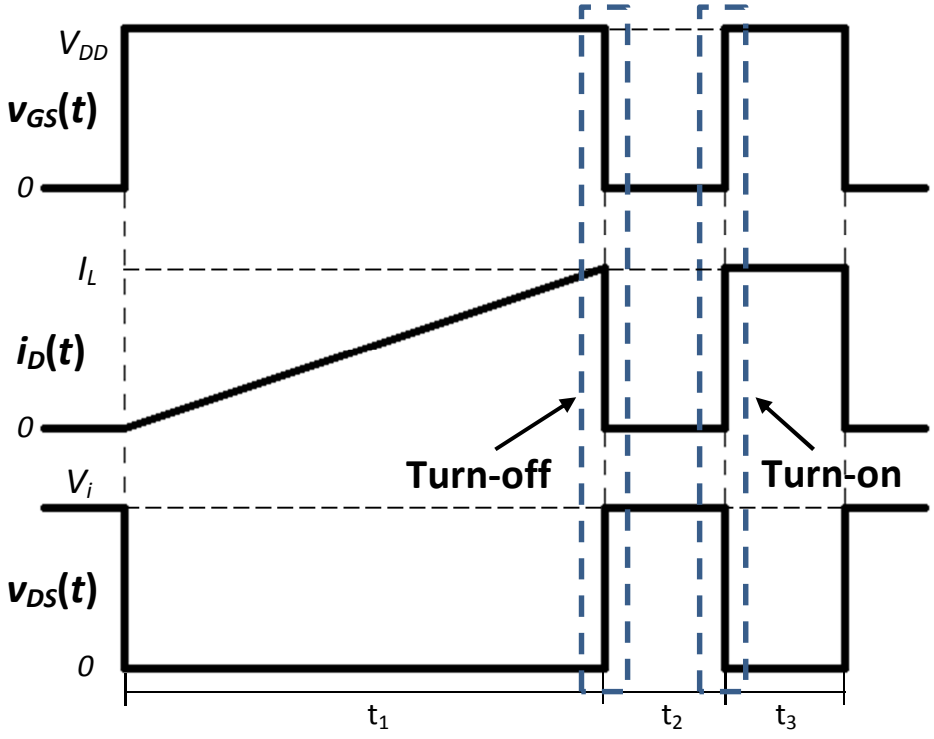


Figure 4.2: Double pulse tester waveforms

Once I_L is set, $v_{GS}(t)$ switches to zero starting the turn-off process. This is the instant when the turn-off waveforms are generated and measured. The off state is

maintained for a duration t_2. The current in the DUT is zero during t_2 and the DUT is blocking the forward voltage V_i. The inductor current flows in the freewheeling diode. The reduction of I_L during t_2 can be neglected if t_2 is relatively short. At the end of t_2, v_{GS} switches from zero to V_{DD} and the DUT is turned-on again. This is the instant where the freewheel diode current commutates back to the transistor and the turn-on waveforms are generated and measured. The DUT stays on during t_3 and is turned off at the end of this interval; t_3 is typically of similar duration to t_2.

Analysis of the captured v_{GS}, v_{DS} and i_D waveforms allows the detailed switching behaviour and parameters to be examined, including the reverse recovery and junction capacitance effects in the freewheel diode. The transistor switching losses (E) are computed by integrating the instantaneous v_{DS} * i_D product whilst the reverse recovery and junction charges (Q_{rr}) of the freewheeling diode can be obtained by integrating the transistor current overshoot at the turn-on instant. Figure 4.3 illustrates these calculations at the turn-on instant.

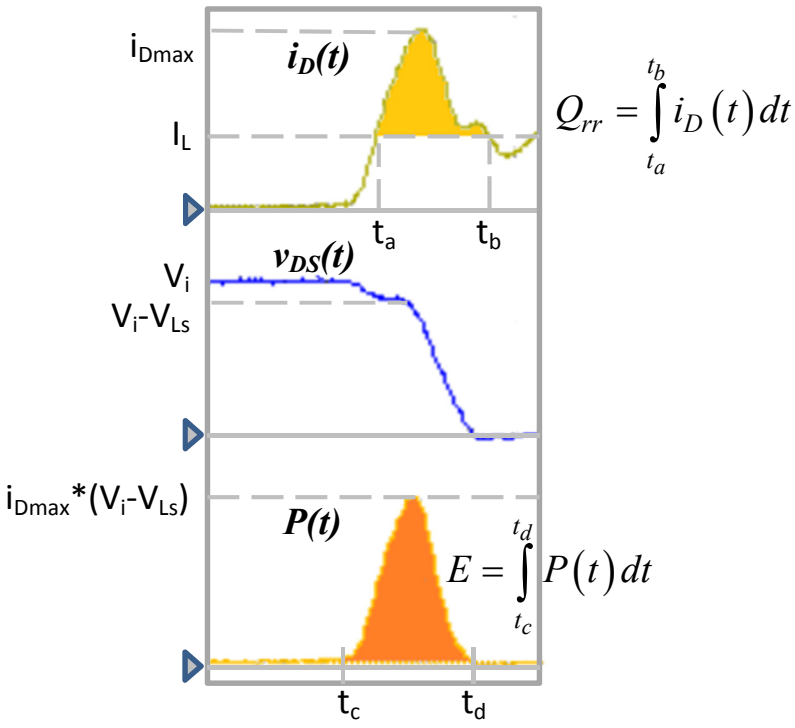


Figure 4.3: Calculation of the switching power loss using $i_D(t)$ and $v_{DS}(t)$ waveforms and Q_{rr} using $i_D(t)$ waveform

4.2.2 Devices selection

Driver

A Fairchild FAN3122TMX single channel, 9A, high-speed, low-side gate driver [168] was chosen to drive the DUT. The device is packaged in a surface mount SMD SOIC-8 package. It provides high current pulses in a compact integrated circuit, allowing a compact gate drive layout with minimum parasitic impedance. A low inductance 1µF or larger ceramic capacitor is recommended, [168], to bypass the power pins. An AVX 08051C104K4Z2A, 100nF, 100V, X7R and 0805 surface mount packaged ceramic capacitor and a Murata GRM21BR71H105KA12L, 1µF, 100V, X7R and 0805 SMD packaged ceramic capacitor were connected to each of the two power pins to meet this requirement. Two 0805 SMD packaged resistors were placed in parallel to form R_G.

Inductor

Two different inductors were used to establish the test current. A lower current component of 1.5mH with a saturation current of 9A, and a higher current inductor of 0.5mH with a saturation current of 23A.

Both inductors were formed by connecting three separate inductors in series to reduce the overall parasitic capacitance. Each individual inductor was implemented using a Ferroxcube ETD593122 core made of 3C90 material. Figure 4.4 shows an image of one of the individual inductors.

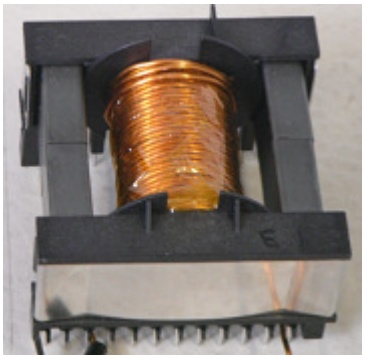


Figure 4.4: DPT inductor

4.2.3 Layout

The circuit layout was designed to minimise the stray inductance by reducing the size of the switching loops. Two main switching loops were identified: the power loop and the gate loop. Figure 4.5 shows these loops.

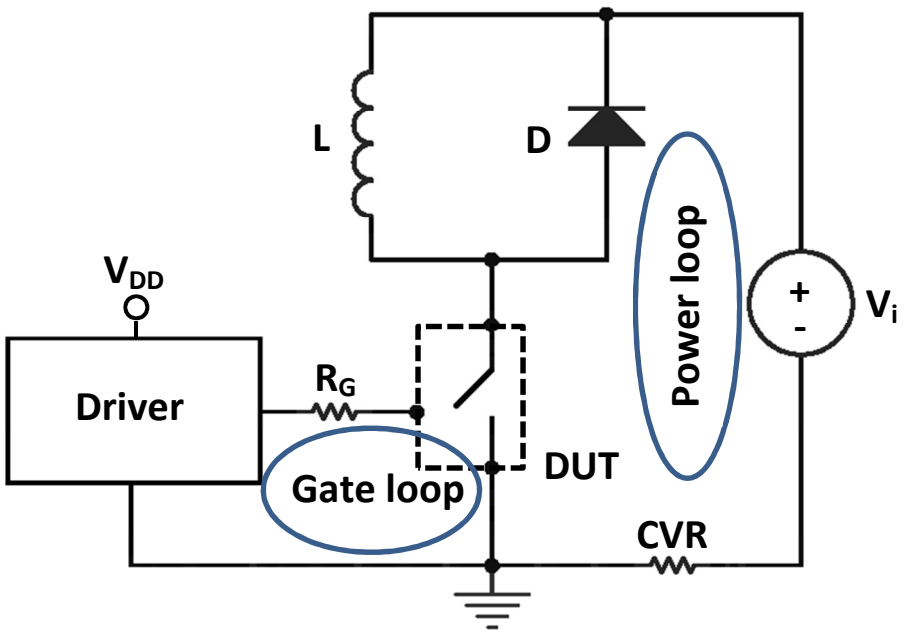


Figure 4.5: DPT switching loops

Two different approaches were implemented in the double pulse tester boards. The first, a lateral arrangement is shown in Figure 4.6.

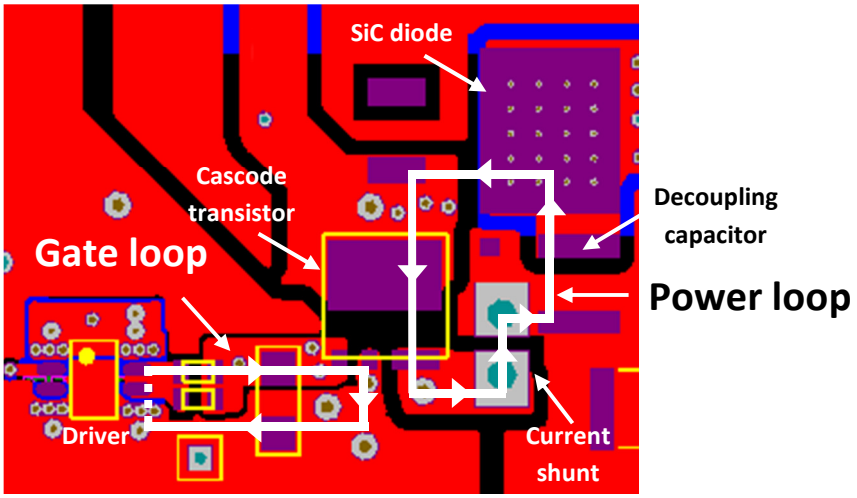
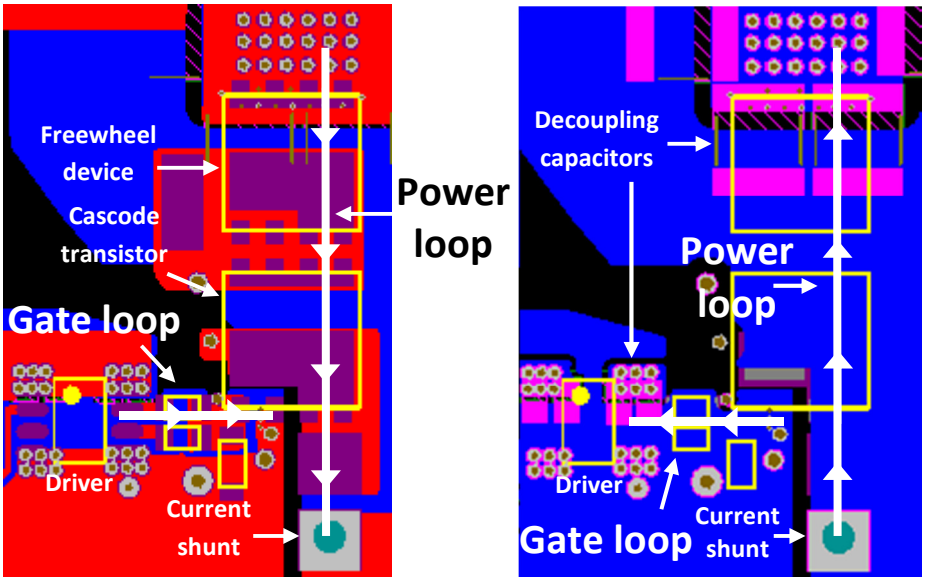


Figure 4.6: Power loops of double pulse tester board, Transphorm GaN cascode device along with a D2PAK SiC diode, lateral layout

The second approach is a vertical layout design where the power and gate loop devices are on both sides of the printed circuit board as shown in Figure 4.7.



Top layer Bottom layer

Figure 4.7: Power loops of double pulse tester board, two GaN Systems devices in an inverter leg configuration, vertical layout

The boards' power and gate loops stray inductance was measured on bare boards using an Agilent 4284A LCR meter at 1MHz and are shown in Table 4.1. The test frequency is commonly used to specify high frequency parameters by device manufacturers. The measured stray inductances are relatively constant from 1MHz up to 10MHz (less than 3% of variation) dropping up to 15% at 40MHz with respect to measurements at 1MHz. The loops were closed by short-circuiting the pads of the devices and the stray inductance was measured on the pads of the decoupling capacitors. The switching node to ground and switching node to V_i capacitances were also measured and are reported in Table 4.1.

Table 4.1: Parasitic elements of double pulse tester boards

Parasitic element	**Lateral layout board**	**Vertical layout board**
Power loop stray inductance (nH)	10	9
Gate loop stray inductance (nH)	9	4
Switching node to ground capacitance (pF)	5	5
Switching node to V_i capacitance (pF)	5	4

The power loop stray inductance of the vertical layout board is slightly lower than that of the lateral design. Although stray inductance reductions may be achieved by the vertical layout design, the length of the power loop path is longer limiting the improvement. The vertical approach and the further reduction of the distance between the driver and the gate of the cascode device resulted in a reduction of more than a half in the gate loop stray inductance. The measured parasitic capacitances were similar.

Table 4.2 presents the layout design approaches implemented in the fabricated double pulse tester boards.

Table 4.2: Layout design implementation on the fabricated double pulse tester boards

DPT board	Power loop layout approach	Gate loop layout approach
Transphorm cascode transistor along with a SiC diode	Lateral	Lateral
Two Transphorm GaN cascode devices in an inverter leg configuration + SiC diode	Lateral (for the cascode device used as freewheeling element) / vertical (for the SiC diode)	Vertical
Super junction Si MOSFET along with a SiC diode	Lateral	Lateral
GaN Systems cascode transistor along with a SiC diode	Vertical	Vertical
Two GaN Systems GaN cascode devices in an inverter leg configuration	Vertical	Vertical

4.2.4 Instrumentation

Equipment

The following equipment and probes were used:

1. **Current shunt.** A T&M Research SDN-414-05, 50mΩ, 2W current viewing resistor was used to measure the transistor drain current. It has low parasitic inductance and high bandwidth (2GHz). The coaxial connection to the oscilloscope was terminated with 50Ω to avoid reflection issues.

2. **Oscilloscope.** A Teledyne LeCroy Wave Runner WR610Zi oscilloscope was used for the measurements. The bandwidth of the instrument is 1GHz.
3. **Voltage probes.** A Teledyne LeCroy 10:1, 400V, 500MHz, PP008 passive probe was used for the gate to source voltage measurements and an 100:1, 2kV, 400MHz, PPE2KV passive probe for the drain to source measurement. The ground spring of the probes was used during the measurements to reduce the loop size and stray inductance of the probe.

Skew

The different propagation delays of the voltage and current measurement transducers and cables can generate a skew or phase error in the oscilloscope waveforms resulting in inaccuracies in the power and energy loss calculations.

To estimate the magnitude of this effect, the propagation delay for the coaxial cables used in the measurements was estimated as shown in Table 4.3. The velocity factor (v_F) was obtained using typical data for similar cables and the propagation delay (t_{PD}) was calculated as:

$$t_{PD} = \frac{l}{cv_F} \tag{4.1}$$

l is the cable length and c the speed of light in free space.

The results in Table 4.3 indicate differential delays of several ns.

Table 4.3: Estimated propagation delays

Probe	Section	Length (m)	Velocity factor	Propagation delay (ns)
Current	Shunt	0.041	0.69	2.9
	Coaxial cable (RG58 C/U MIL-C-17)	0.5	0.66	
Voltage PP008 (for V_{GS} measurement)	All	1.39	0.76	6.1
Voltage PPE2kV (for V_{DS} measurement)	All	2.16	0.76	9.5

By using the oscilloscope's built-in, fast-edge waveform generator as a calibration source the skew between the current shunt coaxial cable and the voltage probes was

measured. Sample waveforms for the skew compensation process of the current shunt coaxial cable and the PP008 voltage probe are shown in Figure 4.8. The test procedure is described in [169].

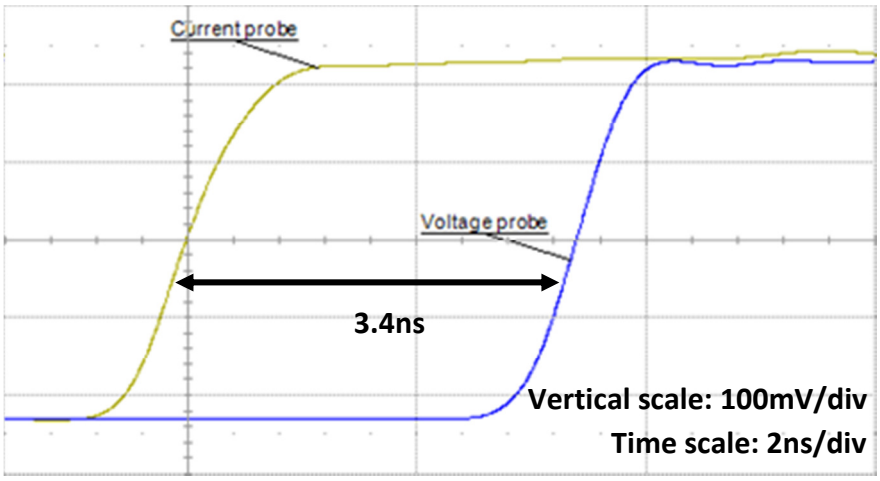


Figure 4.8: Propagation delay difference between current probe and PP008 voltage probes

Figure 4.8 shows that the voltage probe signal is delayed 3.4ns with respect to the current probe coaxial cable, which is consistent with the estimated figure in Table 4.3. The propagation delay of the current measurement device itself was estimated to be of the order of 0.25ns, therefore the skew between the signals is 3.15ns. Similarly the skew between the PP008 voltage probe and the PPE2kV high voltage probe was found to be 3.0ns.

The skew compensation of the probes was made with respect to the PP008 probe. Therefore, +3.15ns (backward time shift) was set for the current probe and -3.0ns (forward time shift) for the high voltage probe.

4.2.5 Physical implementation

The DPT was implemented in a two layer plated-through hole (PTH) FR4 board. A photograph of one of the DPT boards is shown in Figure 4.9, [107].

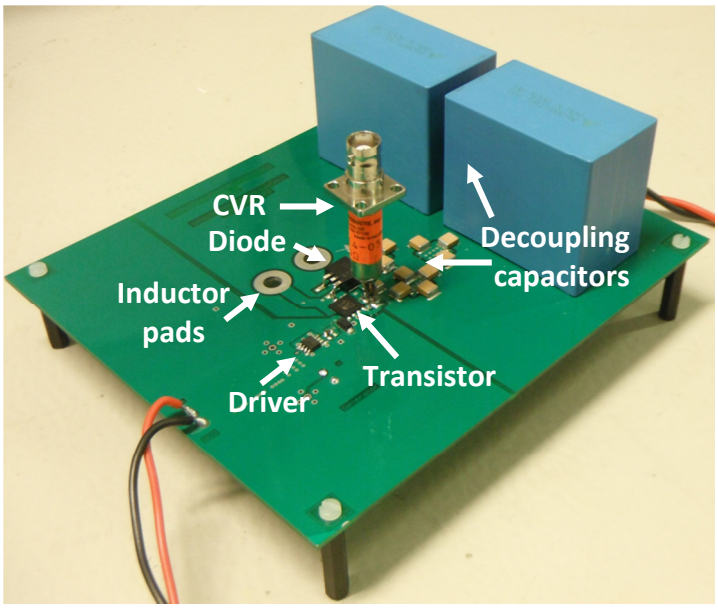


Figure 4.9: DPT board, [107]

4.3 Super-junction Si MOSFET waveforms

This section presents the results from two super-junction Si MOSFETs to serve as a basis for comparison for GaN devices.

The first is a ST MDmesh II STL24NM60N super-junction Si MOSFET rated at 600V, 16A, $R_{DS\text{-}ON}$ = 0.2Ω (typical at 25°C) in a PQFN 8x8 package and the second is a state-of-the-art Infineon C7 IPP65R125C7 super-junction Si MOSFET rated at 650V, 18A, $R_{DS\text{-}ON}$ = 0.111Ω (typical at 25°C) and through hole packaged. The first MOSFET is a currently available part and has a similar rating to the Transphorm GaN cascode device. The Infineon part represents the best Si alternative similarly rated to the Transphorm device. Both MOSFETs were tested along with a Rohm SCS210AJ SiC diode. Figure 4.10 presents some sample waveforms of the turn-off and turn-on transients of the MDmesh Si MOSFET at V_i = 400V, I_L = 10A, V_{DD} = 10V and R_G = 10Ω whilst Figure 4.11 presents the switching transitions of the C7 super-junction Si MOSFET at the same conditions.

The turn-off waveforms of the MDmesh II MOSFET exhibit very slow transients, the measured current fall time is 12.4ns (-0.6kA/µs) and the voltage rise time is 15ns (21.0kV/µs) whilst the C7 Si MOSFET presented significantly quicker transients showing a current fall time of 8ns (-1.0kA/µs) and a voltage rise time of 6.4ns (50.0kV/µs). As a consequence, the C7 Si MOSFET waveforms trigger more

parasitic oscillations. The plateau seen in the turn-off current waveforms is due to the current drawn by the freewheel diode output capacitance as it is discharged. The magnitude of the current drop during the drain-source voltage transition is proportional to the non-linear diode capacitance and the drain-source voltage switching speed. The current drop is more pronounced for the C7 MOSFET due to the much more rapid rate of rise of the drain-source voltage. The voltage overshoot in the turn-off voltage waveform reaches 468V in the C7 waveforms, 30V higher to that in the MDmesh II MOSFET due to the higher switching speed.

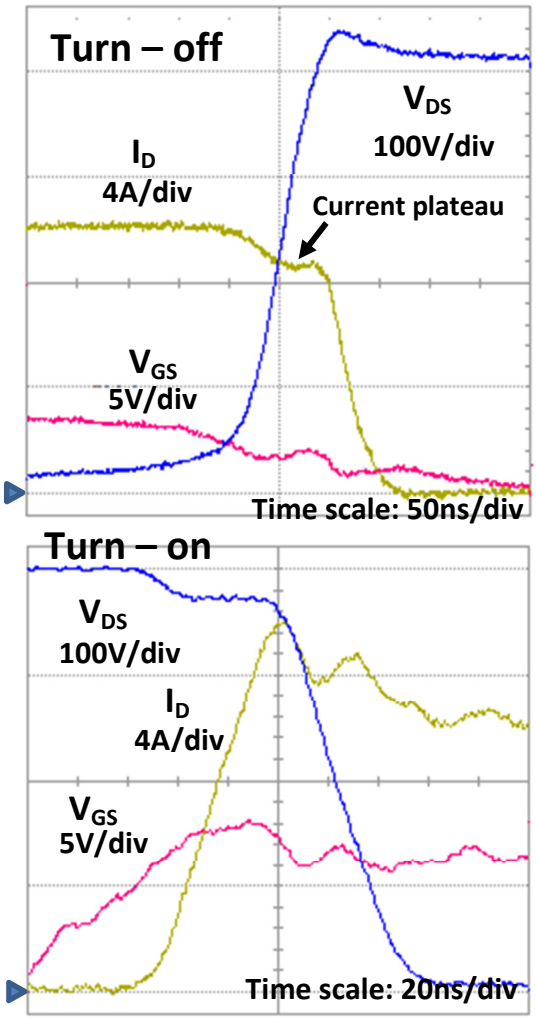


Figure 4.10: Single MDmesh Si MOSFET along with a SiC diode switching waveforms at V_i = 400V, I_L = 10A, V_{DD} = 10V and R_G = 10Ω

The MDmesh Si MOSFET waveforms are quicker during turn-on than those measured for the C7 Si MOSFET, the main difference is in the current rise time whilst the voltage fall time is very similar. The measured current rise time was 5.5ns (1.5kA/µs) for the MDmesh part and 8.1ns for the C7 Si MOSFET (1.0 kA/µs). The

voltage drop in the turn-on drain-source waveforms is generated by the total stray inductance of the power loop as discussed in 3.6.2. An estimation of the boards power loop stray inductance can be obtained by dividing the voltage drop by the rate of change of current. The power loop inductances are shown in Table 4.4.

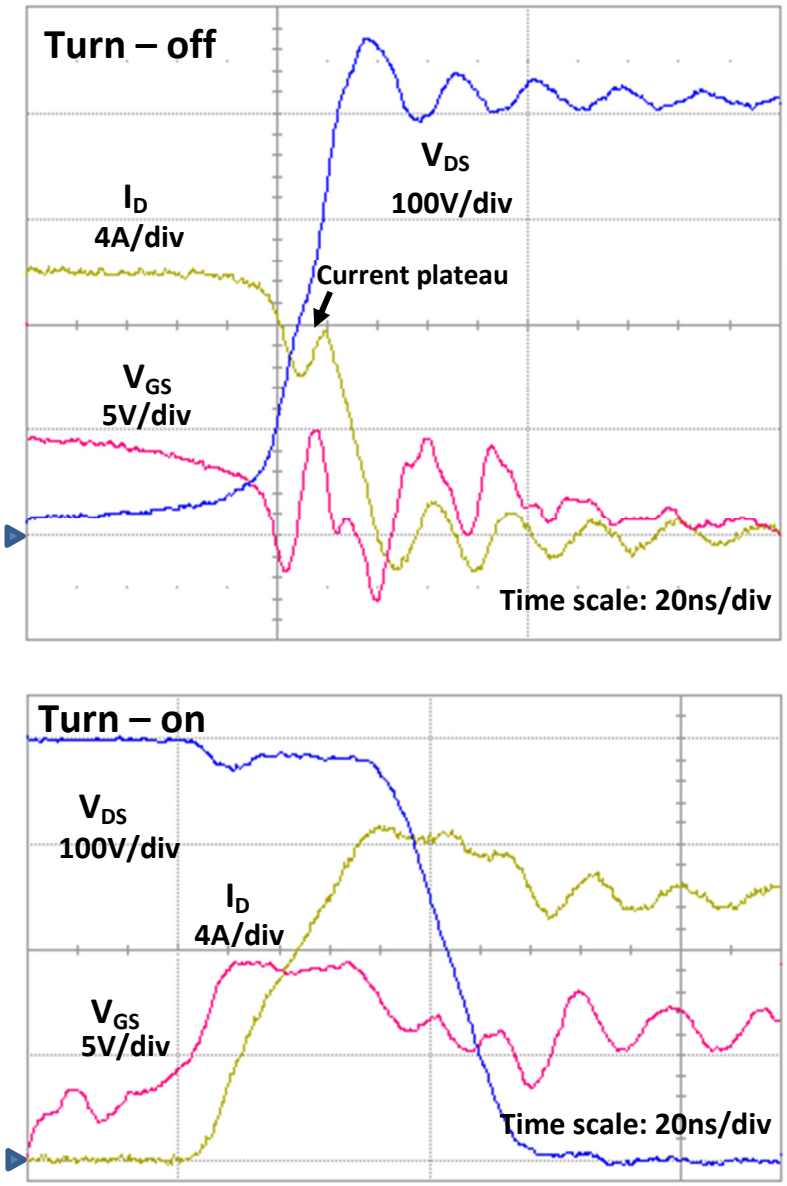


Figure 4.11: Single C7 super-junction Si MOSFET along with a SiC diode switching waveforms at V_i = 400V, I_L = 10A, V_{DD} = 10V and R_G = 10Ω

Table 4.4: Estimated power loop inductances

Board	Power loop inductance (nH)
MDmesh Si MOSFET+ SiC diode	20.7
C7 Si MOSFET + SiC diode	24

The estimations in Table 4.4 are consistent with measured power loop stray inductance in Table 4.1 and Table 4.2, 10nH, considering that the current shunt has a stray inductance of 2nH, the typical stray inductance is 2nH for a PQFN package, 6nH for a D2PAK package and at least 6nH for a TO-220 package, [170]. Therefore, around 20nH may be expected for the MDmesh Si MOSFET board power loop and around 24nH for the C7 board power loop as shown in Table 4.5.

Table 4.5: Si MOSFETs' double pulse tester board estimated power loop inductances

Inductance	**MDmesh Si MOSFET+ SiC diode board**	**C7 Si MOSFET + SiC diode board**
PCB inductance (nH)	10	10
Diode inductance (nH)	6	6
Transistor inductance (nH)	2	6
Current shunt inductance (nH)	2	2
Total power loop inductance (nH)	**20**	**24**

The current overshoot at turn-on looks relatively smooth in both cases reaching 4A above the inductor current for the MDmesh II MOSFET and 3A for the C7 MOSFET. The difference is explained by the higher current switching speed observed in the MDmesh MOSFET during turn-on.

The devices were tested at different current and voltage operating conditions, the measured switching times and switching speeds are summarised in Table 4.6 and Table 4.7.

The highest measured turn-off current switching speed was -1.3kA/μs whilst it was 1.5kA/μs for the turn-on current. The highest measured voltage switching speed was 50kV/ μs and was observed at 400V and 10A for the turn-off voltage transient of the C7 Si MOSFET. The highest voltage speed of the MDmesh part was 41.6kV/ μs and was measured at 400V and 5A during the turn-on voltage transient.

Table 4.6: Si MOSFETs' switching times at V_{DD} = 10V and R_G = 10Ω over different operating conditions

Test conditions	DPT board	Turn-off		Turn-on	
		Current fall time (ns)	Voltage rise time (ns)	Current rise time (ns)	Voltage fall time (ns)
200V, 5A	MDmesh II + SiC diode	8.2	13.4	3.1	6.1
	C7 + SiC diode	9.7	12.3	2.9	6.9
200V, 10A	MDmesh II + SiC diode	18.4	14.6	5.4	7.8
	C7 + SiC diode	6.1	6.5	8.8	7.3
400V, 5A	MDmesh II + SiC diode board	12.3	15.8	3.2	7.7
	C7 + SiC diode	12.5	13.4	3.4	8.2
400V, 10A	MDmesh II + SiC diode board	12.4	15.0	5.5	9.2
	C7 + SiC diode	8.0	6.4	8.1	9.2

Table 4.7: Si MOSFETs' switching times at V_{DD} = 10V and R_G = 10Ω over different operating conditions

Test conditions	DPT board	Turn-off		Turn-on	
		Current switching speed (kA/µs)	Voltage switching speed (kV/µs)	Current switching speed (kA/µs)	Voltage switching speed (kV/µs)
200V, 5A	MDmesh II + SiC diode	-0.5	11.9	1.3	-26.2
	C7 + SiC diode	-0.4	13.0	1.4	-23.1
200V, 10A	MDmesh II + SiC diode	-0.4	11.0	1.5	-20.5
	C7 + SiC diode	-1.3	24.6	0.9	-21.9
400V, 5A	MDmesh II + SiC diode board	-0.3	20.3	1.3	-41.6
	C7 + SiC diode	-0.3	23.9	1.2	-39.0
400V, 10A	MDmesh II + SiC diode board	-0.6	21.0	1.5	-35.0
	C7 + SiC diode	-1.0	50.0	1.0	-35.0

4.4 Evaluation of Transphorm GaN transistors

Two different GaN cascode transistor samples were obtained for evaluation. The first devices were provided by Transphorm, and are TPH3006LD, in a PQFN 8x8 SMD package rated at 600V, 17A and 0.15Ω at 25°C.

4.4.1 Single device along with a SiC diode

Figure 4.12 shows some sample waveforms for the Transphorm device with a Rohm SCS210AJ SiC diode.

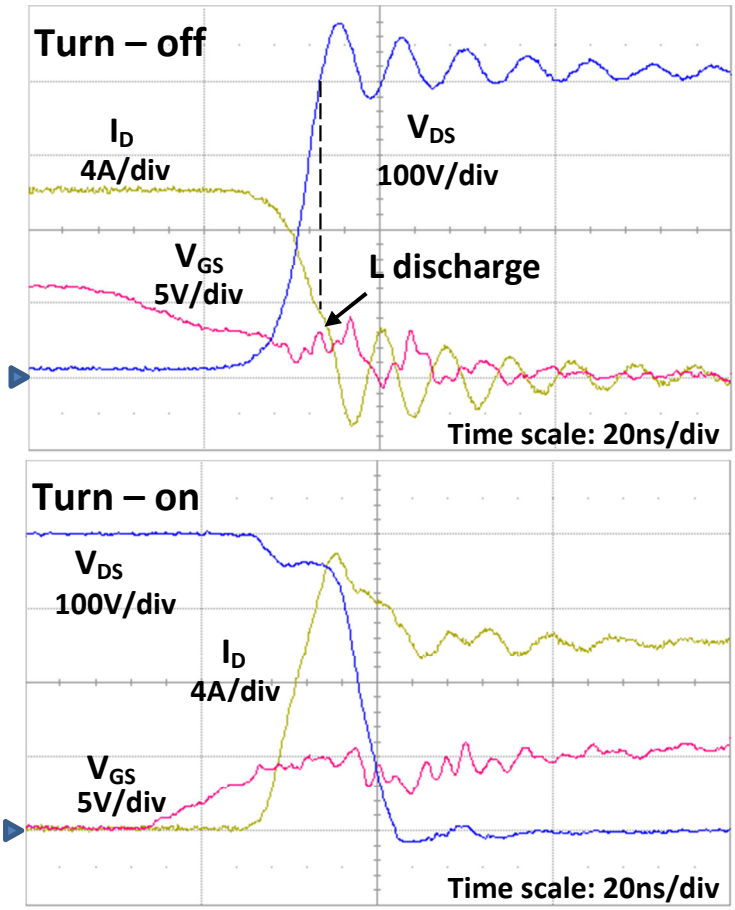


Figure 4.12: Single Transphorm device along with a SiC diode switching waveforms at $V_i = 400V$, $I_L = 10A$, $V_{DD} = 6V$ and $R_G = 10\Omega$

At turn-off the transition time of the drain current is 6.6ns and 5.2ns for the drain to source voltage; the switching speeds are -1.2kA/µs and 69.6kV/µs respectively. The measured switching speeds are 20% and 39% higher respectively that in the C7 Si MOSFET in Table 4.7 of section 4.3. High frequency oscillations are observed in the waveforms as a result of the resonance between the stray inductance and the parasitic capacitance of the GaN switch. The current and voltage waveforms are switching

simultaneously resulting in smaller losses in comparison with a more traditional waveform where the current switches under high voltage conditions and the voltage switches under high current conditions. The voltage overshoot reaches 480V, 12V higher than what was reported in section 4.3 for the C7 Si MOSFET. The higher switching speed of the GaN device explains the difference.

The turn-on switching time is 4.1ns for the current and 4.0ns for the voltage; the switching speed is 1.9kA/μs for the current and -90.7kV/μs for the voltage. The measured current switching speed is 27% higher and the voltage switching speed is 2.6 times higher than measured for the quicker Si MOSFET under similar conditions reported in Table 4.7 of section 4.3. The superior switching speed of the GaN cascode device will result in reduced switching losses. The voltage drop can be used to estimate the power loop stray inductance as detail in section 4.3, resulting in a value of 21.1nH, very close to the value for the MDmesh Si MOSFET, Table 4.4, which is expected as the boards are virtually identical.

At turn-on, the current overshoot over the steady state value is 4.8A, 20% higher than was measured for the MDmesh II Si MOSFET in section 4.3. The higher switching speed of the GaN explains the difference.

The turn-on switching process of the GaN device looks similar to that in a single device (as in the Si MOSFET) where the current switches under high voltage conditions and the voltage switches under high current conditions. Any reduction in turn-on energy loss in the GaN device would be related to its more rapid switching speed.

Different driver voltage and gate resistors values were tested to evaluate their effect on the switching time of the main waveforms. Figure 4.13 shows the switching times with different gate resistor values for a 400V and 10A condition.

The plot shows that no switching time measurement was above 11 ns, even at the higher gate resistor value of 30 Ω.

The current fall time during turn-off remains relatively constant up to R_G = 18 Ω. After that, it starts to increase. The drain to source voltage rise time is relatively constant up to R_G = 5 Ω when it starts to increase; its increase is less than 10% at 10Ω. The data confirms the small effect of the gate resistance on the turn-off process

as predicted by the simple model in section 3.6.3. The output capacitance of the cascode device is mainly charged during $S_{4\text{-OFF}}$ and its charge is insensitive to the driving parameters of the Si MOSFET. As R_G increases, $S_{3\text{-OFF}}$ duration is longer and most of the output capacitance is charged during this stage where R_G controls the current flow of the channels. The measurements suggest that this effects starts to be significant when R_G>15Ω.

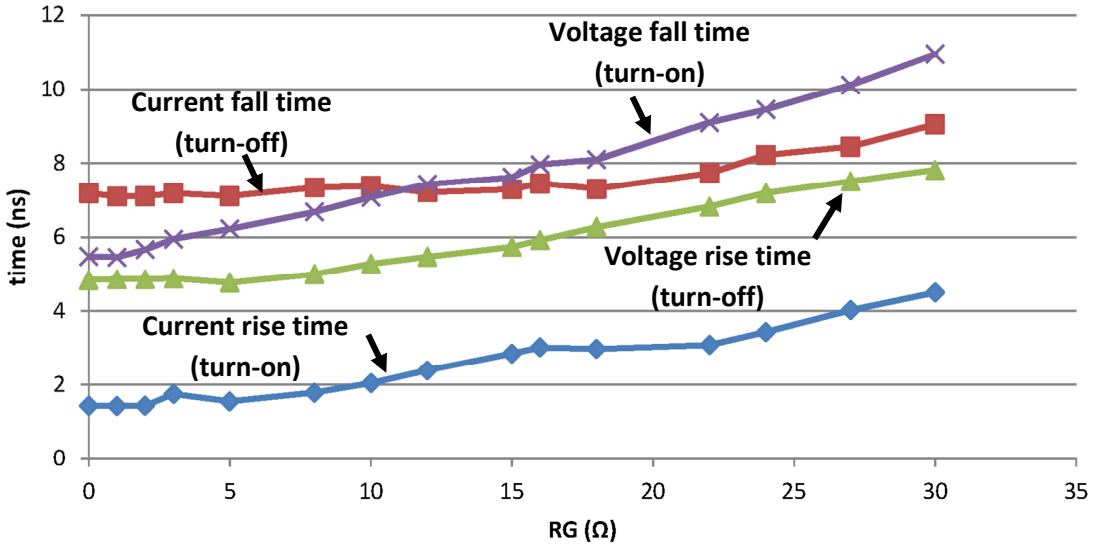


Figure 4.13: Cascode transistor switching times vs. R_G – V_i = 400V, I_L = 10A, V_{DD} = 10V

The turn-on switching transients are more affected by the gate resistor. The tendency is that the switching times increase as the gate resistor increases. The variation of the switching times is less than 15% up to R_G = 5Ω for both the voltage fall time and the current rise time. The overall change over the entire range is 3.1ns for the current rise time (3.1 times at 30Ω with respect to 0Ω) and 5.5ns for the voltage fall time (2 times at 30Ω with respect to 0Ω). Again the experimental measurements verify the predictions of the simple model.

Figure 4.14 shows the switching times for different driver voltages at 400V and 10A. The reported voltage fall time is not the transition from the 90% to the 10% of the operating voltage in this case because of the effect of the voltage drop in V_{DS} waveform, therefore the voltage fall time is measured from the operating voltage to zero.

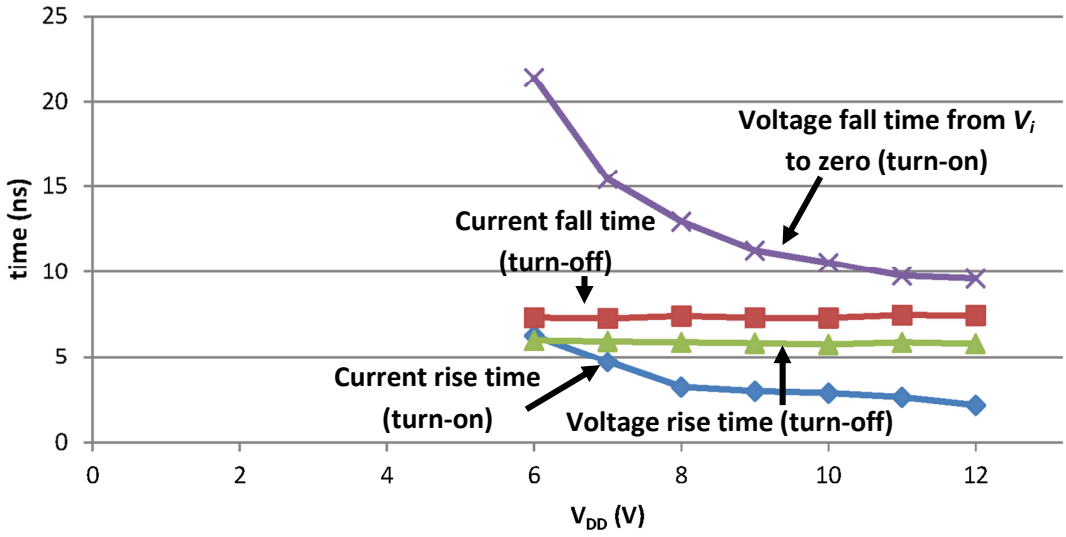


Figure 4.14: Cascode transistor switching times vs. $V_{DD} - V_i = 400\text{V}$, $I_L = 10\text{A}$, $R_G = 15\Omega$

The results show that the turn-off switching times are not sensitive to variations in the driver voltage as predicted by the simple model since only $S_{1\text{-OFF}}$ is affected by the change in V_{DD} as discussed in section 3.6.3. The variation is less than 3% for the current fall time and less than 4% for the voltage rise time.

On the other hand, the turn-on switching times are significantly affected by changes in the driver voltage as predicted by the simple model. As V_{DD} increases, the switching times decrease because of the higher gate current induced by the higher driver voltage. The greatest change is observed when the gate voltage changes from 6V to 7V. The current rise time continues to decrease over the full V_{DD} range, but more gradually for V_{DD} above 8V.

At high switching speeds the parasitic oscillations in the waveforms become more pronounced as illustrated in Figure 4.15, which shows the turn-on waveforms with $R_G = 2\Omega$ at 400V, 10A conditions.

The oscillations in the gate voltage are a particular concern and could result in the transistor turning on and off, potentially increasing the switching losses. In addition, the gate of the transistor can be damaged if the amplitude of the oscillations exceeds the absolute maximum rating, 18V for this Transphorm part. The oscillations in the drain current and drain to source voltage may result in an increased switching loss.

In a practical application a balance must be made between achieving very high switching speeds and restricting the amplitude of the parasitic oscillations.

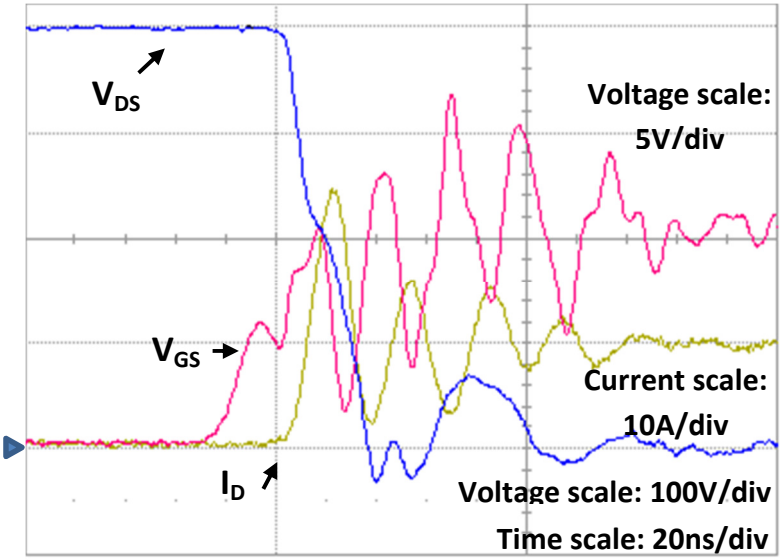


Figure 4.15: Single Transphorm device along with a SiC diode switching waveforms at V_i = 400V, I_L = 10A, V_{DD} = 10V and R_G = 2Ω

Switching energy losses

The turn-off switching energy loss (E_{OFF}), turn-on switching energy loss (E_{ON}) and total switching energy loss ($E_T = E_{OFF} + E_{ON}$) in the Transphorm devices when operating with the SCS210AJ SiC diode were calculated from the measured voltage and current waveforms over a range of operating and driving conditions. Figure 4.16 presents the results.

The plots clearly show that the turn-off loss is insensitive to the driver voltage V_{DD} and the gate resistor R_G. It is also only slightly sensitive to the change in the operating current I_L but much more sensitive to the operating voltage V_i. As discussed in section 3.7.2, the turn-off loss mainly consists of the energy stored in the output capacitance of the transistor, which is only dependent on the operating voltage. The lack of control of the switching behaviour through the driver voltage and the gate resistor results in the small variation of the turn-off loss with operating current. The turn-on loss tends to be significantly higher than the turn-off loss and its sensitivity to the different parameters is much higher. The turn-on energy loss can be controlled by the driver voltage and the gate resistor because of the relation of the switching transients' duration with the gate current as predicted by the simple model in section 3.6.3.

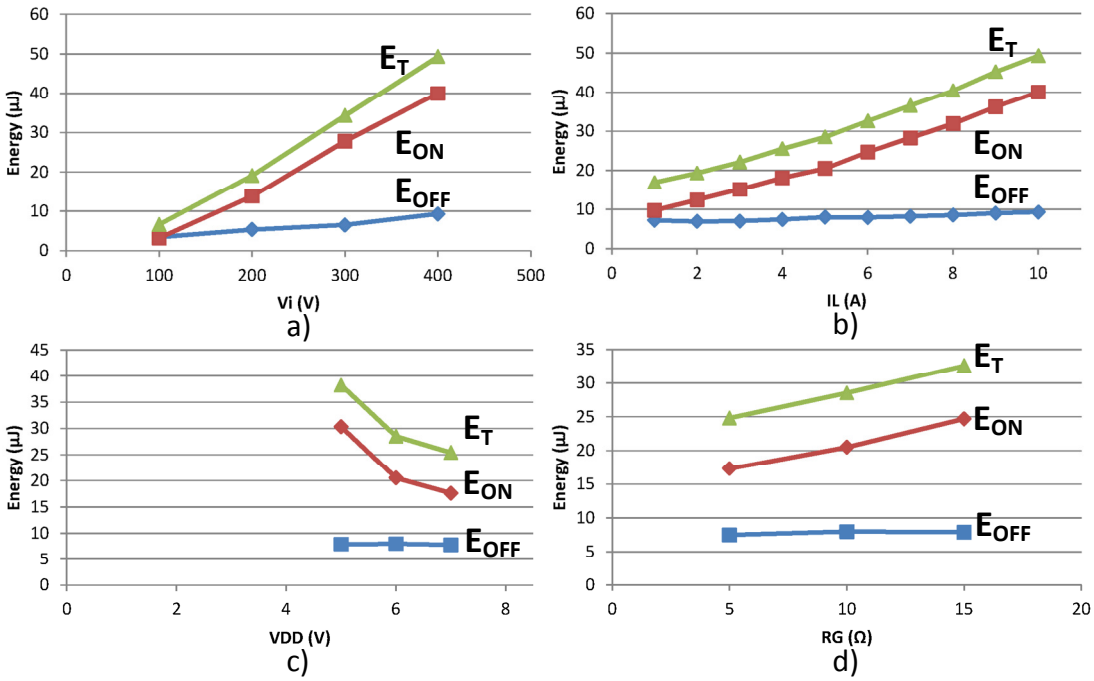


Figure 4.16: Transphorm transistor switching losses using SCS210AJ SiC diode against: a) V_i with I_L = 10A, R_G = 10Ω and V_{DD} = 6V, b) I_L with V_i = 400V, R_G = 10Ω and V_{DD} = 6V, c) V_{DD} with V_i = 400V, I_L = 5A and R_G = 10Ω, d) R_G with V_i = 400V, I_L = 5A and V_{DD} = 6V

The accuracy of the simple model in predicting the total switching energy losses was verified at different sample conditions using the corresponding parameters according to Table 3.4 and Table 3.5. Figure 4.17 presents the results.

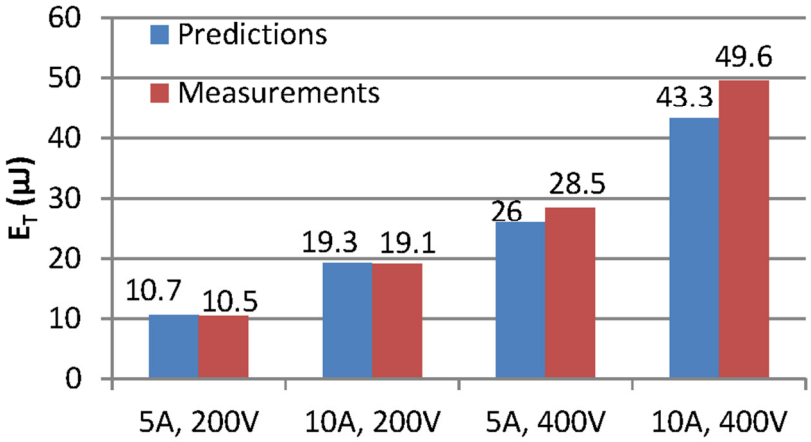


Figure 4.17: Total energy losses, GaN cascode transistor using a SiC diode. Model vs. practical measurements at different operating conditions. V_{DD} = 6V and R_G = 10Ω

Very good agreement is observed at 200V and the predicted values were only 12.7% lower than the measured ones at 400V and 10A. The differences are attributed to the model assumptions of constant capacitances and transconductance and the omission

of the stray inductance. Nevertheless, the model delivers accurate predictions of the total switching energy losses.

4.4.2 Body diode

The cascode transistor body diode is an important part of the arrangement because it provides a reverse conduction path when the channel of the Si MOSFET is closed. The Q_{rr} of a typical high voltage Si MOSFET body diode is very high, usually in the order of μC. The body diode of the low voltage Si MOSFET of the cascode arrangement provides a high quality body diode with low Q_{rr} in the order of just a few tents of nano-coulombs. Using the body diode as the freewheeling path in a circuit application represents an alternative to the addition of an external anti-parallel SiC diode, which is common practice in some Si applications.

Its conduction and switching characteristics are evaluated to assess its performance.

I-V curve

The I-V curve for the body diode of a Transphorm cascode device is plotted in Figure 4.18 along with the characteristics of the SiC diode. The body diode of the Transphorm device has lower forward voltage at lower forward currents than the SiC diode whilst the SiC diode has lower forward voltage at higher forward currents. The slope of the curves suggests that the body diode of the cascode transistor has higher resistance than the SiC diode. In addition, the difference between the forward voltages of the devices will increase as the forward current increases. Part of the measured forward voltage of the body diode of the cascode device is generated by the channel resistance of the GaN HEMT. Therefore, the SiC diode conduction losses are expected to be lower at high operating current (above 2.2A) when compared against the cascode body diode.

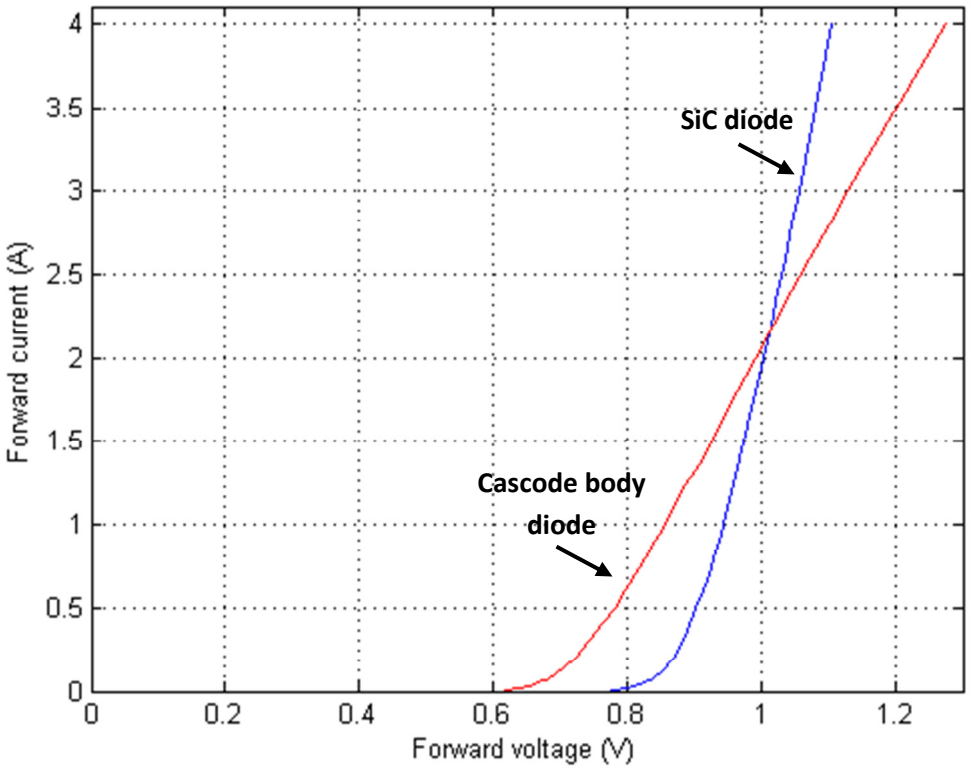


Figure 4.18 : I-V curves - Rohm SiC diode vs. Transphorm GaN cascode transistor body diode

Reverse recovery charge

The next figures present the Transphorm GaN cascode transistor body diode Q_{rr} measurements over different operating current (Figure 4.19), operating voltage (Figure 4.20) and current switching speed (Figure 4.21) using the DPT board with two GaN devices in an inverter leg configuration that is described in section 4.4.3. The turn-on current switching speed is controlled by changing the driver voltage at fixed $R_G = 51\Omega$.

The first plot shows that the operating current has only a small influence on Q_{rr}. The second plot indicates that the operating voltage has high influence on Q_{rr}, an increase of 47% is observed from $V_i = 100V$ to $V_i = 480V$, which is attributed to capacitive effects. Finally, the third plot shows that the current switching speed increases Q_{rr}. A variation of 26% is observed.

A SiC Schottky diode has no reverse recovery charge, only capacitive charge. The SiC diode used for the comparison in the previous section has Q_{rr} = 15nC at $V_R = 400V$ and di/dt = 350A/µs which is less than a third of the value of the cascode body diode that is specified in the cascode device datasheet.

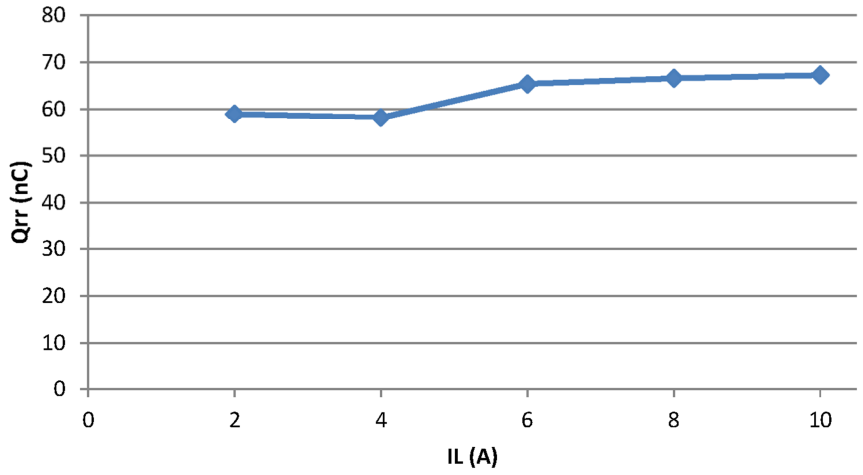


Figure 4.19: Transphorm GaN cascode transistor body diode Q_{rr} against operating current at di/dt = 1kA/µs, V_i = 400V

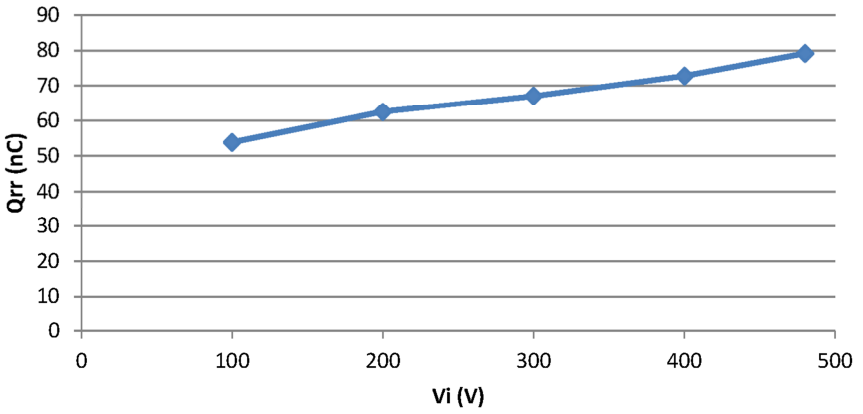


Figure 4.20: Transphorm GaN cascode transistor body diode Q_{rr} against operating voltage at di/dt = 1.5kA/µs, I_L = 10A

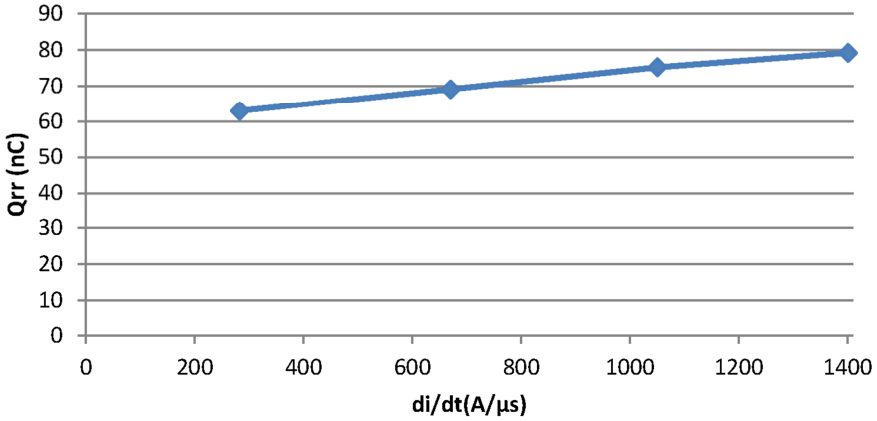


Figure 4.21: Transphorm GaN cascode transistor body diode Q_{rr} against di/dt at V_i = 480V, I_L = 10A

Whilst the SiC diode has far superior performance, the body diode of the cascode device is a significant improvement over the body diode of a single high- voltage Si MOSFET.

4.4.3 Two GaN cascode devices in an inverter leg configuration

The DPT was modified to accommodate a second GaN cascode device in the freewheeling diode position. The second GaN device gate and source pads were short-circuited to hold the device in the off-state. The freewheel path is then through the body diode of the Si MOSFET and the channel of the GaN HEMT. Figure 4.22 illustrates the new circuit.

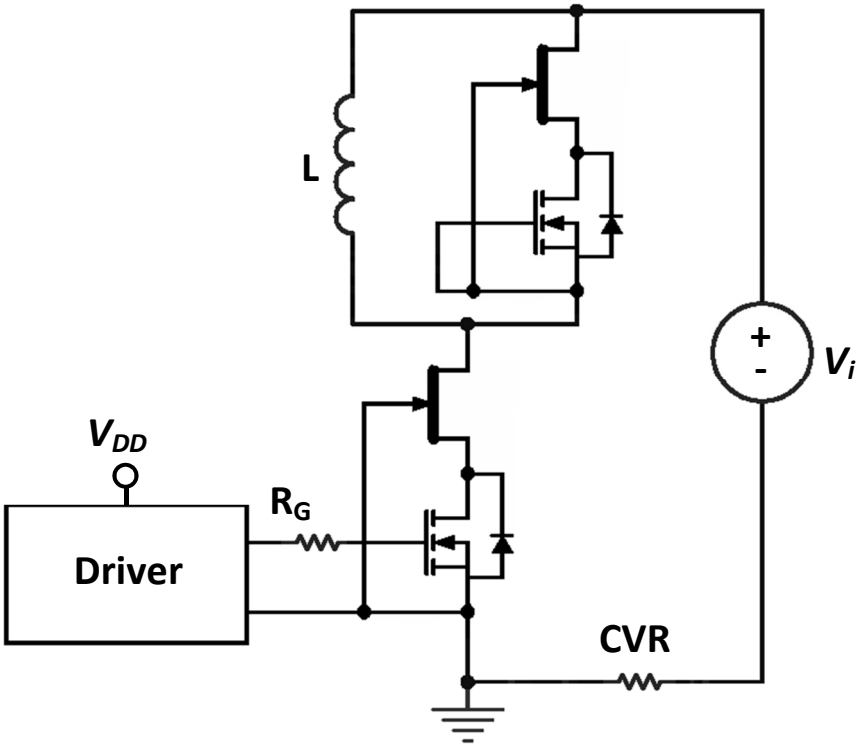


Figure 4.22: Two GaN cascode devices in an inverter leg configuration DPT circuit

The switching waveforms of this circuit are compared against the ones obtained with a single GaN cascode device and a SiC diode. Figure 4.23 and Figure 4.24 show the comparison at V_i = 400V, I_L = 10A, V_{DD} = 6V and R_G = 10Ω.

Table 4.8 compares the switching times of the waveforms in Figures 4.23 and 4.24 .

The turn-off switching times are longer for the case of two GaN devices in a leg. The difference in turn-off switching times can be explained by the higher output capacitance of the cascode device when compared with the SiC diode capacitance.

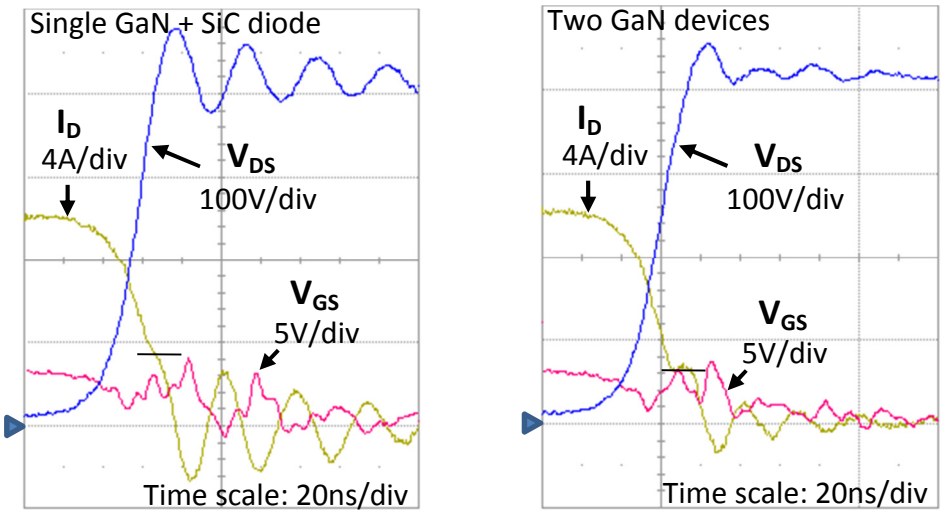


Figure 4.23: Turn-off waveforms, single GaN device along with a SiC and two GaN cascode devices in an inverter leg configuration at V_i = 400V, I_L = 10A, V_{DD} = 6V and R_G = 10Ω

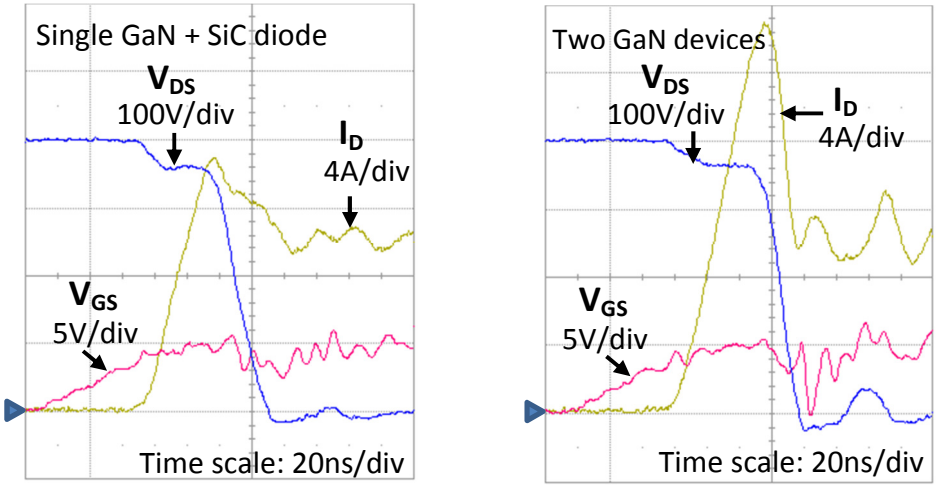


Figure 4.24: Turn-on waveforms, single GaN device along with a SiC and two GaN cascode devices in an inverter leg configuration at V_i = 400V, I_L = 10A, V_{DD} = 6V and R_G = 10Ω

Table 4.8: Switching times, GaN cascode device and SiC diode vs two GaN cascode devices in an inverter leg configuration

Arrangement	Turn-off		Turn-on	
	Current fall time (ns)	Voltage rise time (ns)	Current rise time (ns)	Voltage fall time (ns)
Single GaN cascode device + SiC diode	6.6	5.2	4.1	7.1
Two GaN cascode devices in an inverter leg configuration	8.1	6	4.1	5.1

The difference in capacitance between the cascode device and the SiC diode also explains why the current plateau predicted by the simple model at turn-off is at a slightly lower level in the case of the two GaN devices in a leg. Also, the voltage switches at slightly lower current levels during turn-off in the case of the two GaN devices in a leg potentially reducing the energy losses. However, the switching times are longer for the two GaN devices in a leg, potentially increasing the energy losses. Similar turn-off energy losses are expected in these configurations.

The turn-on waveforms show a very high current overshoot when two GaN cascode devices are used, as a result, higher diode induced switching loss will occur. The diode induced switching loss (D_{IL}) can be estimated by the integrating the transistor current overshoot at turn-on as shown in Figure 4.3:

$$D_{IL} = \int_{t_a}^{t_b} \left(i_D(t) - I_L \right) v_{DS}(t)\, dt \tag{4.2}$$

The diode induced switching loss was estimated to be 7.4μJ for the single GaN cascode device along with a SiC diode and 23.4μJ for the two GaN cascode devices for the waveforms in Figure 4.24. The arrangement of two GaN cascode devices results in 3.2 times higher diode induced loss. The diode induced switching loss represents 18.5% of the total turn-on loss for the GaN device and SiC diode whilst it represents a 37.9% of total turn-on loss for the two GaN devices. The complete energy loss data for the two GaN device arrangement is presented later in this section in Figure 4.25 whilst the information for the single device along with a SiC diode was presented in Figure 4.16 in section 4.4.1.

The current rise time is very similar in the two arrangements, but the voltage fall time is smaller with the two GaN cascode devices. The difference can be explained by the higher transient current when two GaN cascode devices are used allowing a more rapid discharge of the output capacitance of the switching device.

Switching energy losses

The switching energy loss of the configuration was measured over the same driver and operating conditions as with the arrangement of a cascode device and a SiC diode. The data is presented in Figure 4.25. The tendencies are very similar to the

ones observed in the single cascode device and SiC diode combination but the turn-on and total losses are higher by around 50%. The increase can be explained by the poor reverse recovery characteristics of the Si MOSFET body diode of the cascode device in comparison with the SiC diode. Even so, the increase in loss is not excessive and allows the possibility of using the two GaN cascode devices in an inverter leg configuration without the need of adding separate freewheeling diodes reducing the component count. This would not be possible with super junction Si MOSFETs because of their extremely poor reverse recovery characteristics, [109], and the charge added by their non-linear output capacitance.

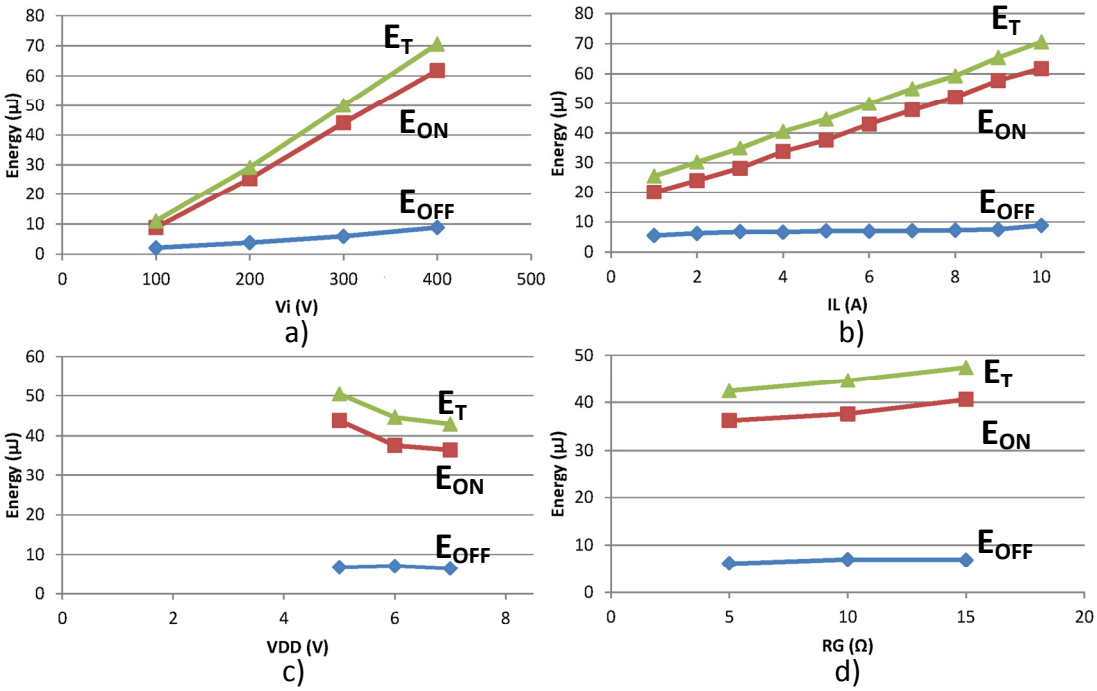


Figure 4.25: Two Transphorm transistors in an inverter leg configuration switching energy losses over: a) V_i with I_L = 10A, R_G = 10Ω and V_{DD} = 6V, b) I_L with V_i = 400V, R_G = 10Ω and V_{DD} = 6V, c) V_{DD} with V_i = 400V, I_L = 5A and R_G = 10Ω, d) R_G with V_i = 400V, I_L = 5A and V_{DD} = 6V

The turn-off loss is lower in this arrangement when compared against the single cascode device along with a SiC diode due to the comparatively higher capacitance of the cascode device with respect to the SiC diode.

The simple model can be used to predict the switching losses of this configuration by considering the diode capacitance, C_D, to have an equivalent value based on the reverse recovery charge value of the cascode transistor body diode. The capacitance is calculated using the following equation:

$$C_D = \frac{Q_{rr}}{V_i} \tag{4.3}$$

The Transphorm device datasheet specifies a Q_{rr} value at specific conditions of current, voltage and current switching speed. Figure 4.26 shows the simple model total switching energy (E_T) predictions at different conditions using the datasheet Q_{rr} value (in all the cases) against measurement values. The model used the parameters listed in Table 3.4 and Table 3.5 at the specific operating conditions. The specified cascode body diode Q_{rr} is 54nC from the datasheet, therefore the diode capacitance was assumed to be 135pF for 200V and 270pF for 400V.

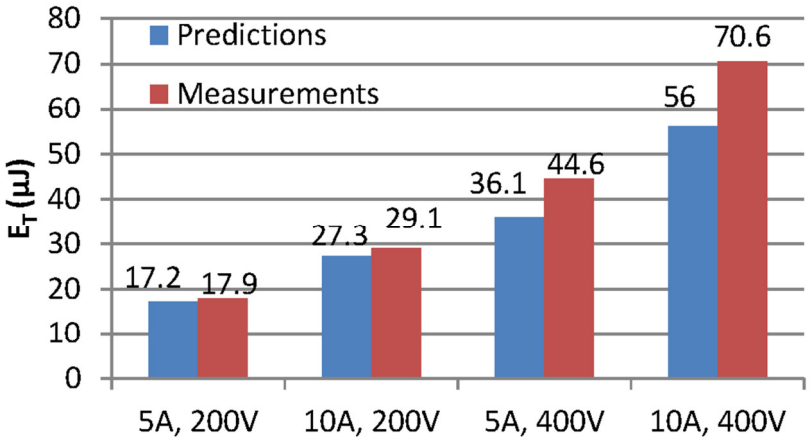


Figure 4.26: Total switching energy losses, two GaN transistors in an inverter leg configuration. Simple model vs. practical measurements. V_{DD} = 6V and R_G = 10Ω

The predicted values are very close to the practical measurements at 200V (less than 7% of variation) whist the predicted values are up to 20.7% smaller at 400V. The use of a Q_{rr} value different from the actual operating conditions, the omission of the stray inductance and the consideration of constant capacitances is thought to explain the differences.

Table 4.9 presents the measured reverse recovery charge values at different conditions and its equivalent diode capacitance calculated using (4.3). Closer predicted values are obtained using the model with the same parameters but using the equivalent capacitances of Table 4.9 as shown in Figure 4.27.

The predicted values are up to 10% smaller than the practical measurements at 400V and much better agreement is obtained at 200V.

Table 4.9: Measured Q_{rr} values at different conditions and their equivalent diode capacitance at V_{DD} = 6V and R_G = 10Ω

Conditions	Q_{rr} (nC)	C_D (pF)
5A, 200V	58.4	292
10A, 200V	66.1	330.5
5A, 400V	67.6	169
10A, 400V	76.4	191

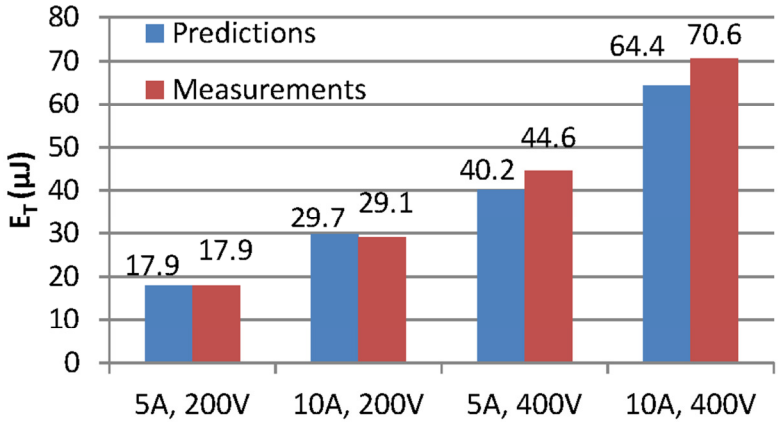


Figure 4.27: Energy losses, two GaN transistors in an inverter leg configuration. Simple model vs. practical measurements using measured Q_{rr} values to calculate C_D. V_{DD} = 6V and R_G = 10Ω

4.4.4 Energy losses comparison

The Transphorm device energy losses were measured under different operating conditions and compared against other device combinations to evaluate the feasibility of using GaN devices in an inverter leg configuration and to identify the most effective configuration. Different DPT boards were built to evaluate the following device arrangements:

1. **Body diode suppression and separate SiC anti-parallel diode.** The leg is formed by two GaN cascode devices with antiparallel SiC diodes and series Si Schottky diodes to block the cascode device body diode. The circuit is presented in Figure 4.28.

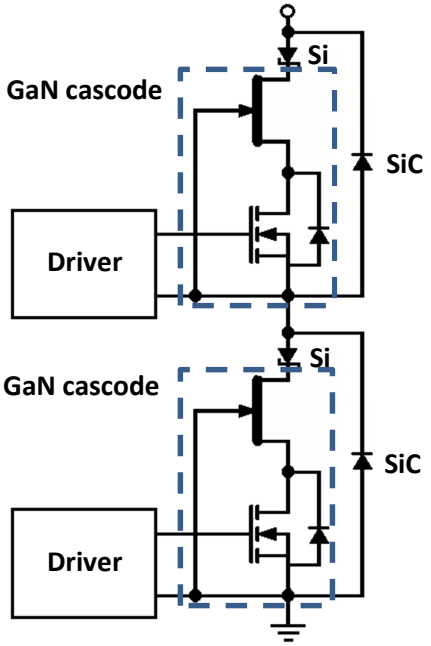


Figure 4.28: Body diode suppression and SiC freewheel diode

2. **Two GaN cascode devices.** This configuration uses only two devices and exploits the body diodes of the cascodes to provide the freewheel path as shown in Figure 4.29.

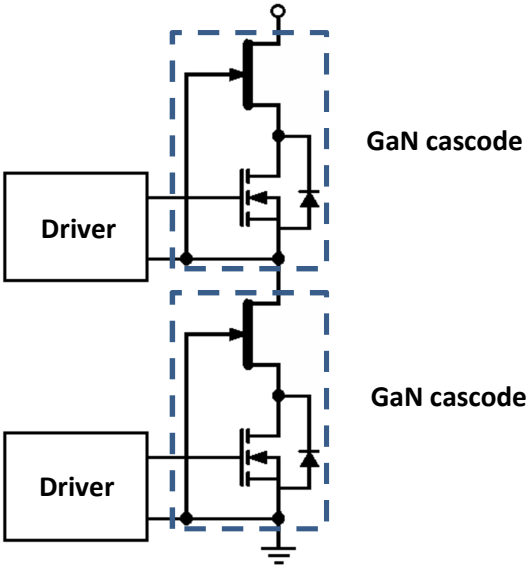


Figure 4.29: Two GaN cascode devices in an inverter leg configuration

3. **Two GaN cascode devices + an antiparallel SiC diode**. An antiparallel SiC diode is used, but without any diodes in series with the cascode to suppress the body diode conduction. Four devices are required for this combination, Figure 4.30.

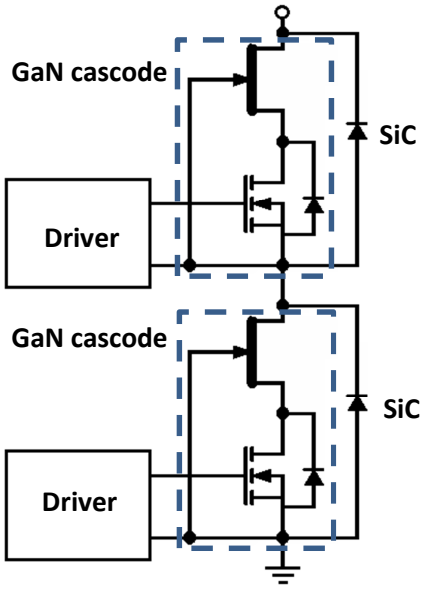


Figure 4.30: Two GaN cascode devices in an inverter leg configuration + SiC diode

4. **A MDmesh II super junction Si MOSFET + SiC diode.** This combination is same as that in Figure 4.28 except that the GaN cascode devices are replaced by Si MOSFETs. The device used is a ST MDmesh II super junction Si MOSFET, 600V, 16A, R_{DS} = 0.2Ω (typical at 25°C) in a PQFN 8x8 package. This currently available MOSFET has a similar rating to the cascode device and some waveforms were presented in section 4.3.

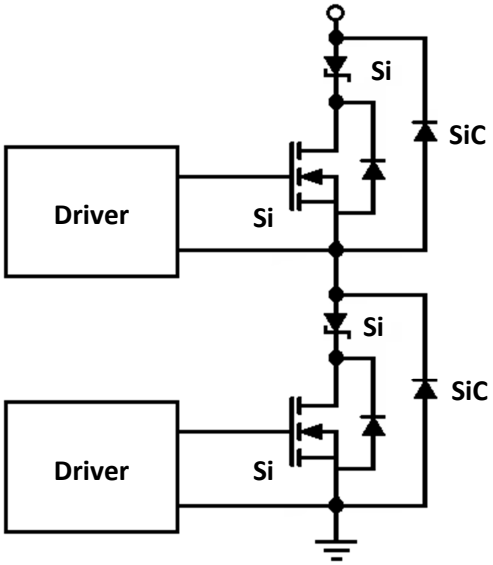


Figure 4.31: MDmesh II super junction Si MOSFET + SiC diode

5. **A C7 super junction Si MOSFET + SiC diode.** This combination is similar to that in Figure 4.31 but with the Si MOSFETs replaced by state-of-the-art C7 super junction Si MOSFETs. An Infineon IPP65R125C7 in through hole package was used; its rating being 650V, 18A, $R_{DS\text{-}ON}$ = 0.111Ω (typical at 25°C). This combination presents the best solution that can be obtained using Si transistors and SiC diodes and will be used as a base to compare the performance of the GaN combinations. Sample waveforms were presented in section 4.3.

Figure 4.32, [107], presents the energy loss measurements of the five different device combinations under four different current and voltage operating conditions. Turn-off, turn-on and total losses are shown and compared. The driver voltage was 6V for the GaN device combinations and 10V for all the Si combinations; R_G = 10Ω for all the cases.

As expected, the total energy losses of the two GaN cascode devices in a leg are higher when compared against the single device along with a SiC diode arrangement, around 50% higher. The turn-off losses of the two GaN cascode devices in a leg are slightly lower than the ones in the single device along with a SiC diode because of the higher capacitance of the GaN cascode transistor with respect to the SiC diode. For example, the output capacitance of the cascode devices is around 63pF at 200V and the diode capacitance at the same level of reverse voltage is around 42pF.

The addition of an antiparallel SiC diode to the cascode device results in an increase in the total switching loss at low current and in a reduction at high current conditions. The explanation of this is that the cascode device body diode conducts most of the current at low current conditions, whilst the SiC diode conducts most of the current at high current conditions. The device conducting most of the current will have a more significant effect on the turn-on switching losses. The lower forward voltage at higher operating currents of the SiC diode (as presented in Figure 4.18) allows it to conduct most of the current and by consequence to dominate the switching behaviour of the overall parallel combination.

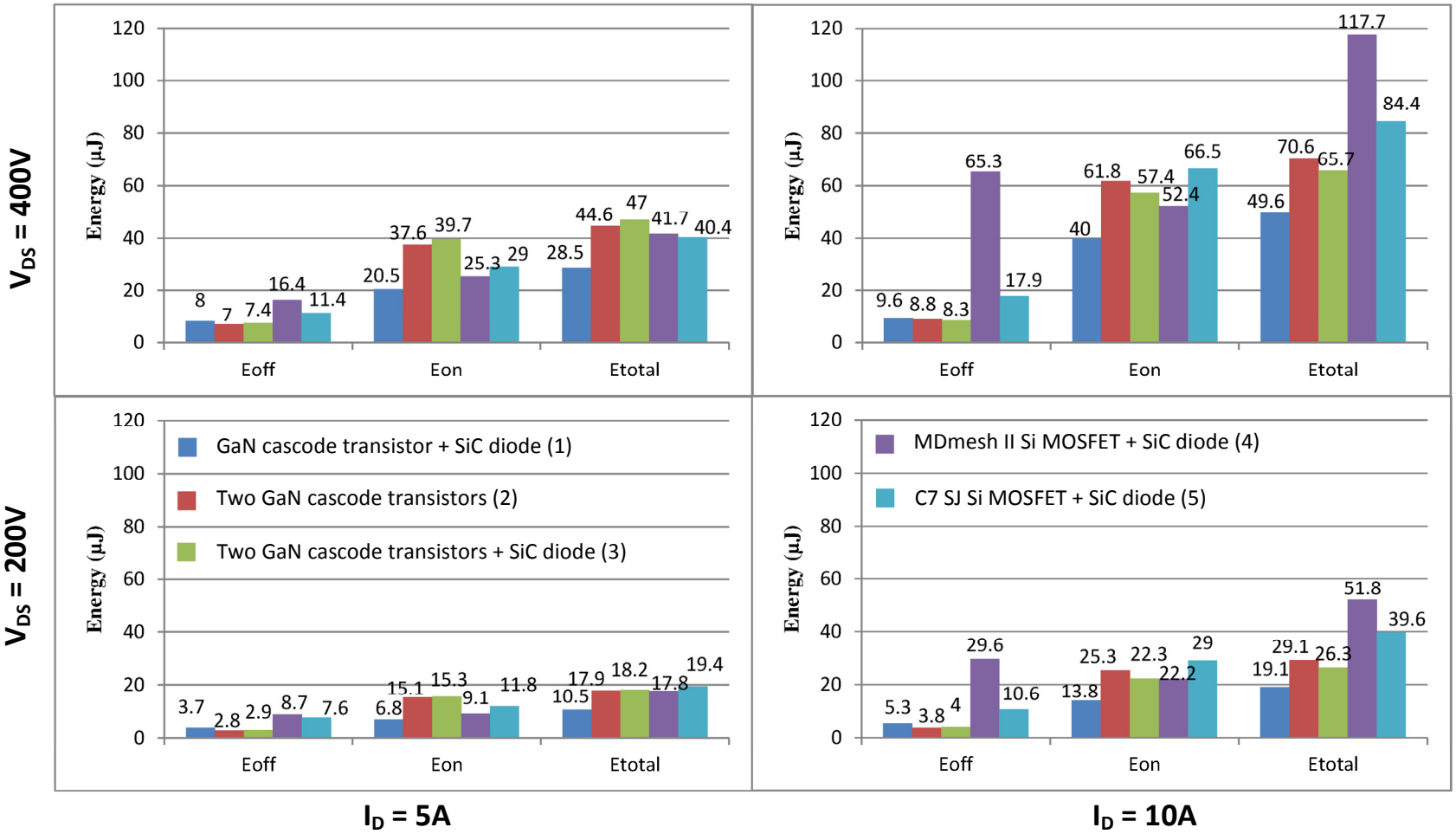


Figure 4.32: Switching energy losses at different voltage and current levels, V_{DD} = 6V (GaN) and 10V (Si); R_G = 10Ω, [107]

The total energy losses of the MDmesh II Si MOSFET along with a SiC diode combination are more than 46% higher at low current and up to 240% higher at high current when compared with the losses of the single cascode device + SiC diode. The single GaN device + SiC diode is superior over all the operating conditions when compared with the MDmesh II Si MOSFET combination. The MDmesh II Si MOSFET + SiC diode presents slightly lower losses than the two GaN cascode devices in a leg configuration at low operating current but has significantly higher losses at high operating current. Even when the turn-on loss of this Si device is lower than that of the state-of-the-art C7 Si SJ, its turn-off loss is significantly higher (up to 3.6 times higher) presenting overall higher losses than the state-of-the-art Si MOSFET.

The state-of-the-art C7 SJ Si MOSFET + SiC freewheel diode combination has up to two times higher losses than the single GaN cascode device + SiC freewheel diode arrangement. At high current and voltage conditions the energy loss is 1.7 times higher. The total energy losses of the state-of-the-art C7 SJ Si MOSFET + SiC freewheel diode combination is up to 36% higher when compared against the two GaN cascode devices in an inverter leg combination at high current conditions. The faster switching speed of the cascode device compensates for the higher body diode induced turn-on loss. In addition, the component count is reduced from six devices to only two cascode devices reducing the system cost and complexity. The practical testing demonstrates the viability of using only two GaN cascode devices in an inverter leg configuration resulting in lower losses and lower component count when compared against the best Si MOSFET solution.

4.5 GaN Systems cascode devices energy losses

GaN Systems samples were evaluated in addition to the ones provided by Transphorm. The parts were tested in two configurations: single device along with a SiC diode and two devices in an inverter leg configuration. The device breakdown voltage is similar to the Transphorm one but the GaN Systems device is rated at higher maximum drain current.

4.5.1 GaN Systems transistors

These transistors were similarly packaged (PQFN 8x8) and rated at 650V, 30A and 60mΩ typically at case temperature of 25°C.

Two DPT boards were built to evaluate the energy losses of a GaN Systems cascode device along with a SiC diode and two GaN devices in an inverter leg configuration.

4.5.2 Single cascode device along with a SiC diode

The GaN Systems transistor was tested along with a Cree C3D06060G SiC diode, [171], in a DPT board. Sample waveforms are shown in Figure 4.33.

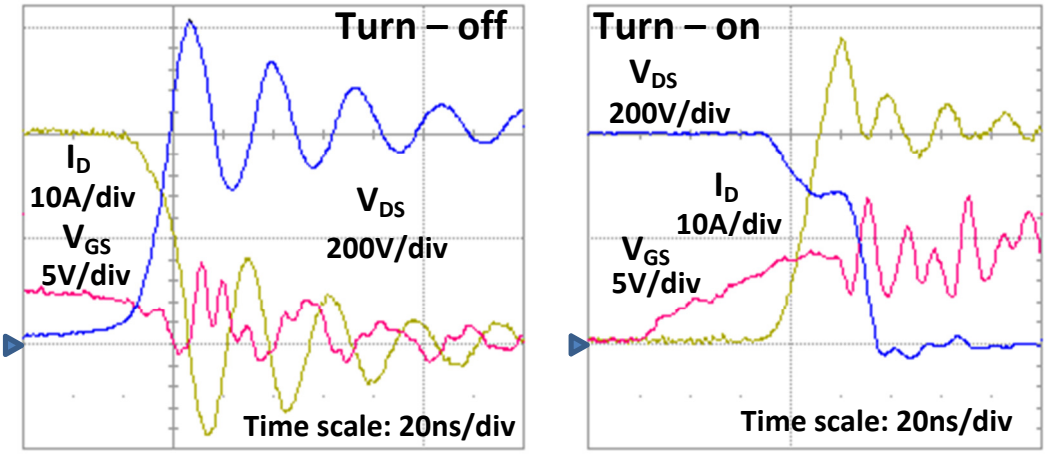


Figure 4.33: Single GaN Systems cascode device along with a SiC diode switching waveforms at V_i = 400V, I_L = 20A, V_{DD} = 6V and R_G = 5Ω

The waveforms present very fast switching transitions mainly during turn-on. The switching speed of the current is -4.4kA/µs during turn-off whilst the voltage switching speed is 106.7kV/µs. The measured turn-on switching speed is 5.5kA/µs for the current and -121.6kV/µs for the voltage transition. The current switching transitions are around three times more rapid than measured for the Transphorm device and the voltage transitions are at least 34% quicker. The high switching speed generates oscillations with the voltage overshoot reaching 610V, close to the breakdown voltage of 650V, during turn-off.

Figure 4.34 presents the energy losses of a single GaN Systems device along with a SiC diode over a range of driving and operating conditions.

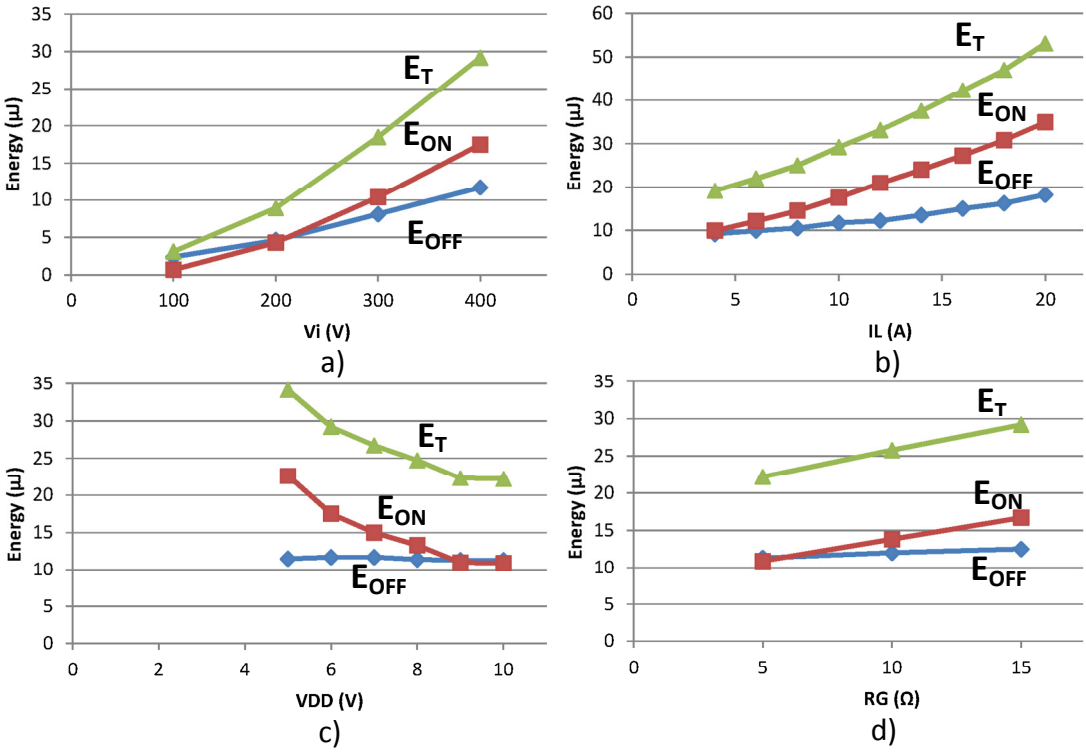


Figure 4.34: GaN Systems transistor + SiC diode switching energy losses over: a) V_i with I_L = 10A, R_G = 5Ω and V_{DD} = 6V, b) I_L with V_i = 400V, R_G = 5Ω and V_{DD} = 6V, c) V_{DD} with V_i = 400V, I_L = 10A and R_G = 5Ω, d) R_G with V_i = 400V, I_L = 10A and V_{DD} = 10V

The overall pattern of the results and the trends are very similar to those seen for the Transphorm devices.

4.5.3 Two GaN cascode devices in a leg

Two GaN cascode devices in an inverter leg configuration were implemented in a DPT board. Some sample waveforms are shown in Figure 4.35.

Slower switching transitions are observed in this case. The current and voltage switching speeds during turn-off are -1.8kA/µs and 69.6kV/µs respectively. The measured current switching speed during turn-on was 4.9kA/µs whilst it was -109.4kV/µs for the voltage. The lower switching speed results in lower amplitude oscillations during turn-off.

The energy losses over a range of conditions are presented in Figure 4.36.

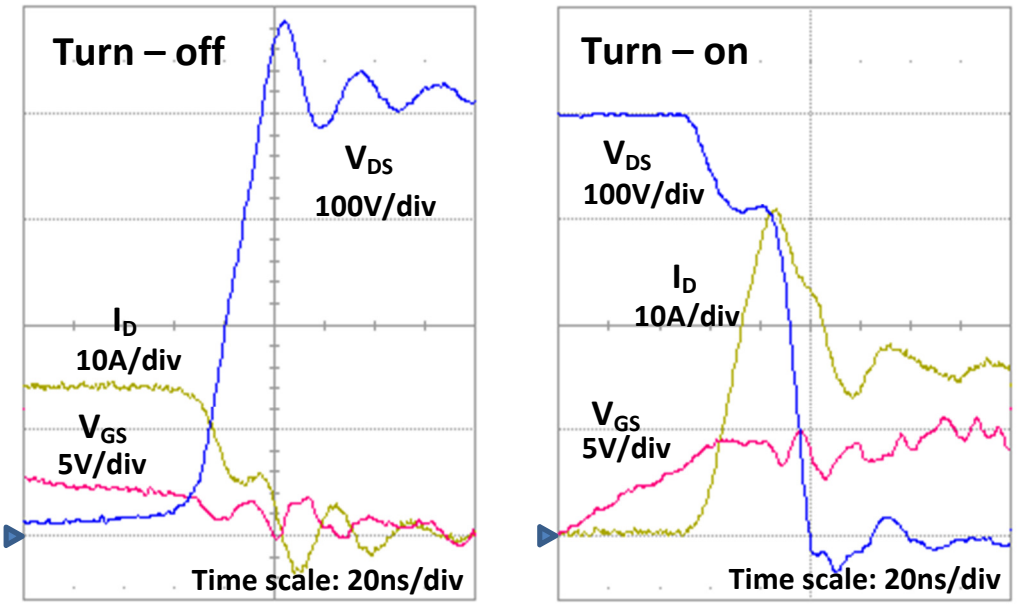


Figure 4.35: Two GaN Systems cascode device in an inverter leg configuration switching waveforms at V_i = 400V, I_L = 14A, V_{DD} = 6V and R_G = 5Ω

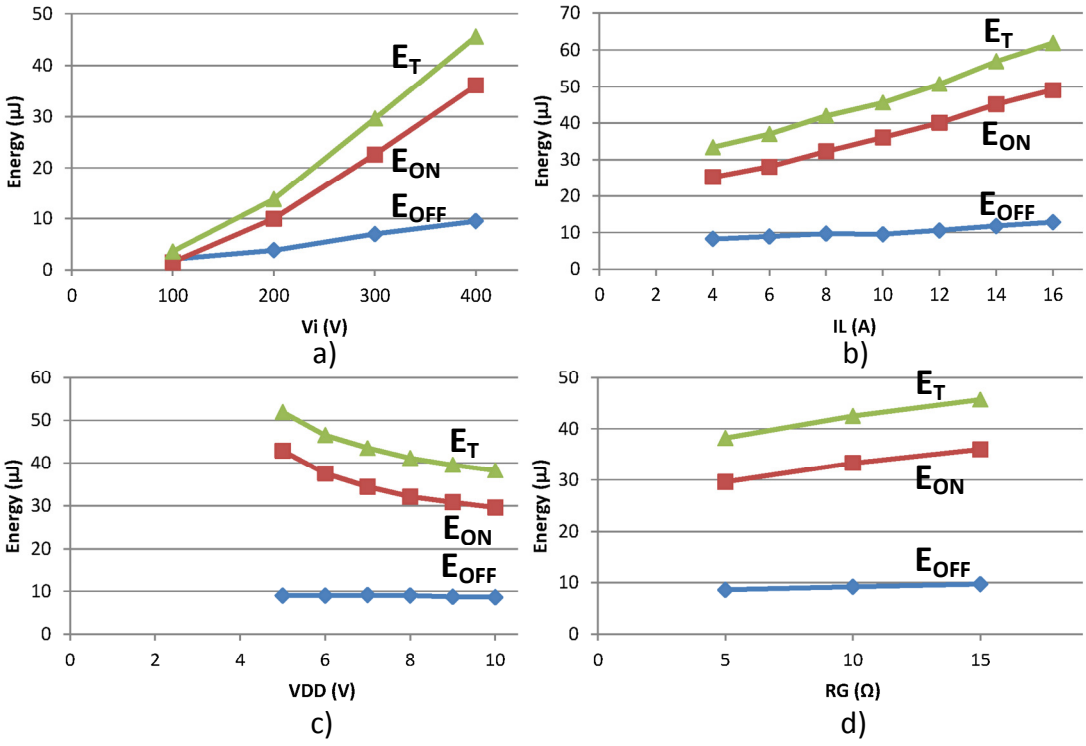


Figure 4.36: Two GaN Systems transistors in an inverter leg configuration switching energy losses over: a) V_i with I_L = 10A, R_G = 5Ω and V_{DD} = 6V, b) I_L with V_i = 400V, R_G = 5Ω and V_{DD} = 6V, c) V_{DD} with V_i = 400V, I_L = 10A and R_G = 5Ω, d) R_G with V_i = 400V, I_L = 10A and V_{DD} = 10V

The pattern of the results and the trends are similar to the ones observed with a single device along with a SiC diode. The turn-on energy loss is sensitive to the driving and

operating conditions whilst the turn-off loss is insensitive to the driving parameters and the operating current.

As in the case of the Transphorm device, the turn-on loss is around 50% higher than in the case where a single cascode device and a SiC diode are used and the turn-off losses are slightly lower because of the higher capacitance of the cascode part compared with the SiC diode.

4.6 Summary

This Chapter presents the practical testing of different GaN devices. The Chapter starts by presenting the design details and characteristics of the double pulse tester board used to measure the switching characteristics of the switching devices. The layout and instrumentation considerations are discussed in detail. The measured parasitic elements of the different boards are presented.

The waveforms of two different Si super junction MOSFETs are analysed at different driving and operating conditions. The highest measured current switching speed was 1.5kA/μs whilst it was 50kV/μs for the voltage transitions.

The switching characteristics of a Transphorm GaN cascode device are evaluated in two configurations, a single device along with a SiC diode and two GaN cascode devices in an inverter leg configuration. Very short switching transitions are recorded for both configurations in the order of a few nano-seconds. Switching speeds of 1.9kA/μs and 90.7kV/μs are reported for a single cascode device along with a SiC diode. The current and voltage turn-off switching speed is not significantly affected by changes in the driver voltage and the gate resistor. The current and voltage turn-on switching speeds are sensitive to these parameters. The analysis of switching losses indicates that two GaN cascode devices in an inverter leg configuration have 50% higher losses than the single device along with a SiC diode combination. The study found that the turn-on losses

Both configurations are compared against state-of-the-art super junction Si MOSFET based arrangements finding that the Si solutions have higher losses which is in accordance with other published work where GaN devices presented lower losses when compared against Si devices, [110, 162, 172]. Two GaN cascode devices in an

inverter leg reduce the losses by 17%. Higher energy loss reductions of at least 40% are obtained when using a GaN cascode device along with a SiC diode.

The tests results were used to confirm the accuracy of the model for calculating switching losses, the errors being around 10-15%.

Finally, results were also obtained using GaN Systems cascode devices (rated at higher current than Transphorm cascode devices), providing further confirmation of the conclusions from the Transphorm tests.

Chapter 5: Converter application of GaN devices

5.1 Introduction

Building on the device modelling and characterisation work in Chapters 3 and 4, this Chapter presents the design and evaluation of a 270V – 28V, 1.5kW isolated, phase-shifted full-bridge converter switching at 1 MHz using Transphorm GaN cascode devices. The prototype provides a demonstration of the capabilities of GaN devices and the impact that they can have on the design and performance of a converter.

First, the circuit and its operating principle are introduced, followed by the detailed design and loss audit. After the description of the construction, the results of the testing are shown, including an analysis of the switching losses. Finally, the benefits and impact of using GaN devices at system level and the related challenges are discussed at the end of the Chapter.

5.2 Phase-shifted full-bridge isolated converter

The phase-shifted full-bridge isolated converter is typically used in high power (>500W) converters where high efficiency and high frequency are required. It is commonly used in battery chargers and server power supply systems.

The converter is a good candidate to take advantage of the GaN cascode device characteristics since it is a soft-switching topology operating with zero voltage switching (ZVS) during turn-on. The energy stored in the device output capacitances is naturally recovered and since this accounts for much of the switching losses under inductive switching conditions, very low switching losses should be achievable without the need of additional snubber capacitors. As a result, a very high operating frequency should be possible, enabling the transformer and filter components to be miniaturised. The input and output voltages were chosen to be of interest to the aerospace sector.

Previous demonstrations of this topology using GaN devices were implemented using EPC devices for a 130V to 50V, 1.7kW converter switching at 50 kHz, [173, 174]; another demonstration used Qorvo RFJS1506Q GaN cascode devices rated at

650V, 15A and $R_{DS\text{-}ON}$ = 85mΩ in a 300V-14V, 600W converter switching at 100 kHz, [175]. Previous demonstrations were focused on evaluating the impact of GaN switches in converter efficiency switching at low frequency. The converter implemented in this research work shows the benefits of GaN technology to increase the switching frequency allowing converter size reductions. The proposed converter will combine high-frequency and high-power operation using GaN devices.

5.2.1 Circuit

Figure 5.1 shows the converter. The circuit is formed by four GaN cascode switches in a full-bridge configuration (T_{A1}, T_{A2}, T_{B1} and T_{B2}), a transformer providing galvanic isolation with 1: N turns ratio, a full-bridge rectifier formed by four Si diodes (D_1-D_4) and the output filter comprising inductor (L_o) and the output capacitor (C_o). C_{A1}, C_{A2}, C_{B1} and C_{B2} represent the output capacitances of the four switches and the associated board parasitic capacitance. L_k is the leakage inductance of the primary of the transformer plus the reflected stray inductance of the secondary side and the stray inductance of the primary side; L_k is represented as a separate element because of its role in achieving soft-switching operation. R_L represents the load resistor.

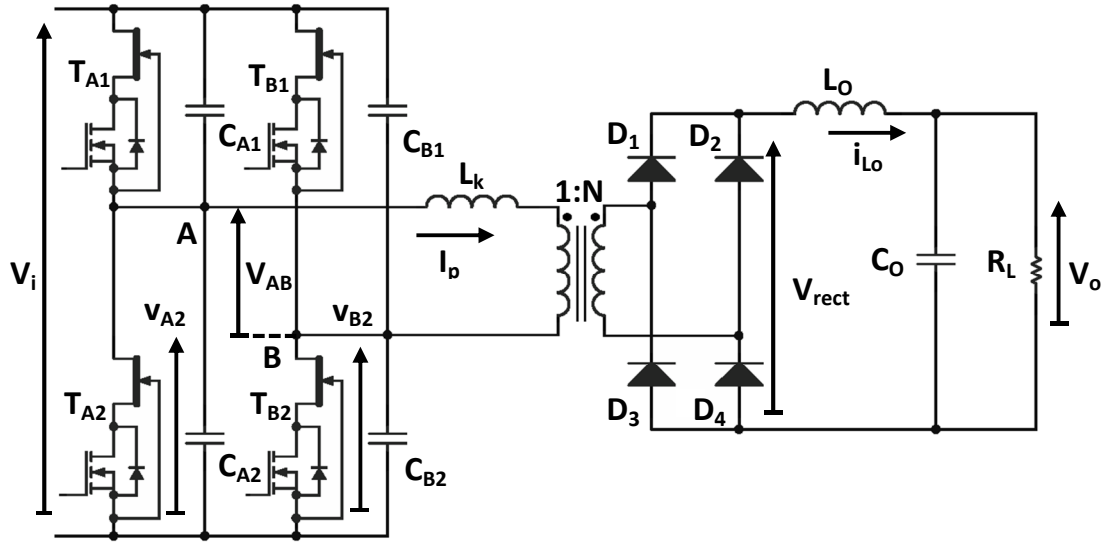


Figure 5.1: Phase-shifted isolated full-bridge converter circuit schematic

The full-bridge stage generates a high-frequency AC waveform from the input DC voltage V_i which is transmitted to the rectifier through the transformer, the rectified voltage is then smoothed by the output filter and passed to the load.

5.2.2 Converter operation

The modulation strategy of the transistors is explained using the sketched waveforms in Figure 5.2. The leg A transistors (T_{A1} and T_{A2}) are operated in antiphase with a duty cycle of 50%. The leg B transistors (T_{B1} and T_{B2}) operate in a similar manner, however, leg B is delayed behind leg A by $\delta T/2$ where T is the switching period and δ is the control variable, $0 \leq \delta \leq 1$; v_{A2} and v_{B2} are the drain to source voltages of T_{A2} and T_{B2} respectively that result from the modulation strategy. V_{AB} is the transformer primary voltage and is equal to the difference between v_{A2} and v_{B2}. V_{AB} is a quasi-square waveform with positive and negative pulse widths equal to $\delta T/2$. The pulse width is controlled through δ, when $\delta = 0$ the primary of the transformer is always zero volts and when $\delta = 1$ the primary voltage is a square waveform. The energy transfer from the primary to the secondary of the transformer is controlled through δ. The state of the transistors define the V_{AB} waveform at all times, however a dead time needs to be included between the turn-off and turn-on transitions in each leg to avoid short-circuiting the input voltage V_i and potentially damaging the GaN switches.

The idealised main waveforms of the circuit are presented in Figure 5.3 and the different stages are explained next.

Power delivery mode, $t = t_1 \rightarrow t_2$ and $t = t_4 \rightarrow t_5$

During these stages V_{AB} is equal to V_i or $-V_i$ and the rectifier output voltage, V_{rect}, is equal to NV_i. The voltage across L_o is then $NV_i - V_o$, which is assumed constant by neglecting the input and output voltage ripples, and the inductor current increases. The average value of this current represents the current delivered to the load (I_o) and the AC part flows through the output filter capacitor. The current flows through the rectifier and the transformer secondary and is reflected to the primary as Ni_{Lo}. When V_{AB} is positive, D_1 and D_4 conduct, and the current of the transformer primary (I_p) is positive. In contrast, when V_{AB} is negative, D_2 and D_3 conduct and I_p is negative. Power is delivered from the transformer primary side circuit to the transformer secondary side circuit.

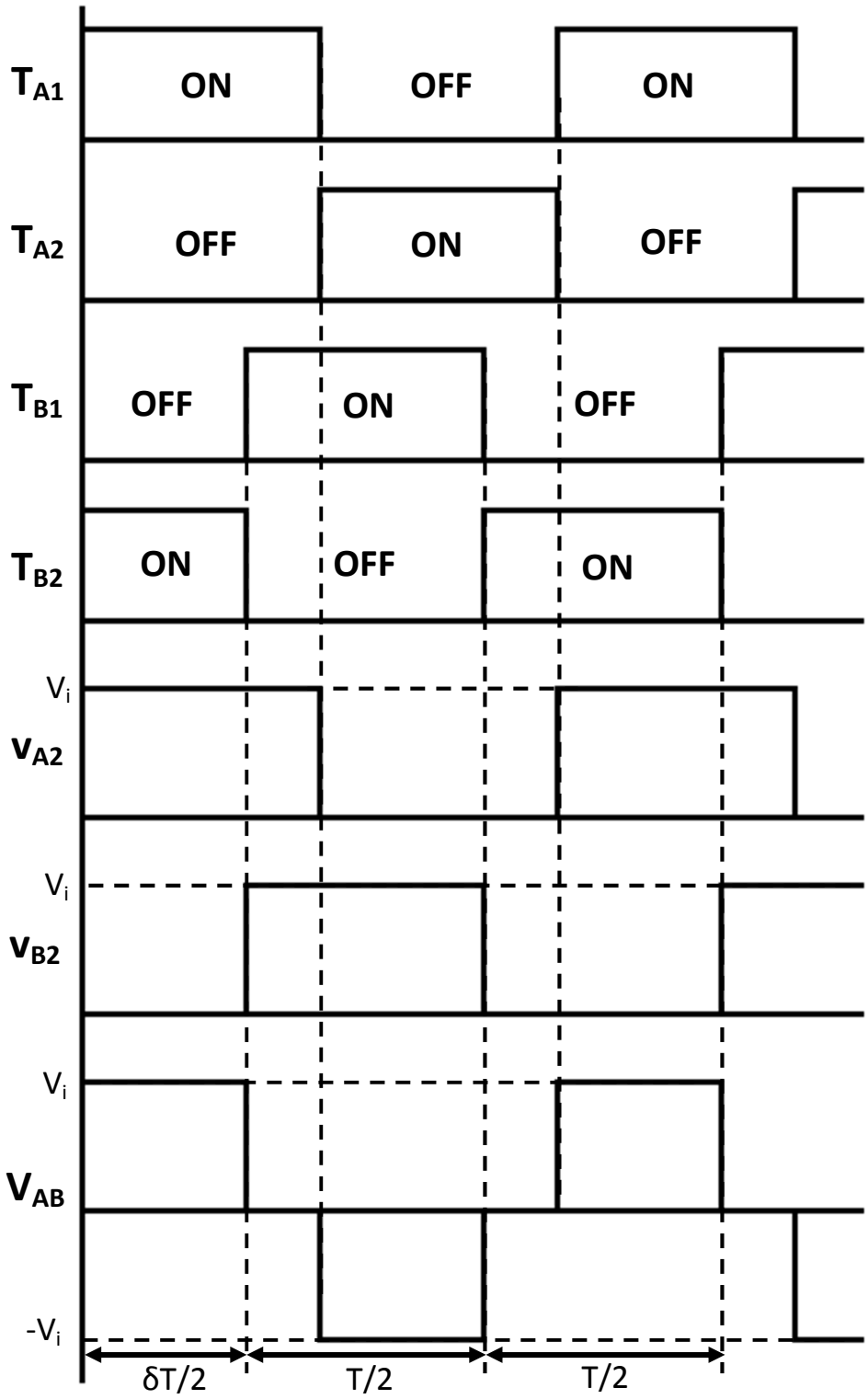


Figure 5.2: Modulation strategy

Freewheeling mode, $t = t_2 \rightarrow t_3$ and $t = t_5 \rightarrow t_6$

The voltage across the primary of the transformer is zero during these stages; V_A and V_B are both V_i if T_{A1} and T_{B1} are turned-on or they are both zero if T_{A2} and T_{B2} are turned-on. V_{rect} is zero as well and $-V_o$ is impressed across L_o and its current falls

linearly. This current flows through the two diodes that were previously conducting and the transformer secondary and is reflected to the primary side. L_k prevents any abrupt change in the primary current. The load power is maintained by the output filter during these stages.

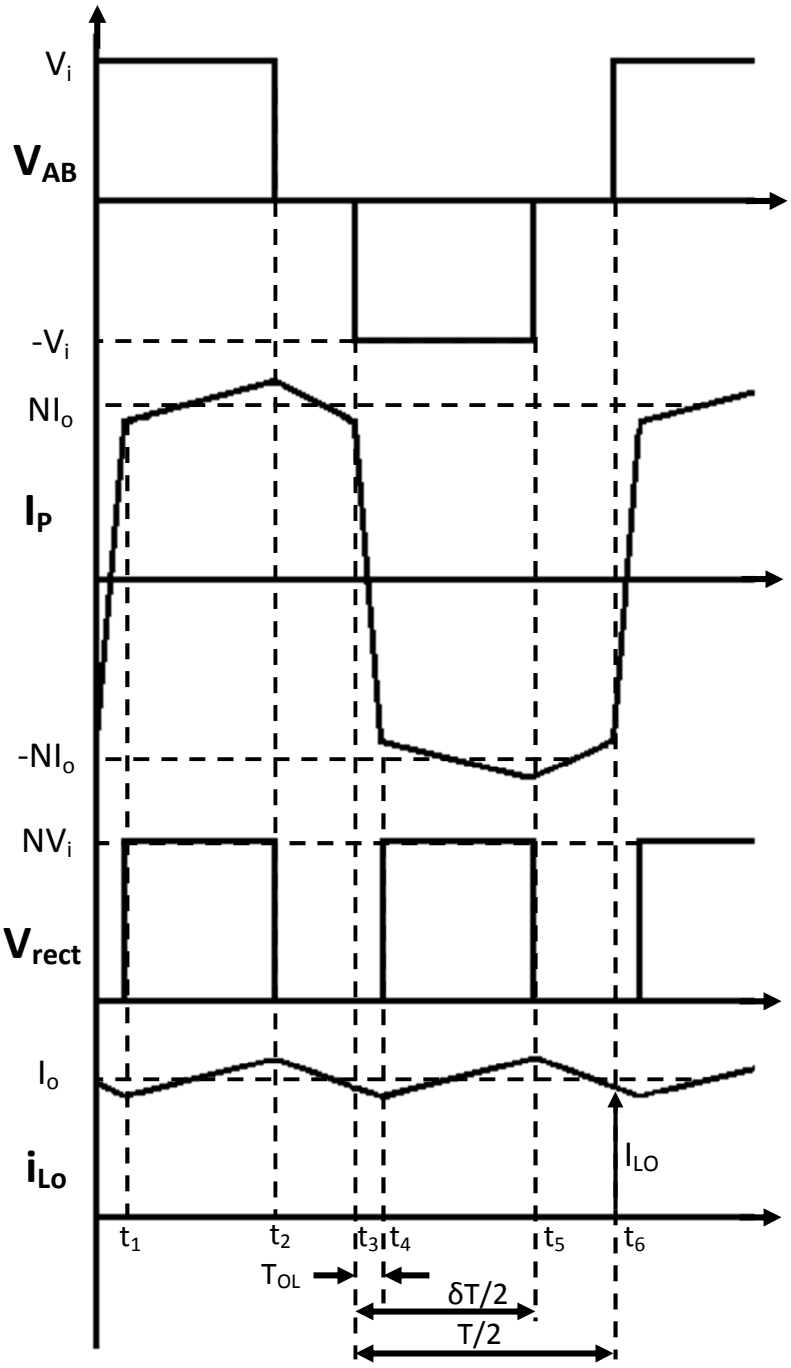


Figure 5.3: Idealised circuit waveforms

Overlap period, t = 0 → t_1 and t = t_3 → t_4

The beginning of these periods is just after the freewheeling stage ends and V_{AB} switches to either V_i or $-V_i$.

Considering the period from t_3 to t_4, initially V_{AB} and V_{rect} are both zero, the primary current is N times the output inductor current, D_1 and D_4 are conducting and D_2 and D_3 are turned-off. Then, V_{AB} changes to $-V_i$ and the change forward biases D_2 and D_3; D_1 and D_4 keep conducting because L_k and L_o prevent any abrupt change in the current. Therefore, the four rectifiers are conducting simultaneously and $-V_i$ is impressed across L_k. The negative voltage reduces I_p linearly. As I_p decreases, the current in D_1 and D_4 decreases and is matched by an increase in the current of D_2 and D_3. An equal current will flow in all the rectifiers when I_p reaches zero. Then, I_p increases in the negative direction and the current in D_2 and D_3 continues increasing whilst the current in D_1 and D_4 continues to fall until their current is zero, which occurs at the moment when the current in D_2 and D_3 are equal to the output inductor current. Once D_1 and D_4 are able to block voltage, the rectifier voltage changes from zero to NV_i and a power delivery stage begins. The rectifier overlap occurring from t = 0 to t_1 can be explained in a similar way.

The converter parameters main equations are introduced in [176-178] and are presented next. During overlap, the leakage inductance controls the rate at which I_p reverses. The duration of the overlap period is denoted T_{OL} and is given by:

$$T_{OL} = \frac{2NI_{LO}L_k}{V_i} \tag{5.1}$$

where I_{LO} is the inductor current at the overlap instant.

Referring to the circuit in Figure 5.1 and the waveforms in Figure 5.3, the output voltage can be determined by calculating the average value of the rectifier voltage (V_{rect}) waveform. The following equation can be established by examining the V_{rect} waveform in Figure 5.3:

$$V_o = \frac{2}{T}\left[\frac{\delta T}{2} - T_{OL}\right] NV_i \tag{5.2}$$

Combining (5.1) and (5.2):

$$V_o = \delta N V_i - \frac{4N^2 I_{LO} L_k}{T} \tag{5.3}$$

If the output inductor ripple current is small when compared against the converter output current (I_o), then I_{LO} will be close to the load current and the output voltage can be approximated as:

$$V_o = \delta N V_i - \frac{4N^2 I_o L_k}{T} \tag{5.4}$$

The overlap has the effect of making the output voltage load dependent. L_k needs to be as small as possible to achieve higher output voltage.

Soft-switching operation

Soft-switching operation is achieved by ZVS during turn-on, that is the current switches under zero or low voltage conditions practically eliminating the switching losses.

The ZVS mechanism is different in the two legs of the full-bridge. The soft-switching equations presented in the following sections are commonly used for defining the required dead time for each leg to achieve soft-switching, [176-178].

Leading leg soft-switching mechanism

From Figure 5.2 we can observe that turning-on any of the leading leg transistors (T_{A1} and T_{A2}) has the effect of changing V_{AB} from zero to V_i or $-V_i$ starting the overlap period. There is a dead time (T_D) between the instant when one of the transistors is turned-off and the other is turned-on. When one of the transistors is turned-off, the overlap period starts and all the rectifiers are conducting. Therefore, the output inductor plays no part in the process. Next, the leakage inductance energy charges the capacitance of the transistor being turned-off and discharges the capacitance of the transistor to be turned-on. If the leakage inductance energy and the dead time are large enough, the output capacitance of the transistor to be turned-on will be completely discharged (dropping its voltage to zero) before it is actually turned-on achieving ZVS. The charge/discharge process occurs while L_k and the output capacitance of the transistors are resonating.

The resonant process after T_{A1} is turned-off is explained using the equivalent circuit of Figure 5.4. Before T_{A1} is turned-off, T_{A1} was conducting (ideally $v_{A1} = 0$) and T_{A2} is blocking the input voltage ($v_{A2} = V_i$), the primary current is equal to the output filter current at the beginning of the overlap period reflected to the primary (NI_{LO}). From Figure 5.4 we observe that any change in the voltage of C_{A1} is reflected as an equal and opposite change in the voltages of C_{A2} and the inductor L_k. Then:

$$\frac{dv_{A1}}{dt} = -\frac{dv_{A2}}{dt} \tag{5.5}$$

$$\frac{dv_{A1}}{dt} = -\frac{dv_{Lk}}{dt} \tag{5.6}$$

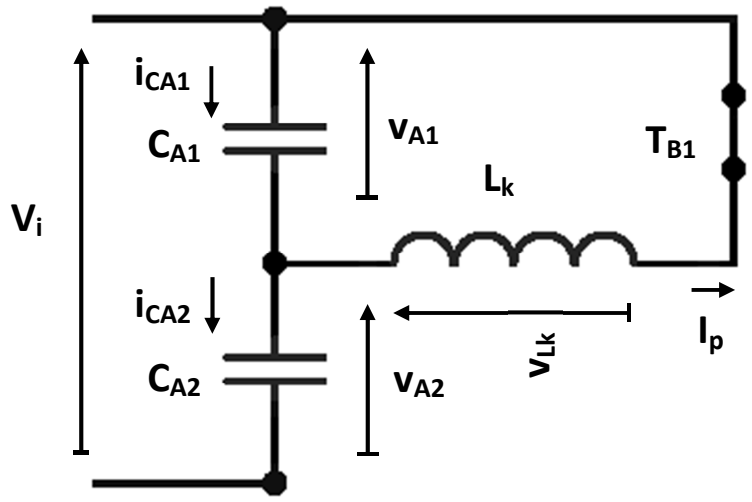


Figure 5.4: Equivalent circuit of the leading leg after T_{A1} is turned-off

By applying Kirchhoff's current law at the common node of the capacitances and the inductor we get:

$$i_{CA1} = i_{CA2} + I_p \tag{5.7}$$

Assuming that C_A is the output capacitance of each of the leg A transistors, that is $C_{A1} = C_{A2} = C_A$:

$$i_{CA1} = C_A \frac{dv_{A1}}{dt} \tag{5.8}$$

$$i_{CA2} = C_A \frac{dv_{A2}}{dt} \tag{5.9}$$

and:

$$v_{Lk} = L_k \frac{dI_p}{dt} \tag{5.10}$$

Substituting (5.8) and (5.9) in (5.7):

$$\frac{dv_{A1}}{dt} = \frac{dv_{A2}}{dt} + \frac{I_p}{C_A} \tag{5.11}$$

Substituting (5.6) in (5.11) to eliminate dv_{A2}/dt and after that (5.5) to eliminate dv_{A1}/dt:

$$2\frac{dv_{Lk}}{dt} + \frac{I_p}{C_A} = 0 \tag{5.12}$$

Finally, substituting (5.10) in (5.12):

$$\frac{d^2 I_P}{dt^2} + \frac{I_p}{2C_A L_k} = 0 \tag{5.13}$$

Equation (5.13) represents an undamped resonant system where the initial conditions are:

$$I_p(0) = NI_{LO} \tag{5.14}$$

$$v_{Lk}(0) = 0 \tag{5.15}$$

$$\frac{dI_p}{dt}(0) = 0 \tag{5.16}$$

The solution of the differential equation in (5.13) using the initial conditions of (5.14), (5.15) and (5.16) is:

$$I_p = NI_{LO}\cos(\omega t) \tag{5.17}$$

where:

$$\omega = \frac{1}{\sqrt{2C_A L_k}} \tag{5.18}$$

The inductor voltage is obtained by combining (5.10) and (5.17):

$$v_{Lk} = -ZNI_{LO}\sin(\omega t) \tag{5.19}$$

where:

$$Z = \sqrt{\frac{L_k}{2C_A}} \tag{5.20}$$

From the circuit in Figure 5.4:

$$v_{A1} = -v_{Lk} \tag{5.21}$$

Therefore, combining (5.19) and (5.21):

$$v_{A1} = ZNI_{LO} \sin(\omega t) \tag{5.22}$$

Applying Kirchhoff's voltage law at the input of the circuit of Figure 5.4:

$$v_{A2} = V_i - v_{A1} \tag{5.23}$$

Equations (5.17), (5.19), (5.22) and (5.23) describe the main circuit waveforms until $v_{A1} = V_i$ and $v_{A2} = 0$. At this point the inductor current is transferred to the T_{A2} body diode and the current stops flowing through the capacitors C_{A1} and C_{A2}. After the resonant transitions ends, the current continues decreasing linearly as described for the overlap period.

The duration of the resonant transition (T_{res}) can be calculated by setting $v_{A1} = V_i$ in equation (5.22):

$$T_{res} = \frac{1}{\omega} \sin^{-1}\left(\frac{V_i}{ZNI_{LO}}\right) \tag{5.24}$$

Sketched waveforms of the resonant transition are show in Figure 5.5.

Previous equations show that for achieving zero voltage switching the amplitude of the sinusoidal trajectory in equation (5.22) must reach at least V_i, that is:

$$ZNI_{LO} \geq V_i \tag{5.25}$$

As I_{LO} is close to the load current, if the ripple current of the output inductor is small when compared against the output current, then the following minimum load current condition can be established:

$$I_o \geq \frac{V_i}{ZN} \tag{5.26}$$

When the load current is below the limit in equation (5.26), the energy stored in L_k will not be sufficient to charge/discharge the output capacitance of the switches and ZVS is partially or totally lost.

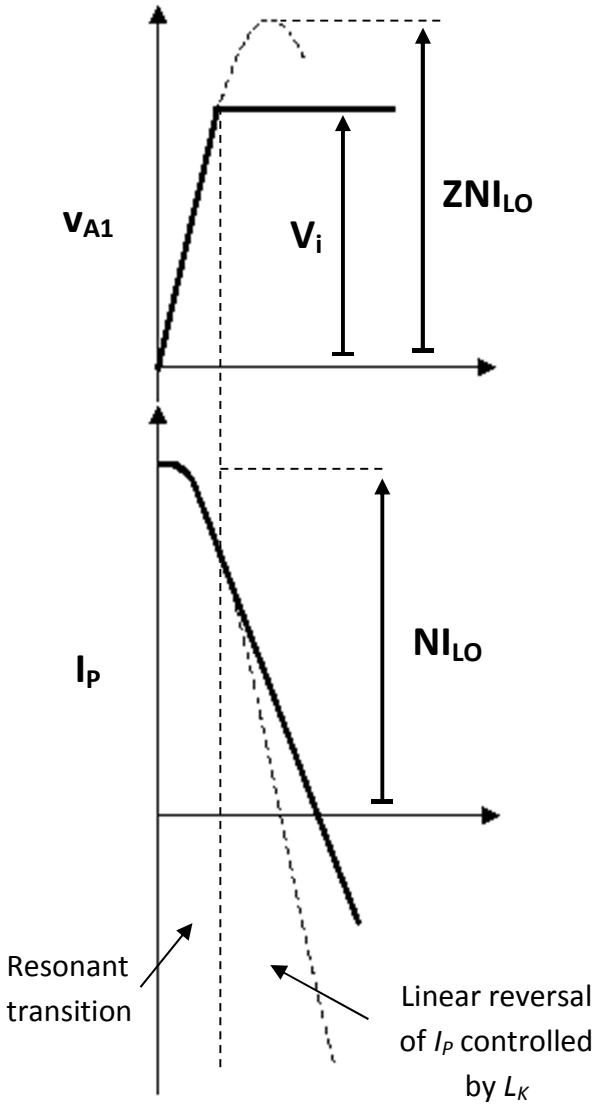


Figure 5.5: Resonant transition of v_{A1} and I_p waveforms after T_{A1} is turned-off

In addition, to allow V_{A1} to reach V_i and achieve soft switching, the dead time (T_D) needs to be set to at least the resonant transition duration:

$$T_D \geq \frac{1}{\omega}\sin^{-1}\left[\frac{V_i}{ZNI_{LO}}\right] \tag{5.27}$$

To allow I_p to reverse the following condition must be met:

$$T_D \leq \frac{T_{OL}}{2} \tag{5.28}$$

Lagging leg soft-switching mechanism

The mechanism of soft-switching is different in the lagging leg (T_{B1} and T_{B2}). When one of these switches is turned-off (before turning-on the other), the converter changes from the power delivery mode to the freewheeling mode as can be seen in the waveforms of Figure 5.2. Two of the rectifier diodes are conducting and the other two are off before and after the transition. Therefore, the output capacitance of the switches is charged/discharged by the series connection of L_k and L_o. If the dead time is high enough, the capacitance of the switch to be turned-on will be discharged before it is actually turned-on achieving ZVS conditions. Since L_o (reflected to the primary) is comparatively large, the device output capacitances are charged/discharged by a constant current and there is no resonant interaction. Figure 5.6 shows the equivalent circuit after T_{B2} is turned-off.

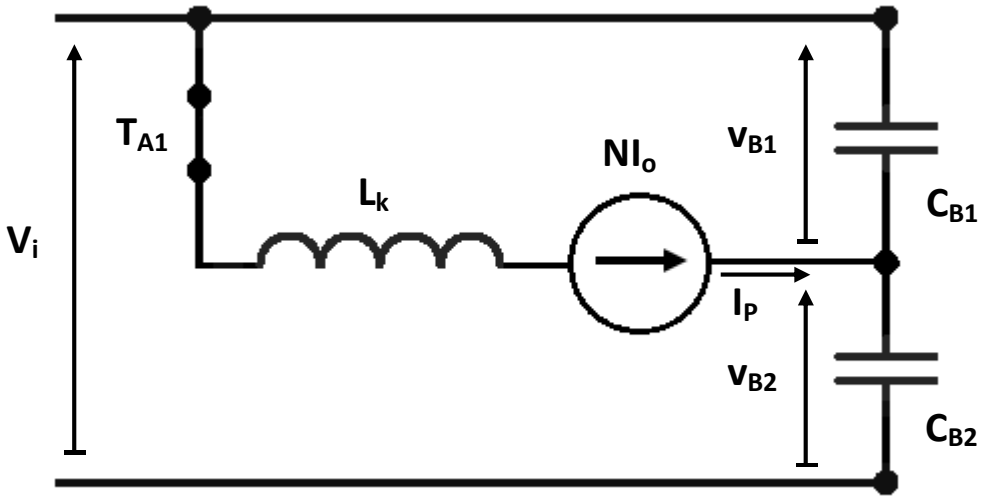


Figure 5.6: Equivalent circuit of the lagging leg after T_{B2} is turned-off

The dead time needs to be at least as long as the duration of the charge/discharge process to ensure soft switching. Therefore:

$$T_D \geq \frac{2C_B V_i}{NI_o} \tag{5.29}$$

where C_B is the output capacitance of each device in the lagging leg, that is $C_{B1} = C_{B2} = C_B$.

5.2.3 Clamp circuit

When the circuit commutates from the freewheeling mode to the power delivery mode, the leakage inductance L_k resonates with the output capacitance of the rectifier diodes as the diode voltage and V_{rect} rise to the level of NV_i. V_{rect} rises in a resonant manner to approximately $2NV_i$, then undergoes a lightly damped oscillation around the final value of NV_i, [177], as shown in the sketched waveform in Figure 5.7. The oscillations are a potential problem from an EMI perspective and the peak voltage could damage the diodes if they are not adequately rated.

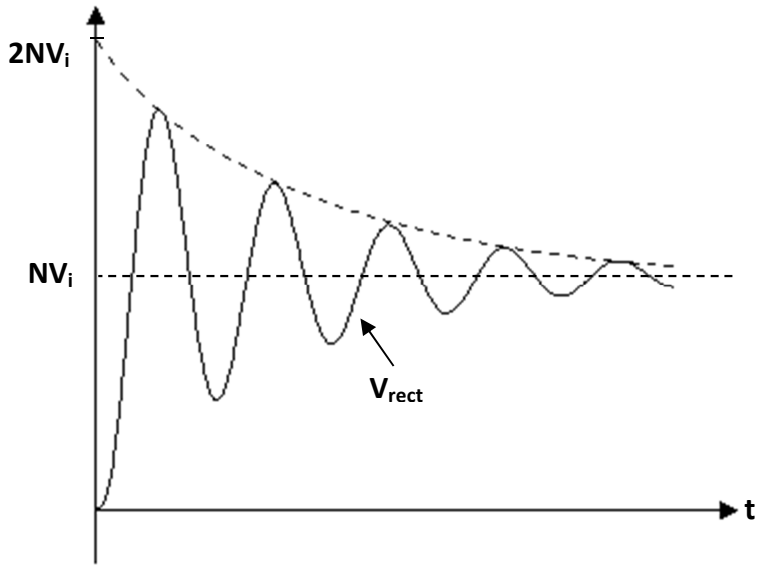


Figure 5.7: V_{rect} waveform during the resonance of L_k and the capacitance of the rectifier diodes

A clamp circuit is shown in Figure 5.8 and was used to restrict the secondary winding voltage oscillations, [177].

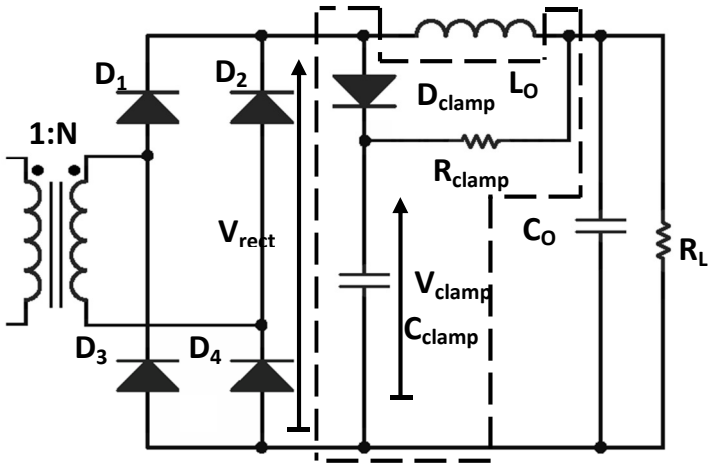


Figure 5.8: Clamp circuit

The circuit consists of a diode (D_{clamp}), a resistor (R_{clamp}), and a capacitor (C_{clamp}). C_{clamp} is sized to maintain a relatively constant voltage V_{clamp}. When the oscillation across the rectifier circuit exceeds V_{clamp}, D_{clamp} is forward biased clamping the rectifier voltage to $V_{clamp} + V_F$. In contrast, when the rectifier voltage is lower than V_{clamp}, D_{clamp} is reverse biased and the clamp circuit doesn't absorb any energy. C_{clamp} is discharged at an approximately constant rate through R_{clamp}. A percentage of the energy taken by the clamp circuit is dissipated in R_{clamp} and D_{clamp} but another part is delivered to the load. The losses in D_{clamp} are small and can be safely dissipated. Figure 5.9 presents a sketched idealised V_{rect} waveform with the clamp circuit added and neglecting the voltage drop of D_{clamp}.

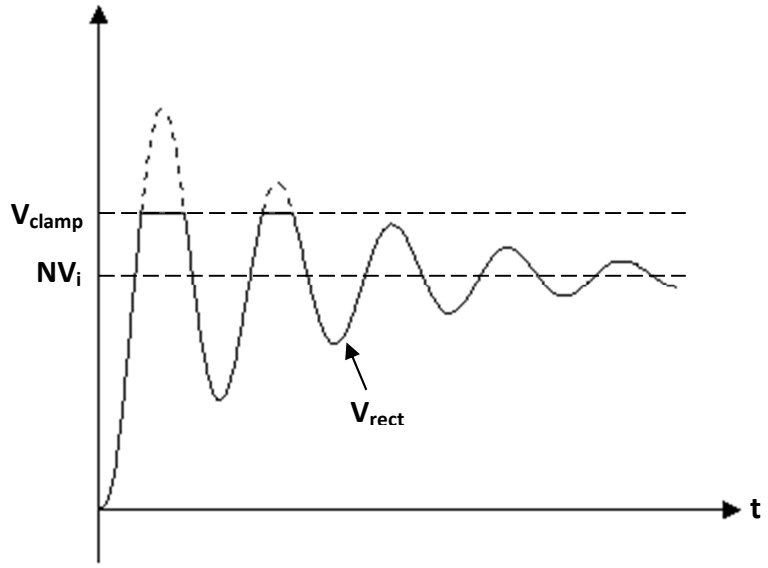


Figure 5.9: V_{rect} waveform with clamp circuit added

5.3 Converter design

This section presents the design of the converter according to the initial specification in Table 5.1.

Table 5.1: Converter initial specification

Parameter	Value
Rated power	1.5kW
Input voltage	270V
Output voltage	28V
Switching frequency	1MHz
Efficiency	>90%
Soft-switching range	1.2kW - 1.5kW
Nominal δ	0.85
Output inductor ripple current	$< 0.2I_{omax}$
Output voltage ripple	$< 0.01V_o$
Ambient temperature	Room temperature

5.3.1 Overall circuit architecture

To provide flexibility during the testing work, a modular approach was used for the construction of the converter, consisting of the following blocks.

1. **Bulk capacitors board.** This board provides the bulk decoupling capacitance at the input.
2. **Full-bridge board.** This consists of the four GaN cascode switches and local decoupling ceramic capacitors.
3. **Leg driver boards.** Each board provides the signals for the GaN cascode switches in one leg and includes the dead time generation.
4. **Transformer.** To provide the galvanic isolation between the input and the output and scaling the voltage and current levels.
5. **Rectifier.** Formed by the four diodes of the full-bridge rectifier.
6. **Output filter.** This board accommodates the output filter inductor and capacitor and also the clamp circuit.

The details of each block are presented in the following sections.

5.3.2 Bulk capacitors board

Two Vishay MKP1848CG5050JP5, 50μF film capacitors rated at 500V were used as bulk decoupling capacitors at the input.

5.3.3 Full-bridge board

This circuit includes the full-bridge GaN cascode devices and high frequency decoupling capacitors. Transphorm TPH3006LD transistors were used for the top side switches and TPH3006LS transistors for the lower switches. Both are SMD PQFN88 packaged, rated at 600V, 12A at a case temperature of 100°C and with a nominal $R_{DS\text{-}ON}$ of 0.15Ω at 25°C. The TPH3006LD has the dissipation pad wired to the drain while the TPH3006LS has the dissipation pad wired to the source. The maximum expected current is around 8A, therefore, the drain current limit is not exceeded.

Six ceramic capacitors in SMD 2220 packages and rated at 100nF and 1kV were used for decoupling the DC input. The layout was carefully designed to reduce the loop size. The layout drawings are shown in Appendix B.

Since SMD packages are used, the main thermal path is through the board, therefore T-Clad HR T30.20 from Bergquist, [179], was used as the substrate board to provide a low thermal resistance. The characteristics of the board are summarised in Table 5.2.

Table 5.2: HR T30.20 PCB characteristics, [179]

Characteristic	Value
Dielectric	HR T30.20
Dielectric thickness	76μm
Thermal conductivity	1.5 W/m-K
Copper thickness	2oz
Aluminium thickness	1mm
Dielectric strength	85kV/mm

The soft switching equations in section 5.2.2 require accurate data of the GaN transistors' output capacitance (cascode gate-drain capacitance plus cascode drain-source capacitance), C_{oss}.

The time related output capacitance ($C_{oss(TR)}$) is calculated using the total charge delivered to the capacitor as the voltage rises from zero to a specific level.

The soft-switching equations of both legs require $C_{oss(TR)}$ since they are related to a charging/discharging process where the transistors' output capacitance charge is going to be added/removed by the leakage inductance, in the case of the leading leg, and the leakage inductance and output inductor in the case of the lagging leg.

The $C_{oss(TR)}$ is therefore calculated using the C-V plot in the datasheet and equation (3.62) in section 3.6.1.

Figure 5.10 shows the plot for the TPH30006LD C_{iss} (cascode gate-source capacitance plus cascode gate-drain capacitance), C_{oss} and C_{rss} (cascode gate-drain capacitance) capacitances extracted from the datasheet, [180]. C_{oss} was modelled by making piecewise approximations of the logarithmic plot of Figure 5.10. The resultant equations are:

$$C_{oss} = 800\left(10^{-0.0062V_{DS}}\right)pF \qquad 0 \le V_{DS} < 19V \tag{5.30}$$

$$C_{oss} = 1051867\left(10^{-0.17V_{DS}}\right)pF \qquad 19V \le V_{DS} < 21.6V \tag{5.31}$$

$$C_{oss} = 255.6\left(10^{-0.003V_{DS}}\right)pF \qquad 21.6V \le V_{DS} < 235V \tag{5.32}$$

$$C_{oss} = 48\,pF \qquad 235V \le V_{DS} \le 270V \tag{5.33}$$

The calculated time related capacitance at V_i = 270V is shown in the table below.

Table 5.3: Time related output capacitance of TPH3006LD at 270V

Parameter	Value (pF)
$C_{oss(TR)}$	146

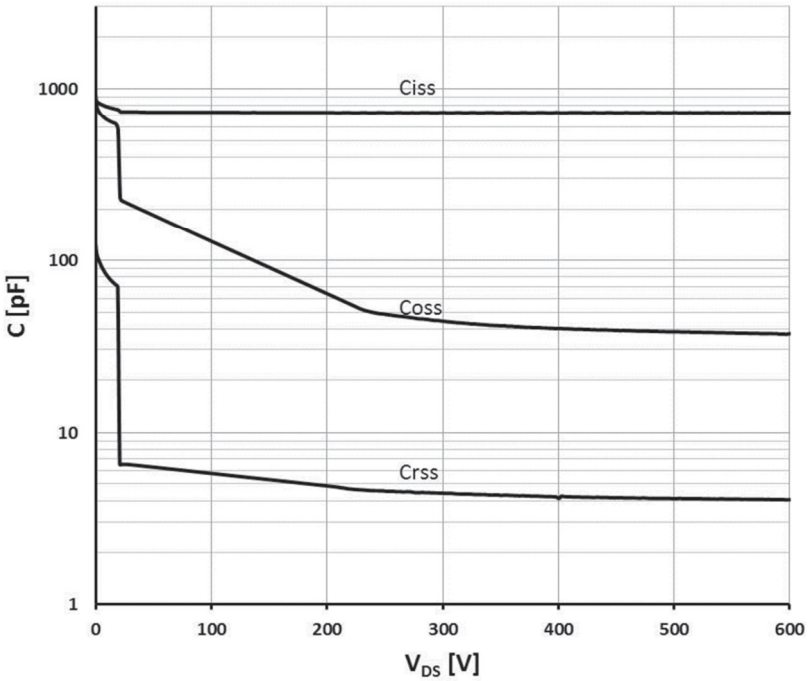


Figure 5.10: TPH3006LD typical output capacitance at V_{GS} = 0V, F = 1MHz, [180]

5.3.4 Leg driver boards

Separate driver boards were built on standard two-layer PCBs for each leg of the full bridge. It was decided not to build the drivers directly on the full-bridge board due to the risk of capacitive coupling through the metal substrate, which could corrupt the drive signals.

The driver was designed to apply a negative voltage of -4.5V to each gate when the switch is turned-off to reduce the risk of false turn-on induced by the high switching speed. The main components of the leg driver circuit are shown in Figure 5.11.

A signal generator having two phase-shifted outputs provides the control signals for the leg driver boards, marked GEN in Figure 5.11. The control signal of each driver board had a 5V amplitude, 50% duty-ratio and 1MHz frequency. The variable phase-shift between the two outputs from the signal generator was used for open loop control of the converter.

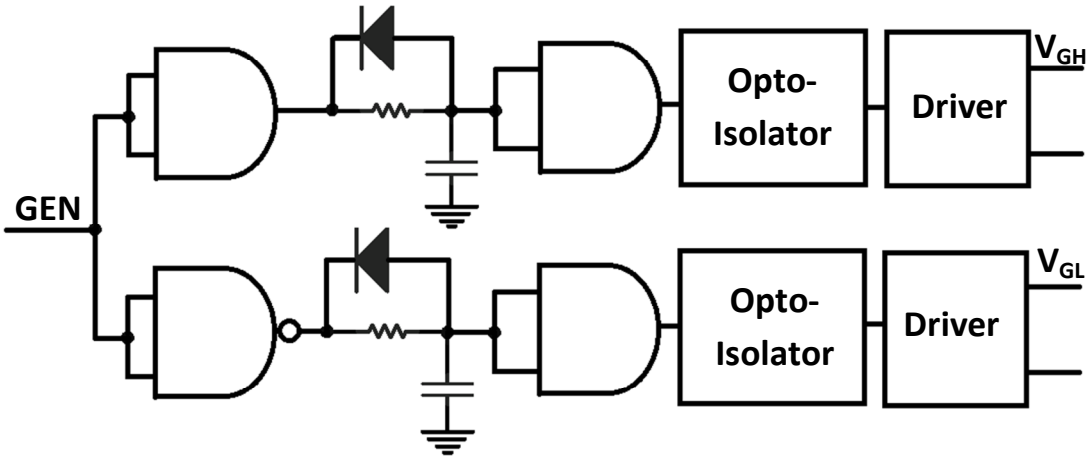


Figure 5.11: Leg driver circuit diagram

In each driver board the GEN signal is used to generate two complementary signals and dead time is then added by delaying the rising edge of each waveform with a simple R-C circuit.

The dead time of the leading leg was set at 18ns whilst the dead time of the lagging leg was set at 20ns according to the design equations of section 5.2.2, the converter initial specification of Table 5.1 and assuming that the cascode device output capacitance is 146pF (as calculated in section 5.3.3), the transformer turns ratio is 1/7 and the leakage inductance is 633nH (as will be defined in section 5.3.5).

Signal isolation for each driver channel was provided using opto-isolators. The devices selected were the Avago Technologies ACPL-P484-000E due to their high speed, low capacitive coupling and high common mode dV/dt capability of at least 30kV/μs.

A high current-buffer was used to drive each gate and isolated power supplies were generated for each gate circuit using R12P212S and R12P205S parts, which have a very small capacitive coupling of between 1.5pF and 10pF. The driver voltages were set to +6V for turn-on and -4.5V for turn-off; the gate resistors were set to 10Ω. The values V_{DD} = 6V and R_G = 10 Ω proved to generate well-damped and stable switching waveforms with low energy values as described in section 4.4.3. Furthermore, the transistor switching losses are not sensitive to gate voltage since they are only composed of the transistor turn-off losses as the turn-on losses are eliminated by the soft-switching operation.

The full schematic of the leg driver circuit is shown in Appendix B. The layout was designed to minimise the parasitic inductance particularly in the gate drive loop and the different voltage levels of the board are carefully isolated. Copper planes for each reference signal can be easily identified in the layout. No signals are tracked below the opto-isolators or the isolated power supplies to avoid unwanted capacitive coupling. The layout drawings can be found in Appendix B.

5.3.5 Transformer

To calculate the transformer turns-ratio, a nominal value of δ of 0.85 was assumed. This value is towards the maximum, which is desirable to reduce the primary current level, but leaves some control flexibility to compensate for circuit losses. Neglecting the lost voltage due to overlap the turns ratio N may be estimated using:

$$NV_i\delta = V_o + 2V_F \tag{5.34}$$

where V_F is the forward voltage of the secondary rectifiers. Assuming V_F = 0.7V, then 1/N = 7.8, and the turns ratio was therefore chosen to be 1/7.

A planar transformer topology was chosen since this offers a compact, easy-to-manufacture structure and there is a good range of ferrite cores available, although the 1MHz frequency is at the top end of the range that is normally used for planar designs. To minimise the number of turns a single-turn secondary was used, requiring seven primary turns. The number of turns was calculated using Faraday's law and assuming that the primary voltage is a square wave of $\pm V_i$:

$$N_P = \frac{V_i 10^4}{4Bf_s A_c} \tag{5.35}$$

where B is the peak flux density, A_c is the effective core area in square centimetres and f_s is the switching frequency. The peak flux density was set at around 50mT to restrict the core losses to the region of 500mW/cm^3 which is the maximum level recommended by manufacturers for air-cooled designs. The actual core losses may be calculated using the Steinmetz equation, [181]:

$$P_{cv} = k \bullet f_s^{\alpha} \bullet B^{\beta} \tag{5.36}$$

Searching through the available core sizes and materials a Ferroxcube planar core E38/8/25 of 3F4 material was chosen for the converter transformer. The volume of

two cores is 10.2cm^3 and the effective area is A_c = 1.94cm^2 and Figure 5.12 provides the dimensions,[182].

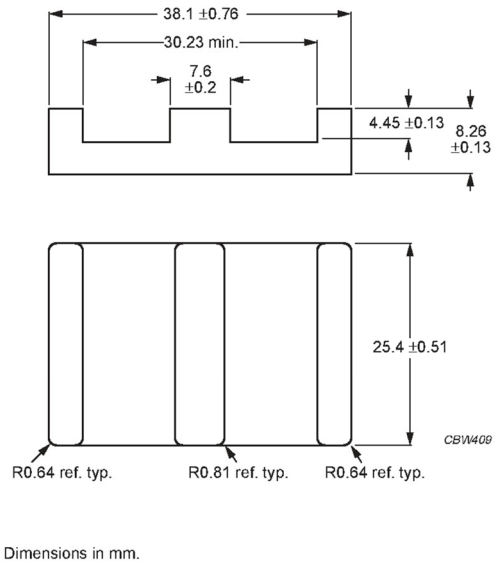


Figure 5.12: E38/8/25 core dimensions, [182]

The peak flux density is calculated to be 49.7mT resulting in a core loss of 6.2W.

The individual turns in the transformer winding were cut from a copper sheet and then assembled and interconnected to form the complete winding assembly. To limit the eddy currents in the windings, which cause skin and proximity effect losses, the copper thickness was chosen to be two skin depths, where the skin depth, ε, in copper is calculated by the following equation, [183]:

$$\varepsilon = \frac{6.62}{\sqrt{f_s}} \tag{5.37}$$

where ε is given in centimetres. For copper at 1 MHz the skin depth is 0.066mm and 0.125mm copper foil was selected for the transformer windings.

Considering insulation clearances, the dimensions of each turn are as shown Figure 5.13. To limit the current density in the windings to 6A/mm^2 seven turns will be connected in parallel for the secondary and seven turns in series for the primary. Each turn will be insulated using kapton tape.

To minimise the proximity effect losses in the windings and the leakage inductance, a number of interleaved winding arrangements were tested experimentally.

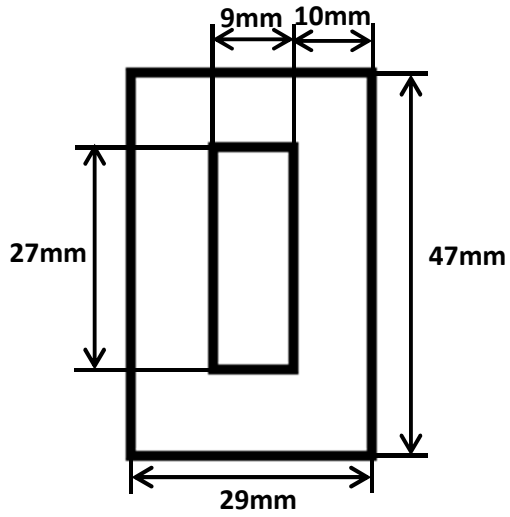


Figure 5.13: Transformer turns drawing

The leakage inductance and the windings' AC resistance were measured by short-circuiting the secondary winding.

A summary of the results is shown in Table 5.4 where the winding arrangement is described by a notation where the number indicates the number of turns, P and S indicates if the turns correspond to the primary winding or the secondary winding respectively. Therefore, 4P7S3P means that the winding arrangement consisted of four primary turns followed by the seven secondary turns and then the remaining three primary winding turns. The measurements were performed using an Agilent Impedance Analyser 4284A; the measurements were performed at 1 MHz.

Table 5.4: Measured leakage inductance and windings' AC resistance of different winding arrangements at 1MHz

Arrangement	**Leakage inductance (nH)**	**Winding AC resistance (mΩ)**
Not interleaved 7P7S	902	470
4P7S3P	633	356
3P3S4P4S	543	330
Fully interleaved 1P1S1P1S1P1S1P1S1P1S1P1S	312	208

The measured data shows that the leakage inductance and the windings' AC resistance change in a similar way, higher leakage inductance tends to be associated with higher losses which is in accordance with other published work, [184, 185]. The fully interleaved arrangement provides the lowest leakage inductance and AC

resistance. Therefore, to expand the soft-switching range of the converter by increasing the leakage inductance of the transformer will almost certainly increase the windings' power loss.

The second arrangement provides the required minimum leakage inductance to guarantee soft-switching as established in the design assumptions in Table 5.1 and was the option implemented.

The actual leakage inductance seen by the primary side will be higher in the final converter implementation since these measurements do not account for the added stray inductance of the transformer termination and circuit connections.

The windings' DC resistance (R_{DC}) was calculated to be 23mΩ and the R_{AC} and R_{DC} ratio (R_{AC} / R_{DC}) was 15.5, where R_{AC} is the windings' AC resistance.

Table 5.5 presents the measurements of the inductance of the primary and secondary side with the other winding left open. The primary magnetising inductance of 191μH will carry a peak magnetising current of 550mA which is comparatively small compared with the main primary current of 7.65A.

Table 5.5: Transformer primary and secondary windings inductance measurements

Winding	Inductance (μH)
Primary	191
Secondary	3.9

5.3.6 Rectifier

The full-bridge rectifier was implemented using two ST STPS200170TV1 Schottky rectifier modules. Each package contains two independent Schottky diodes having the characteristics in Table 5.6. The relatively high reverse breakdown voltage was chosen to give some margin to withstand the parasitic oscillations between transformer leakage inductance and diode capacitance discussed in section 5.2.3.

The diodes are in an ISOTOP package, which has an isolated metallic base for thermal management.

Table 5.6: STPS200170TV1 main electrical parameters

Characteristic	Rating
Reverse Breakdown Voltage	170V
Maximum average forward current per diode	100A
Maximum operating junction temperature	150°C
Forward voltage at 50A and 25°C	0.72V

5.3.7 Output filter and clamp circuit board

The output filter board consists of the output inductor, the output capacitor and the clamp circuit and is built on a T-Clad board to facilitate thermal management.

The filter inductor L_o value is chosen to limit the peak-to-peak ripple current ΔI_{Lo} to less than 20% or 10.7A. Considering the inductor discharge period (t_2-t_4 in Figure 5.3), where $-V_o$ is applied to the inductor, the following relation can be established:

$$V_o = \frac{2 f_s L_o \Delta I_{Lo}}{1 - \delta + \frac{2T_{OL}}{T}} \tag{5.38}$$

Using the converter initial specification of Table 5.1 and assuming that the leakage inductance is 633nH and the turns-ratio is 1/7 (as defined in section 5.3.5) the overlap period using (5.1) is 36ns and the required inductor value is 290nH with a 54A DC current capability. A Vishay IHLP8787MZERR47M5A, 470nH, SMD inductor was selected as the closest available. Table 5.7 summarises the main parameters.

Table 5.7: Output inductor main parameters

Parameter	Rating
Inductance	470nH
Typical DC resistance at 25°C	0.56mΩ
Maximum DC resistance at 25°C	0.67mΩ
Thermally limited maximum current	80A
Saturation current DC typical	100A

The output capacitor is chosen to limit the peak-to-peak output ripple voltage ΔV_o to 1% or 0.28V. By integrating the triangular capacitor ripple current the required output capacitor may be expressed as:

$$C_o = \frac{\Delta I_{Lo}}{16 \Delta V_o f_s} \tag{5.39}$$

Using ΔI_{Lo} = 6.6A, corresponding with L_o = 470nH, then the output capacitance is 1.47µF.

Four ceramic Murata capacitors (GRM31CR72A105KA01L) of 1µF in 1206 SMD packages were chosen. The four parallel capacitors are used to share the ripple current. Furthermore, the capacitor exhibits a 30% reduction in capacitance at 30V. Its *ESR* is 3mΩ at 1MHz.

The clamp circuit was designed to have a clamp voltage of at least 45V and a maximum clamp voltage ripple of 100mV. The circuit was designed based on the analysis and design equations in [177].

The circuit used a SK100/50SA Schottky diode rated at 100V, and 5.5A from Vishay; three parallel 2.2µF, 1206 SMD packaged ceramic capacitors rated at 100V; and a 27Ω D2PAK power resistor rated at 35W. The board layout is shown in Appendix B.

5.4 Converter energy losses

This section analyses the main losses in the converter.

5.4.1 GaN cascode devices

The device currents are made up by the reflected secondary current, assumed to be a square wave of $\pm NI_o$, plus the magnetising current, assumed to be a triangular waveform with an amplitude of I_{mag}, which may be estimated as:

$$I_{mag} = \frac{V_i \left(\frac{\delta T}{2} - T_{OL} \right)}{2 L_{prim}} \tag{5.40}$$

where L_{prim} = 191µH.

The conduction power loss per transistor, P_{QC}, is then estimated as:

$$P_{QC} = \frac{1}{2} \left({I_{D-ON}}^2 + \frac{{I_{mag}}^2}{3} \right) R_{DS-ON} \tag{5.41}$$

The transistor switching losses are obtained from the practical measurements described in Chapter 3.

The turn-off energy loss includes the energy stored in the output capacitance of the cascode device, however this energy will be recovered by zero voltage switching at turn-on, therefore the capacitive stored energy is subtracted using the datasheet output capacitance value. The energy stored in the output capacitance at 270V is 3.24µJ. Figure 5.14 shows the actual power loss in each device at 1 MHz, assuming V_i = 270V, R_G = 10Ω and V_{DD} = 6V for different currents.

The black line represents a fourth order polynomial trend line to facilitate the approximation of the power loss between data points.

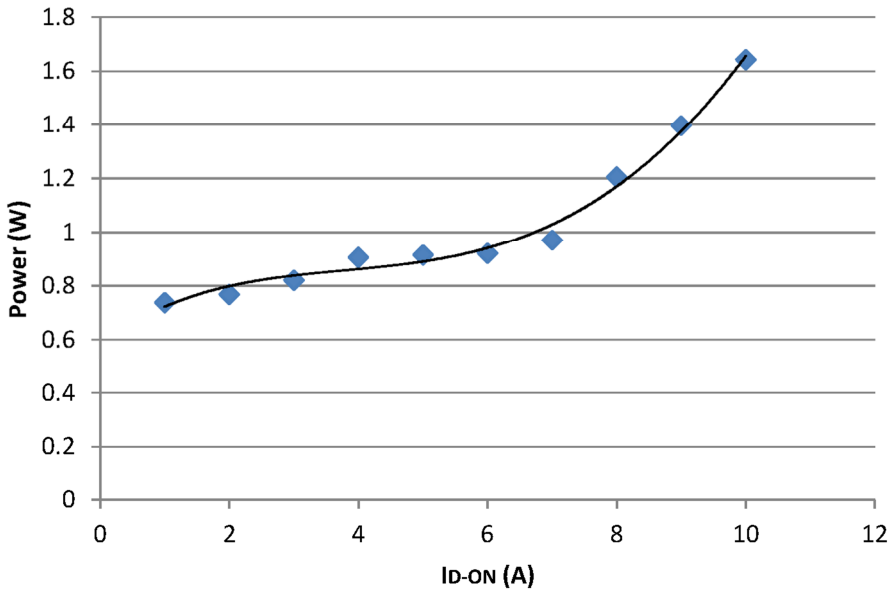


Figure 5.14: Cascode device switching power loss at different current level. F = 1 MHz, V_i = 270V, R_G = 10Ω and V_{DD} = 6V

5.4.2 Transformer

The core loss (P_{TC}) is estimated using the Steinmetz equation, (5.36) and the coefficients of the equation at 100°C are given in Table 5.8, [186].

Table 5.8: 3F4 Steinmetz equation coefficients

Ferrite	Frequency Range (kHz)	k	α	β
3F4	400-1000	5.8×10^{-5}	1.8	2.9

The copper loss is estimated by assuming the transformer current referred to the primary is a square wave of $\pm NI_o$, and using the measured winding resistance at 1MHz from the short-circuit test, section 5.3.5.

5.4.3 Rectifier diodes

The rectifier diode conduction losses are calculated assuming each diode conducts a square pulse of current of value I_o with a duty ratio of 50%. The diode forward voltage is taken from the SPICE model of the diode, 0.67V at 53.34A.

Each diode will undergo switching losses as the reverse bias voltage is re-applied and the losses may be estimated using the reverse bias capacitance from the datasheet and equation (5.42), [177].

$$P_{Diode-SW} = \frac{16}{3} C_{rect} V_{rect}^2 f_s \tag{5.42}$$

5.4.4 Output filter

The inductor losses were calculated using the DC and AC resistances, DCR and ACR respectively taken from the datasheet and the DC and AC components of inductor current. The total loss P_L was therefore:

$$P_L = I_o^2 DCR + ACR \frac{\Delta I_{Lo}^2}{12} \tag{5.43}$$

where ΔI_{Lo} is the peak-to-peak inductor ripple current and DCR = 0.6mΩ and ACR = 51.4mΩ at 2MHz.

Filter capacitor loss was estimated from the equivalent series resistance, ESR, taken from the datasheet using:

$$P_C = \left(\frac{\Delta I_{Lo}}{\sqrt{12}} \right)^2 ESR \tag{5.44}$$

However, the loss in the output capacitors is only a few mW and was neglected in the converter loss estimation.

5.4.5 Clamp circuit

The loss in the clamp resistor P_{clamp} is calculated as:

$$P_{clamp} = \frac{\left(V_{clamp} - V_o\right)^2}{R_{clamp}} \tag{5.45}$$

5.5 Physical implementation

Photographs of the assembled driver circuit and power converter are shown in Figures 5.15, 5.16 and 5.17.

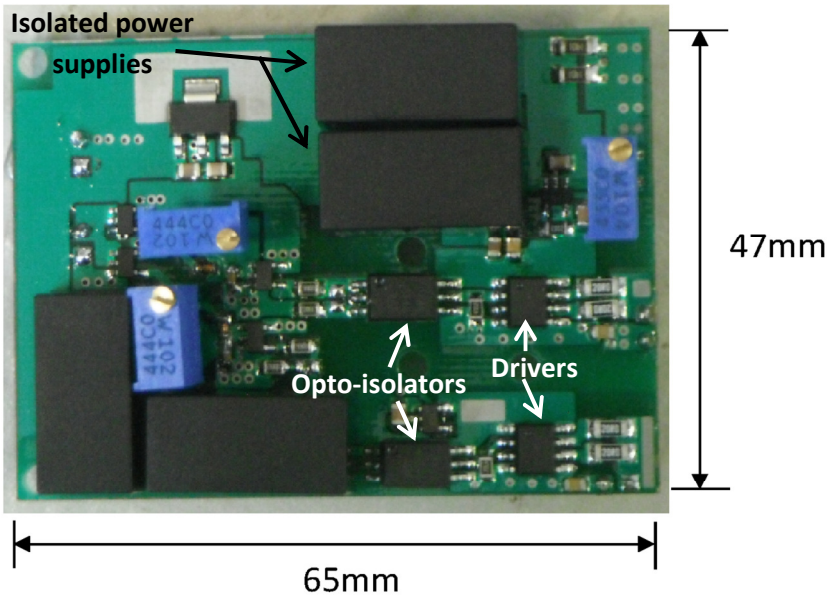


Figure 5.15: Leg driver board

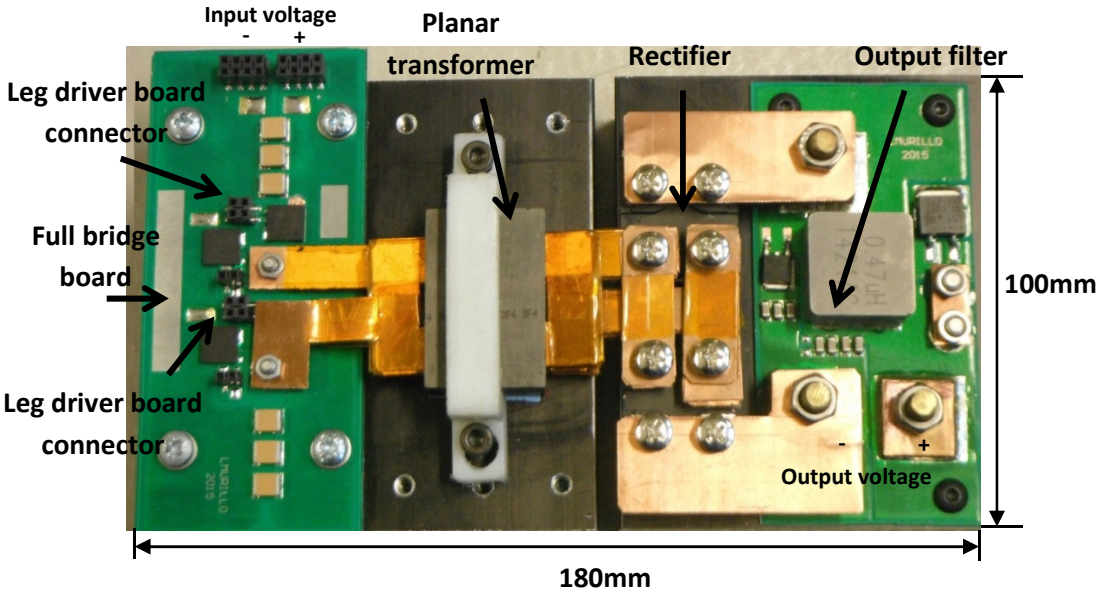


Figure 5.16: Physical implementation of the GaN power converter (top view)

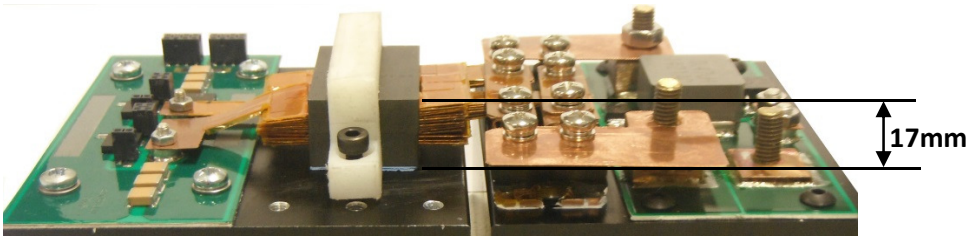


Figure 5.17: Physical implementation of the GaN power converter (side view)

The two potentiometers to the left on the driver board are used to set the dead time of the leg whilst the one on the right is used to set the positive driver voltage. The opto-isolators and drivers are in the right-bottom part of the board. Two header connectors are soldered on the bottom layer to connect the driver board to the bridge board.

The images of the converter show the four blocks of the circuit: the full-bridge board on the left, the planar transformer in the centre and, the rectifiers, output filter and clamp circuit on the right.

The T-Clad full-bridge board is screwed to a 1.4°C/W heatsink with thermal grease at the interface. The leg driver connectors and the bottom side switches of the legs are in the centre of the board. The ceramic decoupling capacitors are towards the top centre and bottom centre of the board.

A non-metallic bracket is used to clamp the planar transformer onto the heatsink and a sheet of “gap-pad” with a thermal conductivity of 3W/m-K is placed between the core and the heatsink.

The two rectifier packages are to the right of the transformer and are screwed to a second heatsink with thermal grease at the interface.

The output filter and clamp circuit board (at the right of the rectifier) shows the filter inductor in the centre and the four ceramic output capacitors just below. The clamp circuit diode and capacitors are to the left of the output filter inductor while the clamp resistor is to the right. The output filter T-Clad board is screwed to the heatsink again using thermal grease at the interface.

5.6 Testing

A Teledyne LeCroy Wave Runner 610Zi 1GHz and 20Gs/s oscilloscope was used to measure the circuit waveforms. The secondary current was measured using a PEM Rogowski coil CWT (20mV/A), and the primary and secondary voltages were measured using Teledyne LeCroy ADP305 high voltage differentials probes. Figure 5.18 shows the four gate signals before the converter was energised. The waveforms show the leg dead times of 18ns in leg A and 20ns in leg B.

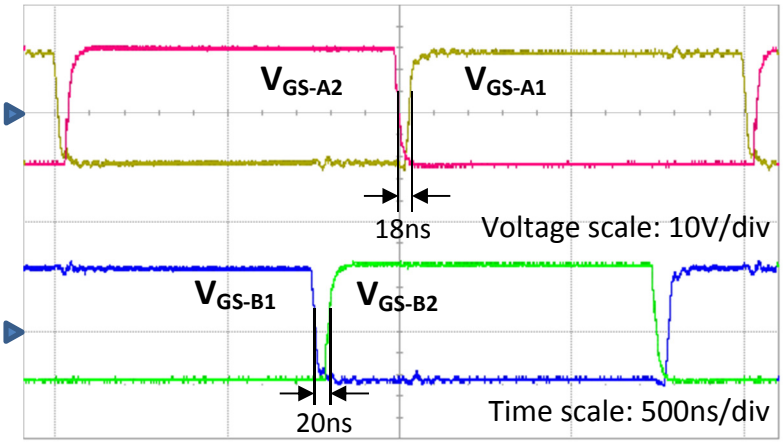


Figure 5.18: Full-bridge gate signals

The converter was initially tested at 1.23kW, δ was set to 0.88. Figure 5.19 presents the main waveforms of the converter. The waveforms show the secondary current I_{SEC}, the full-bridge output voltage V_{AB}, and the secondary voltage V_{SEC}. The V_{AB} waveform is clean and the voltage transitions are well-controlled with virtually no parasitic oscillations due to the zero-voltage switching. The diode overlap period during which I_{SEC} reverses is clearly evident in the I_{SEC} waveform, having a duration of 50ns, and during this time V_{SEC} remains at a low voltage. The overshoot in I_{SEC} immediately after the current reverses is attributed to the charging of the secondary diode capacitance at the end of the overlap transient.

Oscillations are seen in the secondary winding voltage at the beginning of the power delivery stage and are attributed to the interaction of the transformer leakage inductance with the clamp circuit and the parasitic capacitance of the secondary.

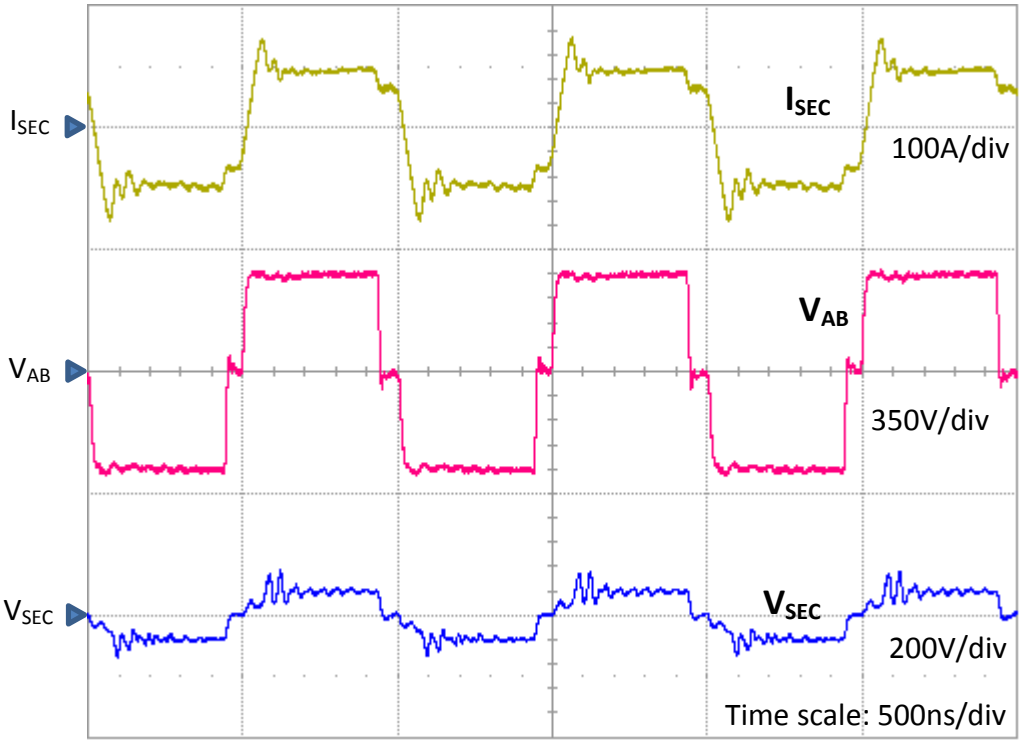


Figure 5.19: GaN power converter waveforms at 1.23kW

However the oscillations are fairly well controlled due to the operation of the clamp circuit. The clamp voltage V_{clamp} was 46.7V and the calculated clamp circuit power losses were 13W. Figure 5.20 shows the expanded V_{SEC} waveform.

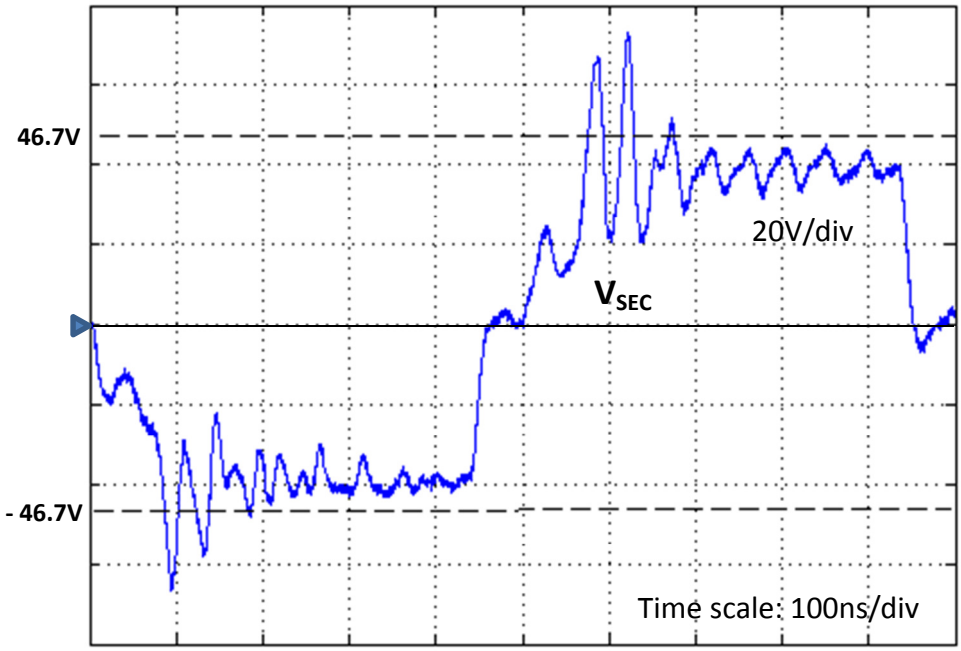


Figure 5.20: V_{SEC} expanded waveform at 1.23kW

The converter output power was increased to 1.5kW. The control parameter, δ, was increased to 0.908 to compensate for the drop in V_o. The main waveforms under these conditions are shown in Figure 5.21 whilst expanded waveforms are shown in Figures 5.22 to 5.24.

The waveforms in Figure 5.21 are similar to these in Figure 5.19 but the current level is increased. The measured clamp circuit voltage V_{clamp} was 48V as indicated in the expanded V_{SEC} waveform of Figure 5.22. The secondary voltage exceeds the clamp level due to the parasitic inductance of the circuit loop through the clamp circuit.

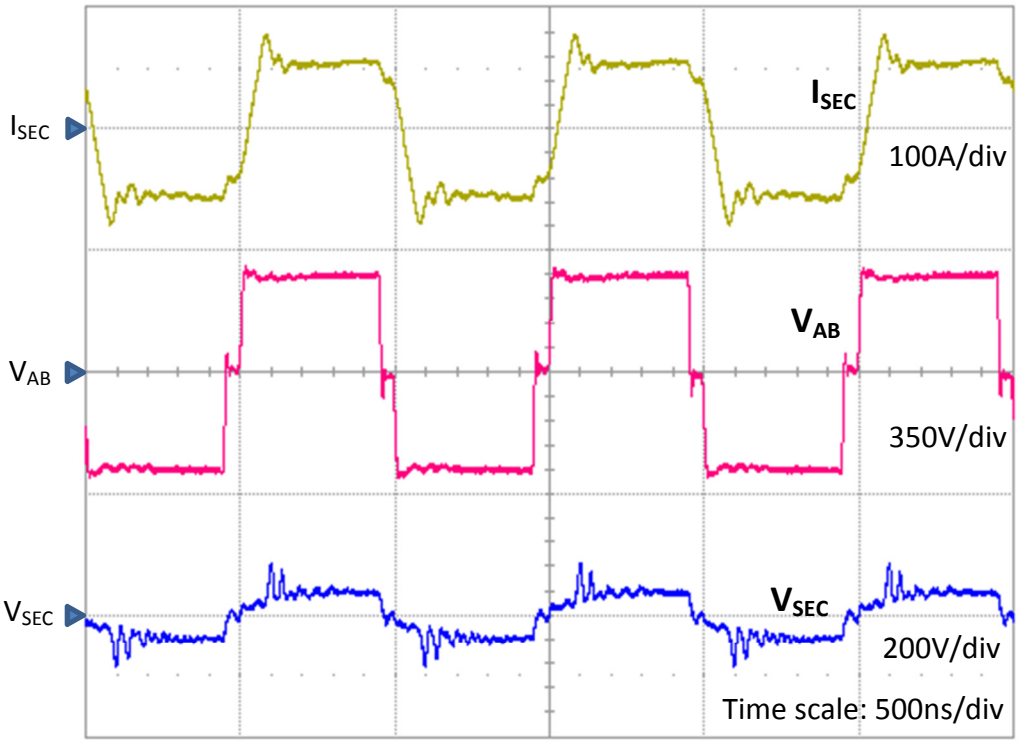


Figure 5.21: GaN power converter waveforms at 1.5kW

The total leakage and stray inductance seen by the primary can be determined by measuring the rate of change of the secondary current during the overlap transition. The total primary-referred inductance, L_k, is then calculated as:

$$L_k = \frac{V_i}{N\dfrac{dI_{SEC}}{dt}} \tag{5.46}$$

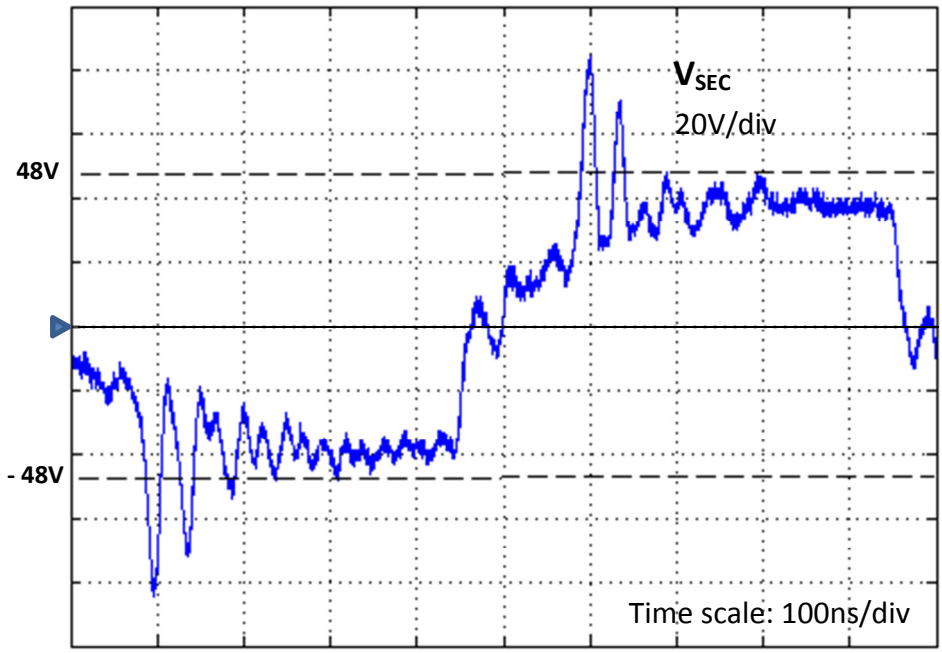


Figure 5.22: V_{SEC} expanded waveform at 1.5kW

The measured secondary current switching speed is 1.48A/ns (Figures 5.23 and 5.24) and the resulting leakage inductance L_k is 1.28µH. The measured transformer leakage inductance is 633nH as indicated in Table 5.4. The difference between the measurements is the primary-referred stray inductance and layout inductance of the secondary rectifier circuit. Referring the value to the secondary side of the transformer gives the result of 13.2nH.

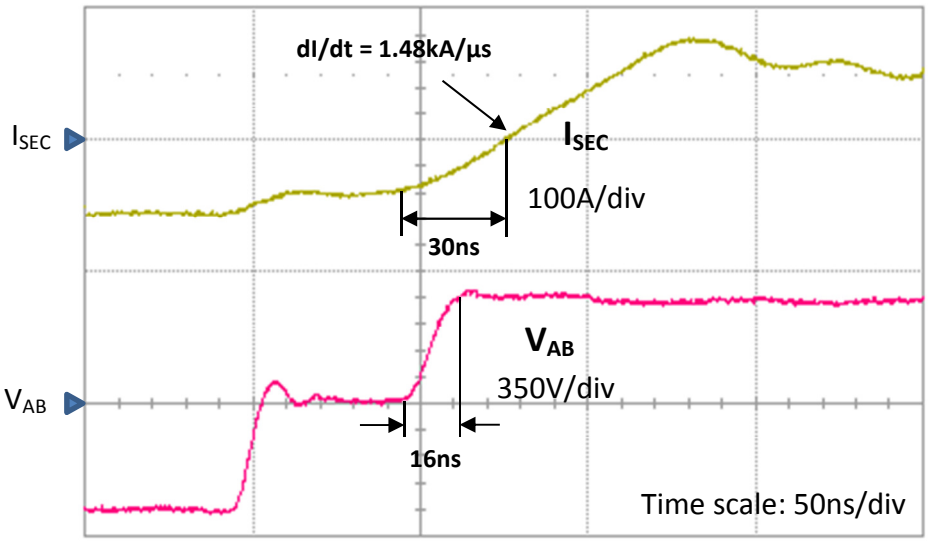


Figure 5.23: I_{SEC} and V_{AB} expanded waveforms, rising edge of I_{SEC} at 1.5kW

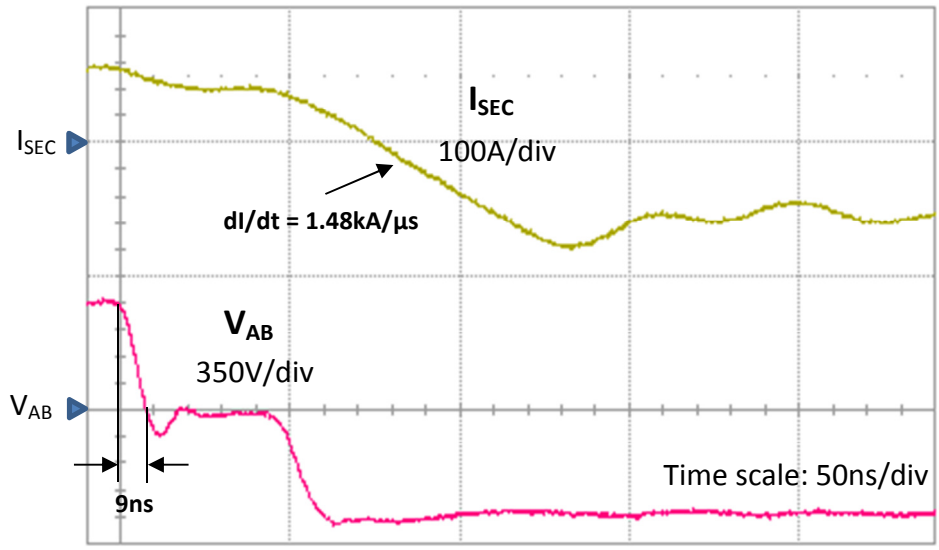


Figure 5.24: I_{SEC} and V_{AB} expanded waveforms, falling edge of I_{SEC} at 1.5kW

The measured primary voltage switching time from the end of the freewheeling mode to the start of the overlap transient is 16ns as indicated in Figure 5.23 and is the voltage switching time of the leading leg. Therefore, the dead time needs to be set to at least 16ns to allow complete zero voltage switching in the leading leg switches. On the other hand, during the overlap transient the secondary current falls to zero in around 30ns as indicated in Figure 5.23, this is the maximum allowed dead time of the leading leg since the incoming transistor must be turned-on to allow I_p to reverse. Both conditions are met since the leading leg switches' dead time was set to 18ns.

The measured primary voltage switching time when it commutes from the power delivery mode to the freewheeling mode is 9ns as indicated in Figure 5.24. Then, the minimum dead time of the lagging leg needs to be set to at least this value. The condition is met since the dead time was set to 20ns.

The input voltage, input current, output voltage and output current of the converter were measured to determine its efficiency (E_{ff}) and total power loss (P_T). The input and output currents were measured using Murata current shunts. Agilent 34401A 6 ½ digit multimeters were used to measure the shunt voltages and the input and output voltages. The measured powers and efficiency at 1.5kW are shown in Table 5.9.

Table 5.9: Converter measured parameters at 1.5kW, 270V-28V

Parameter	Value
P_i	1627W
P_o	1494W
Losses	133W
Efficiency	**91.8%**

The efficiency is 91.8% and could be potentially be 92.7% without the additional losses in the clamp circuit.

The energy losses in the individual components were estimated using the analysis and calculations presented in section 5.4. Table 5.10 presents a summary of the results.

Table 5.10: Summary of losses calculation at 1.5kW, 270V – 28V, 1MHz and ambient temperature = 23°C

Circuit	Assumptions	Calculated loss
Transistors	R_{DSON} = 0.15Ω P_{QS} = 1.2W	Total conduction loss = 18.7W
		Total switching loss = 4.8W
Transformer		Core loss = 6.2W
		Copper loss = 22.2W
Rectifier	V_F = 0.67V C_{rect} = 1.2nF	Total conduction loss = 71.4W
		Total switching loss = 9.5W
Output filter	DCR = 600μΩ ACR = 51.4mΩ	Inductor loss = 1.9W
Clamp	V_{clamp} = 48V	Clamp resistor loss = 14.8W
	Total loss =	149.5W

The difference between the estimated losses in Table 5.10 and the input-output power measurements in Table 5.9 is 17W or just over 10% which is considered to be a good correspondence considering all the potential errors in the component parameters and the potential errors in calculating efficiency from input and output power measurements. The temperature effects and the parasitic elements of the circuit are also potential sources of error.

Figure 5.25 presents a pie-chart of the energy loss distribution from Table 5.10. The conduction loss of the diodes is the dominant loss mechanism followed by the

transformer copper loss and the transistor conduction loss. These three mechanisms represent three quarters of the total loss.

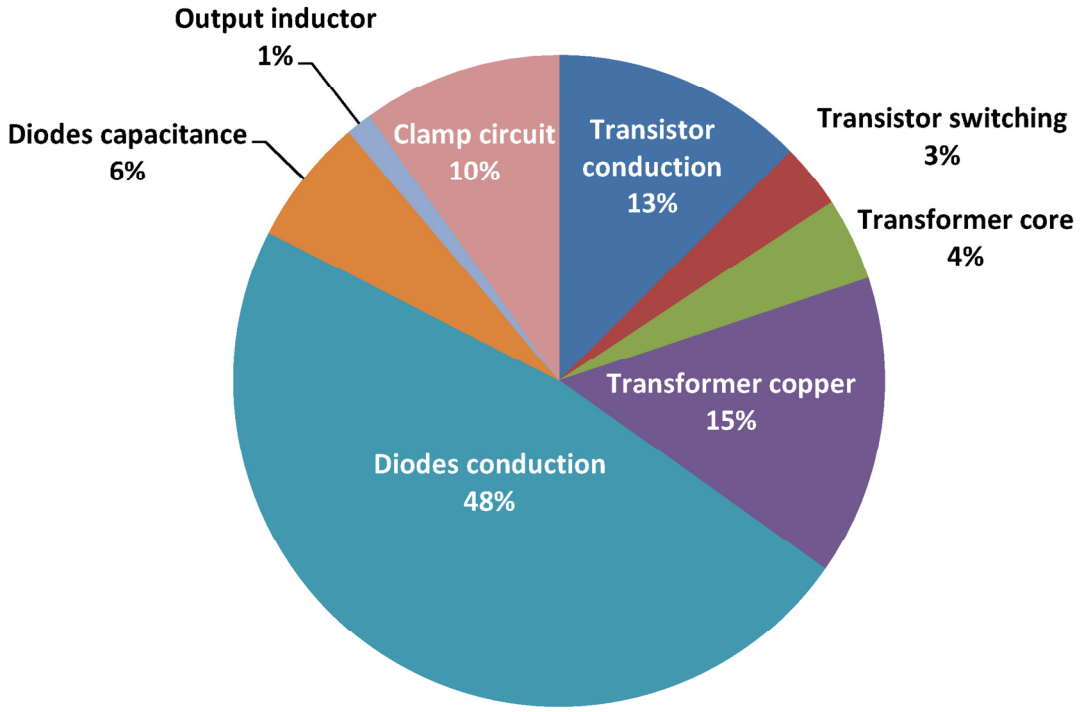


Figure 5.25: GaN power converter loss distribution at P_o = 1.5kW, 270V-28V

The clamp circuit represents 10% of the loss and this is the cost of controlling the diode voltage transient and oscillations.

The transistors' switching losses contribute only 3% of the total loss even at 1MHz, confirming the excellent switching performance of the devices. This indicates the potential to make significant further increases in operating frequency and reduce passive components size.

The transformer losses are dominated by the winding losses resulting in a winding temperature of 130°C. A more highly interleaved winding would allow these losses to be reduced, but would also reduce the leakage inductance, which is required for zero voltage switching. Improved thermal management is needed to limit the winding temperature, but even so a more radical change in transformer technology may be needed if the frequency is to be increased significantly.

The rectifier losses represent 48% of the converter losses. This is due to the use of four diodes with effectively two in series with the load current, a centre-tapped secondary winding would allow the number of diodes to be halved, but at the cost of

an increased diode off-state voltage and a more complicated transformer. Furthermore, significant loss reductions could be achieved by replacing the diodes with MOSFETs operating as synchronous rectifiers. For example, a state-of-the-art MOSFET (Infineon IPI041N12N3) rated at 120V, 100A has a maximum $R_{DS\text{-}ON}$ of 3.8mΩ and could potentially reduce the rectifier conduction power loss from 71.4W to 10.8W if a two device synchronous rectifier is used, increasing the efficiency to around 95%.

5.7 Impact of the GaN cascode devices

The impact of the GaN cascode devices in comparison with Si can be assessed from two perspectives: considering a converter designed under the same conditions but using Si super junction MOSFETs with a similar $R_{DS\text{-}ON}$ and second considering a converter designed to operate with Si devices at lower frequency where the transistor switching losses would be similar to those in the GaN devices at 1MHz.

5.7.1 Analysis considering the use of a similarly rated Si SJ MOSFET under the same operation conditions

The impact of using the Si super junction MOSFET IPP65R125C7 that was characterised in the switching test work described in Chapter 4 instead of the GaN device may be assessed by comparing the switching losses in the two devices under zero-voltage switching. The two devices are assumed to have similar on-state resistances. The zero-voltage switching turn-off losses were calculated by subtracting the capacitive stored energy in the off-state from the measured turn-off loss in the double pulse testing experiments. The results are plotted in Figure 5.26 where a 1MHz switching frequency was assumed to give a device power loss.

Assuming a turn-off current of 8A, the average loss in the Si device due to switching is 7.2 times the figure in the GaN transistor, which results in an additional loss of 29.7W considering all four transistors, an increase of 22.3% in the total losses, which would reduce the efficiency from 91.8% to 90.2%. The significantly increased losses would require a larger heatsink and may also result in an increased junction temperature, which would result in a higher on-state resistance and increased conduction losses.

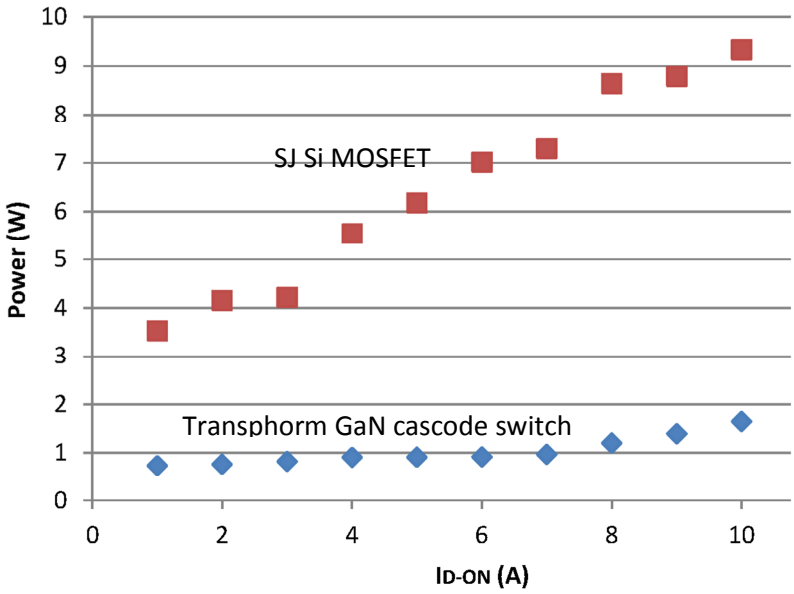


Figure 5.26: Transphorm GaN cascode transistor vs SJ Si MOSFET effective turn-off power loss under zero voltage switching at f_s = 1 MHz, V_i = 270V, R_G = 10Ω and V_{DD} = 6V (GaN) and V_{DD} = 10V (Si)

It can be concluded that the silicon design would have increased losses of 22.3%, reducing the efficiency by 1.6 percentage points and a reduced power density due to a larger heatsink.

5.7.2 Analysis considering the use of a similarly rated Si SJ MOSFET but operating at lower frequency with similar transistor switching losses

Based on the comparison of losses in Figure 5.26, the Si devices are seen to have 7.2 times the loss of the GaN devices under zero-voltage switching, therefore to have a comparable loss the switching frequency of the silicon design must be reduced by a factor of 7.2. Therefore the impact of designing the converter to operate at 100 kHz is examined in this section.

Full-bridge board

This would be unchanged since the Si MOSFETs are assumed to have the same package and the same pad assignments. The cooling requirements would be the same as in the GaN converter.

Transformer

At a much lower frequency a complete re-design of the transformer is needed, which is likely to require a much larger core with increased magnetic area, and/or an

increased number of turns, which is also likely to require a larger core to provide the winding space.

A simple solution that fits the requirements of the hypothetical Si-based converter is to consider an available commercial part with approximately the required rating, the HIMAG 80200P1 transformer. Side by side images of this transformer against the one used in the 1 MHz GaN converter are presented in Figure 5.27 and Figure 5.28 whilst Table 5.11 shows a comparison of the volume envelope and weight.

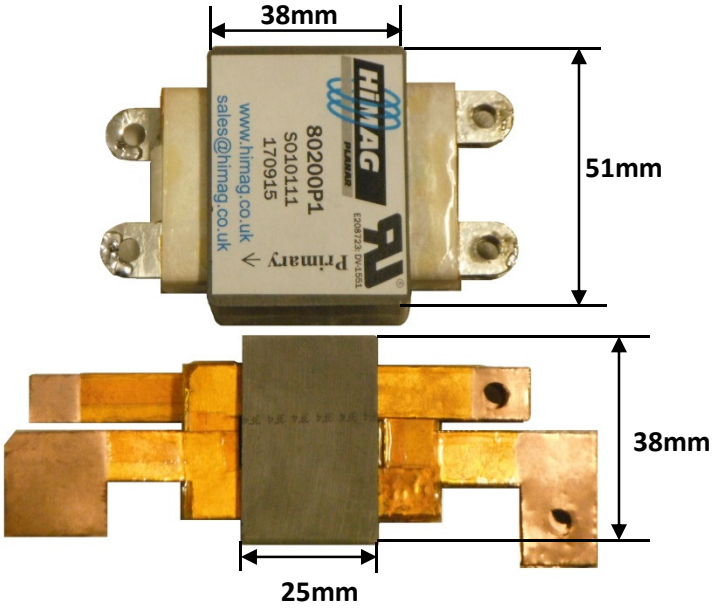


Figure 5.27: HIMAG vs GaN converter transformer (top view)

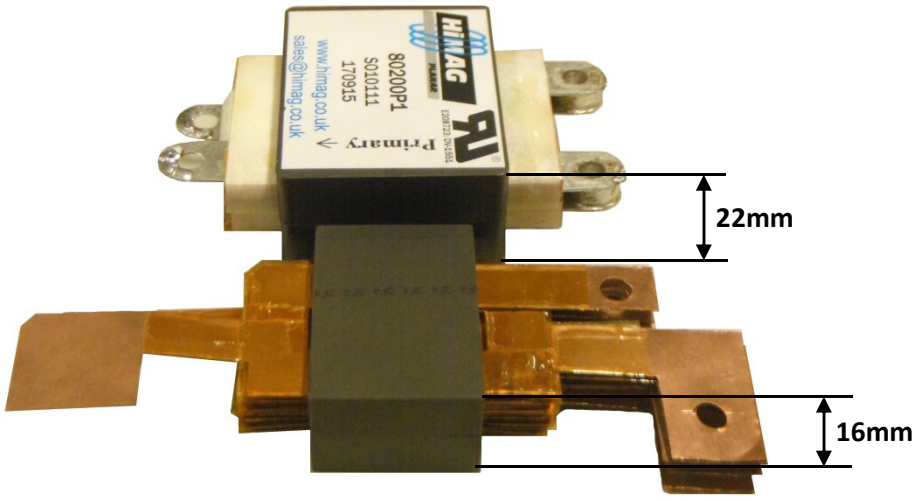


Figure 5.28: HIMAG vs GaN converter transformer (side view)

Table 5.11: Weight and volume comparison of the transformer used in the 1MHz GaN converter and a 100 kHz Si-based converter equivalent transformer

Characteristic	1MHz GaN prototype transformer	100kHz Si equivalent transformer
Volume (cm^3)	27.4	65
Weight (g)	74	240

The volume of the HIMAG transformer is 2.4 times that of the 1MHz component whilst the HIMAG transformer is 3.2 times heavier. The increased weight is due to the larger core and also the larger number of turns, which increases the copper weight.

Summarising, high frequency operation results in a significant reduction of volume and weight of the power transformer.

Rectifier

At 100 kHz the rectifier selection would be unchanged as the key consideration is limiting the conduction loss, however the switching loss associated with the diode output capacitance will reduce in proportion with the reduced frequency. Therefore the rectifier loss will be reduced by 11.5% or approximately 9W.

Output filter

To maintain the same ripple current the inductor value in the 100kHz converter must be increased by a factor of ten, requiring 4.7µH with an average current capability of 54A. One readily available option is the 310 series power inductor offered by West Coast Magnetics. Its inductance is 7.3 µH and it is rated at 55A and has a DCR of 1.13mΩ. Table 5.12 presents a comparison of the volume and weight of this inductor against the one used in the 1MHz converter.

Table 5.12: Weight and volume comparison of the output filter inductor used in the 1MHz GaN converter and a 100 kHz Si-based converter equivalent inductor

Characteristic	1MHz GaN prototype transformer	100kHz Si equivalent transformer
Volume (cm^3)	6.4	104
Weight (g)	36	226

The filter inductor volume for the Si-based converter is 16.25 times the volume of the filter inductor used for the GaN-based converter, whilst the weight of the inductor of the Si-based converter is 6.3 times heavier than the one used in the GaN-based converter. Furthermore the larger inductor requires through hole assembly.

To maintain the same output ripple voltage in the 100 kHz converter the filter capacitor value must be increased by a factor of ten. Therefore the minimum required output capacitance is 40µF, which may be provided using nine parallel 4.7µF, 2220, X7R ceramic capacitors. This capacitor is 7.5 times bigger in volume than the 1206 ceramic capacitor in the 1MHz prototype.

Clamp circuit

The physical size of the clamp circuit will not change significantly at the lower frequency, however the losses will be reduced by approximately a factor of ten.

Driver

GaN devices have a much lower gate charge than the Si counterparts. For example, the Transphorm GaN cascode device has a gate charge of 6.2nC whilst the SJ Si MOSFET has a gate charge of 35nC. The difference directly impacts the driver power loss. The transistor driver circuit power loss (P_{driver}) is largely dependent on the gate charge, which must be drawn from the gate circuit power supply every switching cycle, but also includes the internal losses within the driver integrated circuit. Using the information in the gate driver datasheet, the gate driver power loss for the Transphorm device at 1 MHz is 144mW per device whilst the power loss using the SJ Si MOSFET at 1 MHz is 446mW per device at the same voltage condition. The SJ Si MOSFET driver loss is 3.1 times higher than the losses in the GaN circuit. Considering the four devices, the total power losses are 576mW for the GaN switches and 1.78W for the Si SJ MOSFETs.

Whilst this is only a small proportion of the total losses it may have a significant impact on the driver circuit operating temperature, thermal management requirements and possibly reliability.

5.7.3 Summary of the comparison and opportunity areas

The comparison of section 5.7.1 showed that using a similarly rate Si SJ MOSFET under the same operating conditions results in an increase of 22.3% in the total converter losses reducing the power density because of the requirement of a larger heatsink. On the other hand, the analysis of section 5.7.2 showed that if the Si SJ MOSFET is used in the converter but operating at ten times lower frequency, the transformer would be 2.5 times bigger in volume and 3.2 times heavier, whilst the output filter inductor would be 16.25 times bigger in volume and 6.3 times heavier. Similarly, the output capacitor would be 7.5 bigger in volume in the low frequency converter against the high frequency one. In addition, the use of GaN devices allows a reduction of 67.6% in the driver loss when compared against a similarly rated Si SJ MOSFET.

This comparison has highlighted the significant impact of GaN technology on power converter design and performance, but also indicates areas for further development. The losses in the GaN transistors in the soft-switching converter are dominated by conduction loss, suggesting that larger area devices with lower on-state resistance may be beneficial and it is anticipated that these will emerge as the technology matures. The secondary rectifier losses are very high in the prototype and a synchronous rectifier circuit using MOSFETs could reduce this significantly, furthermore as the low voltage, high current GaN transistors are developed they may offer the opportunity to reduce synchronous rectifier losses below the level of that in a silicon implementation. Making further increases in switching frequency appears to be quite viable from a semiconductor perspective, but is likely to create significant challenges for the magnetic components such as increased losses and more complex thermal management if their size is to be reduced, alternative component topologies and improved thermal management are likely to be needed. The parasitic oscillations in the secondary circuit of the phase-shift controlled converter topology used in this work are likely to become more problematic at higher operating frequencies and an alternative converter circuit may be a better option, for example a resonant topology or one which provides soft-switching of the rectifier diodes.

5.8 Summary

This Chapter presented the design and implementation of a 270V – 28V, 1.5kW, 1MHz, phase-shifted, full-bridge isolated converter. This converter uses ZVS during turn-on allowing full advantage to be taken of the very low turn-off loss of the GaN cascode devices.

The converter includes four Transphorm GaN cascode devices and a planar transformer which allows a compact design. The rectifier is formed with four Schottky diodes. The gate driver circuit was designed to generate a positive voltage for turn-on and a negative voltage for turn-off to avoid shoot through issues in the leg circuit. A secondary-side clamp circuit is used to limit the parasitic voltage oscillations across the rectifier circuit, but at the cost of additional power losses.

The converter was tested at 1.5kW, 1 MHz and its main waveforms are shown. An analysis of the losses in the converter showed good agreement with the efficiency measurements. The measured efficiency was 91.8%, it may be improved by implementing synchronous rectification and by circuit optimisation. The efficiency of a typical DC-DC converter for aerospace applications is in the order of 90% due to the high switching and conduction energy losses of the Si switches, [187].

The analysis showed that the transistor conduction losses were much more significant than the switching loss. The transistor switching losses accounted for 3% of the total power losses while the conduction losses are around 13% of the total loss.

The impact of the GaN cascode devices in the converter is analysed from two perspectives: considering a converter under the same operating conditions but using Si devices and second considering a converter operating at lower frequency but with similar transistor switching losses. The first analysis revealed that the efficiency of the converter will drop by at least 1.6 percentage points if SJ Si MOSFETs are used. The second analysis shows that the same converter implemented using SJ Si MOSFETs at 100 kHz would require a planar transformer which is 2.4 times bigger and 3.2 times heavier than the transformer of the 1MHz GaN-based converter. The analysis also showed that the output filter size would increase significantly having the output filter 16.25 times the volume of the filter inductor in the GaN converter

and being 6.3 times heavier. The increased size and weight of the magnetic components is likely to have a significant impact on the converter overall since these components can account for 30-40% of a converter's weight. The output filter capacitor volume is increased 7.5 times. The use of GaN devices also affects the driver power loss. The losses are 68% lower using GaN devices than using a state-of-the-art SJ Si MOSFET.

One of the key challenges of using the GaN switching devices is dealing with the high-switching speed; taking advantage of the switching speed to reduce loss, but minimising parasitic oscillations and voltage overshoots. Very compact layout design is required to limit parasitic elements, however this is made difficult by the need for high current connections and excellent thermal paths. The high switching speed of the devices also affects the drivers' design since gate waveforms may be easily corrupted by parasitic capacitive coupling or common source inductance coupling. Low impedance drive circuits are needed with a reverse bias in the off-state.

Further increases in the operating frequency of the converter are thought to be possible, although this is likely to be particularly challenging for the magnetic component design. Reducing the rectifier losses should be a high priority in the next stages of the converter prototype development and solutions based on the synchronous rectifier concept would seem to be particularly attractive.

Chapter 6: Conclusions

6.1 Introduction

This Chapter presents a summary of the findings of the research work and the conclusions derived from them. The final remarks are presented. The achievements and contributions are highlighted and the research opportunities are listed. The overall conclusions of the research are presented at the end of the Chapter.

6.2 Thesis summary

Cascode device simple model

A simple model of the cascode structure was developed to understand the switching energy processes and to predict the turn-off and turn-on energy losses. The model considers the parasitic capacitance and transconductance of the devices as constant and neglects the parasitic inductance.

The turn-off and turn-on switching processes are divided into four sub-stages. Laplace and time domain equations are generated for each sub-stage which can be easily used to obtain plots of the switching transients. The proposed model can be used for leg arrangements comprising a single cascode device and freewheeling diode or two cascode devices in a leg by obtaining an equivalent capacitance of the freewheeling body diode.

The model is validated against practical measurements. It accurately predicts the switching speed of the main current and voltage waveforms and generates very similar power plots during the switching transients when compared against those obtained experimentally. The predicted energy losses were up to 13% lower than measurements in an arrangement of a cascode device along with a SiC diode. The maximum discrepancy with experimental measurement was 10% when predicting the switching energy losses of two GaN cascode devices in an inverter leg configuration using an experimental Q_{rr} value at the particular operating conditions.

The model reveals that most of the turn-off energy is stored in the device output capacitance and later dissipated during turn-on. The cascode device turn-off mechanism generates very low losses because the channel switches under low

voltage conditions. The turn-on loss mechanism is very similar to the one observed in a Si MOSFET where the current switches under high-voltage conditions and the voltage switches under high-current conditions. The high speed switching transitions of the GaN device result in lower turn-on loss than in its Si counterpart.

Since the turn-off loss is very low, the cascode device is a good candidate for use in soft-switching converter topologies presenting ZVS during turn-on.

Practical testing of GaN cascode devices

A DPT was used to evaluate the switching characteristics of two super junction Si MOSFETs and a Transphorm GaN cascode device. The measured switching times of the GaN cascode were shorter than those measured in the Si MOSFETs. The turn-off switching speed of the GaN device was largely independent of the driver parameters such as driver voltage and gate resistor whilst the turn-on switching speed does depend on these parameters.

The body diode of the Transphorm device is evaluated against an equivalent SiC diode. The results show that the cascode device body diode has higher conduction loss at high current and three times higher Q_{rr} when compared against a similarly rated SiC device. Therefore, higher switching losses during turn-on are expected when a GaN device body diode is used as the freewheeling path instead of a SiC diode.

The switching energy losses of different device arrangements were evaluated and compared. The measurements show that the GaN cascode device along with a SiC diode presents the lowest losses of all the arrangements, but may require the addition of a series Schottky diode to suppress the body diode of the cascode device in some circuit applications. Two GaN cascode devices in an inverter leg configuration had 50% higher losses than the single GaN device arrangement, but the losses still are up to 26% lower than the best Si MOSFET along with a SiC diode. The use of two GaN cascode devices in an inverter leg could offer a highly efficient circuit with very low component count compared with a Si alternative. The simple addition of an antiparallel SiC diode to a GaN cascode device in the inverter leg configuration only slightly reduces the energy loss at high current.

The measurements verify that low turn-off loss is obtained using cascode devices.

The conclusions based on the Transphorm devices were confirmed by tests on a similar part from GaN Systems.

GaN power converter

A 270V – 28V, 1.5kW and 1 MHz phase-shifted full-bridge isolated converter was implemented using four Transphorm GaN cascode devices. A clamp circuit was used to limit the rectifier oscillations but at the cost of increasing the power loss of the converter. The transistor switching losses represent only 3% of the total converter losses. The measured efficiency was 91.8%.

The prototype demonstrates the feasibility of implementing high-frequency converters using the emerging GaN devices and indicates the potential benefits. An equivalent Si-based converter switching at the same frequency as the GaN prototype would increase the converter loss by at least 22% requiring improvements in the thermal management to achieve the same temperature, operating range and thermal performance. The study also showed that a Si-based converter switching ten times slower than the GaN converter, (a common switching frequency for the topology using Si switches) will need a transformer that is 2.4 times bigger and 3.2 times heavier; furthermore, the required output filter inductor would be 16.25 times bigger and 6.3 times heavier.

The GaN devices allow converter efficiency to be significantly increased if operating at similar switching frequency or a system volume reduction if operating at higher switching frequency.

Also, the GaN devices allow a reduction of 68% in the driver power loss with respect to its equivalent Si counterpart when switching at the same frequency.

6.3 Contributions of the research work

Cascode device simple model

A new simple model of the cascode configuration makes possible a more convenient balance between simplicity and accuracy than current models provide. The model can be easily applied to a single GaN device along with a SiC diode and also to the inverter leg configuration formed by two cascode devices which is not considered in other models.

The model allows the quick prediction of the turn-off and turn-on energy loss using device datasheet data with variations of less than 20% against practical measurements.

The model generates time-domain equations that can be used to generate plots of the cascode main waveforms and has proved to be useful in explaining the energy interactions within the devices. The advantage of using the cascode configuration in soft-switching converter topologies is another conclusion arising from the simple model.

Demonstration of the effect of driving parameters and operating conditions on the switching speed and energy loss

Extensive testing using two different cascode devices in an inverter leg configuration demonstrates the influence of the gate resistor, driver voltage, operating current and operating voltage on the switching speed and switching losses confirming the model predictions. Previous studies considered a single device with a SiC diode.

Demonstration of the feasibility of using two GaN cascode devices in an inverter leg configuration

The benefits of operating two GaN cascode devices in an inverter leg configuration are quantified and compared with other device combinations for the first time. The experimental work demonstrated that this operating mode allows a reduction of the device count from six to two components and a reduction of the switching energy loss of at least 17% at high current operation when compared with a silicon alternative. Furthermore, the addition of an anti-parallel SiC diode to the GaN cascode device allows a loss reduction of over 40% with the same number of components as a silicon design.

GaN power converter demonstration

A 270V-28V, 1.5kW, phase-shifted full-bridge isolated buck converter using GaN devices and switching at 1MHz has been demonstrated for the first time. The measured efficiency was > 91%. The operating frequency represents a ten times increase with respect to most recent publications using this topology. The high operating frequency was achieved thanks to the superior switching characteristics of the GaN cascode devices.

As a result of the increased switching frequency, a reduction of 58% in volume and 69% in weight is achieved in the converter transformer when compared against estimations of an equivalent Si-based converter operating at 100 kHz. Similarly, the output filter inductor volume is reduced 94% whilst the weight is reduced 84%. The savings are likely to have a large impact at equipment level since the magnetic components account for 30-40% of the total converter component weight.

The design and testing of the converter showed the benefits and challenges of using GaN devices at converter level. The study demonstrates that GaN cascode devices are well suited for soft-switching converters allowing operating frequencies not possible with current Si-based devices.

6.4 Research opportunities

Current collapse measurement

Current collapse measurement circuits could be improved through improvements in its clamp circuit which limits the time to obtain data.

GaN devices packaging

Current GaN devices mainly use traditional Si device packages. These packages can add significant parasitic inductance to the different circuit loops generating oscillations, under-shoots and over-shoots which may limit the performance of the devices. New low impedance packages need to be developed to take full advantage of the characteristics of GaN devices and which also provide improved thermal management. The monolithic integration of drivers and power devices would be a useful area of development.

Synchronous rectification using GaN devices

The efficiency of the converter presented on this research work could be significantly improved by using a synchronous rectification scheme. Emerging high-current, low on-state resistance GaN devices could be used to show the additional benefits of using these devices in a high current converter.

Magnetic components for high frequency applications

Whilst GaN devices provide the opportunity to increase operating frequencies and reduce passive component size, limitations are likely to occur in traditional magnetic component topologies using existing materials. New low-loss core materials and new methods to improve the thermal management of magnetic devices are required to gain maximum benefit of the increased operating frequency.

EMC implications of the usage of GaN devices

GaN devices can achieve very high switching speeds reducing the switching energy loss. However, the effect of the circuit parasitic elements is magnified resulting in signal oscillations accompanied by over and undershoots that generate undesirable electromagnetic emissions. In addition, sharper voltage and current edges are produced generating more electromagnetic emissions. Construction methods and design techniques are required to manage the EMC issues effectively.

6.5 Conclusion

GaN devices have superior switching characteristics to silicon technology, offering the opportunity to reduce circuit losses and/or make a step increase in operating frequency. As a result equipment size could be significantly reduced through smaller heatsinks and/or smaller passive components.

The migration to this new technology poses many challenges with regard to understanding the behaviour of the new devices and the most effective way of using them. This research has contributed to the modelling and analysis of the cascode connection, providing a basis for converter design and has quantified the potential impact of the technology through the development of a 1.5kW, 1MHz demonstrator.

6.6 Publications

A conference paper was published based in Chapters 3 and 4. The details of the publication and its abstract are presented next:

- L. C. Murillo Carrasco and A.J. Forsyth, "Energy analysis and performance evaluation of GaN cascode switches in an inverter leg configuration," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, 2015, pp. 2424-2431.

  This paper presents an analysis of the energy loss distribution in a cascode array and a study of the behaviour of two GaN cascode devices in an inverter leg configuration. A simple model of the cascode connection is developed to get estimations of energy losses and its accuracy is validated through experimental measurements using a Double Pulse Tester (DPT). The simple model is then applied to analyse the energy loss distribution between the two devices within the cascode switch during turn-off and turn-on. The analysis shows that most of the energy involved in the turn-off process is stored and that most of the energy is dissipated in the GaN HEMT during turn-on. The results are compared against other device combinations including silicon super junction technology. The analysis shows that two GaN cascode devices in an inverter leg configuration represent an improvement over the Si MOSFET plus SiC diode combinations reducing the energy losses up to 26 percent at high current conditions and eliminating the requirement for body diode suppression and the use of an external SiC diode. The switching losses of a single GaN device and SiC diode were shown to be 40 percent lower than the latest generation super junction Si MOSFET.

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Appendix A

Simple model constants definition

This appendix presents the definition of the constants that are used in the simple model developed in Chapter 3. The constants are classified per turn-off or turn-on switching processes and according to the stage where they are used.

Turn-off

Stage 2, $i_{D\text{-}Si}$ (t) > 0:

$$k_{F201} = \frac{g_{m-Si} R_G C_{GD-Si} + C_{oss-Si}}{R_G \left(C_{oss-Si} C_{iss-Si} - C_{GD-Si}^{\,2} \right)} \tag{A.1}$$

$$k_{F202} = -\frac{R_G C_{GD-Si} \left(g_{m-Si} V_{TH-Si} + I_L \right)}{g_{m-Si} R_G C_{GD-Si} + C_{oss-Si}} \tag{A.2}$$

$$k_{F203} = \frac{C_{iss-Si}}{C_{GD-Si}} \left(v_{GS-Si} \left(t_{1-OFF} \right) - k_{F202} \right) - \frac{v_{GS-Si} \left(t_{1-OFF} \right) + k_{F202}}{k_{F201} R_G C_{GD-Si}} \tag{A.3}$$

$$k_{F204} = -\frac{k_{F202}}{R_G C_{GD-Si}} \tag{A.4}$$

Stage 2, $i_{D\text{-}Si}$ (t) = 0:

$$k_{F201} = \frac{C_{oss-Si}}{R_G \left(C_{iss-Si} C_{oss-Si} - C_{GD-Si}^{\,2} \right)} \tag{A.5}$$

$$k_{F202} = -\frac{R_G C_{GD-Si} I_L}{C_{oss-Si}} \tag{A.6}$$

k_{F203} *and* k_{F204} are defined as when $i_{D\text{-}Si}$ (t) > 0.

Stage 3, $i_{D\text{-}Si}$ (t) > 0:

$$k_{F301} = -\frac{C_{GD-GaN} + C_D}{C_{oss-GaN} + C_D} \tag{A.7}$$

$$k_{F302} = \frac{g_{m-GaN}}{C_{oss-GaN} + C_D} \tag{A.8}$$

$$k_{F303} = \frac{I_L + g_{m-GaN} V_{TH-GaN}}{C_{oss-GaN} + C_D} \tag{A.9}$$

$$k_{F304} = \frac{\left(C_{oss-GaN} + C_D\right) v_{DS-GaN}\left(t_{2-OFF}\right) + \left(C_{GD-GaN} + C_D\right) v_{DS-Si}\left(t_{2-OFF}\right)}{C_{OSS-GaN} + C_D} \tag{A.10}$$

$$k_{F305} = \frac{C_{GD-Si}}{C_{iss-Si}} \tag{A.11}$$

$$k_{F306} = \frac{C_{iss-Si} v_{GS-Si}\left(t_{2-OFF}\right) - C_{GD-Si} v_{DS-Si}\left(t_{2-OFF}\right)}{C_{iss-Si}} \tag{A.12}$$

$$k_{F307} = \frac{1}{R_G\left(C_{GS-Si} + C_{GD-Si}\right)} \tag{A.13}$$

$$k_{F308} = g_{m-Si} V_{TH-Si} - g_{m-GaN} V_{TH-GaN} \tag{A.14}$$

$$k_{F309} = -C_{DS-GaN} v_{DS-GaN}\left(t_{2-OFF}\right) + C_{oss-Si} v_{DS-Si}\left(t_{2-OFF}\right)$$

$$-C_{GD-Si} V_{GS-Si}\left(t_{2-OFF}\right) \tag{A.15}$$

$$k_{F310} = C_{DS-GaN} k_{F302-1} - g_{m-GaN} \tag{A.16}$$

$$k_{F311} = C_{DS-GaN} k_{F301-1} - C_{oss-Si} + C_{GD-Si} k_{F305-1} \tag{A.17}$$

$$b_3 = \frac{C_{DS-GaN} k_{F301} k_{F307} - C_{oss-Si} k_{F307} + k_{F310} - g_{m-Si} k_{F305}}{k_{F311}} \tag{A.18}$$

$$c_3 = \frac{k_{F310} k_{F307}}{k_{F311}} \tag{A.19}$$

$$k_{F312} = -\frac{-b_{31} + \sqrt{b_{31}^2 - 4c_{31}}}{2} \tag{A.20}$$

$$k_{F313} = -\frac{-b_{31} - \sqrt{b_{31}^2 - 4c_{31}}}{2} \tag{A.21}$$

$$k_{F314} = -\frac{C_{DS-GaN}k_{F303} + k_{F308}}{k_{F311}} \tag{A.22}$$

$$k_{F315} = -\frac{k_{F306}C_{GD-Si}}{k_{F311}} \tag{A.23}$$

$$k_{F316} = \frac{-C_{DS-GaN}k_{F304} - k_{F309}}{k_{F311}} \tag{A.24}$$

$$k_{F317} = -\frac{g_{m-Si}}{C_{GD-Si}} \tag{A.25}$$

$$k_{F318} = \frac{k_{F314}k_{F307}}{k_{F312}k_{F313}} \tag{A.26}$$

$$k_{F319} = \frac{k_{F314}\left(k_{F307} - k_{F312}\right)}{k_{F312}\left(k_{F312} - k_{F313}\right)} + \frac{k_{F315}\left(k_{F312} - k_{F317}\right)}{k_{F312} - k_{F313}} + \frac{k_{F316}\left(k_{F312} - k_{F307}\right)}{k_{F312} - k_{F313}} \tag{A.27}$$

$$k_{F320} = \frac{k_{F314}\left(k_{F313} - k_{F307}\right)}{k_{F313}\left(k_{F312} - k_{F313}\right)} + \frac{k_{F315}\left(k_{F317} - k_{F313}\right)}{k_{F312} - k_{F313}} + \frac{k_{F316}\left(k_{F307} - k_{F313}\right)}{k_{F312} - k_{F313}} \tag{A.28}$$

$$k_{F321} = \frac{k_{F305}k_{F319}k_{F312}}{k_{F312} - k_{F307}} \tag{A.29}$$

$$k_{F322} = \frac{k_{F305}k_{F320}k_{F313}}{k_{F313} - k_{F307}} \tag{A.30}$$

$$k_{F323} = k_{F305}k_{F318} + k_{F306} + \frac{k_{F305}k_{F319}k_{F307}}{k_{F307} - k_{F312}} + \frac{k_{F305}k_{F320}k_{F307}}{k_{F307} - k_{F313}} \tag{A.31}$$

$$k_{F324} = C_{oss-GaN} + C_D \tag{A.32}$$

$$k_{F325} = I_L + g_{m-GaN}k_{F318} + g_{m-GaN}V_{TH-GaN} \tag{A.33}$$

$$k_{F326} = \frac{\left(C_{GD-GaN} + C_D\right)k_{F312}k_{F319} + g_{m-GaN}k_{319}}{k_{F324}} \tag{A.34}$$

$$k_{F327} = \frac{\left(C_{GD-GaN} + C_D\right)k_{F313}k_{F320} + g_{m-GaN}k_{320}}{k_{F324}} \tag{A.35}$$

Stage 3, $i_{D\text{-}Si}$ (t) = 0:

k_{F301} - k_{F307}, $k_{F309} - k_{F311}$, c_3, $k_{F312} - k_{F316}$ *and* $k_{F318} - k_{F327}$ are defined as when $i_{D\text{-}Si}$ (t) > 0.

$$k_{F308} = -g_{m-GaN} V_{TH-GaN} \tag{A.36}$$

$$b_3 = \frac{C_{DS-GaN} k_{F301} k_{F307} - \left(C_{DS-Si} + C_{GS-GaN} + C_{GD-Si}\right) k_{F307} + k_{F310}}{k_{F311}} \tag{A.37}$$

$$k_{F317} = 0 \tag{A.38}$$

Stage 4, $i_{D\text{-}Si}$ (t) > 0:

$$k_{F401} = k_{F301} \tag{A.39}$$

$$k_{F403} = \frac{I_L}{C_{oss-GaN} + C_D} \tag{A.40}$$

$k_{F404} - k_{F407}$ are equal to $k_{F304} - k_{F307}$ respectively.

$$k_{F408} = g_{m-Si} V_{TH-Si} \tag{A.41}$$

$$\mathrm{k_{F409}} = \mathrm{k_{F309}} \tag{A.42}$$

$$\mathrm{k_{F410}} = 0 \tag{A.43}$$

k_{F411} and k_{F412} are equal to k_{F311} and b_3 respectively.

k_{F414} - k_{F417} are equal to k_{F314} - k_{F317}.

$$k_{F418} = \frac{k_{F407}}{k_{F412}} \tag{A.44}$$

$$k_{F419} = \frac{k_{F407} - k_{F412}}{k_{F412}^{\,2}} \tag{A.45}$$

$$k_{F420} = \frac{-k_{F418}\left(-k_{F407} + k_{F412}\right) - k_{F419} k_{F407}^{\,2}}{\left(-k_{F407}\right)\left(k_{F407} + k_{F412}\right)} \tag{A.46}$$

$$k_{F421} = k_{F414}k_{F420} + \frac{k_{F415}k_{F417}}{k_{F412}} + \frac{k_{F407}k_{F416}}{k_{F412}} \quad \text{(A.47)}$$

$$k_{F422} = k_{F414}k_{F418} \quad \text{(A.48)}$$

$$k_{F423} = k_{F414}k_{F419} + k_{F415}\left(\frac{k_{F412} - k_{F417}}{k_{F412}}\right) + k_{F416}\left(\frac{k_{F412} - k_{F407}}{k_{F412}}\right) \quad \text{(A.49)}$$

$$k_{F424} = \frac{k_{F405}k_{F422}}{k_{F407}} \quad \text{(A.50)}$$

$$k_{F425} = k_{F405}k_{F421} + k_{F406} - \frac{k_{F405}k_{F422}}{k_{F407}} + \frac{k_{F405}k_{F423}k_{F407}}{k_{F407} - k_{F412}} \quad \text{(A.51)}$$

$$k_{F426} = \frac{k_{F405}k_{F423}k_{F412}}{k_{F412} - k_{F407}} \quad \text{(A.52)}$$

Stage 4, $i_{D\text{-}Si}$ (t) = 0:

k_{F401} - k_{F411}, k_{F416}, $k_{F418} - k_{F420}$ and $k_{F424} - k_{F426}$ are defined as when $i_{D\text{-}Si}$ (t) > 0.

$$k_{F412} = \frac{C_{DS-GaN}k_{F401}k_{F407} - C_{oss-Si}k_{F307} + k_{F310}}{k_{F311}} \quad \text{(A.53)}$$

$$k_{F421} = k_{F403}C_{DS-GaN}k_{F420} + \frac{k_{F416}k_{F407}}{k_{F412}} \quad \text{(A.54)}$$

$$k_{F422} = k_{F403}C_{DS-GaN}k_{F418} \quad \text{(A.55)}$$

$$k_{F423} = k_{F403}C_{DS-GaN}k_{F419} + C_{GD-Si}k_{F406} + \frac{k_{F416}\left(k_{F412} - k_{F407}\right)}{k_{F412}} \quad \text{(A.56)}$$

Turn-on

Stage 2:

$$k_{N201} = -\frac{C_{oss-Si} + g_{m-Si}R_GC_{GD-Si}}{R_G\left(C_{GD-Si}^{\ 2} - C_{oss-Si}C_{iss-Si}\right)} \quad \text{(A.57)}$$

$$k_{N202} = -\frac{C_{oss-Si} + g_{m-Si}R_GC_{GD-Si}}{V_{DD}C_{oss-Si} + g_{m-Si}V_{TH-Si}R_GC_{GD-Si}} \quad \text{(A.58)}$$

$$k_{N203} = \left(\frac{C_{iss}}{C_{GD-Si}} - \frac{1}{k_{N201} R_G C_{GD-Si}} \right) \left(v_{GS-Si}\left(t_{1-ON}\right) + k_{N202} \right) \tag{A.59}$$

$$k_{N204} = -\left(\frac{k_{N202} + V_{DD}}{R_G C_{GD-Si}} \right) \tag{A.60}$$

Stage 3:

$$k_{N304} = k_{F304} \tag{A.61}$$

$$k_{N306} = k_{F305} \tag{A.62}$$

$$k_{N307} = \frac{V_{DD}}{R_G C_{iss-Si}} \tag{A.63}$$

$$k_{N308} = \frac{-C_{GD-Si} v_{DS-Si}\left(t_{2-ON}\right) + C_{iss-Si} v_{GS-Si}\left(t_{2-ON}\right)}{C_{iss-Si}} \tag{A.64}$$

$$k_{N309} = C_{oss-Si} + C_{DS-GaN} \tag{A.65}$$

$$k_{N310} = g_{m-Si} V_{TH-Si} - g_{m-GaN} V_{TH-GaN} \tag{A.66}$$

$$k_{N311} = k_{N309} v_{DS-Si}\left(t_{2-ON}\right) - C_{GD-Si} v_{GS-Si}\left(t_{2-ON}\right) \tag{A.67}$$

$$k_{N312} = k_{N309} - C_{GD-Si} k_{N306} \tag{A.68}$$

$$k_{N313} = \frac{k_{N304} k_{N309} + g_{m-GaN} + g_{m-Si} k_{N306}}{k_{N312}} \tag{A.69}$$

$$k_{N314} = \frac{g_{m-GaN} k_{N304}}{k_{N312}} \tag{A.70}$$

$$k_{N315} = -\left(\frac{-k_{N313} + \sqrt{{k_{N313}}^2 - 4k_{N314}}}{2} \right) \tag{A.71}$$

$$k_{N316} = -\left(\frac{-k_{N313} - \sqrt{{k_{N313}}^2 - 4k_{N314}}}{2} \right) \tag{A.72}$$

$$k_{N317} = -\frac{g_{m-Si}}{C_{GD-Si}} \tag{A.73}$$

$$k_{N320} = \frac{k_{N307} C_{GD-Si} k_{N317}}{k_{N312} k_{N315} k_{N316}} + \frac{k_{N310} k_{N304}}{k_{N312} k_{N315} k_{N316}} \tag{A.74}$$

$$k_{N321} = \frac{k_{N307} C_{GD-Si} \left(k_{N317} - k_{N315}\right)}{k_{N312} k_{N315} \left(k_{N315} - k_{N316}\right)} + \frac{k_{N308} C_{GD-Si} \left(k_{N315} - k_{N317}\right)}{k_{N312} \left(k_{N315} - k_{N316}\right)}$$

$$+ \frac{k_{N310} \left(k_{N304} - k_{N315}\right)}{k_{N312} k_{N315} \left(k_{N315} - k_{N316}\right)} + \frac{k_{N311} \left(k_{N315} - k_{N304}\right)}{k_{N312} \left(k_{N315} - k_{N316}\right)} \tag{A.75}$$

$$k_{N322} = \frac{k_{N307} C_{GD-Si} \left(k_{N316} - k_{N317}\right)}{k_{N312} k_{N316} \left(k_{N315} - k_{N316}\right)} + \frac{k_{N308} C_{GD-Si} \left(k_{N317} - k_{N316}\right)}{k_{N312} \left(k_{N315} - k_{N316}\right)}$$

$$+ \frac{k_{N310} \left(k_{N316} - k_{N304}\right)}{k_{N312} k_{N316} \left(k_{N315} - k_{N316}\right)} + \frac{k_{N311} \left(k_{N304} - k_{N316}\right)}{k_{N312} \left(k_{N315} - k_{N316}\right)} \tag{A.76}$$

$$k_{N323} = \frac{k_{N307}}{k_{N304}} \tag{A.77}$$

$$k_{N324} = \frac{k_{N306} k_{N321} k_{N315}}{k_{N315} - k_{N304}} \tag{A.78}$$

$$k_{N325} = \frac{k_{N306} k_{N322} k_{N316}}{k_{N316} - k_{N304}} \tag{A.79}$$

$$k_{N326} = k_{N306} k_{N320} + \frac{k_{N306} k_{N321} k_{N304}}{k_{N304} - k_{N315}} + \frac{k_{N306} k_{N322} k_{N304}}{k_{N304} - k_{N316}} - \frac{k_{N307}}{k_{N304}} + k_{N308} \tag{A.80}$$

Stage 4:

$$k_{N401} = k_{F301} \tag{A.81}$$

$$k_{N402} = -\frac{g_{m-GaN}}{C_{GD-GaN} + C_D} \tag{A.82}$$

$$k_{N403} = -k_{N401} \frac{g_{m-GaN} V_{TH-GaN} + I_L}{C_{GD-GaN} + C_D} \tag{A.83}$$

$k_{N404} - k_{N408}$ are equal to $k_{N304} - k_{N308}$ respectively.

$$k_{N409} = C_{oss-Si} \tag{A.84}$$

$$k_{N410} = k_{N310} \tag{A.85}$$

$$k_{N411} = k_{N409} v_{DS-Si}\left(t_{3-ON}\right) - C_{GD-Si} v_{GS-Si}\left(t_{3-ON}\right)$$

$$-C_{DS-GaN} v_{DS-GaN}\left(t_{3-ON}\right) \tag{A.86}$$

$$k_{N412} = k_{N409} - k_{N406} C_{GD-Si} - C_{DS-GaN} k_{N401} \tag{A.87}$$

$$k_{N413} = \frac{k_{N404} k_{N409} + g_{m-GaN} + k_{N406} g_{m-Si} - C_{DS-GaN} k_{N401}\left(k_{N402} + k_{N404}\right)}{k_{N412}} \tag{A.88}$$

$$k_{N414} = \frac{k_{N404} g_{m-GaN} - C_{DS-GaN} k_{N401} k_{N402} k_{N404}}{k_{N412}} \tag{A.89}$$

$$k_{N415} = -\left(\frac{-k_{N413} + \sqrt{{k_{N413}}^2 - 4k_{N414}}}{2}\right) \tag{A.90}$$

$$k_{N416} = -\left(\frac{-k_{N413} - \sqrt{{k_{N413}}^2 - 4k_{N414}}}{2}\right) \tag{A.91}$$

$$k_{N417} = k_{N317} \tag{A.92}$$

$$k_{N418} = k_{N403} C_{DS-GaN} + k_{N410} \tag{A.93}$$

$$k_{N419} = C_{DS-GaN}\left(v_{DS-GaN}\left(t_{3-ON}\right) - k_{N401} v_{DS-Si}\left(t_{3-ON}\right)\right) + k_{N411} \tag{A.94}$$

$$k_{N420} = \frac{k_{N407} C_{GD-Si} k_{N417}}{k_{N412} k_{N415} k_{N416}} + \frac{k_{N418} k_{N404}}{k_{N412} k_{N415} k_{N416}} \tag{A.95}$$

$$k_{N421} = \frac{k_{N407} C_{GD-Si}\left(k_{N417} - k_{N415}\right)}{k_{N412} k_{N415}\left(k_{N415} - k_{N416}\right)} + \frac{k_{N408} C_{GD-Si}\left(k_{N415} - k_{N417}\right)}{k_{N412}\left(k_{N415} - k_{N416}\right)}$$

$$+ \frac{k_{N418}\left(k_{N404} - k_{N415}\right)}{k_{N412} k_{N415}\left(k_{N415} - k_{N416}\right)} + \frac{k_{N419}\left(k_{N415} - k_{N404}\right)}{k_{N312}\left(k_{N415} - k_{N416}\right)} \tag{A.96}$$

$$k_{N422} = \frac{k_{N407} C_{GD-Si} \left(k_{N416} - k_{N417} \right)}{k_{N412} k_{N416} \left(k_{N415} - k_{N416} \right)} + \frac{k_{N408} C_{GD-Si} \left(k_{N417} - k_{N416} \right)}{k_{N412} \left(k_{N415} - k_{N416} \right)}$$

$$+ \frac{k_{N418} \left(k_{N416} - k_{N404} \right)}{k_{N412} k_{N416} \left(k_{N415} - k_{N416} \right)} + \frac{k_{N419} \left(k_{N404} - k_{N416} \right)}{k_{N412} \left(k_{N415} - k_{N416} \right)} \tag{A.97}$$

$k_{N423} - k_{N426}$ are equal to $k_{N323} - k_{N326}$ but substituting the constants k_{N3XX} by k_{N4XX}.

$$k_{N427} = k_{N401} k_{N420} + \frac{k_{N401} k_{N421} k_{N402}}{k_{N415}} + \frac{k_{N401} k_{N402} k_{N422}}{k_{N416}}$$

$$+ v_{DS-GaN} \left(t_{3-ON} \right) - k_{N401} v_{DS-Si} \left(t_{3-ON} \right) \tag{A.98}$$

$$k_{N428} = k_{N401} k_{N402} k_{N420} + k_{N403} \tag{A.99}$$

$$k_{N429} = \frac{k_{N401} k_{N421} \left(k_{N415} - k_{N402} \right)}{k_{N415}} \tag{A.100}$$

$$k_{N430} = \frac{k_{N401} k_{N422} \left(k_{N416} - k_{N402} \right)}{k_{N416}} \tag{A.101}$$

Appendix B

GaN power converter circuit schematics and board layouts

This appendix presents the schematics and board layouts of the developed GaN power converter presented in Chapter 5.

Figure B.1 presents the layout of the full-bridge GaN board. Figure B.2 presents the schematic of the leg driver circuit whilst Figures B.3, B.4, B.5 and B.6 show the respective layouts. Two different layouts were developed for the same schematic to optimise the space utilisation. Figures B.3 and B.5 refers to the top layer view while Figures B.4 and B.6 are the bottom layer view.

Figure B.7 shows the layout of the output filter board.

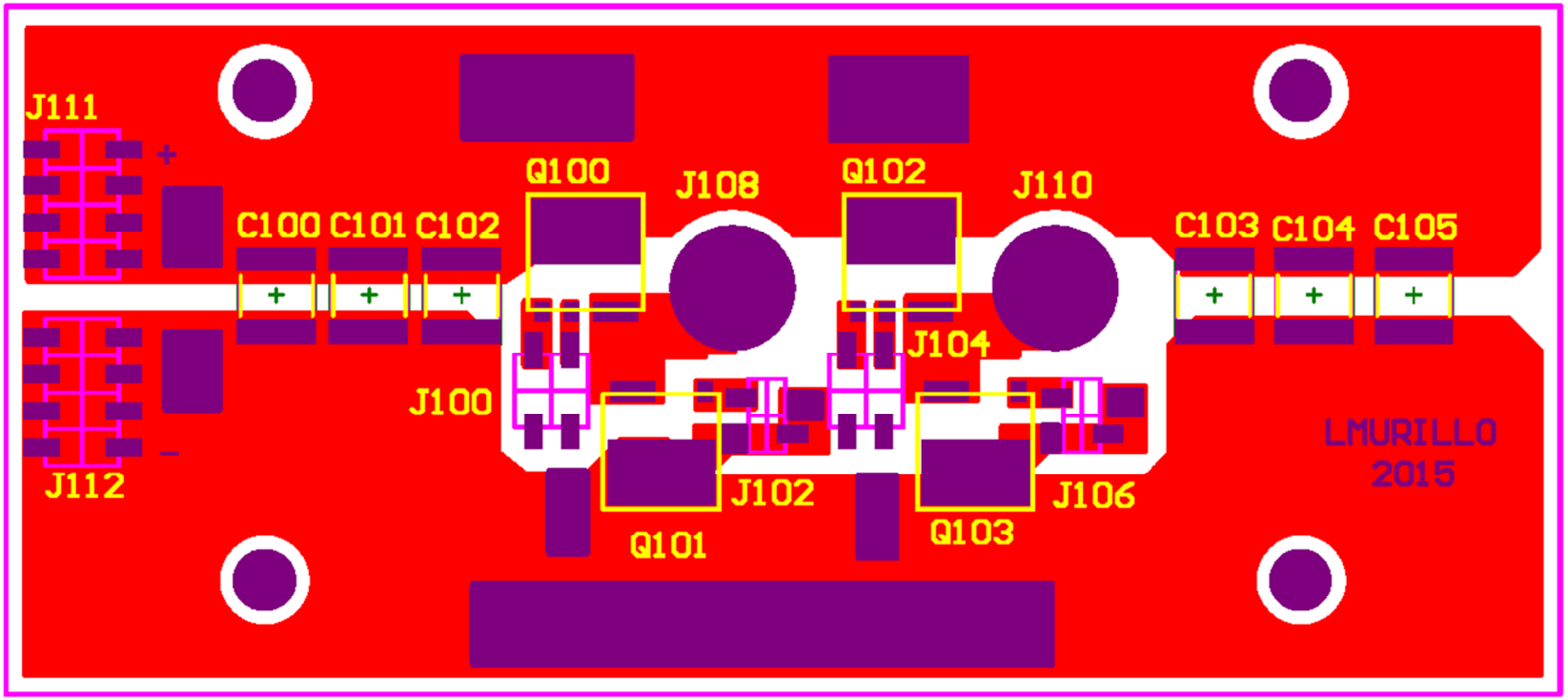

Figure B.1: GaN power converter – full-bridge board layout

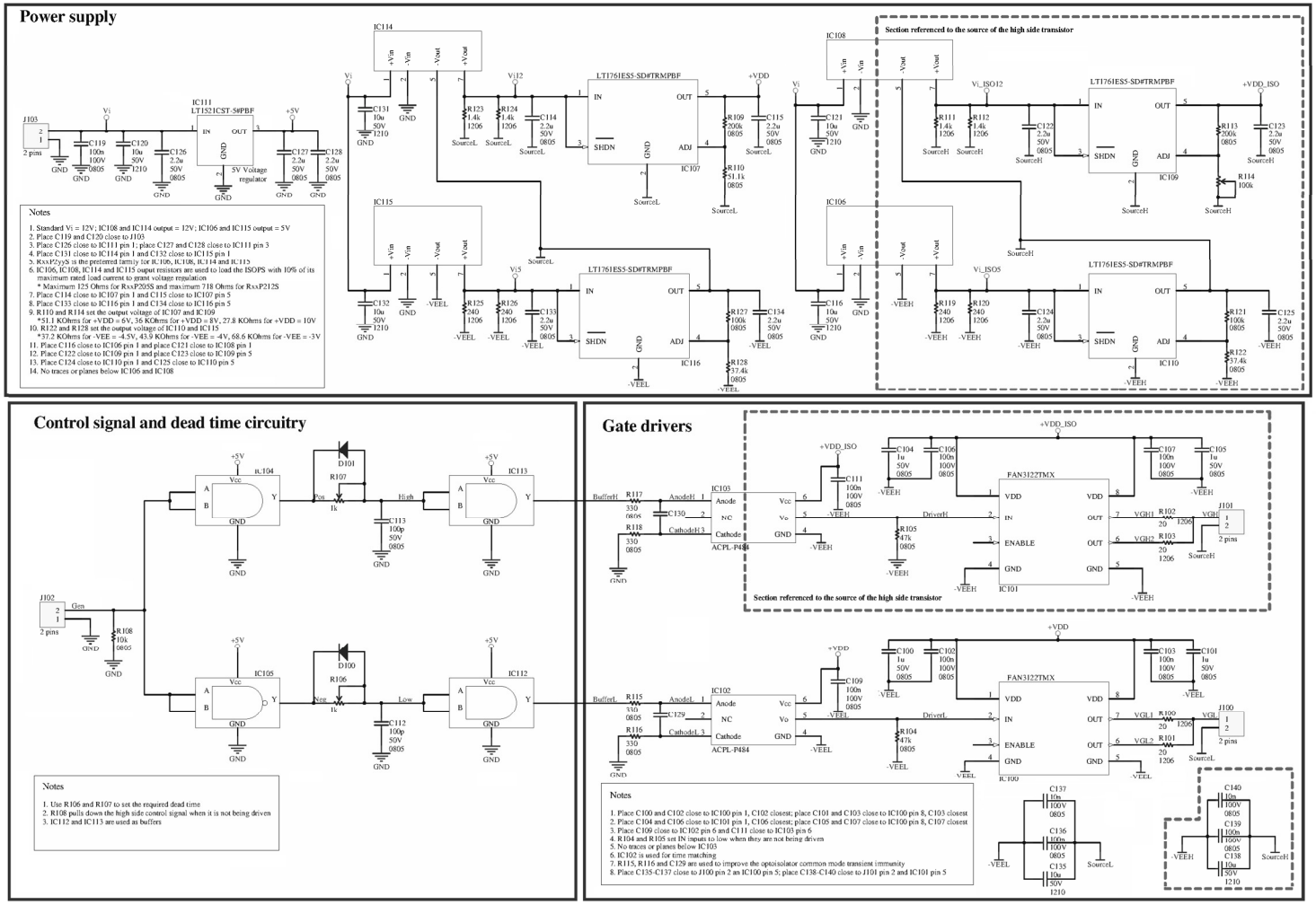

Figure B.2: GaN power converter – leg driver circuit schematic

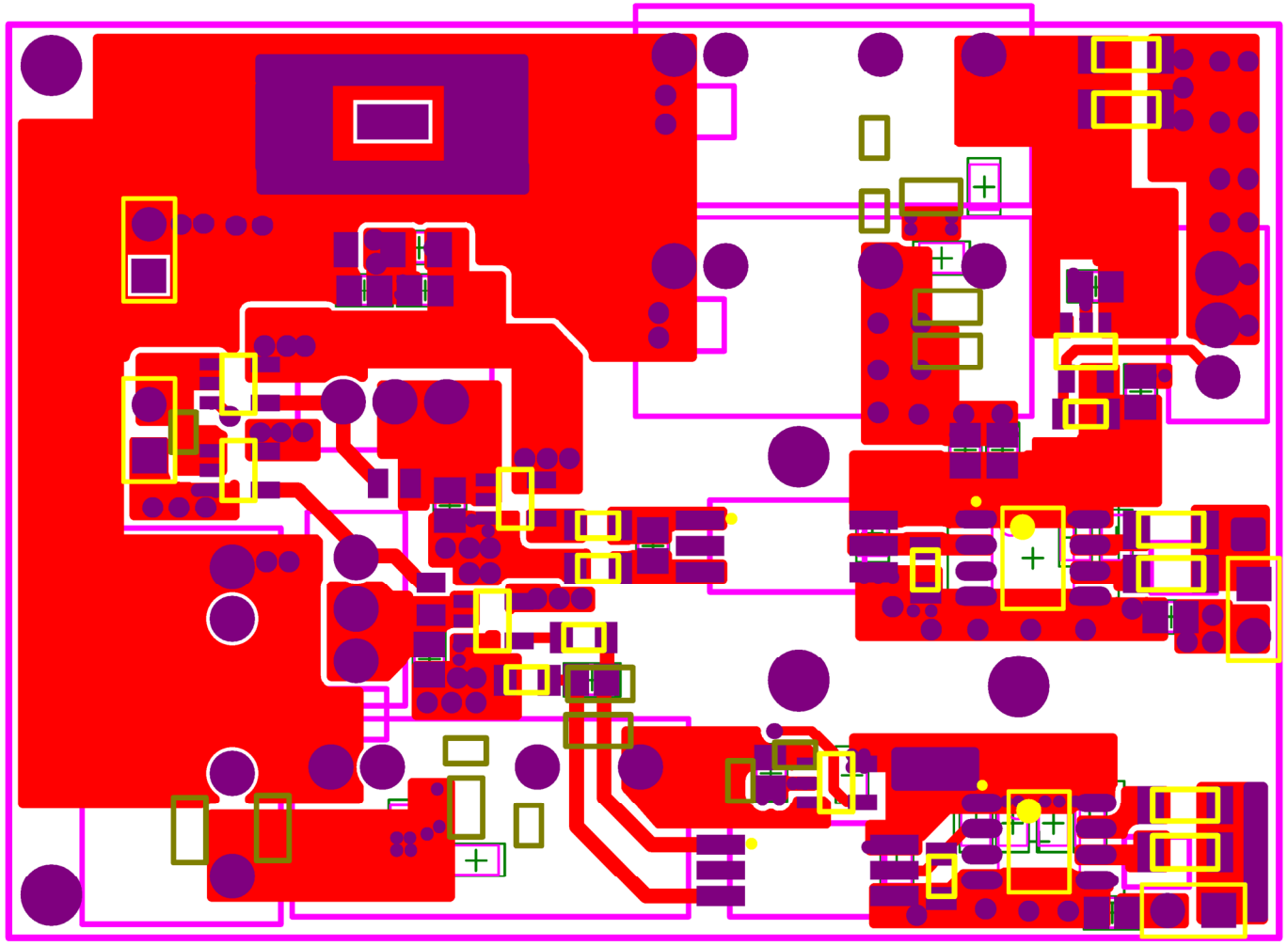

Figure B.3: GaN power converter – leg driver leading leg board layout, top side

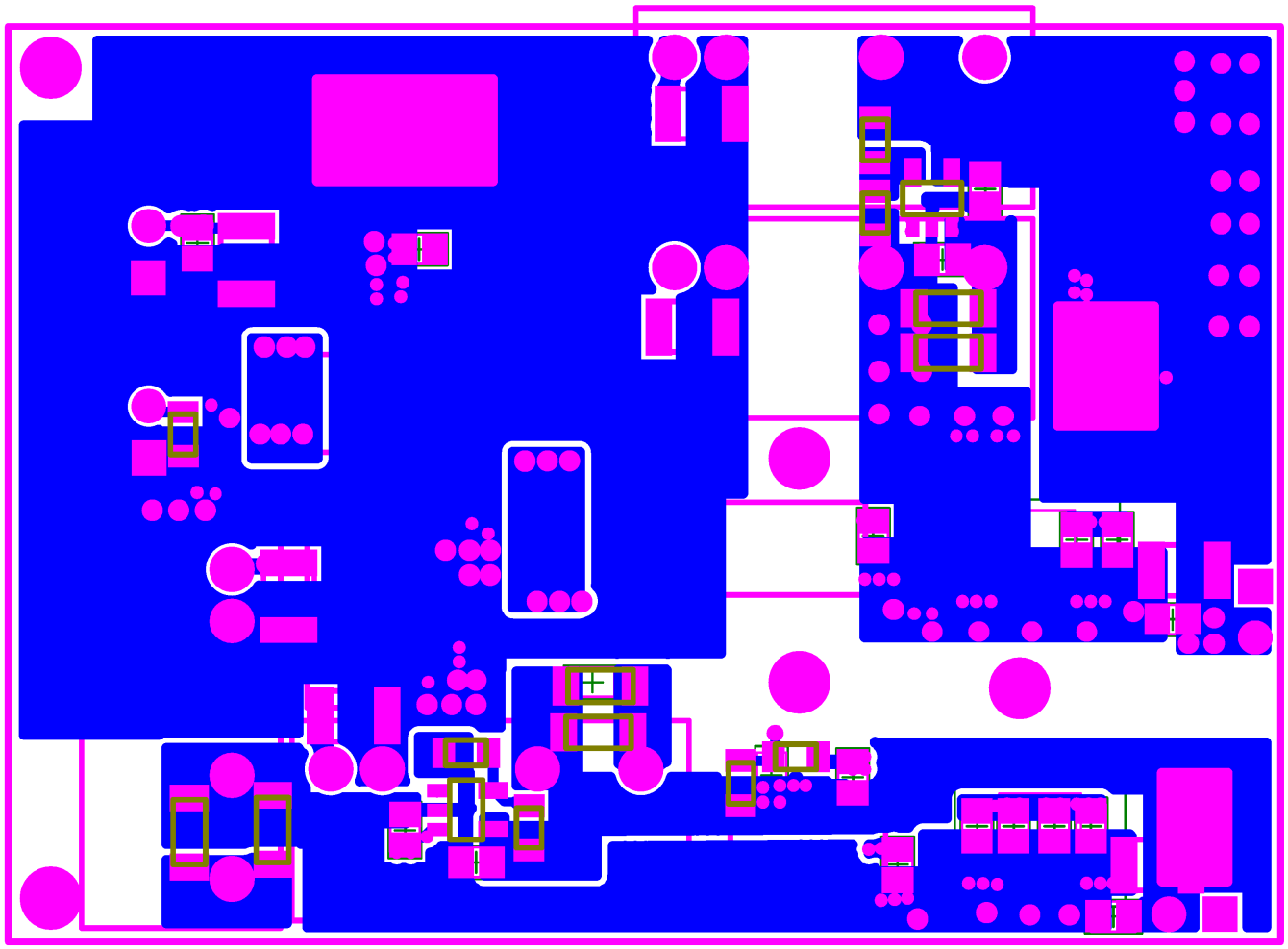

Figure B.4: GaN power converter – leg driver leading leg board layout, bottom side

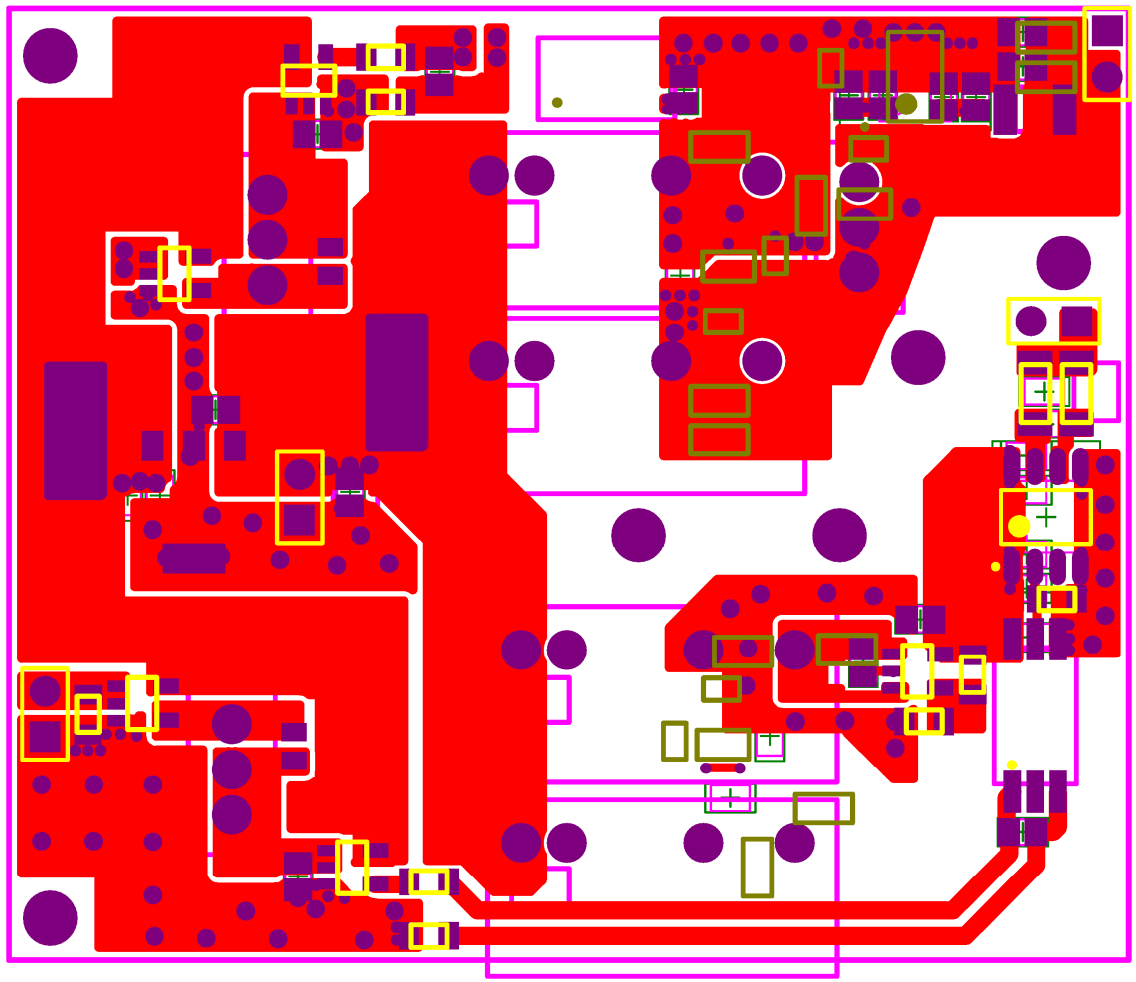

Figure B.5: GaN power converter – leg driver lagging leg board layout, top side

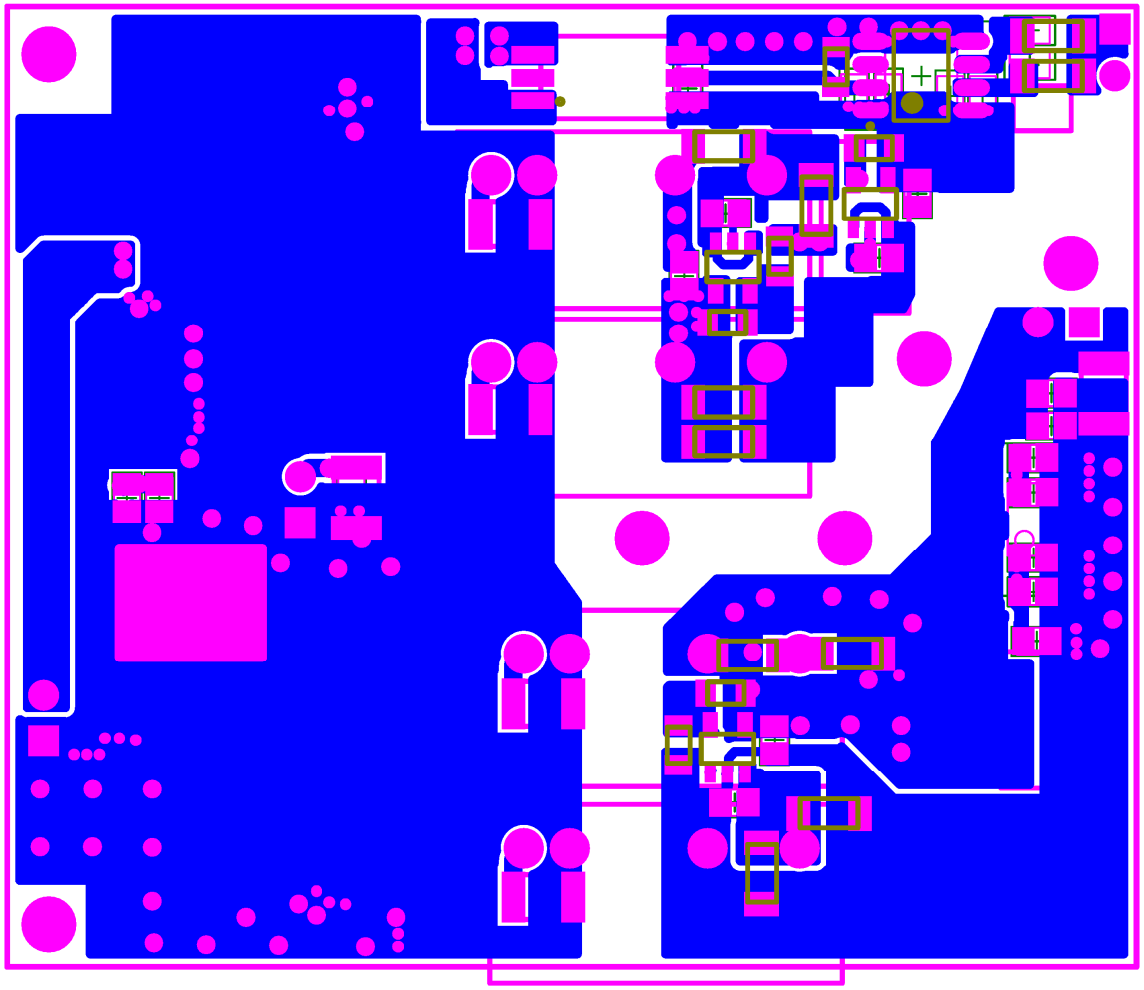

Figure B.6: GaN power converter – leg driver lagging leg board layout, bottom side

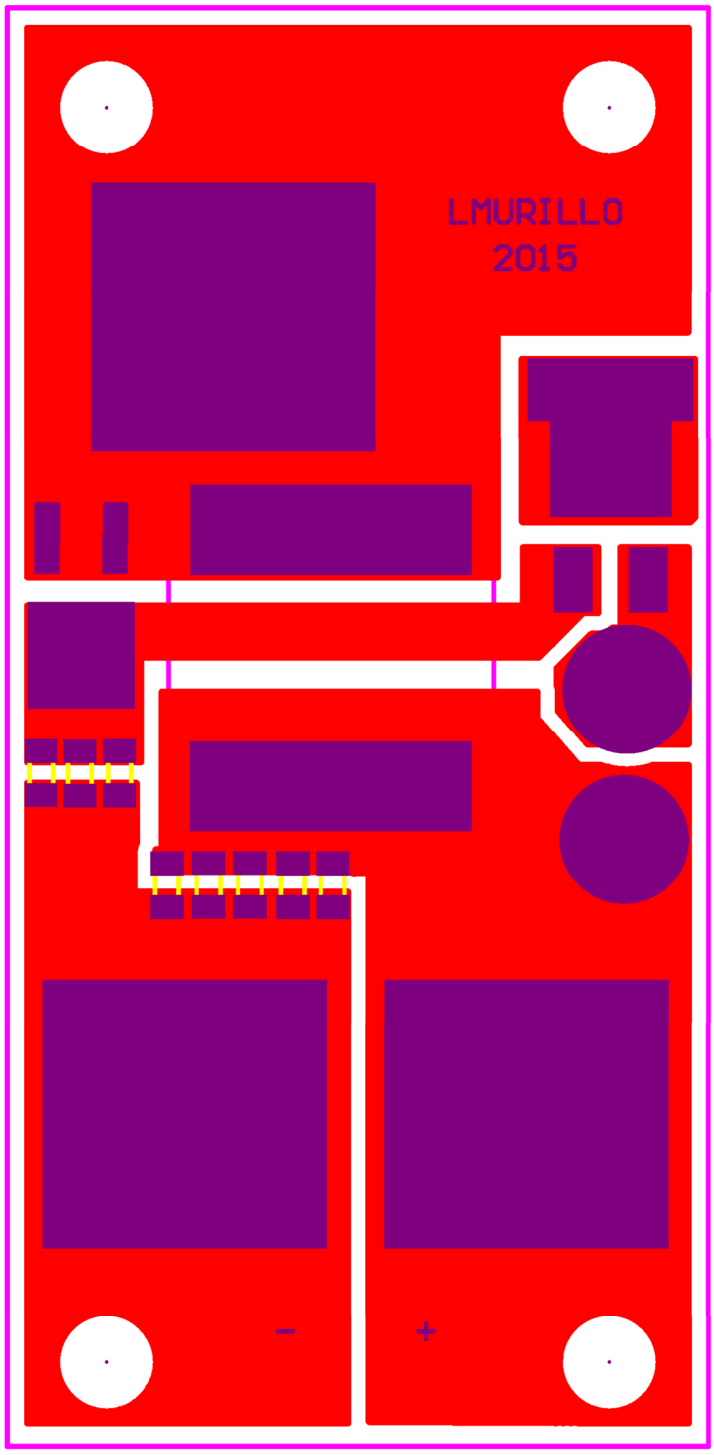

Figure B.7: GaN power converter – output filter board layout