Operation, Control and Stability Analysis of Multi-Terminal VSC-HVDC Systems

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Nomenclature

List of Acronyms

AC	Alternating Current
ACE	Area Control Error
AGC	Automatic Generation Control
ASC	Additive Stabilising Control
AVM	Average-Value Model
AWU	Anti-Windup
BPF	Band-Pass Filter
BW	Bandwidth
DC	Direct Current
DCCB	HVDC Circuit Breaker
DCPSS	Direct Current Power System Stabiliser
DFIG	Double-Fed Induction Generator
DSC	Direct Setpoint Calculation
DSPF	DIgSILENT PowerFactory
EMT	Electromagnetic Transient
FB	Feedback
FF	Feedforward
FRC	Fully Rated Converter
FRT	Fault Ride-Through
GM	Gain Margin
GSC	Grid Side Converter
HVDC	High Voltage Direct Current
IMC	Internal Model Control
INV	Inverter
ISC	Integrator-based Setpoint Control
LA	Lower Arm
LCC	Line Commutated Converter
LHP	Left-Half Plane
MI	Mass Impregnated
MIMO	Multi-Input-Multi-Output
MMC	Modular Multilevel Converter
MPC	Model Predictive Control
MSC	Multiplicative Stabilising Control

MTDC	Multi-Terminal High Voltage Direct Current
OP	Operating Point
OPF	Optimal Power Flow
OPWM	Optimum Pulse-Width Modulation
PCC	Point of Common Coupling
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PLL	Phase-Locked Loop
PM	Phase Margin
PMSG	Permanent Magnet Synchronous Generator
POD	Power Oscillation Damping
PSS	Power System Stabiliser
PWM	Pulse-Width Modulation
REC	Rectifier
RHP	Right-Half Plane
RMS	Root Mean Square
SCR	Short-Circuit Ratio
SIMC	Skogestad Internal Model Control
SISO	Single-Input-Single-Output
SM	Sub-Module
SO	Symmetrical Optimum
SRF	Synchronous Reference Frame
STATCOM	Static Compensator
STFT	Sensitivity Transfer Function Based Tuning
SWF	Simplified Wind Farm Model
TGR	Transient Gain Reduction
TSO	Transmission System Operator
UA	Upper Arm
VCO	Voltage Controlled Oscillator
V-I	Voltage-Current
V-P	Voltage-Power
VSC	Voltage Source Converter
WFC	Wind Farm Side Converter
WTG	Wind Turbine Generator
XLPE	Cross-Linked Polyethylene

List of Symbols

A, B, C, D	State-Space matrices
C	Capacitance
C_0	Equivalent capacitance with a value close to 0
C_c	Cable capacitance
C_{dc}	Equivalent converter capacitance
C_f	Capacitance of the filter at PCC bus
d	Disturbance variable
$e_{(abc)}$	Phase voltages of VSC AC terminal
f	Frequency
$G_d(s)$	Disturbance transfer function
$i_{(abc)}$	VSC phase currents
i_{brake}	DC chopper current
i_{con}	DC current of average-value model
i_d	d-axis current across converter reactor
i_{dc}	DC current into converter
i_q	q-axis current across converter reactor
i_{sd}	d-axis current across the AC system impedance
i_{sq}	q-axis current across the AC system impedance
J	Jacobian matrix
K_d	Derivative gain
K_{droop}	Droop gain of DC voltage droop control
K_i	Integral gain
K_p	Proportional gain
K_t	Anti-windup gain
K_{VQ}	Droop gain of AC voltage droop control
L	Inductance
l	Length of a cable section
L_{arm}	Arm inductance
L_{armdc}	DC side equivalent arm inductance
L_c	Cable inductance
L_{dc}	DC reactance of a DC breaker system
L_s	Equivalent AC system inductance
L_t	Aggregated inductance of AC system, converter transformer and converter reactor
L_T	Transformer inductance

M_s	Frequency domain peak of sensitivity transfer function
M_T	Frequency domain peak of complementary sensitivity transfer function
n	Index of numbers or noise signal
N_p	Number of sub-modules in parallel in each arm
N_s	Number of sub-modules in series in each arm
P	Active power
P_{loss}	Converter loss
Q	Reactive power
R	Resistance
R_{arm}	Arm resistance
R_{armdc}	DC side equivalent arm resistance
R_{brake}	DC braking resistor
R_c	Cable resistance
R_{droop}	Droop constant of DC voltage droop control
R_o	On-State slope resistance of IGBT
R_s	Equivalent AC system resistance
R_t	Aggregated inductance of AC system, converter transformer and converter reactor
R_T	Transformer capacitance
u	Control signal(s)
$v_{(abc)}$	Phase voltages at PCC
v_{ac}	Instantaneous AC voltage
V_{ac}	Steady-State AC voltage
v_d	d-axis component of PCC voltage
V_{dc}	Steady-state DC voltage
v_{dc}	Converter DC voltage
v_{eq}	DC voltage across the equivalent converter capacitor
$v_{l(abc)}$	Lower arm phase voltage
V_o	On-State slope voltage of IGBT
V_{pcc}	Steady-State PCC bus voltage
v_q	q-axis component of PCC voltage
$v_{s(abc)}$	AC source phase voltage
v_{sd}	d-axis AC source voltage
v_{sq}	q-axis AC source voltage
$v_{u(abc)}$	Upper arm phase voltage

X	Reactance
x	State variable
X_s	AC system reactance
Z	Impedance
z	Exogenous output
α	Tuning parameter
δ	Angle of PCC bus voltage
δ_c	Angle of converter AC terminal voltage
ζ	Damping ratio
θ_d	Effective time delay
θ_i	Current measurement delay
θ_m	Reference angle generated by PLL
θ_{pcc}	Angle of PCC bus voltage
λ	Eigenvalue or stored energy constant
τ_{id}	Equivalent time constant of current control loop
τ_m	Time constant of measurement filter
τ_v	Equivalent time constant of VSC modulation control
ϕ	Right eigenvector
ψ	Left eigenvector
ω	Frequency
ω_B	Closed-Loop bandwidth, defined as the frequency where $\|S(j\omega)\|$ crosses 0.707 from below
ω_{BT}	The highest frequency where $\|T(j\omega)\|$ crosses 0.707 from above
ω_d	Desired closed-loop bandwidth
ω_n	Natural frequency
ω_o	Nominal AC system frequency (50 Hz)

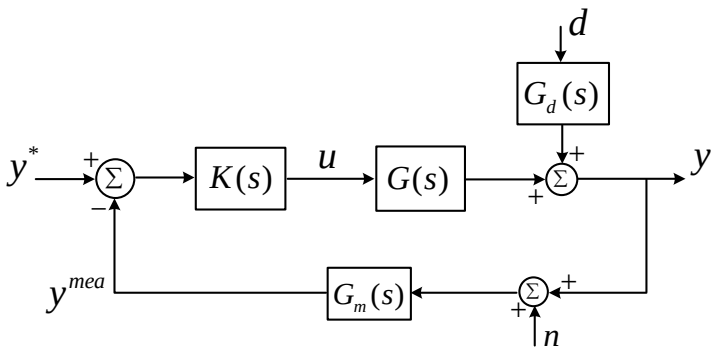
Subscripts

∞	Infinity
AC	AC system quantity
av	Average
base	Base values
c	Converter or cable
con	Converter
cond	Conduction
d	d-axis
dc	DC system quantity
des	Desired
eq	Equivalent
f	Filter
G	DC grid network
H	Higher reference
i	Integral, or index value (where *i*=1,2,3 …)
id	d-axis current control
in	Input
iq	q-axis current control
j	Index value, where *j*=1,2,3 …
L	Lower reference
lim_L	Lower limit
lim_H	Higher limit
m	Measurement, or index value (where *j*=1,2,3 …)
max	Maximum
min	Minimum
o	Operating point or output
P	Active power
pll	Phase-Locked loop
pss	DC damping control
Q	Reactive power
q	q-axis
r	Reference
rated	Rated
red	Reduced

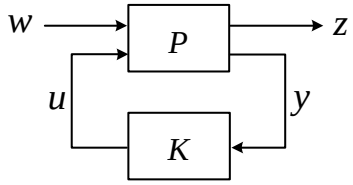
s	AC system or supplementary
SM	Sub-Module
sp	Specified
T	Transformer or transient
tr	Transform
wf	Wind farm

Superscripts

-	Negative
*	Control setpoint
+	Positive
id	d-axis current control
iq	q-axis current control
LA	Lower arm
line	Line
mea	Measured value
P	Active power control
pu	Per unit
pll	Phase-locked loop
Q	Reactive power control
ref	Reference
UA	Upper arm
vac	AC voltage control
vdc	DC voltage control



Classical control system



Generalised multivariable control system [1]

List of Symbols for Control Studies

$G(s)$	System plant model
$K(s)$	Controller model
$L(s)$	Loop transfer function $L(s)=G(s)\cdot K(s)$
$T(s)$	Complementary sensitivity transfer function $T(s) = [I+G(s)K(s)]^{-1}G(s)K(s)$
$S(s)$	Sensitivity transfer function $S(s) = [I+G(s)K(s)]^{-1}$
$G_d(s)$	Disturbance model
$G_dS(s)$	Closed-Loop disturbance model $G_dS(s)=G_d(s)\cdot S(s)$
u	Control input(s)
y	Plant output(s)
r or y^*	Reference(s)/Set-point(s)
d	Disturbance(s)
y^{mea}	Measured output(s)
P	Generalised plant model, including G and G_d
w	Exogenous inputs
z	Exogenous outputs
n	Noise

Abstract

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Voltage source converter high voltage direct current (VSC-HVDC) technology has become increasingly cost-effective and technically feasible in recent years. It is likely to play a vital role in integrating remotely-located renewable generation and reinforcing existing power systems. Multi-terminal VSC-HVDC (MTDC) systems, with superior reliability, redundancy and flexibility over the conventional point-to-point HVDC, have attracted a great deal of attention globally. MTDC however remains an area where little standardisation has taken place, and a series of challenges need to be fully understood and tackled before moving towards more complex DC grids. This thesis investigates modelling, control and stability of MTDC systems.

DC voltage, which indicates power balance and stability of DC systems, is of paramount importance in MTDC control. Further investigation is required to understand the dynamic and steady-state behaviours of various DC voltage and active power control schemes in previous literature. This work provides a detailed comparative study of modelling and control methodologies of MTDC systems, with a key focus on the control of grid side converters and DC voltage coordination.

A generalised algorithm is proposed to enable MTDC power flow calculations when complex DC voltage control characteristics are employed. Analysis based upon linearised power flow equations and equivalent circuit of droop control is performed to provide further intuitive understanding of the steady-state behaviours of MTDC systems.

Information of key constraints on the stability and robustness of MTDC control systems has been limited. A main focus of this thesis is to examine these potential stability limitations and to increase the understanding of MTDC dynamics. In order to perform comprehensive open-loop and closed-loop stability studies, a systematic procedure is developed for mathematical modelling of MTDC systems. The resulting analytical models and frequency domain tools are employed in this thesis to assess the stability, dynamic performance and robustness of active power and DC voltage control of VSC-HVDC. Limitations imposed by weak AC systems, DC system parameters, converter operating point, controller structure, and controller bandwidth on the closed-loop MTDC stability are identified and investigated in detail. Large DC reactors, which are required by DC breaker systems, are identified in this research to have detrimental effects on the controllability, stability and robustness of MTDC voltage control. This could impose a serious challenge for existing control designs. A DC voltage damping controller is proposed to cope with the transient performance issues caused by the DC reactors. Furthermore, two active stabilising controllers are developed to enhance the controllability and robust stability of DC voltage control in a DC grid.

Declaration

No portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

Copyright Statement

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Chapter 1 Introduction

1.1 Background

The UK is aiming to reach 30% to 45% penetration of renewable energy in all of its energy consumption by 2030 [2, 3]. Offshore wind power generation will play a vital role in helping the UK to achieve this target. According to the Gone Green scenario of the National Grid's Electricity Ten Year Statement [4], a total offshore wind capacity of 35.5 GW may be available by 2030 and this could account for 70% of all the renewable generation by 2030. In any scenario in [4], offshore wind generation is being developed rapidly especially around the North Sea region as Europe is committed to reduce its carbon emission.

High voltage direct current (HVDC) typically becomes the most feasible option for the connection of large offshore wind farms located more than 50 to 100 km from the main onshore grid[1]. One key drawback of using alternating current (AC) transmission for this application is that, a large amount of current has to be used for reactive power flow due to the high cable capacitance and this results in high cost and large power losses. HVDC is likely to be employed for the integration of a majority of the Round 3 wind farms [5]. As shown in Figure 1.1, the UK is planning to build a large number of HVDC links, which are going to play a critical role in interconnecting renewable energy generation, reinforcing the onshore AC system and allowing increased energy trading between the UK and mainland Europe.

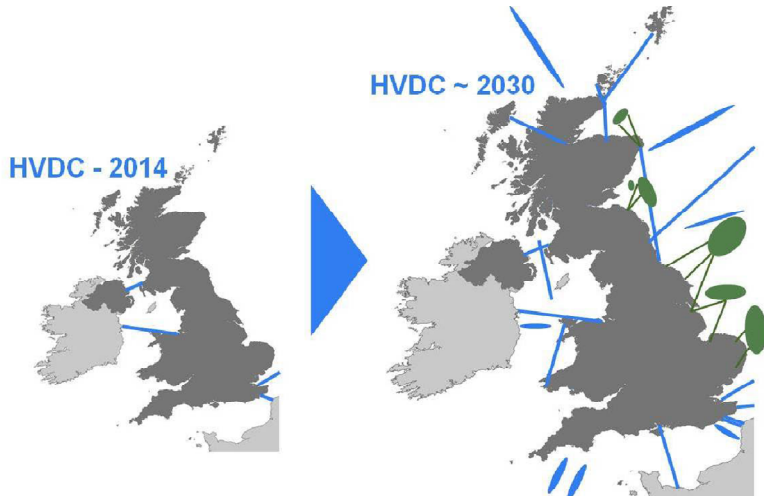

Figure 1.1: HVDC plans from 2014 until 2030 [6] (based on Electricity Ten Year Statement 2013 [7]).

[1] Present consensus is 50 to 100 km. But this number may be conservative as the break-even-distance could be 140 to 200 km for some scenarios.

All the HVDC projects up-to-date are either based upon line commutated converter (LCC) or voltage source converter (VSC). The more conventional LCC-HVDC is primarily used for bulk power transfer over long transmission distances. VSC-HVDC is favoured for offshore wind connection, mainly due to its reduced footprint, its capability to support a weak AC system, its black start capability and its ability to use cross-linked polyethylene cable (XLPE), which is low-cost compared with traditional mass impregnated cable. Furthermore, active and reactive power output of a VSC-HVDC system is usually highly controllable and this feature increases its potential in applications of onshore system reinforcement.

A majority of the existing VSC-HVDC links are point-to-point systems. As the number of such systems grows and large wind farms reach multi-GW ratings, a multi-terminal HVDC (MTDC) system where multiple converters are connected to a common DC circuit [8] becomes an attractive solution. This solution offers potential advantages including high reliability, efficient utilisation of converters and cables, economic system reinforcement and flexible energy trading. VSC-HVDC is particularly favoured for MTDC applications since reversal of voltage polarity is not required for change of power flow direction. This DC grid vision has attracted a great deal of attention worldwide.

1.2 Up-to-date VSC-HVDC Technology

Introduced by ABB in 1997, VSC-HVDC has been developed rapidly in recent years. A two-level converter, which typically relies on pulse-width modulation (PWM) to synthesise the AC voltage, was employed by ABB in *HVDC Light* as its first generation. A three-level converter topology was utilised in the second generation of VSC-HVDC to reduce switching losses. The third generation also employed a two-level topology, where ABB's harmonic cancellation switching scheme "Optimum PWM (OPWM)" was employed, to further reduce the converter loss down to 1.8% from an initial 3.7% for the standard PWM switching method [9]. The first planned VSC-HVDC link for offshore wind farm integration, BorWin1, employs this technology.

A modular multilevel converter (MMC) VSC-HVDC topology was used for the first time by Siemens for VSC-HVDC in the Trans Bay Cable project in 2010. Since then, major manufacturers have been focusing on MMC-type converters. The use of MMC reduces the converter loss to around 1%, which starts to become comparable to the power loss of LCC-HVDC. Furthermore, a large number of voltage levels can be provided by

switching the sub-modules in the MMC, which results in a significant reduction of harmonics. However, besides its complex modulation scheme [10, 11], the MMC control also has to deal with additional issues, such as the unbalance of the sub-module capacitor voltages [11, 12] and the circulating currents between the converter limbs [13].

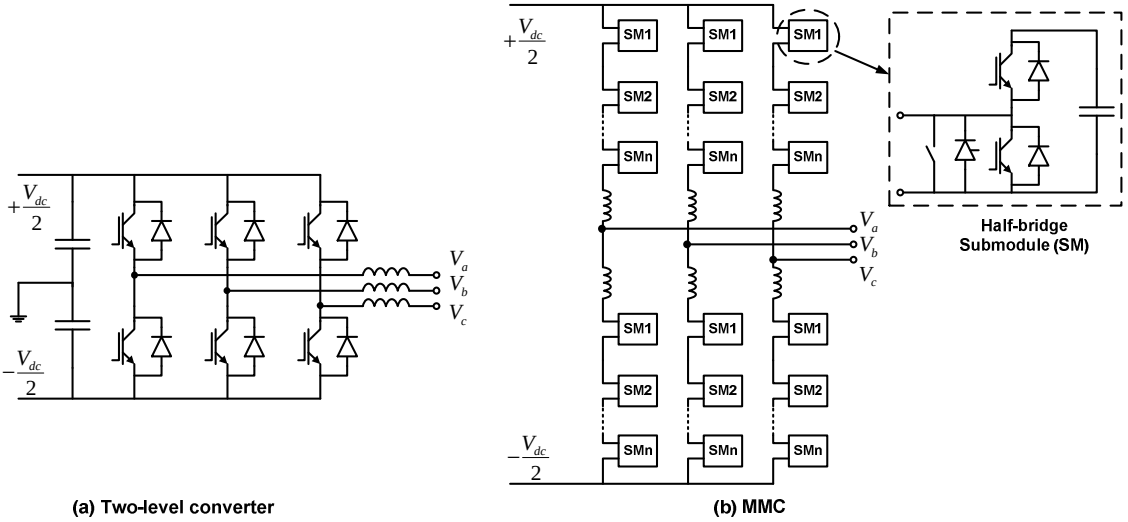

Figure 1.2: Two-Level and MMC converter topologies.

The voltage and power rating of VSC-HVDC have been growing consistently in recent years. There are a number of VSC-HVDC links for offshore wind connection being commissioned this year, including the DolWin1 (±320 kV DC, 800 MW) and DolWin2 (±320 kV DC, 900 MW) links that employ ABB's cascaded-two-level (CTL) converters [14], and BorWin2 (±300 kV DC, 800 MW) and SylWin1 (±320 kV DC, 864 MW) links that use Siemens's MMC technology [15]. Most of the existing VSC-HVDC links have employed a symmetrical monopole topology. The Skagerrak4 HVDC link commissioned in 2014, which is the first VSC-HVDC in bipole arrangement with LCC-HVDC, uses the record-level DC voltage of 500 kV for its VSC [14]. Further research into new converter topologies and steady development of the semiconductor and cable technologies will continue to improve efficiency, functionality and the maximum capacity of VSC-HVDC.

1.3 Multi-Terminal VSC-HVDC

Early investigation into multi-terminal HVDC (MTDC) systems can be dated back to the 1980s [8, 16]. The Phase II Quebec-New England HVDC system, which involves three large-scale LCC converters, was commissioned in 1992 as the first MTDC system in the world [14]. The Nan'ao HVDC project involving China Southern Grid, RXPE, NR Electric and XD Electric, which was initially a three-terminal system and commissioned

in late 2013, is the first MTDC system based upon VSC technology [17]. The Zhoushan five-terminal HVDC with a rated DC voltage of ±200 kV, led by the State Grid of China, was commissioned later in 2014 [18].

A number of potential multi-GW multi-terminal systems are being planned, including the Atlantic Wind Connection in the US [19], the South West Link in Sweden [20], and the Eastern HVDC Link in the UK [2, 6], and the North-East Agra Link in India [14]. The European Supergrid vision based upon VSC technology has been considered by many energy authorities a competitive solution to integrate a large number of diversified renewable energy sources and to enhance the balancing of this renewable generation [21, 22]. Such large-scale DC grids are expected to be developed gradually and modularly by interconnecting point-to-point links and radial-type MTDC systems. The recent breakthrough in HVDC breakers [23-25] started with ABB's proactive hybrid HVDC breaker [23], significantly increases the feasibility and reliability of large HVDC grids with multiple protection zones.

Some coordination work that intends to provide suggestions and specifications for future MTDC systems has been initiated in recent years [22, 26-29]. However, understanding and practical experience of MTDC systems remain limited. MTDC remains an area where little standardisation has taken place, and there are a series of key issues that need to be tackled before moving towards more complex DC grids. These challenges can be mainly categorised into the following aspects: control of MTDC and AC/DC systems, DC fault protection schemes, operation and regulation (interoperability between AC/DC TSOs), assessment of techno-economic benefits, etc. [21, 22, 28].

DC voltage, which indicates the power balance and determines the power flow of DC systems, is of paramount importance in MTDC control. The stability of DC voltage ensures the stable operation of the overall DC system. Unlike frequency in AC systems, DC voltage varies at different terminals, which increases the difficulty in controlling the DC voltage and power flow [30]. This feature together with the fact that the frequency range of DC system dynamics is usually much faster than that of AC systems imply that the DC voltage regulation could be quite challenging. MTDC control has so far attracted a great deal of interest. Limited information however exists to provide a systematic description of the plant models and controller designs for MTDC studies. A variety of MTDC control strategies have been introduced in the previous literature, but, further

investigation is required to understand the implementations, dynamic performance and limitations of these control schemes.

The utilisation of various DC voltage and active power control characteristics could significantly increase the complexity of power flow in DC grids. New algorithms are required to provide power flow solutions in this case. Further analysis is required to assess the impact of droop control on quasi-steady-state behaviours of MTDC systems, and to understand the sharing of unbalanced power between converters. Moreover, the structure and operation of the HVDC grid controller, which is used to achieve desired operating point by adjusting converter control references, remain unclear.

The stability, performance and robustness of key VSC control designs, particularly active power control and DC voltage control have not been previously assessed using detailed analytical models. The previous literature tends to oversimplify AC and DC side dynamics for stability analysis, which can lead to some of the key dynamic limitations to be neglected. The constraints imposed by system plant, operating point and controller designs on the closed-loop behaviours of active power and DC voltage control need to be identified and analysed.

DC voltage control in MTDC systems is in fact a complex multi-variable problem. Analysing the MTDC stability under various system and control configurations requires a generalised and detailed mathematical model. Classical analytical tools, such as frequency-response analysis, can be employed to provide intuitive insight into the key constraints imposed on the MTDC stability and robustness. Previous research work considering the overall DC system dynamics has been limited, and further investigation is needed to improve the understanding of MTDC transients. The impact of new components, such as the DC breaker system, on the MTDC stability needs to be addressed. New controllers may be required in some scenarios to achieve DC voltage stability and satisfactory transient performance.

1.4 Project Objectives

The objectives of this project can be summarised as follows:

- To investigate and evaluate VSC-HVDC control strategies including both local converter control and MTDC control.
- To investigate the quasi-steady-state behaviours of MTDC system and perform detailed power flow analysis.
- To develop dynamic MTDC models in DIgSILENT PowerFactory (DSPF) suitable for MTDC transient stability studies.
- To identify the key limitations imposed on the stability of the local VSC-HVDC system.
- To investigate the key constraints imposed on the stability of the MTDC system.
- To develop new controllers to improve the stability of the MTDC systems.

1.5 Main Contributions of the Thesis

The main contributions of this thesis are:

- Systematic modelling, control implementation and controller tuning for an MTDC system have been developed. The modelling and dynamic studies in this thesis have focused on the low-frequency stability of MTDC systems below 50 Hz. Key features and weaknesses of various types of DC voltage control characteristics have been identified.
- A new generalised algorithm containing two layers of iteration loops has been developed to enable the power flow calculation for MTDC systems where various DC voltage characteristics are employed. A linearised power flow analysis has also been performed.
- An equivalent circuit of droop control has been developed to provide an intuitive assessment of the impact of droop settings and network impedances on the quasi-steady-state variations of MTDC system.
- A detailed comparative study has been performed to assess the stability of two leading active power control schemes.
- The limitations imposed by the AC system strength, the converter operating point and the current loop bandwidth on the active power loop have been evaluated. This leads to a recommendation for active power control design.

- A generalised and systematic procedure has been developed for the mathematical modelling of MTDC systems, capturing the key dynamics of the converter system and the DC network.
- A participation factor analysis and sensitivity studies based upon modal analysis have been conducted to investigate the impact of the plant and controller parameters on the MTDC stability and dynamics.
- Key stability limitations imposed by rectifier operation, weak AC systems (without considering resonance effects) and constant power control on the stability of DC voltage control, particularly the voltage-power droop control, have been identified using frequency-response analysis.
- A droop controller with transient compensation has been proposed to enhance its robust stability.
- Control implementation and parameterisation issues associated with voltage-current droop control have been identified.
- Stability, robustness and dynamic performance issues imposed by the use of large DC reactors, which are required by HVDC circuit breakers, have been identified through frequency domain analysis and time domain simulations.
- A new damping controller has been proposed to enhance the dynamic performance of the DC voltage control in a DC grid. Two methods have been proposed to select the location of this DC damping controller.
- Two active stabilising controllers have been developed to reduce the impact of power flow variation on the MTDC stability and to improve the controllability of the system.

1.6 Outline of the Thesis

This thesis has eight chapters in total. The seven chapters which follow the introduction are outlined as:

Chapter 2 – Modelling and Control of MTDC

This chapter presents a methodology for modelling, controller implementation and control tuning of VSC-HVDC system, with a key focus on the control of grid side converters and DC voltage coordination. Dynamics and control design methods for the inner and outer control loops of VSC-HVDC are discussed. DC voltage control strategies for MTDC systems, including voltage margin control and voltage droop control, are discussed in detail.

Chapter 3 – Steady-state Analysis of MTDC

In this chapter, a generalised DC power flow algorithm is proposed for the calculation of the MTDC steady-state operation when complex DC voltage characteristics are employed. This is followed by the linear analysis and the development of the equivalent circuit for droop control to provide a clear understanding of the power flow variation. A possible MTDC control hierarchy containing multiple control stages is also presented.

Chapter 4 – Analysis of Active Power Control of VSC-HVDC

This chapter provides a comprehensive analysis of the dynamic behaviours of active power control of VSC-HVDC systems, focusing on the key limitations imposed by VSC plant models and control designs. Mathematical models of the closed-loop systems are derived for two main controller structures. Key factors which impact on the power loop stability are identified using frequency domain tools and cross-verified by time domain simulations.

Chapter 5 – Small-Signal Modelling of VSC-MTDC

This chapter presents a generalised methodology for analytical modelling of MTDC systems. The mathematical models for the grid side converter, wind farm side converter and DC network are presented. The modelling technique which is used to interconnect the sub-systems to formulate the MTDC model is described. Participation factor analysis is applied to identify the key variables which affect the modes of interest. Following this, sensitivity studies with respect to a number of system and control parameters are performed.

Chapter 6 – Stability Analysis of DC Voltage Control of VSC-HVDC

This chapter provides the stability analysis of DC voltage control, particularly voltage droop control, considering detailed converter dynamics and simplified AC/DC system dynamics. Key constraints imposed by AC and DC systems on the DC voltage stability are identified. A compensator-based droop controller is developed to improve the robust stability of voltage droop control. Controller parameterisation issues related to voltage-current droop are also briefly discussed. The viability of using a feedforward of DC power for a DC voltage controller is assessed.

Chapter 7 – Impact of DC Reactor on MTDC Stability and Damping Enhancement

In this chapter, stability and dynamic performance problems caused by the DC breaker system are investigated in detail by analysing poles, zeros and frequency responses. A new DC voltage damping controller is introduced to improve the dynamic performance of MTDC systems with large DC reactors. Furthermore, two active stabilising controllers are suggested to enhance the controllability and robustness of DC voltage control in a DC grid.

Chapter 8 – Conclusion and Future Work

The main conclusions of this research are summarised in this chapter. Suggestions for future research are provided to improve the work presented in this thesis.

1.7 List of Publications

Journal Papers:

1. W. Wang and M. Barnes, "Power Flow Algorithms for Multi-Terminal VSC-HVDC With Droop Control," *IEEE Trans. Power Syst.*, vol. 29, pp. 1721-1730, 2014.
2. W. Wang, A. Beddard, M. Barnes, and O. Marjanovic, "Analysis of Active Power Control for VSC-HVDC," *IEEE Trans. Power Del.*, vol. 29, pp. 1978-1988, 2014.
3. W. Wang, M. Barnes, O. Marjanovic, and O. Cwikowski, "Impact of DC Breaker Systems on Multi-terminal VSC-HVDC Stability," *accepted by IEEE Trans. Power Del.*, 2015.

Conference Papers:

1. W. Wang, M. Barnes, and O. Marjanovic, "Droop control modelling and analysis of multi-terminal VSC-HVDC for offshore wind farms," in *Proc. IET 10th Int. Conf. AC-DC Power Transmission*, Birmingham, UK, 2012.
2. W. Wang, M. Barnes, and O. Marjanovic, "The impact of control design on dynamic behaviour of multi-terminal VSC-HVDC (MTDC) system under AC grid fault conditions," in *Proc. IET 7th Int. Conf. Power Electron., Machines and Drives*, Manchester, UK, 2014.
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4. L. Shen, W. Wang, and M. Barnes, "The influence of MTDC control on DC power flow and AC system dynamic responses," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, Washington D.C., 2014.
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Chapter 2 Modelling and Control of MTDC

This chapter provides a generic study of modelling and control of MTDC systems, with a key focus on control of grid side VSC-HVDC and DC voltage coordination. All the following chapters will be based on further analysis and in-depth study of the fundamental modelling and control approaches introduced in this chapter.

The software used throughout is either DIgSILENT PowerFactory (DSPF), a power system simulation tool, or MATLAB, which is used for analyses of mathematical models.

There has been a great deal of interest into control of MTDC systems. However, limited literature exists to provide systematic plant model derivations and controller design principles. Furthermore, various DC voltage regulation methods and their dynamic implementations require more detailed investigation.

This chapter is organised as follows. Firstly, an overview of a hierarchical control system for grid side converters is presented and an average-value converter model is briefly introduced. This is followed by a detailed study on the vector current loop and its tuning. Key dynamics and controller design methods for multiple control systems including the phase-locked loop, active and reactive power control, and AC voltage control are discussed. The second section of this chapter addresses techniques for modelling of a simplified wind farm system, control of a wind farm side VSC, and fault-ride through control. Finally, DC voltage control techniques for MTDC systems, including DC slack bus control, voltage margin control and voltage droop control, are introduced, with a comparative simulation study provided in Section 2.3.

2.1 Modelling and Control of Grid Side VSC-HVDC

In a HVDC grid, grid side converter (GSC) stations are expected to maintain the stability of the DC system, achieve the desired amount of power transfer, provide AC system support, and fulfil various aspects of the grid code requirements from both AC and DC transmission system operators (TSOs). From the perspective of DC grid control, the controllability of the wind farm converters (WFC) is relatively low, therefore, steady-state and transient behaviours of the DC system will be predominantly affected by GSCs. The modelling and analysis of the hierarchical GSC control system that forms the foundation of this thesis is presented in this section. Firstly, the overall cascaded control

structure is briefly introduced. This is followed by the discussion regarding the average-value converter model and inner current control. Then modelling and control designs of various outer control loops are then discussed in detail.

2.1.1 Overview of GSC Control

Most of the previous literature appears to adopt one of the following three control methods for GSCs: direct control (power-angle control), vector current control, or power synchronisation control [29, 31]. The principle of direct control is to control reactive power (or AC voltage) and active power (or DC voltage) respectively by adjusting the magnitude and angle of VSC AC terminal voltage. However, this control may have not been implemented in any real VSC-HVDC projects, due to the following two fundamental flaws: it does not have a current limiting capability; and its control bandwidth is limited by various AC resonance frequencies especially the fundamental grid frequency [31, 32]. Thus, power-angle control is not considered here. Vector current control was initially designed for motor drives and has been successfully implemented in a number of commercial VSC-HVDC systems [31]. Active and reactive components of the AC currents are controlled independently in a reference frame created by a phase-locked loop (PLL). A degree of current protection can be provided, and a bandwidth that is much higher than the grid frequency can be employed. Power synchronisation control [33, 34], which could be viewed as a combination of direct control and vector current control to some extent, might be suitable for connections to weak AC systems, but has not been widely utilised so far.

Figure 2.1 describes a generalised cascaded control system for a typical GSC, based upon vector current control. The control structure can be categorised into five layers: voltage modulation control, dq current control, outer loop for the control of AC/DC voltage and active/reactive power, supplementary control, and supervisory control. The switching-based voltage modulation control, which represents the PWM control for a two-level converter or the nearest level control and capacitor balancing control for an MMC, is out of the scope of this thesis, and will not be discussed in detail. The voltage reference for the converter switching control is produced by the current controllers.

A PLL is typically used to track the angle of the voltage vector of the point of common coupling (PCC), in order to achieve an independent active and reactive power control. Consequently, the converter outer controls can be divided into two branches. The active

current reference is supplied by active power control or DC voltage control. The reactive current reference is provided by reactive power control or AC voltage control. Furthermore, DC voltage and AC voltage control can also be achieved by utilising droop-based supplementary signals to modify the converter outer control references. Other supplementary controls, such as frequency support control and power oscillation damping control, can also be integrated by modifying the outer control references.

Some form of distributed DC voltage control is required for a MTDC system; however, the implementation of such control has not been standardised. A supervisory control, which possibly involves a secondary control and a centralised tertiary control, is mainly used to achieve optimal steady-state operation of a DC grid. A telecommunication link between VSC stations and the control centre is necessary to perform this high-level control.

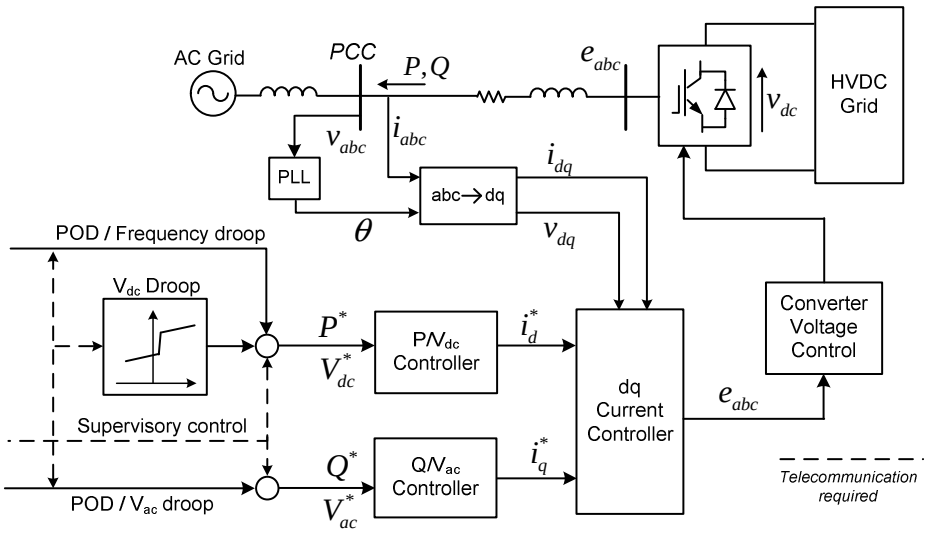


Figure 2.1: Cascaded control structure for VSC-HVDC.

2.1.2 Average-Value Model (AVM)

In power electronic systems, average-value models (AVMs) typically represent the averaged dynamics with switching details neglected [35, 36]. Simulations of detailed MMC or two-level VSC models containing a large number of semiconductor switches require very small time steps (μs) and the large state matrices have to be solved at high frequencies. MTDC system models based upon AVMs are normally able to capture the key transient behaviours and stability issues in low frequency range, but with significantly reduced computation burdens. Furthermore, stability analysis for a VSC-HVDC system is greatly facilitated by employing AVMs. Thus AVMs have been utilised throughout this thesis.

The AVM representation for a two-level pulse-width modulation (PWM) converter has been established and widely used. AVMs have been developed and compared with the detailed model (DM) of a 401-level MMC HVDC system [37-39]. Detailed voltage and current dynamics of submodules (SM) in MMC systems are not explicitly modelled in the AVM. It is assumed in the AVM that the circulating currents are well suppressed and the SM DC voltages are balanced.

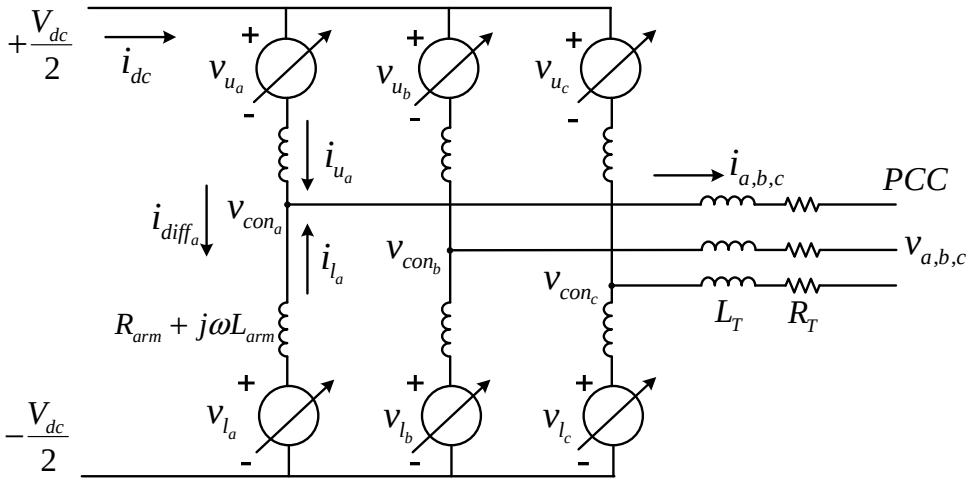


Figure 2.2: AVM representation of MMC AC side.

The MMC AC side can be represented as shown in Figure 2.2, by modelling the converter arms as controlled voltage sources. For each phase leg, both the currents flowing through the upper arm and the lower arm are comprised of a common term and a difference term [10]:

$$i_{u_m} = \frac{i_m}{2} + i_{diff_m},\ i_{l_m} = \frac{i_m}{2} - i_{diff_m},\ m = a,b,c \tag{2.1}$$

where the difference current i_{diff} is comprised of a DC current component $i_{dc}/3$ and a circulating current component between the phase legs. According to equivalent circuit in Figure 2.2, the converter AC terminal voltage can be represented by the upper or lower arm voltage as:

$$\begin{aligned} v_{con_m} &= \frac{V_{dc}}{2} - v_{u_m} - L_{arm}\frac{di_{u_m}}{dt} - R_{arm}i_{u_m} \\ v_{con_m} &= -\frac{V_{dc}}{2} + v_{l_m} - L_{arm}\frac{di_{l_m}}{dt} - R_{arm}i_{l_m} \end{aligned} \tag{2.2}$$

where L_{arm} and R_{arm} represent the arm inductance and resistance respectively. By adding (2.1) and (2.2), the arm voltages and currents can then be eliminated as shown in (2.3), where the internal voltage e_m is defined as (2.4).

$$v_{con_m} = e_m - \frac{L_{arm}}{2}\frac{di_m}{dt} - \frac{R_{arm}}{2} i_m \tag{2.3}$$

$$e_m = \frac{v_{l_m} - v_{u_m}}{2}. \tag{2.4}$$

By incorporating the transformer impedance (R_T+$j\omega L_T$) with (2.3), the dynamics of the current flow between the converter and the PCC bus are derived as:

$$e_m - v_m = L\frac{di_m}{dt} + Ri_m \tag{2.5}$$

where i_m is the phase current flowing into the PCC bus from the VSC, v_m is the phase voltage of the PCC bus, and

$$L = L_T + \frac{L_{arm}}{2},\ R = R_T + \frac{R_{arm}}{2}. \tag{2.6}$$

The reference of the MMC internal voltage e^*_{abc} is used as the manipulated input for the vector current controller.

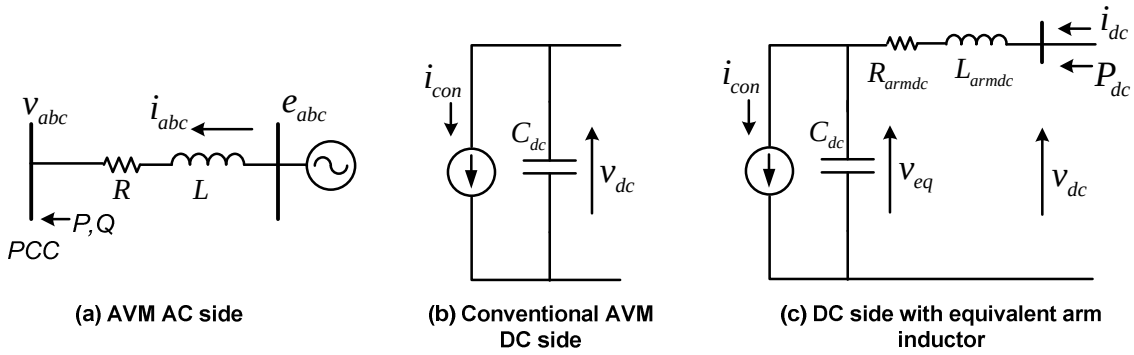


Figure 2.3: Single-Line diagram of the AVM model for MMC[2].

As shown in Figure 2.3(c), a DC current source i_{con} in parallel with an equivalent DC capacitor C_{dc} is used to model the MMC DC side in the AVM presented in [37-39]. The instantaneous DC current i_{con} is calculated according to the active power of the VSC AC side and the DC voltage v_{eq} across the capacitor:

$$i_{con} = \frac{e_a i_a + e_b i_b + e_c i_c}{v_{eq}}. \tag{2.7}$$

According to [40], the total capacitance is typically dimensioned based on a stored energy of 30 to 40 kJ/MVA. Normally, in each phase leg, only half of the submodule capacitors are connected between +V_{dc}/2 and –V_{dc}/2. Therefore, the energy stored in C_{dc}

[2] The positive directions of AC/DC currents and active/reactive power flow used this chapter are defined as shown in this figure.

may only correspond to half of the total energy in the SM capacitors, and accordingly, the equivalent capacitance can be calculated as:

$$\frac{1}{2}C_{dc}V_{dc}^2 = \frac{1}{2}\lambda S_{rated} \Rightarrow C_{dc} = \frac{\lambda S_{rated}}{V_{dc}^2} \tag{2.8}$$

where λ is the stored energy constant in J/MVA, S_{rated} is the MVA rating of the MMC. If the submodule capacitance is known, the equivalent capacitance C_{dc} can be calculated as:

$$\frac{1}{2}C_{dc}V_{dc}^2 = \frac{1}{2}\times 6N_{arm}\cdot\frac{1}{2}C_{SM}\left(\frac{V_{dc}}{N_{arm}}\right)^2 \Rightarrow C_{dc} = \frac{3C_{SM}}{N_{arm}} \tag{2.9}$$

where C_{SM} is the SM capacitance and N_{arm} is the number of SMs in each arm.

However, the equivalent capacitance calculated based on the energy conservation principle is more widely adopted [37-39]:

$$\frac{1}{2}C_{dc}V_{dc}^2 = \lambda S_{rated} \quad \Rightarrow \quad C_{dc} = \frac{2\lambda S_{rated}}{V_{dc}^2}. \tag{2.10}$$

The equivalent capacitance can also be calculated based on SM capacitance as [39]:

$$\frac{1}{2}C_{dc}V_{dc}^2 = 6N_{arm}\cdot\frac{1}{2}C_{SM}\left(\frac{V_{dc}}{N_{arm}}\right)^2 \Rightarrow C_{dc} = \frac{6C_{SM}}{N_{arm}} \tag{2.11}$$

The estimated value in (2.8) is very conservative, as SM capacitor balancing control is not considered, and thus it may be more suitable for stability and fast transient studies. The capacitor value in (2.10) is preferred for slow transient simulations, since the unbalanced energy in the DC link is assumed to be perfectly shared by all the SM capacitors. The capacitor size should be carefully selected based on the frequency range of interest. For the ±320 kV, 1000 MW VSC model used in this thesis, an equivalent capacitance of 146 μF is used in Chapters 2 and 3 for low-frequency studies, while a relatively low capacitance of 98 μF is used in Chapters 5, 6 and 7 for stability analysis.

As one third of the DC current flows through the arm inductors in each phase, the AVM is extended in [39] to include the arm inductor in the DC side:

$$L_{armdc} = \frac{2}{3}L_{arm},\ R_{armdc} = \frac{2}{3}R_{arm}. \tag{2.12}$$

As DC fault studies are not one of the key concerns of this thesis, the representation of AVM under DC fault conditions is not discussed here.

The AVM for two-level PWM converters can also be represented using the equivalent circuit shown in Figure 2.3, but with the DC side reactance excluded and with the AC side impedance ($R+j\omega L$) representing the aggregated impedance of converter reactor and transformer.

2.1.3 Vector Current Control

Based upon the instantaneous power theory [41], vector current control is implemented in a synchronous dq-coordinate system (see Appendix A.1 for dq transformation). The currents and voltages measured at the PCC bus are transformed to dq quantities according to the reference angle provided by the PLL. The PLL is normally configured to enable the d-axis to be aligned with the voltage vector of the PCC bus, in order to achieve an independent control of active and reactive power [42].

By transforming equation (2.5) to dq domain, the plant model of the vector current control is established as:

$$L\frac{di_d}{dt} = e_d - v_d - Ri_d + \omega Li_q \tag{2.13}$$

$$L\frac{di_q}{dt} = e_q - v_q - Ri_q - \omega Li_d \,. \tag{2.14}$$

Proportional-Integral (PI) controllers are adopted for the current control, since the plant model is a dominant first-order model. The equations (2.13) and (2.14) indicate that the d-axis and q-axis current dynamics are coupled through the terms ωLi_q and ωLi_d. One popular solution is to use nulling terms to reduce the cross coupling effect, as shown in the closed-loop feedback diagram in Figure 2.4. In addition, feedforward voltage measurements v_d^{mea} and v_q^{mea} are employed to compensate variations of the PCC bus voltage. The feedforward terms shown in Figure 2.4 do not have to be perfectly accurate as the small residual coupling usually has a limited impact on the performance. The VSC modulation control is approximated using a first-order transfer function with a time constant τ_v. The time delay of the current measurement is denoted as θ_i.

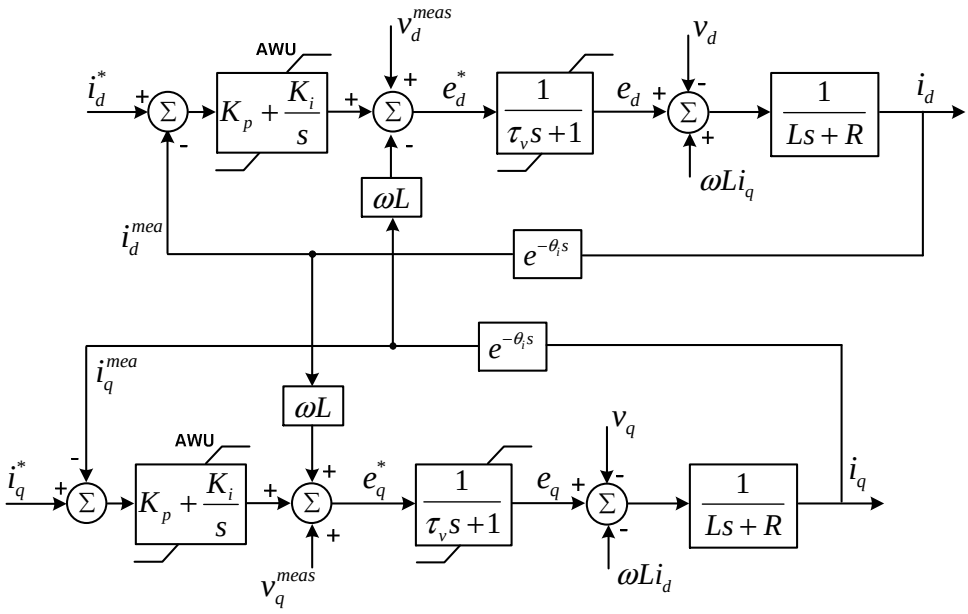


Figure 2.4: Closed-Loop feedback diagram for dq current control.

2.1.3.1 Anti-Windup Control

Due to the feedforward terms and dq transformations, it is not straightforward to set limits for the outputs of the PI current controllers. According to the priority given to the active and reactive current control [43, 44], the dq converter AC terminal voltage references generated by the vector current controllers are limited together, as shown in Figure 2.5, where the maximum converter voltage in per unit (pu) is calculated according to DC voltage V_{dc}^{pu} and the maximum modulation index $P_m^{\max}$ according to the following equation:

$$e_{\max}^{pu} = \frac{V_{dc}^{pu} V_{dc}^{base}}{2} \cdot P_m^{\max} \Big/ \left(\frac{\sqrt{2}}{\sqrt{3}} V_{ac}^{base} \right) = \frac{\sqrt{3} V_{dc}^{base}}{2\sqrt{2} V_{ac}^{base}} P_m^{\max} V_{dc}^{pu} . \tag{2.15}$$

An anti-windup (AWU) design with feedback has been developed based on the back calculation method discussed in [45-47]. As shown in Figure 2.5, when the voltage reference produced by the current controller saturates, the integrator output will be modified by the AWU control to maintain the references e_{dq}^{ref} very close to their limits. This design allows AWU to be applied to control systems with complex limit settings. Furthermore, smoother transient behaviours can be obtained by this dynamic reset of the integrator than an instantaneous reset. A larger AWU gain K_t provides a shorter reset time and enables tighter voltage limit control under saturated conditions however it should not be too large to unnecessarily disturb the nominal controller [46, 48]. The impact of the AWU on the stability of the nonlinear converter control system was not

assessed. To achieve guaranteed stability, more advanced AWU techniques may have to used [49]. The internal stability of the AWU control A rule of thumb is to choose K_t as a fraction of K_i/K_p [46].

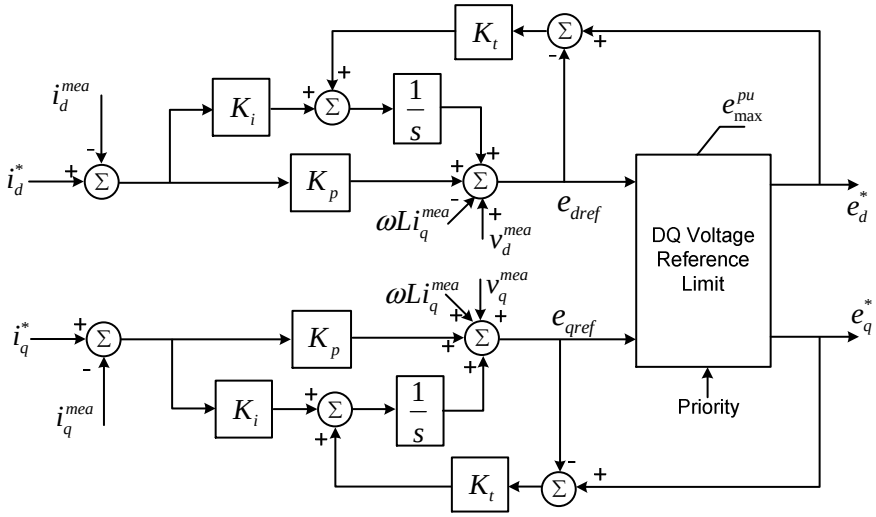


Figure 2.5: Anti-Windup design for the vector current controller.

2.1.3.2 Current Controller Tuning

Three methods for tuning of the current controller are developed and compared here. The closed-loop bandwidth ω_B used in this thesis is defined as the frequency upon which the magnitude of the sensitivity transfer function $S(j\omega)$ crosses -3dB from below, as interpreted in [1]. The bandwidth ω_{BT} where the magnitude of the complementary sensitivity transfer function $T(j\omega)$ crosses -3dB from above may be inaccurate as $|T| \approx 1$ is insufficient for an effective control performance [1]. The gain crossover frequency ω_c typically lies between ω_B and ω_{BT} ($\omega_B < \omega_c < \omega_{BT}$).

Analytical tuning

Since scaling could greatly simplify the model analysis, per unit values are used in all the control system equations in this thesis. With the time retained in real values, the base values shown in (2.16) are employed for the current control model (see Appendix A.4 for details).

$$v_{dq}^{base} = \frac{\sqrt{2}}{\sqrt{3}} V_{ac}^{base},\ i_{dq}^{base} = \sqrt{2} I_{ac}^{base},\ R^{base} = L^{base} = Z_{ac}^{base} \tag{2.16}$$

The PI controller in the following form is employed:

$$K(\mathrm{s}) = K_p + \frac{K_i}{s} = K_p \left(\frac{\tau_I s + 1}{\tau_I s} \right) \tag{2.17}$$

where τ_I is the integral time constant. By neglecting the voltage modulation dynamics and the measurement delay, the sensitivity transfer function of the current loop can be derived based on model shown in Figure 2.4 as (2.18)

$$S(\mathrm{s}) = \frac{s^2 + \frac{R}{L}s}{s^2 + \left(\frac{K_p + R}{L}\right)s + \frac{K_i}{L}} = \frac{s^2 + \frac{R}{L}s}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{2.18}$$

With the damping ratio ζ and the desired closed-loop bandwidth ω_d (in rad/s) specified, the proportional and integral gains can be derived as:

$$K_p = 2\zeta L\omega_d\sqrt{(1-2\zeta^2) + \sqrt{(1-2\zeta^2)^2 + (1+\frac{2}{\omega_d^2}\frac{R^2}{L^2})}} - R \tag{2.19}$$

$$K_i = \omega_d^2 L(1-2\zeta^2) + \omega_d^2 L\sqrt{(1-2\zeta^2)^2 + (1+\frac{2}{\omega_d^2}\frac{R^2}{L^2})}\,. \tag{2.20}$$

This sensitivity transfer function based tuning (STFT) achieves good accuracy on control specifications, but it may not be suitable for the tuning of a complex plant.

Internal model control (IMC)

Alternatively, when the modulation lag and measurement delay are considered in the tuning process, a simplified model reduction rule proposed in [50] can be employed here to reduce the plant transfer function $G(s)$ to a dominant first-order model with an effective time delay θ_d:

$$G(s) = \frac{1}{Ls+R}\cdot\frac{1}{\tau_v s+1}e^{-\theta_i s} \approx \frac{1}{R}\cdot\frac{1}{(\frac{L}{R}+\frac{\tau_v}{2})s+1}\cdot e^{-(\theta_i+\frac{\tau_v}{2})s} = \frac{1}{R}\frac{1}{\tau_1 s+1}e^{-\theta_d s}. \tag{2.21}$$

The internal model control (IMC) design [51, 52] is a well-established tuning method and has been widely applied to industrial processes [53, 54]. The key idea is to solve the controller based on the desired closed-loop response. With the reduced plant factorized to a minimum-phase part and a non-invertible part, the desired tracking process $T(s)$ can be described by:

$$T_{des}(s) = \frac{\omega_d}{s+\omega_d}e^{-\theta_d s}. \tag{2.22}$$

Consequently, the resulting PI controller is solved as:

$$K_{des}(\mathrm{s}) = \frac{1}{G(s)} \frac{T_{des}(s)}{1 - T_{des}(s)} \tag{2.23}$$

$$\Rightarrow \quad K_p = R \cdot \frac{\tau_1}{1/\omega_d + \theta_d} = \frac{\omega_d (L + \frac{\tau_v}{2} R)}{1 + \omega_d (\theta_i + \frac{\tau_v}{2})} \approx \omega_d L, \quad \tau_I = \tau_1 = \frac{L}{R} + \frac{\tau_v}{2} \approx \frac{L}{R} \tag{2.24}$$

The corresponding loop transfer function *L(s)* can then be calculated as:

$$L(s) = \frac{\omega_d}{1 + \omega_d \theta_d} \frac{1}{s} e^{-\theta_d s} \tag{2.25}$$

The IMC design usually leads to a fairly robust current controller. Since θ_d is normally much less than $1/\omega_d$ in this case, according to (2.25), the resulting closed-loop model will have a very large gain margin and a phase margin close to 90 degrees.

Skogestad internal model control (SIMC)

The closed-loop transfer function regarding the input disturbance, which can be seen as the mismatch between the feedforward terms and real coupling values, is derived as:

$$G_d S(\mathrm{s}) = \frac{1}{Ls + R} \cdot \frac{s^2 + \frac{R}{L} s}{s^2 + \frac{K_p + R}{L} s + \frac{K_i}{L}} = \frac{\frac{s}{L}}{s^2 + \frac{(K_p + R)}{L} s + \frac{K_i}{L}}. \tag{2.26}$$

A large integral gain is desired in order to reject the input disturbance at low-frequency range. However, the integral gain obtained from the IMC design is much smaller than the gain resulted from the STFT design and this may lead to a long settling time in case of the failure of the feedforward compensation. This drawback of IMC design for lag dominant plants ($\tau_1 \gg \theta_d$) has been acknowledged in [55] and [50]. Skogestad IMC (SIMC) design is introduced in [1, 50] to improve the disturbance rejection of the IMC design by increasing K_i appropriately.

By applying the SIMC rule to the reduced model shown in (2.21), the controller parameters can be computed as:

$$\begin{aligned} K_p &= R \cdot \frac{\tau_1}{1/\omega_d + \theta_d} = \frac{\omega_d (L + \frac{\tau_v}{2} R)}{1 + \omega_d (\theta_i + \frac{\tau_v}{2})} \\ \tau_I &= \min\left\{\tau_1, 4\left(\frac{1}{\omega_d} + \theta_d\right)\right\} = \min\left\{\frac{L}{R} + \frac{\tau_v}{2}, 4\left(\frac{1}{\omega_d} + \theta_i + \frac{\tau_v}{2}\right)\right\}. \end{aligned} \tag{2.27}$$

As the desired bandwidth ω_d of current loop is usually much larger than R/L, the integral time constant τ_I is selected to be the latter term in (2.27).

With ω_d=195 Hz, τ_v=82 µs and θ_i=0 µs, the three tuning methods discussed above are applied and the corresponding frequency responses of selected transfer functions are presented in Figure 2.6. The quantified results are demonstrated in Table 2.1 for two desired bandwidths.

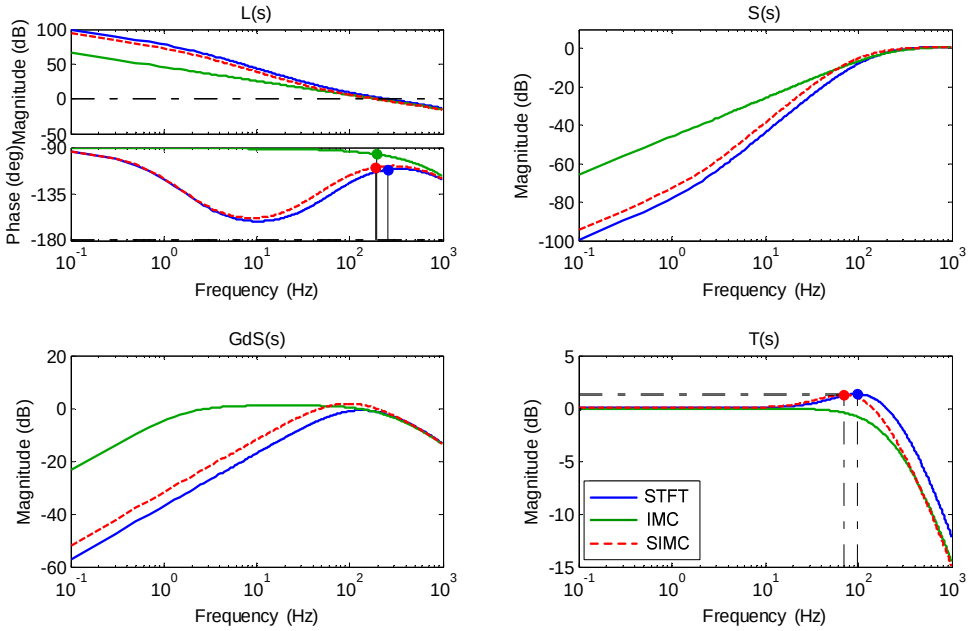


Figure 2.6: Frequency responses of L(s), S(s), G_dS(s) and T(s) for the three tuning methods.

Table 2.1: Comparison of the frequency-response measures for multiple current controller designs.

	ω_d = 195 Hz			ω_d = 250 Hz		
Method	STFT	IMC	SIMC	STFT	IMC	SIMC
PM (*deg*)	69	84.3	71.2	67	82.8	69.6
ω_B (*Hz*)	177	179	135	221	221	167
ω_{BT} (*Hz*)	351	219	252	464	285	325
Peak *T*(*s*)	1.35	0	1.28	1.41	0	1.17

All of the three designs result in a satisfactory gain margin (GM) and a phase margin (PM) larger than 65°. Particularly, the IMC design generates a PM close to 90°, as the dominant pole of the plant is cancelled by the zero in the PI controller. The response of G_dS clearly shows that the controllers based upon the STFT and SIMC methods provide a superior disturbance rejection capability over the IMC controller. The resulting bandwidths for the STFT and IMC scenarios are close to the desired bandwidth while the SIMC design normally results in a slightly lower bandwidth. The mismatch of the

bandwidths will be reduced for a system with faster modulation control and smaller measurement delay. The bandwidth ω_{BT} regarding $T(s)$ is much higher than ω_B, especially for the IMC and SIMC cases, however the tracking is probably out of phase in the frequency range between ω_B and ω_{BT}. The peak of $T(s)$ is an effective measure of the damping of the tracking response. The IMC design gives a more damped tracking performance than the other two cases.

Realistically, if the feedforward elements ($\omega L i_{dq}$ and v_{dq}) are employed and the voltage and current measurements are sufficiently fast and accurate, the IMC design is recommended due to its simplicity and excellent tracking performance. Furthermore, application of the IMC method in a cascaded system will reduce the order of the plant model and facilitate outer controller design. However, if a good degree of rejection capability to the inaccurate measurement of disturbance is required (e.g. the estimated value of L may largely differ from the real value in faulted scenarios), the SIMC and STFT methods are preferred.

2.1.4 Phase-Locked Loop

The PLL forms the foundation of vector control by providing the rotating reference angle, which is extracted from the measured three-phase quantities by a feedback control system. The locking performance of the PLL directly impacts on the response of the overall system, particularly on the interaction between active and reactive power control.

The synchronous reference frame (SRF) PLL, with its configuration shown in Figure 2.7, is the most widely adopted three-phase PLL structure [56-59]. In terms of the application for VSC HVDC, the instantaneous phase voltages v_{abc} at the PCC bus are sampled, and then transformed to the voltages v_{dq}, which are DC values if the system frequency is tracked by the PLL. A loop filter, usually in the form of PI, is used to generate the frequency in order to drive the q-axis voltage to zero. The angle of the voltage vector is generated by a voltage-controlled oscillator (VCO) by integrating the frequency.

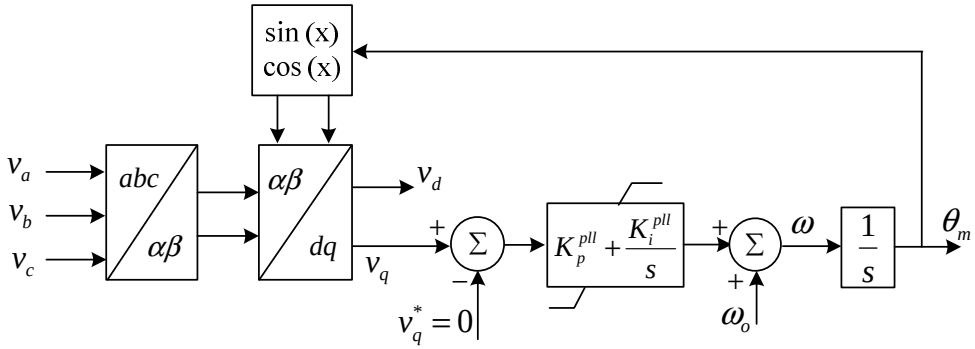


Figure 2.7: Control diagram for the synchronous reference frame (SRF) PLL.

The PLL system is highly nonlinear, especially under unbalanced and large transient conditions, such as frequency jump, angle shift and AC fault clearance. Assuming that the PCC bus voltage is balanced, the voltages obtained via Clark transformation are:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} \hat{V}_o \cos\theta \\ \hat{V}_o \cos\left(\theta - \frac{2}{3}\pi\right) \\ \hat{V}_o \cos\left(\theta + \frac{2}{3}\pi\right) \end{bmatrix} = \hat{V}_o \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} \tag{2.28}$$

where $\hat{V}_o$ and θ are respectively the amplitude and instantaneous angle of the phase a voltage. Consequently, the dq voltages can be derived as:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta_m & \sin\theta_m \\ -\sin\theta_m & \cos\theta_m \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \hat{V}_o \begin{bmatrix} \cos(\theta - \theta_m) \\ \sin(\theta - \theta_m) \end{bmatrix} \tag{2.29}$$

where θ_m is the output angle of the PLL. For a small tracking error (θ-θ_m), the q-axis voltage can be approximated as $\hat{V}_o(\theta$-$\theta_m)$. Therefore, the linearised model of the closed-loop PLL can be presented as shown in Figure 2.8, where θ_{pcc} is the angle of the voltage vector at PCC bus.

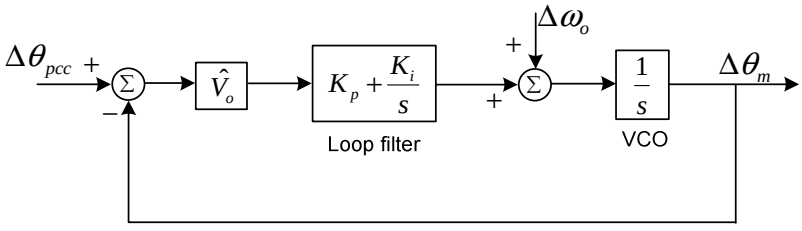


Figure 2.8: Linearised model for SRF PLL.

Consequently the complementary sensitivity transfer function of the PLL loop, and the corresponding damping ratio ζ and natural frequency ω_n are:

$$T_{PLL}(\mathrm{s}) = \frac{\hat{V}_o\left(K_p s + K_i\right)}{s^2 + \hat{V}_o K_p s + \hat{V}_o K_i} \Rightarrow \zeta = \frac{1}{2}K_p\sqrt{\frac{\hat{V}_o}{K_i}},\ \omega_n = \sqrt{K_i \hat{V}_o} \tag{2.30}$$

The controller can be calculated according to appropriate ζ and ω_n. Please note that the natural frequency is typically smaller than the resulting bandwidth due to the differential term in the numerator. Reduction of the grid voltage will degrade the damping and reduce the response speed, and therefore a slightly overdamped control design is preferred to ensure an acceptable performance under voltage sag conditions.

The SIMC tuning method is also ready to apply to this integrator-based plant model, with the controller parameter calculated as:

$$K_p = \frac{1}{\hat{V}_o}\omega_d,\ K_i = \frac{\omega_d^2}{4\hat{V}_o} \quad \Rightarrow \quad T(\mathrm{s}) = \frac{\omega_d\left(s + \frac{\omega_d}{4}\right)}{\left(s + \frac{\omega_d}{2}\right)^2} \tag{2.31}$$

This results in a critically damped system, as shown in (2.31). The desired bandwidth ω_d is used as a tuning parameter here.

A low-bandwidth PLL system (less than 50 Hz) provides a good loop filtering effect to phase unbalance and voltage harmonics [56, 59]. However a low-bandwidth PLL design may result in an unsatisfactory dynamic tracking performance in case of a phase or frequency jump, and this will lead to non-zero v_q and increase the coupling between active and reactive power control. Furthermore, the strength of the connected AC system should also be considered, as utilisation of a high-bandwidth PLL in a weak system may lead to high frequency interactions with the contaminated grid voltage.

2.1.5 Active and Reactive Power Control

The per unit active and reactive power injected into PCC bus from the VSC can be represented as:

$$P = v_d i_d + v_q i_q \tag{2.32}$$

$$Q = v_q i_d - v_d i_q \tag{2.33}$$

As the q-axis voltage is usually maintained to be zero by the PLL, the active and reactive power can therefore be controlled independently by manipulating the d-axis and q-axis

currents respectively. By assuming v_q=0, a feedforward control approach is to directly calculate the current references based on the power references and measured voltage:

$$i_d^* = \frac{P^*}{v_d}, \quad i_q^* = -\frac{Q^*}{v_d}. \tag{2.34}$$

An alternative approach is to use classical feedback control to generate references for the inner loop. Detailed comparison between the feedforward and feedback power control will be discussed in Chapter 4.

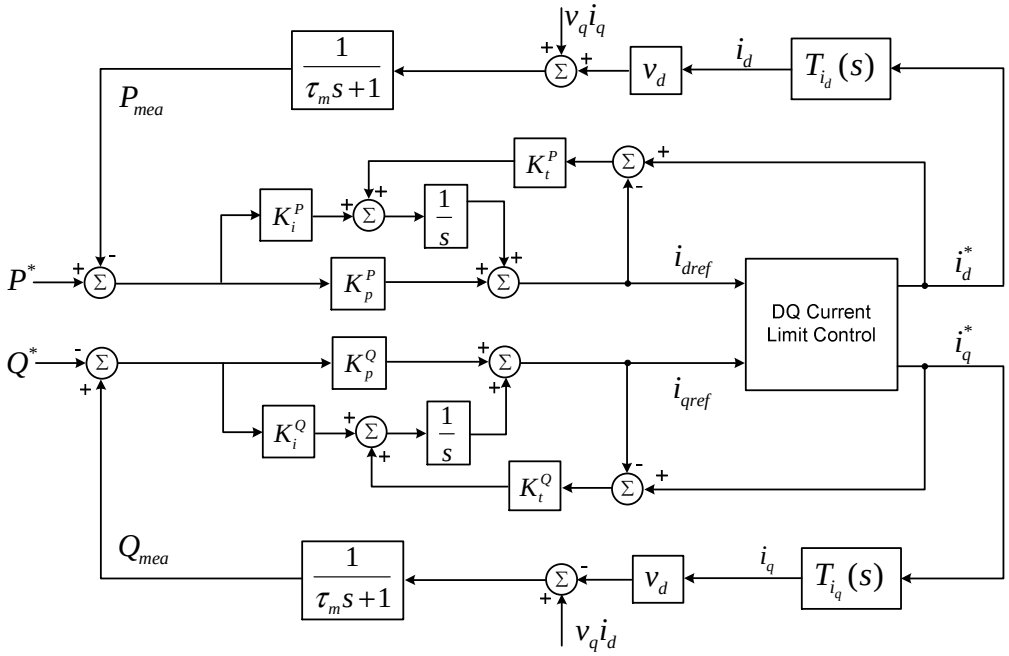


Figure 2.9: Active and reactive power control system with dynamic anti-wind design.

With active and reactive power controlled by two PI controllers, the resulting closed-loop systems are derived as shown in Figure 2.9, where $T_{i_d}(s)$ and $T_{i_q}(s)$ denote the complementary sensitivity transfer functions of the two current loops and τ_m is the filtering time constant of the power measurement. The dq current references are jointly limited, and the limit configuration can be quite complex especially under grid fault scenarios. An anti-windup structure with dynamic feedback is employed to ensure fast recovery of the outer control when VSC is operating in the current limit mode.

By approximating $T_{i_d}(s)$ as a first-order transfer function with time constant τ_{id} and applying the Skogestad model reduction rule, the plant model of the active power control is derived as:

$$G(\mathrm{s}) = v_{do} \frac{1}{\left(\tau_{i_d} + 0.5\tau_m\right)s+1} e^{-0.5\tau_m s} \tag{2.35}$$

where v_{do} is the operating point of v_d. The IMC control design rule can be directly applied to this simplified plant, and the controller parameters are obtained as:

$$K_p = \frac{1}{v_{do}} \frac{\tau_{id} + 0.5\tau_m}{1/\omega_d + 0.5\tau_m},\ \tau_I = \tau_{id} + 0.5\tau_m,\ K_i = \frac{1}{v_{do}} \frac{1}{1/\omega_d + 0.5\tau_m} \tag{2.36}$$

where ω_d is the control tuning parameter indicating the desired bandwidth of the power loop.

As shown in Figure 2.9, when the q-axis voltage is not well controlled by the PLL, the active and reactive power control loops will impose disturbances to each other. The PQ controllers need to have a good rejection capability to input disturbances. Therefore, the SIMC tuning method is preferred over the IMC rule, and the resulting controller parameters are:

$$K_p = \frac{1}{v_{do}} \frac{\tau_{id} + 0.5\tau_m}{1/\omega_d + 0.5\tau_m},\ \tau_I = \min\left\{\tau_{id} + 0.5\tau_m, 4\left(1/\omega_d + 0.5\tau_m\right)\right\} = \tau_{id} + 0.5\tau_m \tag{2.37}$$

which are identical to the parameters shown in (2.36), since the desired bandwidth is normally much smaller than the pole in the plant model (2.35), unlike the case for the current controller design. If the power measurement has a relatively large filtering time constant, the integral gain has to be dropped to ensure sufficient phase margin.

Using the control parameters shown in (2.37), the resulting damping ratio of the transfer function $G_dS(s)$ between disturbance $v_q i_q$ and the active power output can be approximated as:

$$\zeta \approx \frac{1}{2\sqrt{v_{do} K_p}} \approx \sqrt{\frac{\omega_{id}}{4\omega_d}} \tag{2.38}$$

Therefore the transfer function $G_dS(s)$ is usually an overdamped system as the power loop bandwidth is typically selected at least four times slower than the current loop bandwidth ω_{id}. It is also noted that a decrease of the PCC voltage degrades the damping.

This procedure also applies for the reactive power controller design. A relatively strong AC network has been assumed for the control design. More realistic closed-loop models and detailed stability analysis of the active power loop will be discussed in Chapter 4.

2.1.6 Current Limit

A key merit of vector dq current control is its current limiting capability under balanced conditions. Since it is the current modulus that needs to be limited, a priority is normally required to be given to the active or reactive power control branch in order to produce the limited current references. If the priority is given to active power or DC voltage control, the current references should be limited according to (2.39). If reactive power support is prioritised, the equation (2.40) should be adopted for the current limit control shown in Figure 2.9.

$$i_d^* = \max\left(i_{\max}, i_{dref}\right), \quad i_q^* = \max\left(\sqrt{i_{\max}^2 - i_d^{*2}}, i_{qref}\right) \tag{2.39}$$

$$i_q^* = \max\left(i_{\max}, i_{qref}\right), \quad i_d^* = \max\left(\sqrt{i_{\max}^2 - i_q^{*2}}, i_{dref}\right) \tag{2.40}$$

The current limit shown in (2.41) can be applied to scenarios where equal priority is given to the active and reactive control branches [43, 44].

$$i_d^* = \frac{i_{\max}}{\max\left(\sqrt{i_{dref}^2 + i_{qref}^2}, i_{\max}\right)} i_{dref}, \quad i_q^* = \frac{i_{\max}}{\max\left(\sqrt{i_{dref}^2 + i_{qref}^2}, i_{\max}\right)} i_{qref} \tag{2.41}$$

The converter is likely to operate in its current limit mode during severe AC system faults. The results shown in [60] demonstrate that, when an AC fault is cleared and the PLL is not able to track the angle of the PCC bus voltage, interaction between the resulting large q-axis voltage and the dq current control may cause saturations of converter voltages, especially for inverter operations. This phenomena results in an uncontrolled current for a short period of time until the PLL recovers.

An adaptive current limit scheme, shown in Figure 2.10, is proposed to tackle this issue. The key idea of this limit design is to avoid overmodulation of the converter caused by the combining effect of large currents and large q-axis voltage. In the design, the q-axis voltage is used to produce a hysteresis-based signal to trigger the adaptive limit. The value of the current limit is determined by the predefined v_q-i_{max} relation, which enables a tighter current limit for a larger error of the PLL. A rate limiter, with a large falling limit and a small rising limit, is employed to prevent the abrupt change between the adaptive current limit and the constant current limit, and to ensure smooth recovery of the converter system after the clearance. The limits for d-axis and q-axis currents are then computed based on the modulus limit i_{max} and the priority of active/reactive power

control. Practically the PCC voltage is also likely to be needed to determine the limited current references, according to TSO's grid code requirements [61]. The improvement of fault ride-through performance provided by this control is demonstrated in Appendix D.3.

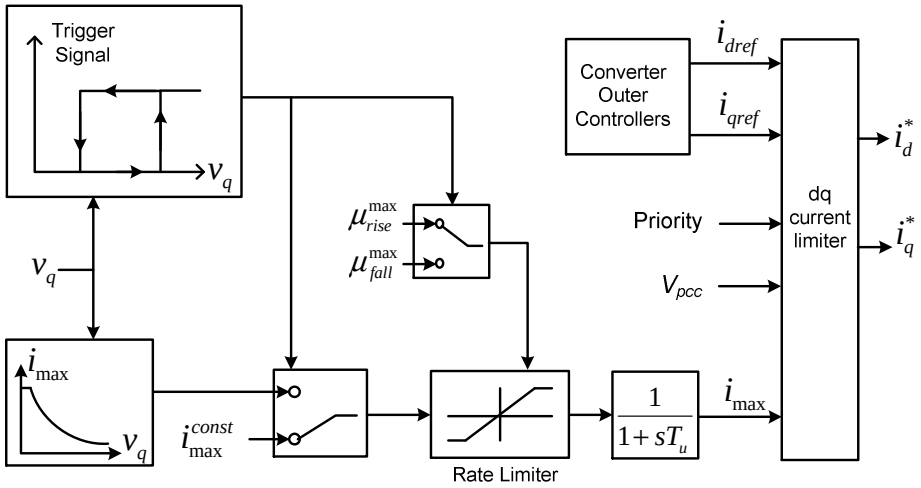


Figure 2.10: Adaptive current limit control.

2.1.7 AC Voltage Control

With respect to VSC-HVDC application in a weak AC system, the PCC bus voltage is likely to be strongly affected by the power variation of the VSC. AC voltage control is thus preferred instead of reactive power control in this case to provide grid support. Accurate tuning of the AC voltage control is difficult, since the plant model is determined by the overall AC network dynamics rather than local converter dynamics and large modelling effort may be needed.

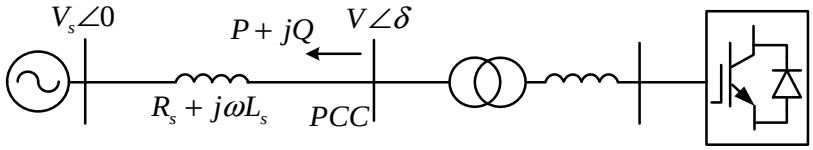


Figure 2.11: RMS model of a VSC connected to a simplified AC system.

Using the Thevenin equivalent model of the AC system as shown in Figure 2.11, the reactive power injected by the VSC into the PCC bus is approximated as:

$$Q = \frac{V\left(V - V_s \cos\delta\right)}{\omega L_s} \tag{2.42}$$

where the phasor of the PCC bus voltage is denoted by $V\angle\delta$ and the phasor of the AC voltage source is denoted by $V_s\angle 0$. Equation (2.42) can be further linearised as:

$$\Delta Q = \frac{\left(2V_o - V_s \cos\delta_o\right)}{\omega L_s}\Delta V + \frac{V_s V_o \sin\delta_o}{\omega L_s}\Delta\delta \tag{2.43}$$

where the subscript 'o' denotes the operating point of the corresponding quantities. By assuming that the steady-state angle's difference between $V\angle\delta$ and $V_s\angle 0$ is relatively small, the second term of (2.43) can then be neglected and the AC voltage can be related to the q-axis current as:

$$\frac{\Delta V}{\Delta i_q} = \frac{\Delta V}{\Delta Q}\frac{\Delta Q}{\Delta i_q} = \frac{\omega L_s}{2V_o - V_s\cos\delta_o}\left(-v_{do}\right). \tag{2.44}$$

Consequently, the closed-loop diagram for the AC voltage control employing a PI regulator can be described as shown in Figure 2.12. Larger active power transfer results in a larger angle excursion δ_o and a reduced loop gain, according to equation (2.44). A robust controller is required to provide sufficient stability margins to deal with the impact of power flow variations. As the closed-loop system shown in Figure 2.12 has a very similar form as the system described in Figure 2.9, therefore, the tuning method used for the active/reactive power control can be directly applied here.

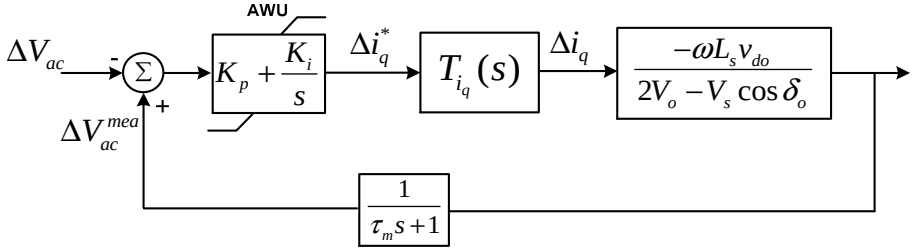


Figure 2.12: Approximated feedback loop for AC voltage control.

It should be noted that the plant model derived above is based upon RMS equations and therefore it is only suitable for AC voltage loops configured with a bandwidth at least 4 to 10 times lower than the system frequency. In order to reduce the interaction between the cascaded control loops, the bandwidth of the AC voltage loop of 7.5 Hz is selected here, which is significantly lower than the current loop bandwidth of 195 Hz.

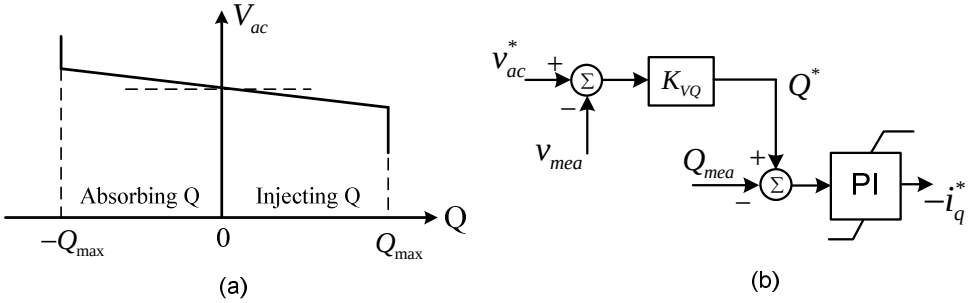


Figure 2.13: (a) V_{ac}-Q droop characteristics; (b) V_{ac}-Q droop controller.

As shown in Figure 2.13, droop characteristics between AC voltage and reactive power, which have been implemented in static synchronous compensators (STATCOMs) and other VAr compensation devices [62], can also be used for AC voltage regulation by VSC-HVDC. This type of control is preferred if there are multiple devices jointly regulating the AC voltages adjacent to the converter station [62, 63].

2.1.8 Frequency Control and Damping Support

As future power systems are likely to have a significant amount of renewable penetration, a degree of frequency support from VSC-HVDC is likely to be required by grid operators to support low-inertia systems. A frequency droop characteristic has been implemented in [64] and [63] to operate the VSC as a virtual synchronous machine.

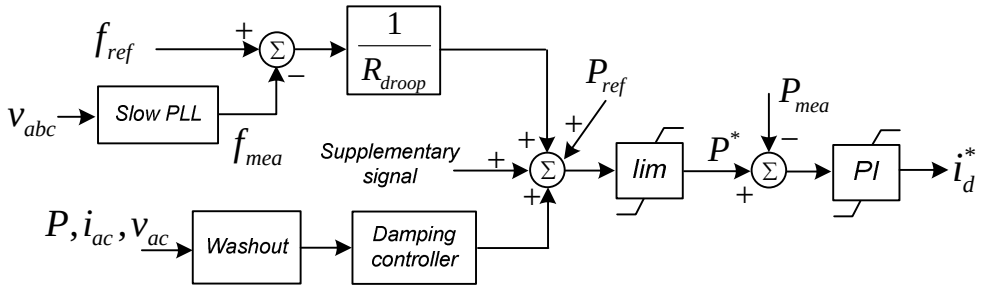


Figure 2.14: Basic structure of frequency droop control and POD control for VSC-HVDC.

A basic implementation of the frequency droop control is presented in Figure 2.14. A supplementary signal in proportion to the frequency deviation is added to the active power reference. The load sharing between different generating units and VSCs is determined by relative ratios of the droop constant R_{droop}, which is typically configured as 4% to 5% for generators. A slow PLL is used to extract the system frequency from the locally measured voltages, since a high-bandwidth frequency control is unnecessary.

However, active power fluctuation caused by the frequency deviation perturbs the balance of DC power and may deteriorate DC voltage performance. Particularly, for a point-to-point HVDC system connecting an offshore wind farm, the onshore converter will only have a very limited capability for frequency support, unless the wind farm has a degree of DC voltage control capability by varying the wind power generation.

Other dynamic support for AC systems, such as power oscillation damping control (POD), can also be incorporated for VSC-HVDC by modulating the active power transfer as shown in Figure 2.14. Like the frequency droop control, the active power variation caused by the POD control will disturb the balance of the DC system. This

issue can be alleviated by using reactive power for damping purposes. A multi-terminal configuration is anticipated to be beneficial for POD control due to the flexibility of active power transfer in a MTDC system [65].

2.2 Modelling of Wind Farm and Offshore VSC Control

One major application of the VSC-HVDC in Europe is to integrate large-scale offshore wind farms in the North Sea. The primary control objective of a wind farm side converter station (WFC) is to absorb all the power generated by the wind farm as well as provide grid support to the local wind farm system. In this section, a typical WFC control system is described. A simplified model of an aggregated wind farm is presented. Furthermore, basic fault ride-through (FRT) control methods using frequency modulation and DC chopper are briefly discussed.

2.2.1 Modelling of WFC Control

As a variable-speed wind turbine generator (WTG) based on doubly fed induction generator (DFIG) or permanent magnet synchronous generator (PMSG) is likely to have its own back-to-back converter system, the grid frequency does not have a direct impact on the power generated by the WTG. Therefore, for simplicity, a direct frequency control is used here by the WFC.

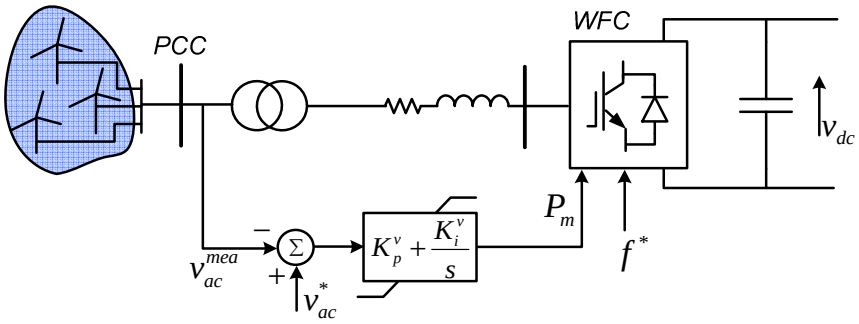


Figure 2.15: Feedback AC voltage and direct frequency control of WFC.

The WFC is typically controlled to behave as the local slack bus by maintaining the AC voltage and frequency, to balance the real and reactive power exchange with the wind farm. As shown in Figure 2.15, a feedback system is used to control the PCC bus voltage by manipulating the modulation index P_m [66-68]. The internal voltage reference of the WFC is accordingly formed by the modulation index and the frequency reference. A control scheme similar to the structure shown in Figure 2.15 has been adopted by the first VSC-MTDC system [69].

2.2.2 Modelling of Simplified Wind Farm (SWF)

A simplified wind farm (SWF) model is developed to approximate an aggregated fully rated converter-based (FRC) WTG. This model only represents the grid side converter, with the mechanical dynamics and aerodynamics of the WTG system excluded. This level of modelling fidelity is sufficient for most studies focusing on the transient performance of MTDC systems rather than detailed wind turbine behaviours, as the generator dynamics are effectively separated from the grid by the DC link [70].

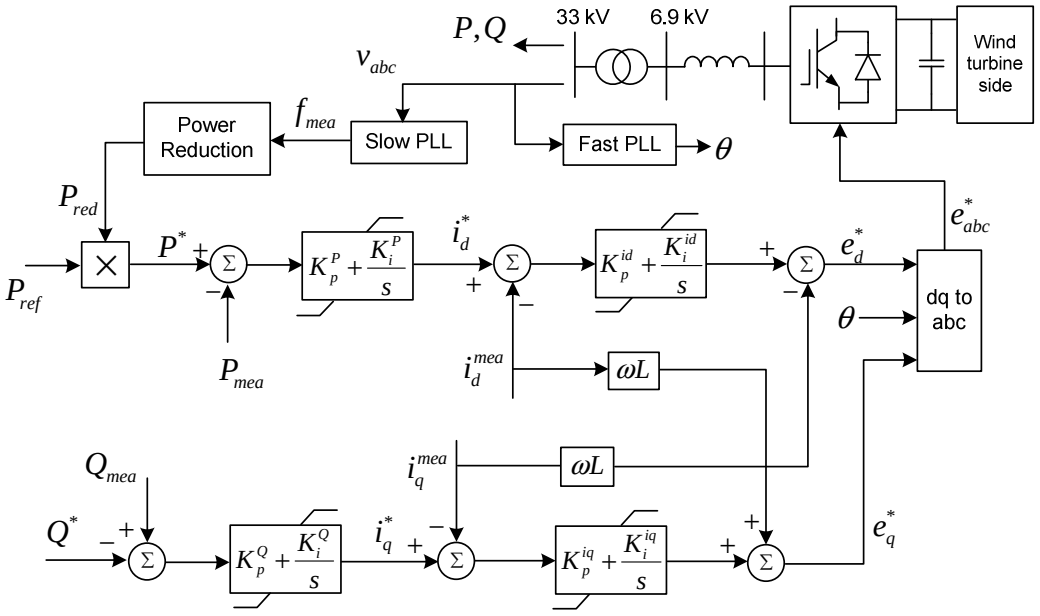


Figure 2.16: Active and reactive power control of the SWF model.

The overall control structure of the SWF model is presented as shown in Figure 2.16, where the DC link voltage is assumed to be perfectly controlled. Vector current control, which is typically used by both of the back-to-back converters in a FRC turbine system [71, 72], is employed by the active and reactive power controllers. Unlike a detailed FRC system where the power or torque reference is calculated from the maximum power tracking curve [71, 73], the power reference of this simplified model is directly scheduled. IMC is applied for the tuning of both the current and power controllers of this model.

2.2.3 Fault Ride-Through Control

For a point-to-point VSC-HVDC link integrating an offshore wind farm, during a severe onshore grid fault, the reduced grid voltage degrades the power transfer capability of the HVDC link and the onshore VSC terminal may have to operate in the current limit mode. Under such scenarios, the WFC may continue to inject the same amount of wind power

to the DC link and cause the DC voltage to rise immediately. A degree of fault ride-through (FRT) capability is demanded by the Grid Code for such VSC-HVDC links. Various FRT methods, including power dissipation through DC chopper [74-77], active power reduction via frequency modulation [66, 77], voltage reduction [78], or power reduction through fast communication [77], have been proposed by previous literature. Realistically, the optimal FRT strategy could be largely affected by the type of the wind turbine system.

An active power reduction method based on frequency modulation is adopted here for the WFC and the SWF model. As shown in Figure 2.17, once DC overvoltage is detected by a hysteresis characteristic, the frequency setpoint of the WFC will be increased in proportion to the DC voltage deviation. The maximum frequency excursion should not be too large, as this may damage certain components in a wind farm. A gradient limiter is employed to avoid frequency jumps that may cause poor PLL performance.

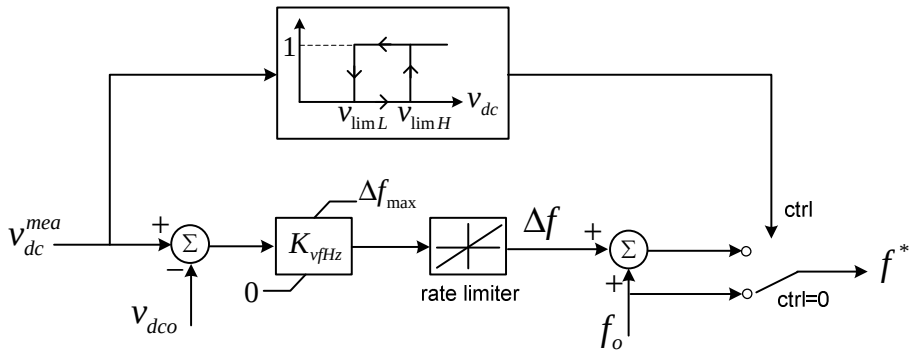


Figure 2.17: DC overvoltage control of WFC by altering wind farm frequency.

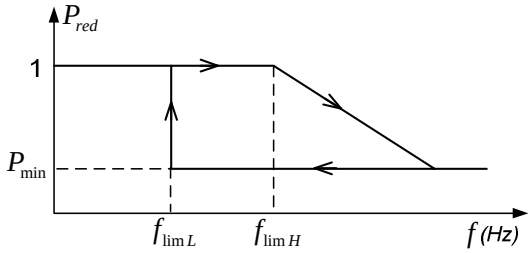


Figure 2.18: Active power reduction characteristic for the SWF model.

A hysteresis characteristic between an active power reduction factor P_{red} and the locally measured frequency is depicted in Figure 2.18, for the simplified wind farm model. Upon the detection of the frequency rise by a slow PLL, the active power reference of the SWF is determined by the multiplication of the original reference and the reduction factor P_{red}, as schematically shown in Figure 2.16. Realistically, in case of onshore faults with long durations, fast pitch control may be required to reduce the mechanical power and

maintain the generator speed within an acceptable level for WTG systems of relatively small inertias. Frequent changes between the normal operation and the power reduction mode can be avoided through the hysteresis function.

The performance of the FRT control through wind power reduction is highly limited by the maximum rate of power change of the wind turbine system. Practically, the control implementations of the WFC and each WTG have to be modified to integrate such a FRT functionality. Alternatively, a robust FRT method is to use a power-electronics-controlled DC braking resistor (DC chopper) to dissipate the surplus power injected by the wind farm [74, 76]. This additional component allows the wind farm's operation to remain unperturbed during the onshore grid fault. Furthermore, the use of DC chopper enables the DC overvoltage to be damped sufficiently fast. However, the DC chopper usually needs to have the same power rating as the VSC station, and therefore may not be cost-effective.

The DC chopper is modelled as a switch in series with a braking resistor in [74, 75, 79], as shown in Figure 2.19 (a). The switch is triggered here using a hysteresis characteristic regarding DC voltage measurement, as shown in Figure 2.19 (b). As described in [76], the average DC current absorbed by the chopper is likely to be determined by the duty ratio, which may be directly related to the DC overvoltage. Therefore, for slow transient studies, it could also be reasonable to model the chopper as a voltage-controlled current source, as shown in Figure 2.19 (c).

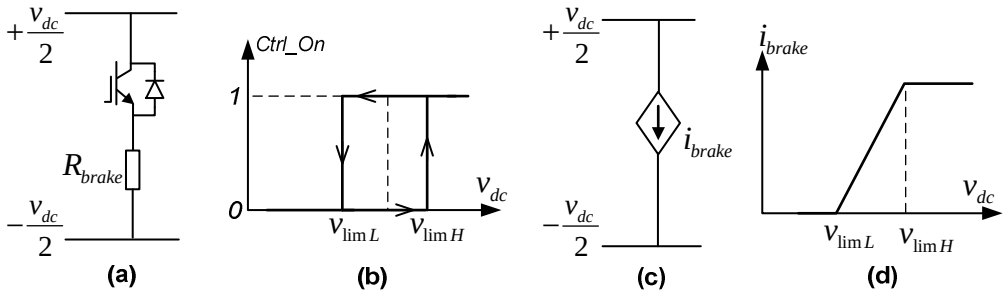


Figure 2.19: (a) Braking resistor representations of DC chopper; (c) Hysteresis-Based switching control of the braking resistor; (b) Current source representation of DC chopper; (d) Voltage-Current characteristic of the current-source-based model.

The simulations shown in Figure 2.20 are conducted using a 1000 MVA ±320 kV point-to-point VSC-HVDC model, to demonstrate the onshore fault ride-through performance of wind farm power reduction and DC chopper. The DC link voltage increases rapidly as a severe fault occurs at the PCC bus of onshore terminal. The DC chopper reacts much faster than the wind farm power reduction and therefore the DC overvoltage is much

better limited. For the DC braking resistor, the smaller the hysteresis detection band, the tighter the voltage will be controlled however with higher switching frequency. The communication between the WFC and the WTGs by varying the frequency is not sufficiently fast mainly due to the relative low bandwidth of the PLL for frequency measurement. The FRT performance based on the frequency modulation is also constrained by the rate of the wind farm power change. Furthermore, for this approach, the larger the pre-fault power transfer is, the higher the DC voltage peak during the fault will be.

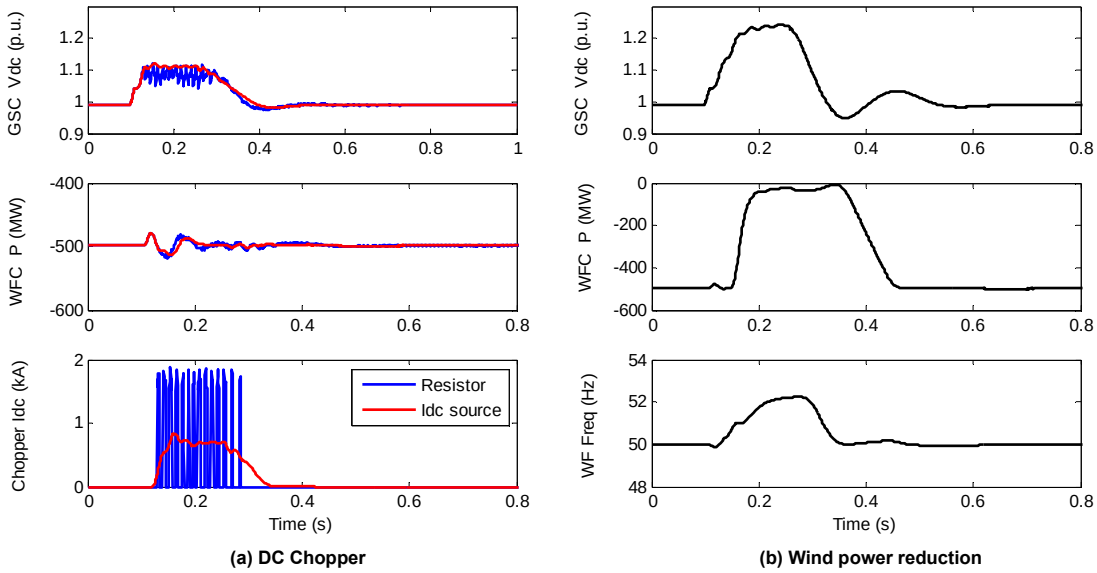


Figure 2.20: Simulations of FRT control based on DC braking resistor, current-source-based DC chopper and wind power reduction in a point-to-point system.

2.2.4 Modelling of DC Cable

A lumped parameter cable model, which is derived based on the series expansion of the parameters defining the distributed parameter model, is employed for DC cable modelling in DIgSILENT PowerFactory (DSPF) [80]. More advanced models which represent the distributed feature of cables, including Bergeron model and frequency-dependent models, are currently not available for DC cables in DSPF. The results in [81] suggest that the frequency-dependent model gives the most accurate responses for fast transient and protection studies, while the transient performance of the lumped model might be more numerically stable in simulations than the Bergeron model. The lumped model cannot represent the propagation delay; however, its time constant is likely to be very small [81] and therefore is insignificant for slow transient studies of MTDC systems.

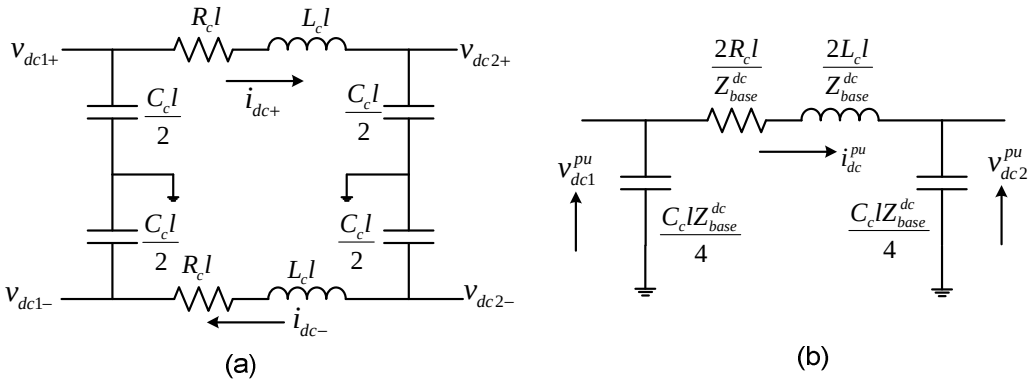


Figure 2.21: (a) Nominal π model of DC cable; (b) per unit representation of the π model.

For a symmetrical monopole system, the equivalent lumped model of length l is presented in Figure 2.21 (a), where the resistance, inductance, and capacitance of per unit length are denoted by R_c, L_c and C_c respectively. The per unit representation of this lumped model is derived as shown in Figure 2.21 (b) (see details in Appendix A.4).

A cascaded π-section model was adopted instead of the nominal lumped model to improve simulation accuracy. Generally, the higher the frequency of interest or the longer the cable, the more line sections are required. However, an excessive number of line sections may extensively reduce simulation speed.

Frequency response is used to select an appropriate number of π sections according to the frequency range of interest and the length of the cable. As an example, Figure 2.22 demonstrates the frequency responses between the current injection of one end and the DC voltage of the other end, for a 180 km DC line modelled by four different numbers of π sections. The parameters are derived based on data provided in [82, 83]. The alignments between the frequency responses of low-order models and high-order models can then be used to identify the number of π sections needed to achieve accurate performance up to the given frequency of interest.

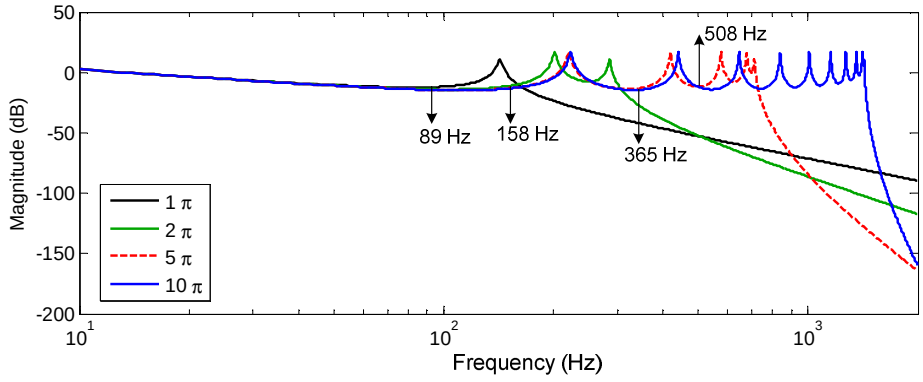


Figure 2.22: Frequency responses for cable models of different numbers of π sections (180 km).

2.3 DC Voltage Control of MTDC

In a conventional power system, the balance between power generation and load demand is indicated by a stable grid frequency. Analogously, DC voltage is of paramount importance with respect to power balance and stability of a MTDC system. Compared with a typical machine-based power system with large inertia, the transients of a capacitance-based DC network are in a much higher frequency range, and, therefore, voltage control in a DC grid is anticipated to be more challenging than the frequency control in a conventional AC system. The steady-state DC voltage should also be maintained at an acceptable range, as an overvoltage will trigger protection devices and impose severe stress on insulation of DC cables, while an excessively low DC voltage will affect converter AC voltage synthesis and increase transmission losses.

Relying on telecommunication for transient DC voltage stabilisation is impractical from the viewpoint of reliability and the fast-response required of a DC system. Distributed DC voltage control based on local measurement, at most modified by a slow central coordinating control for steady-state purposes, seems to be the favoured option. The presently favoured DC voltage regulation techniques can be categorised into DC slack bus control, voltage margin control, and voltage droop control. These control strategies will be discussed in detail in this section.

2.3.1 DC Slack Bus Control

In a typical point-to-point VSC-HVDC system, DC voltage is maintained by one converter through manipulating the power interchange between the AC and DC system. For a radial HVDC link integrating an offshore wind farm, the onshore terminal is typically dedicated to this role. Generally, a cascaded control system employing the d-axis current control as an inner loop is applied to DC voltage regulation. Relatively simple dynamics are considered here for modelling of DC voltage control. More detailed stability analysis will be presented in Chapters 6 and 7.

According to the AVM of MMC shown in Figure 2.3(c), the voltage v_{dc} is measured for the feedback control of DC voltage. This however complicates the modelling and controller design since v_{dc} is not a state variable. It would be more convenient to use the internal voltage across the capacitor v_{eq} for analysis purposes. The feasibility of such an approximation however needs to be justified.

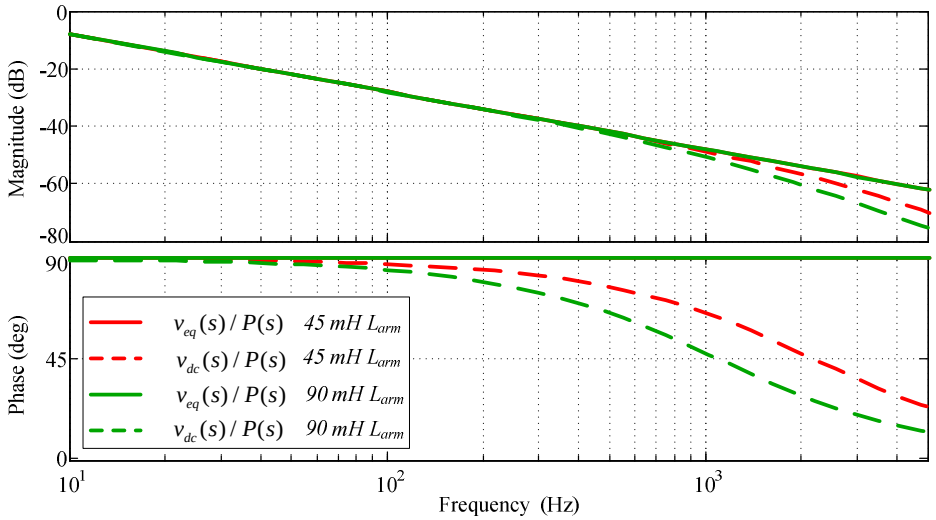


Figure 2.23: Frequency responses of between the converter power and DC voltages measured at two buses.

By considering the VSC as a controllable source of active power, the simplified plant of DC voltage control, which is effectively the transfer function between the converter power and the DC voltage of interest, has been derived with respect to the two DC voltages. The corresponding frequency responses are illustrated in Figure 2.23, for two sizes of arm inductors. The approximation of using v_{eq} as the measured output instead of v_{dc} is very accurate up to 600 Hz in terms of magnitude. There is more phase lag for $v_{dc}(s)/P(s)$ than $v_{eq}(s)/P(s)$ as the frequency increases, due to the DC side model of arm inductor. Basically, this approximation is reasonable for relatively low-frequency studies, as long as sufficient phase margin is assured. Therefore, the conventional DC side model of AVM without the DC side arm inductor shown in Figure 2.3(b) is used for a majority of the analytical studies of this thesis, except for Chapter 5 and Chapter 7.

Considering the single capacitor model in Figure 2.2(b), the dynamic equation regarding v_{dc} is written as:

$$C_{dc}\frac{dv_{dc}}{dt}=\frac{P_{dc}}{v_{dc}}-\frac{v_d i_d+v_q i_q}{v_{dc}}\approx\frac{P_{dc}}{v_{dc}}-\frac{v_d i_d}{v_{dc}}. \tag{2.45}$$

Assuming v_q=0 pu, the equation above can be further linearised as:

$$\begin{aligned}\frac{d\Delta v_{dc}}{dt}&=\frac{1}{C_{dc}v_{dco}}\left(\Delta P_{dc}-v_{do}\Delta i_d-i_{do}\Delta v_d\right)-\frac{1}{C_{dc}}\frac{1}{v_{dco}^2}\left(P_{dco}-v_{do}i_{do}\right)\\&=\frac{1}{C_{dc}v_{dco}}\left(\Delta P_{dc}-v_{do}\Delta i_d-i_{do}\Delta v_d\right)\end{aligned}. \tag{2.46}$$

where the subscript ‘o’ denotes the operating point of the corresponding quantities.

Consequently, the closed-loop control diagram for DC voltage control using a PI controller is derived as shown in Figure 2.24 (a), where τ_m is the time constant of the DC voltage measurement filter. The fluctuation of the power from the DC system into the VSC DC capacitor link ΔP_{dc} acts as the main disturbance to the loop. Unlike the control of current and power, the primary responsibility of DC voltage control is disturbance rejection rather than reference tracking. The measured DC power or current might be added to the controller output for disturbance cancellation, as suggested in [84], [85] and [66]. The associated analysis will be presented in Chapter 6.

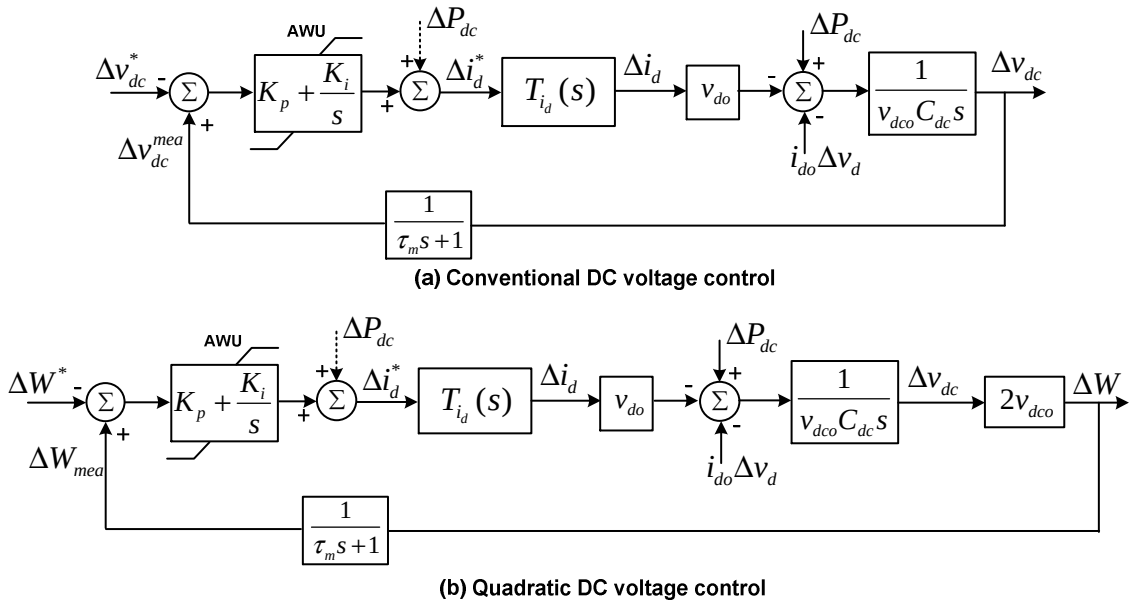


Figure 2.24: Feedback control diagrams for DC voltage control.

The plant model shown in Figure 2.24(a) depends on the operating point v_{dco}. This can be avoided by employing the quadratic of DC voltage as the feedback output, as suggested in [34], [86] and [84]. The differential equation regarding the energy stored in the capacitor can then be written as:

$$\frac{d}{dt}\left(\frac{1}{2} C_{dc} v_{dc}^2\right) = P_{dc} - v_d i_d \,. \tag{2.47}$$

Consequently, by defining $W = v_{dc}^2$, the dynamic equation regarding the new plant model is:

$$\frac{d\Delta W}{dt} = \frac{2}{C_{dc}} \left(\Delta P_{dc} - v_{do} \Delta i_d - i_{do} \Delta v_d\right) \tag{2.48}$$

which is independent of v_{dco}. The corresponding closed-loop diagram for the quadratic DC voltage control is shown in Figure 2.24(b). However, this improvement does not

significantly reduce the nonlinearity of DC voltage dynamics, as the voltage variation is normally very small, except for DC fault conditions. The key nonlinearity for the DC voltage control is in fact caused by the power flow variations, which will be detailed in Chapter 6 and 7.

By approximating the current loop transfer function $T_{id}(s)$ as $1/(\tau_{id}s+1)$, the plant model in Figure 2.24 can be written and further simplified as:

$$G(s)=\frac{1}{\tau_{id}s+1}\cdot\frac{v_{do}}{v_{dco}}\cdot\frac{1}{C_{dc}s}\cdot\frac{1}{\tau_m s+1}\approx K_G\cdot\frac{e^{-(\tau_m+\tau_{id})s}}{s} \tag{2.49}$$

where $K_G=v_{do}/(v_{dco}C_{dc})$, while this gain will equal to $2v_{do}/C_{dc}$ if v_{dc}^2 is used for feedback.

Applying the SIMC rule to the reduced plant shown in (2.49), the PI controller parameters can be tuned as:

$$K_p=\frac{1}{K_G\left(\tau_c+\tau_{id}+\tau_m\right)},\ \tau_I=4\left(\tau_c+\tau_{id}+\tau_m\right) \tag{2.50}$$

where τ_c is a tuning parameter that is the reciprocal of the desired bandwidth ω_d. Since the bandwidths of the current loop and v_{dc} measurement are much higher than the bandwidth of the v_{dc} loop, this SIMC design will result in a critically damped system.

Alternatively, the plant model can be reduced into a second-order transfer function:

$$G(s)=\frac{1}{\tau_{id}s+1}\cdot\frac{v_{do}}{v_{dco}}\cdot\frac{1}{C_{dc}s}\cdot\frac{1}{\tau_m s+1}\approx K_G\cdot\frac{e^{-0.5\tau_{id}}}{s\left(\left(\tau_m+0.5\tau_{id}\right)s+1\right)}. \tag{2.51}$$

A PID controller in the form of (2.52) is then ready to be applied to this second-order process. The resulting parameters tuned by SIMC method are shown as (2.53).

$$K(s)=K_p\left(\frac{\tau_I s+1}{\tau_I s}\right)\left(\tau_D s+1\right) \tag{2.52}$$

$$K_p=\frac{1}{K_G\left(\tau_c+0.5\tau_{id}\right)},\ \tau_I=4\left(\tau_c+0.5\tau_{id}\right),\ \tau_D=\tau_m+0.5\tau_{id} \tag{2.53}$$

The symmetrical optimum (SO) method is a robust tuning method for PI and PID controllers, and is particularly suitable for a plant model containing an integrator [56, 87, 88]. The principal idea is to enable that the maximum phase of the loop transfer function occurs at the crossover frequency ω_c to achieve a good phase margin.

$$G(s)=\frac{1}{\tau_{id}s+1}\cdot\frac{v_{do}}{v_{dco}}\cdot\frac{1}{C_{dc}s}\cdot\frac{1}{\tau_m s+1}\approx K_G\cdot\frac{1}{s}\cdot\frac{1}{(\tau_m+\tau_{id})s+1} \tag{2.54}$$

Applying SO tuning to the reduced plant shown as (2.54), the resulting controller parameters can be obtained as:

$$K_p=\frac{1}{K_G\alpha(\tau_m+\tau_{id})},\ \tau_I=\alpha^2(\tau_m+\tau_{id}),\ K_i=\frac{1}{K_G\alpha^3(\tau_m+\tau_{id})^2} \tag{2.55}$$

where α is the tuning parameter, which can be roughly related to the resulting damping ratio, phase margin and crossover frequency as [56, 88]:

$$\zeta=\frac{\alpha-1}{2},\ PM=\arctan\left(\frac{\alpha^2-1}{2\alpha}\right),\ \omega_c=\frac{1}{\alpha(\tau_m+\tau_{id})}. \tag{2.56}$$

Six controllers have been designed using the three tuning methods, with the selected frequency-response measures shown in Table 2.2. The first five controllers demonstrate excellent GM and PM, whereas the relatively high bandwidth of the sixth design results in decreased stability margins. Realistically, since the detailed and uncertain dynamics of the DC and AC networks are not considered in the design process, a good degree of robust stability is necessary. With the identical setting of τ_c, slightly better robustness as well as faster dynamic response and better disturbance rejection can be obtained by adding a differential action in the controller.

Table 2.2: Comparison of the frequency-response measures for multiple DC voltage controller designs.

Controller	Tuning Parameter	*GM* (dB)	*PM* (deg)	ω_B (Hz)	Peak G_dS (dB)
1. PI	τ_c=0.0114	29.8	68.9	8.75	-9.48
2. PI	τ_c=0.0057	24.6	63.2	14.5	-14.2
3. PID	τ_c=0.0114	45.4	74	10.2	-10.5
4. PID	τ_c=0.0057	39.6	71.8	18.9	-16.2
5. SO	α=4	23.5	61.7	16.0	-15.1
6. SO	α=1.96	15.3	34.1	29.6	-18.1

Generally, power imbalance of the DC system can be compensated faster and the transient peak of DC voltage can be reduced if a DC voltage control loop of a higher bandwidth is used. The closed-loop transfer function between the input disturbance and the output $v_{dc}(s)/P_{dc}(s)$ can be approximated as:

$$G_d S(s) \approx \frac{1}{C_{dc}s} \cdot \frac{1}{1+\frac{K_G}{s} \cdot \frac{K_p s + K_i}{s} \cdot \frac{1}{(\tau_m + \tau_{id})s + 1}} \approx \frac{s}{C_{dc}s^2 + K_p s + K_i}. \qquad (2.57)$$

This equation verifies that larger K_i decreases the gain of G_dS and implies better disturbance rejection at low frequencies. However, the bandwidth should not be too high, since this would deteriorate the stability and the controller would react to high-frequency DC voltage noises. In addition, lower bandwidth of the inner loop and measurement filter will degrade the disturbance rejection performance.

The aforementioned control design focuses on a simplified plant based on a local system. Realistically, the overall DC network dynamics may need to be considered for the analysis of DC voltage stability. Please see Chapters 6 and 7, where this is considered in further detail.

In a MTDC system, if there is only one converter regulating DC voltage, this terminal can be called the “DC slack bus” [26]. However, there are several constraints of using only one converter to maintain the voltage of a MTDC system:

- The slack bus station must have a sufficiently large power rating and the connected AC system has to be sufficiently strong to accommodate the total power variations of all the other terminals.
- Loss of this terminal may cause instability of the whole MTDC system if there is no backup DC slack bus and the communication is not sufficiently fast to schedule another terminal for voltage regulation.
- The feasibility of this control approach will be significantly reduced as the size of the DC network increases.

2.3.2 Voltage Margin Control

Voltage margin control was initially proposed in [89] in 1998 for a back-to-back VSC system, and this method was suggested in [90] to be used for the Shin-Shinano three-terminal system. The voltage margin, which is defined as the difference between voltage references of different terminals, is introduced to enable a redundant voltage control scheme and meanwhile avoid undesirable interference between the voltage controls of different terminals [26, 43, 91].

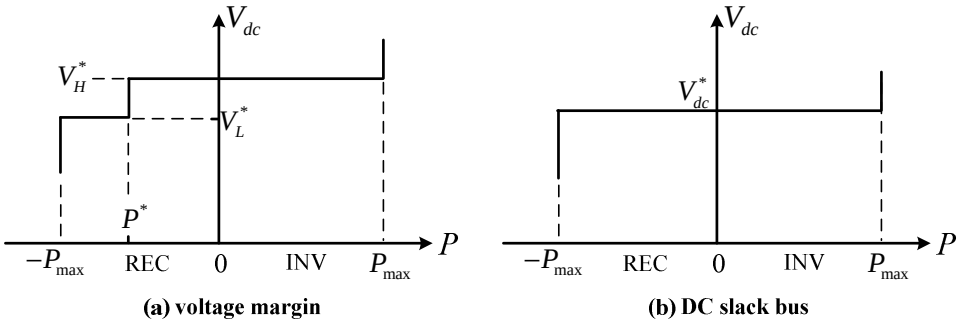


Figure 2.25: Steady-State characteristics of (a) voltage margin (b) DC slack bus.[3]

As shown in the steady-state characteristic in Figure 2.25(a), the voltage margin control, which can be seen as a combination of DC voltage control and active power control, is frequently used in previous literature in conjunction with constant DC voltage control. Under nominal conditions, a VSC terminal configured with voltage margin control normally operates in active power control mode. It will take over the task of voltage regulation when the DC voltage exceeds the upper or lower threshold, without the need of a communication system. The sequence of priority in terms of DC voltage control is determined by the configuration of voltage margins, as a terminal with a voltage reference closer to the nominal setpoint has a higher priority in voltage regulation.

In comparison to slack bus control, the DC system reliability can be significantly enhanced by using the voltage margin strategy. It could be a very feasible option for point-to-point systems or MTDC systems with a small number of terminals, since a good degree of redundancy is ensured and the power transfer can be easily scheduled. This control structure has proved its feasibility in practical VSC-HVDC project [18].

[3] The abbreviations REC (rectifier) and INV (inverter) are used throughout this thesis.

However, voltage margin control may not be considered as a satisfactory approach for coordination control of a large DC grid due to the following reasons:

- Unless voltage droop control or other transient voltage control is incorporated by certain terminals, there is only one converter at a time regulating the DC voltage and this may lead to unsatisfactory transient performance, particularly for large DC grids.
- The voltage margin needs to be sufficiently large to reduce the possibility of interactions between voltage controls of different terminals. However, large margins may result in unsatisfactory steady-state voltage levels.
- As the size of a MTDC system grows, it becomes increasingly difficult to configure the voltage margins between converters to satisfy both steady-state and dynamic requirements.

The steady-state characteristics for voltage margin control have been discussed in a number of publications [26, 43, 92]. Nonetheless, information about the dynamic implementations of this strategy is limited. Two control implementations are introduced here as follows.

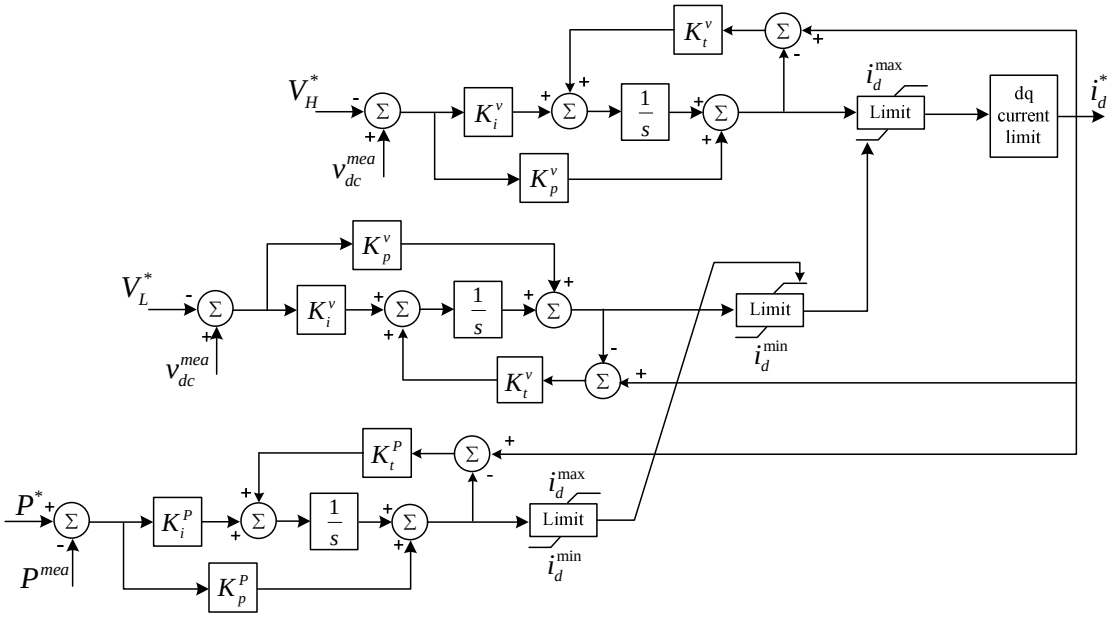


Figure 2.26: Adaptive-Limit-Based implementation of the voltage margin controller.

The first implementation, with the detailed controller structure shown in Figure 2.26, is developed based upon the control system presented in [89]. It is comprised of three PI controllers: two DC voltage controllers and one active power controller. Since usually there is only one controller at a time activated and the switching between controllers can

cause non-smooth transfer, the limited current reference i_d^* is fed to all the integrators. This ensures that the signal i_d^* is tracked by the unused controllers in order to achieve fast and smooth transitions between the outputs of the three PI controllers. The dynamic performance of the voltage margin control is heavily affected by the implementation of the controller limits. A high-bandwidth voltage controller may lead to undesirable and frequent transitions between controllers therefore is not recommended for voltage margin control.

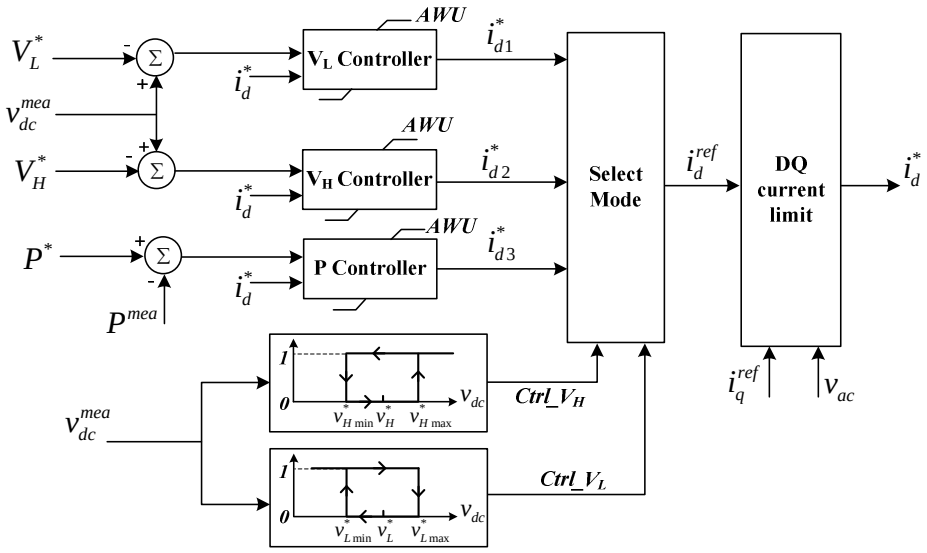


Figure 2.27: Hysteresis-Based implementation of the voltage margin controller.

A more straightforward implementation of the voltage margin control is described as shown in Figure 2.27. Unlike the previous method where the controllers are switched based on dynamic limits, the controller output is selected here according to the hysteresis functions. For example, the output of the V_H controller will be employed if the logic signal *Ctrl_*V_H becomes 1. The hysteresis band effectively extends the margin and may allow the upper and lower voltage references to be configured close to each other. However, inappropriate coordination settings of the hysteresis bands and voltage references for multiple converters could result in poor transient performance.

2.3.3 DC Voltage Droop Control

A majority of literature with respect to MTDC control schemes favours DC voltage droop control [22, 26, 43, 67, 68, 75, 91-99] to allow multiple converters to regulate the system voltage simultaneously and achieve a distributed sharing of power imbalance. The key advantages of this control strategy are:

- Stability and reliability of a MTDC system can be enhanced by incorporating more converter terminals with DC voltage droop control.
- Droop control is a general control scheme and could be configured without modifying the control schemes of other converters. This is preferable as a future DC grid is likely to be formed gradually by adding more multi-vendor converters in the system.
- The power surplus or deficit caused by a severe contingency will be shared by all the droop-controlled converters and thus the stresses on AC systems are reduced.
- In a large DC grid with long transmission distances, dynamic features of DC voltages between remote nodes could be significantly different, and a widespread droop control is advantageous in achieving satisfactory transient performance of the overall system.

Based upon the experience of frequency control in AC systems, a voltage-power (V-P) droop control scheme, as shown in Figure 2.28, is recommended by a number of publications as the primary control for MTDC systems [43, 91, 92, 94, 98-102]. In this scheme, DC voltage is regulated by modifying the converter active power reference in proportion to the DC voltage deviation. A larger droop gain K_{droop} or a smaller droop constant R_{droop} implies that the associated converter station plays a more important role in voltage regulation and its active power is more sensitive to DC voltage fluctuations.

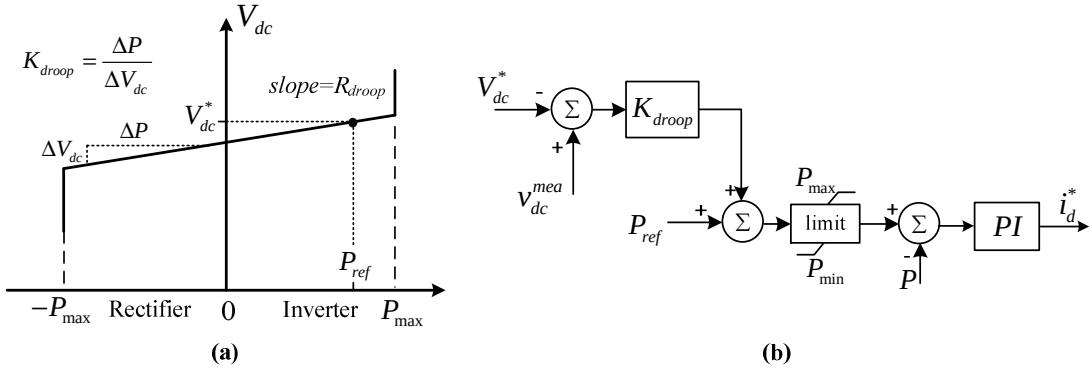


Figure 2.28: (a) Steady-State voltage-power droop characteristic; (b) Voltage-Power droop controller.

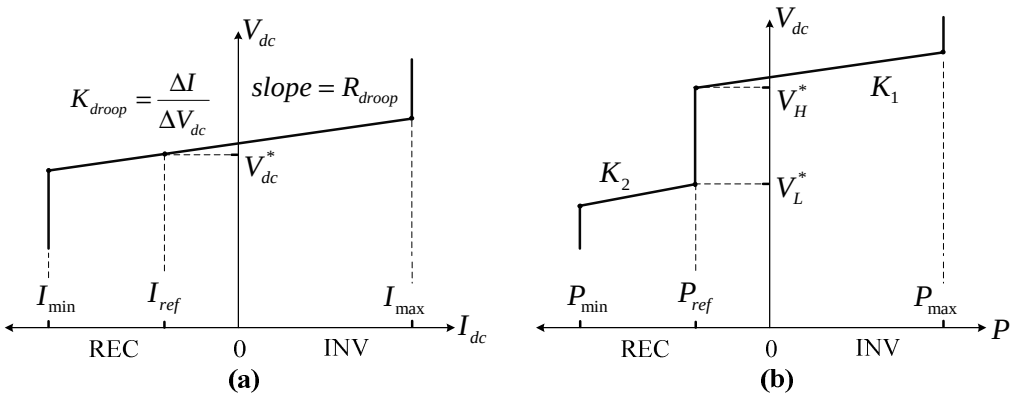


Figure 2.29: Steady-State characteristics of (a) voltage-current droop and (b) voltage-power droop with deadband.

Alternatively, as suggested in [67, 68, 75, 95, 96], distributed DC voltage control can be achieved by employing voltage-current (V-I) based droop characteristics, which have similar steady-state behaviours as V-P droop control [92, 102], as shown in Figure 2.29(a). MTDC stability analysis regarding the V-I droop control has not been discussed in previous literature. As the change of DC currents in a MTDC system relies on the variation of voltage differences between converters, this type of droop control is likely to be implemented as presented in Figure 2.30. The converter DC current is sensitive to the overall DC network dynamics and this increases the difficulty in generalising the control design.

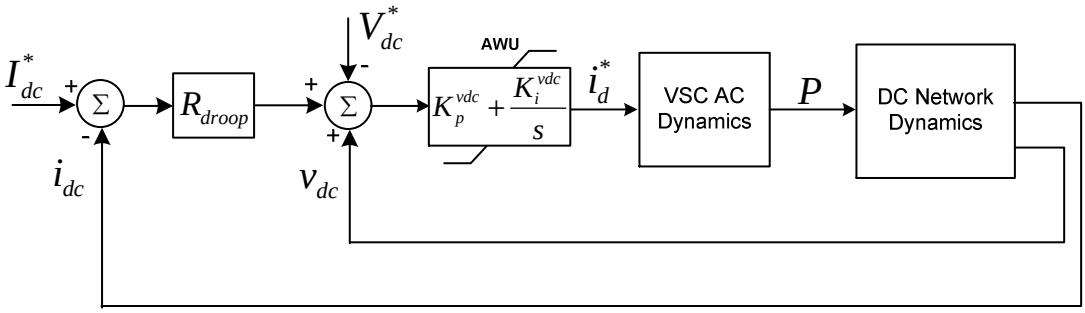


Figure 2.30: Controller implementation of the voltage-current droop characteristic.

2.3.4 Voltage Droop Control with Deadband

One drawback of engaging a large number of converters in droop control is that the active power transfer of all of these converters will be perturbed by DC voltage variations. This issue can be resolved by adding a secondary control on top of the droop control or using a deadband-based droop control [26, 103, 104], which can be interpreted as a combination of droop control and constant power/current control, as shown in Figure 2.29(b).

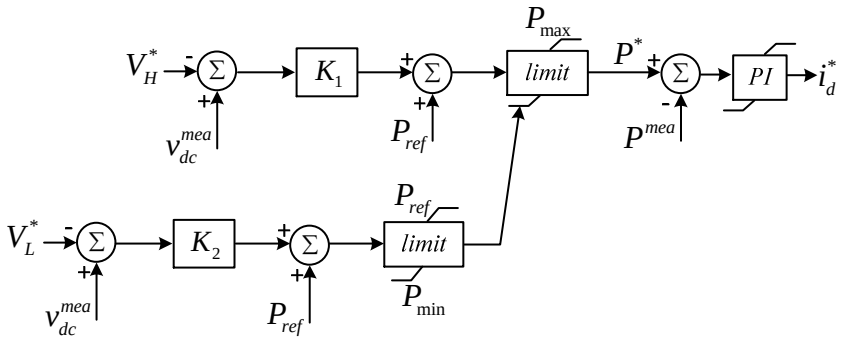


Figure 2.31: A basic control implementation of V-P droop with deadband.

A converter configured with this deadband control normally transfers a desired amount of power or current, and will only participate in voltage control if the voltage thresholds are violated. Multiple stages of droop control can be added to provide stronger support under overvoltage and undervoltage scenarios. A basic controller structure for V-P droop with a deadband is shown in Figure 2.31. It should be noted that the implementation of this deadband controller is highly dependent on the type of the droop controller.

2.3.5 Control Comparison

A four-terminal VSC-HVDC system, schematically shown in Figure 2.32, was employed to compare various DC voltage control strategies. All the converters stations are rated at ±320 kV, 1000 MVA, with a symmetrical monopole topology. This system was built in DIgSILENT PowerFactory (DSPF) based on the AVM discussed in 2.1.2. The transient simulations presented in this section are based on the nominal power flow shown in Figure 2.32.

Four control scenarios, with the steady-state characteristics outlined in Figure 2.33, are designed for the three GSCs to compare the dynamic behaviours of different voltage control strategies. The voltage and active power references and the droop constants are labelled. In the four cases, each terminal is designed to have a degree of DC voltage control capability. The highest priority of controlling the DC voltage is allocated to GSC3 while GSC1 is configured to have the lowest priority, which can be observed from the settings of voltage margins and droop gains.

The primary DC voltage control approach to be evaluated is Case 1, where droop control is adopted by all the GSCs. In Case 2, the droop characteristics of GSC1 and GSC2 are modified by including a deadband in order to maintain unperturbed power transfer as long as the converter DC voltage is within the accepted range. Voltage margin control is adopted in Case 3. A mixture of voltage margin control, droop control and slack bus control, which could be possible future multi-vendor systems, is employed in Case 4.

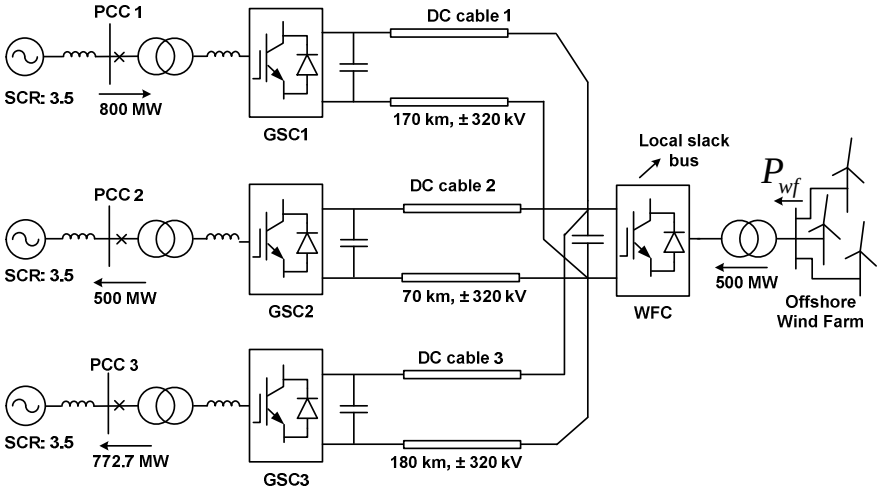
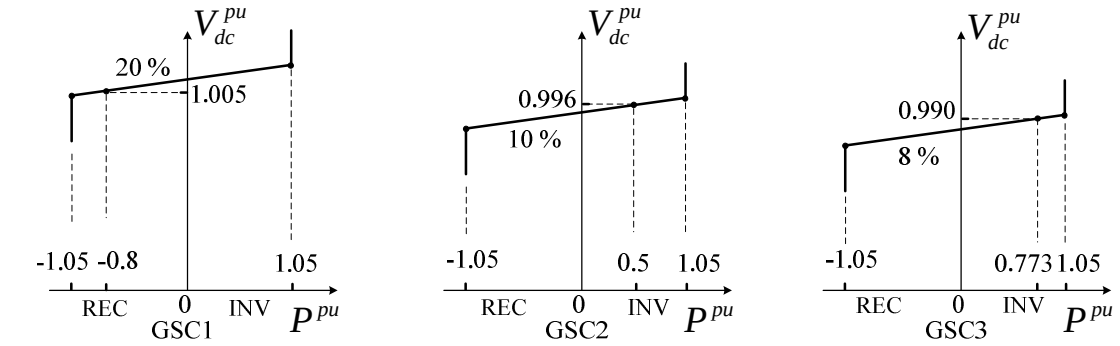
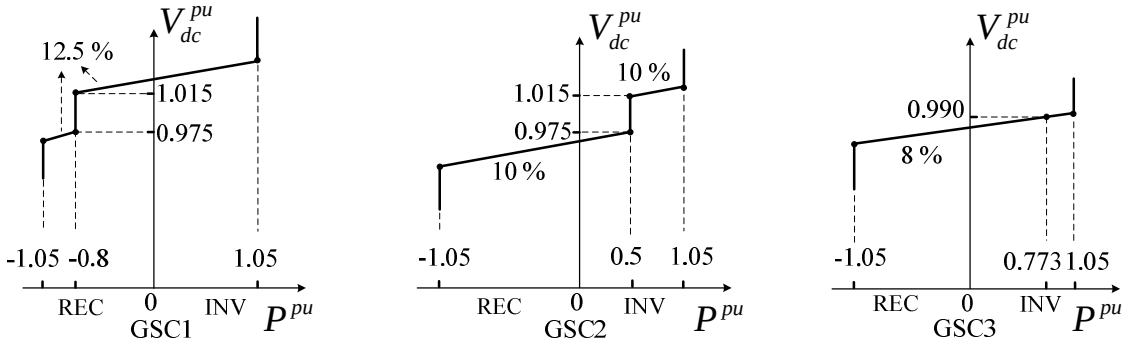


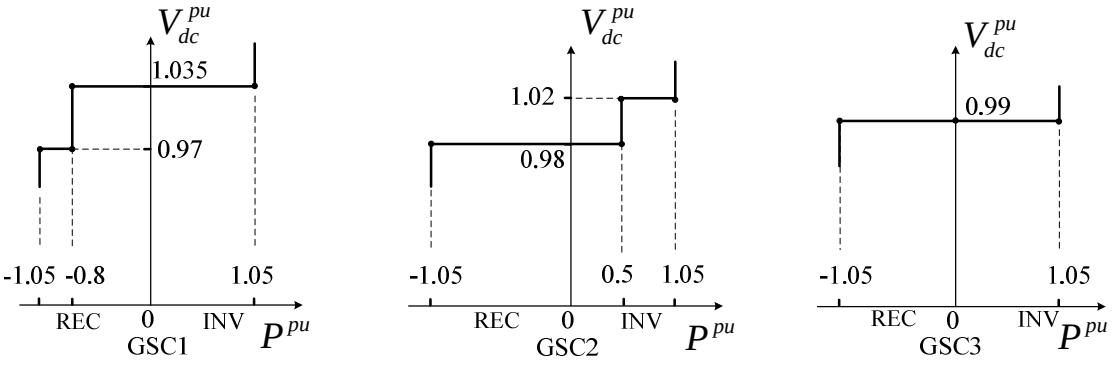
Figure 2.32: Four-Terminal VSC-HVDC test system.



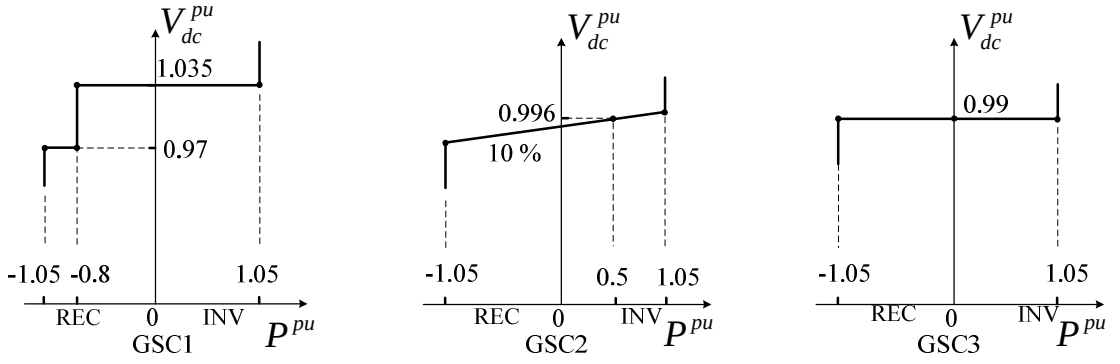
(a) Case 1: voltage droop



(b) Case 2: voltage droop with deadband



(c) Case 3: voltage margin



(d) Case 4: a mixture of voltage droop and margin

Figure 2.33: DC voltage characteristics for the three GSCs.

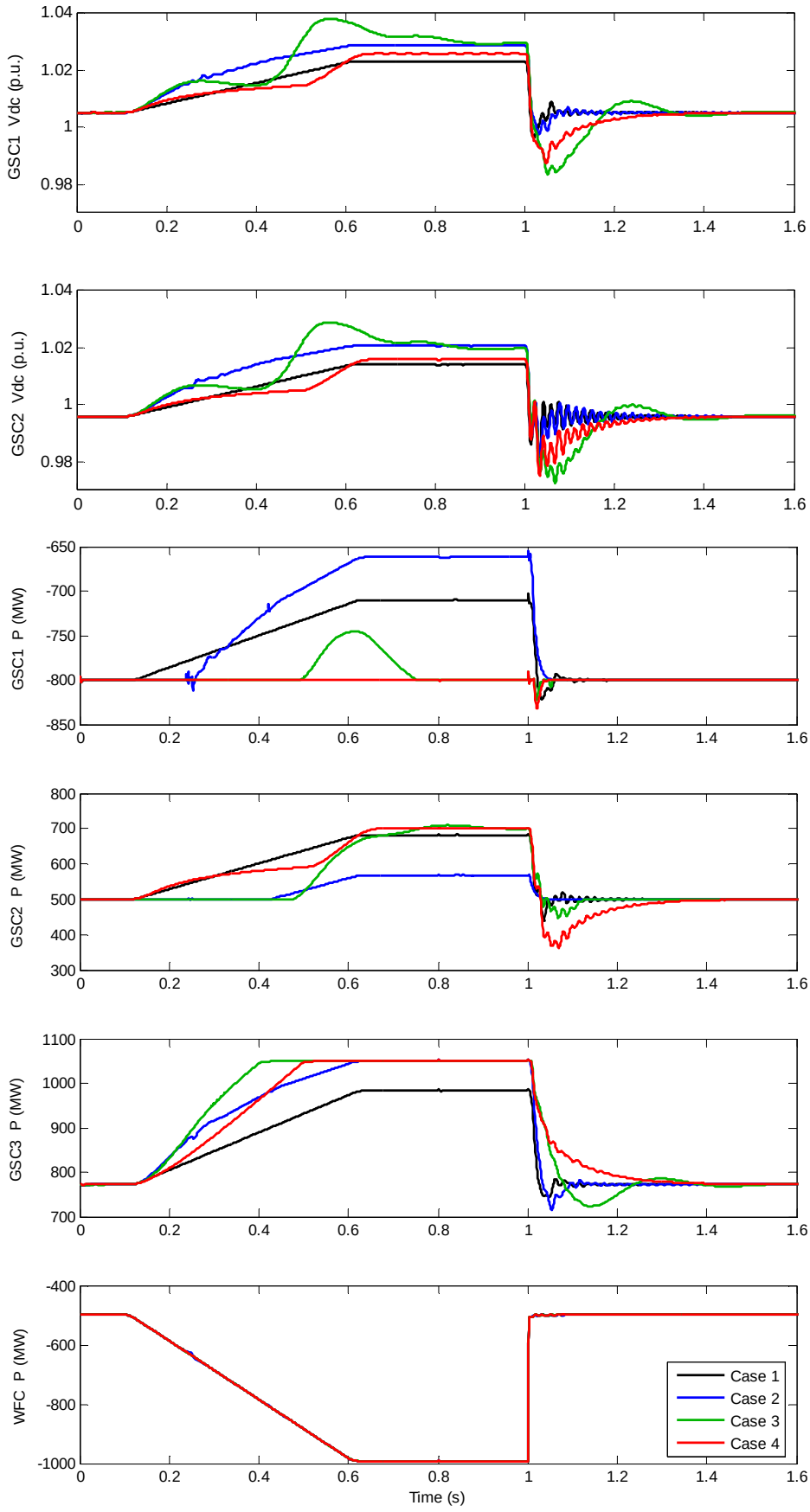


Figure 2.34: Simulation results of wind farm power variation for the four control cases.

Electromagnetic transient (EMT) simulations were performed for the proposed control schemes in DSPF. Selected responses of DC voltages and transmitted powers of the GSCs to a series of wind farm power variations, including a fast ramp starting from 0.1 s to 0.6 s and a sudden loss of half of the wind power generation in 1 s, are shown in Figure 2.34. These significant circumstances, which may be caused by single transformer block and generation shedding, are used to identify key DC system transients. The adaptive limit implementation is used for voltage margin controllers. Please note that inverter orientation is used for power flow direction ($P>0$ for inverter operations).

In terms of DC voltage behaviours, the best performance is provided by the voltage droop scenario due to its low steady-state error during the wind farm power ramp and its fast transient response to the loss of wind farm power. The simulation of Case 2 shows that the rate of DC voltage variation during the wind farm power becomes slower as more GSCs enter droop control mode from the active power mode. The transitions of the DC voltage regulating role can be clearly observed from the voltage margin scenario. Since the bandwidth of the constant DC voltage control is designed to be lower than the droop control, longer settling time is experienced by Case 3 and 4. The dynamic patterns of DC voltages of GSC1 and GSC2 are generally similar, except that the voltage of GSC2 is more oscillatory due to the DC system resonances and its closeness to the wind farm terminal.

The power sharing between the three GSCs in response to the wind farm power variations is clearly demonstrated in Figure 2.34. Unlike the other scenarios, in Case 1, GSC3 does not reach its power limit as the power imbalance is shared by all the GSCs according to the droop settings. Unlike the voltage droop scenario, the powers of GSC1 and GSC2 in Case 2 remain unperturbed in the initial stage of the wind power ramp. Despite that the deadband ranges for GSC1 and GSC2 are identical in Case 2, more power variation is encountered by GSC1 than GSC2, due to the relatively higher DC voltage at GSC1 caused by power flow directions and line impedances. The priority orders regarding the DC voltage regulation for the voltage margin scenario are clearly demonstrated. There is though a short period when GSC1 and GSC2 both operate in DC slack bus mode in Case 3. The smooth transient responses of Case 4 show a good collaboration of the three voltage control methods. When the DC system voltages are regulated together by droop control and slack bus control, more transient responsibility is taken by the droop controlled converter due its faster bandwidth.

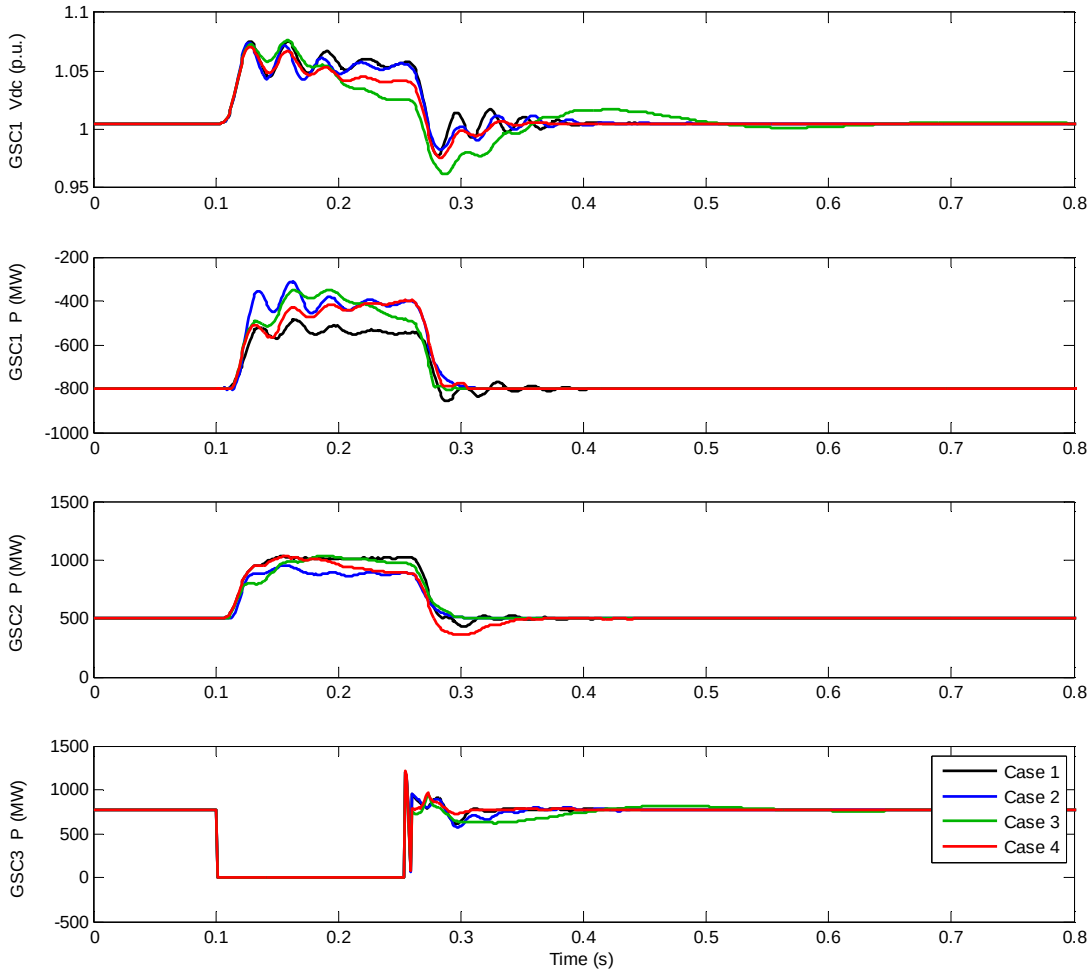


Figure 2.35: Simulation results of a three-phase fault at PCC3 for the four control cases.

Simulations of the four DC voltage control scenarios subjected to a severe three-phase balanced fault are shown in Figure 2.35. The fault at the PCC bus of GSC3 occurred at 0.1 s and was cleared after 150 ms. As the voltage at PCC3 drops very close to 0 pu during the fault, GSC3 loses its power transfer capability and the DC system responses are therefore predominantly affected by the DC voltage control capability of the remaining GSCs. Case 1 and Case 2 have different steady-state behaviours but show relatively similar dynamic performance, since the deadband control mainly operates in the droop control mode rather than the power control mode during severe transients. As the fault happens, the scenarios based upon droop control quickly reach a new stabilised operating point. The comparison of Case 3 and Case 4 shows that the relatively slow performance of Case 3 could be improved by replacing the voltage margin control of GSC2 with droop control. For a multi-vendor MTDC system, voltage droop control is suggested to be equipped in at least part of the converters since it can provide good transient support and collaborate well with other DC voltage control techniques.

Table 2.3: Controller types and upper voltage references for five cases of voltage margin control.

	Case 3a	Case 3b	Case 3c	Case 3d	Case 3e
Controller Type	Adaptive Lim	Adaptive Lim	Adaptive Lim	Hysteresis	Hysteresis
GSC1 V_H^* (pu)	1.025	1.015	1.01	1.025	1.015
GSC2 V_H^* (pu)	1.01	1.01	1.02	1.01	1.01

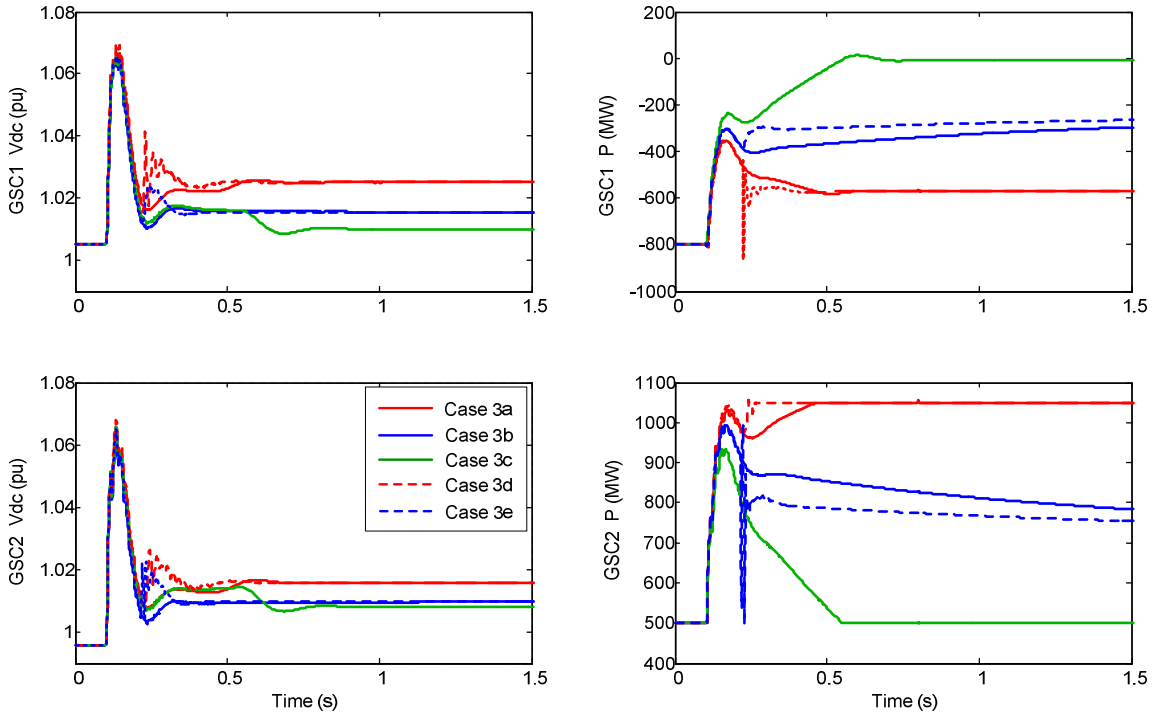


Figure 2.36: Dynamic responses of GSC1 and GSC2 to the loss of GSC3 for the five voltage margin cases.

Five voltage margin scenarios were further developed based upon Case 3, with the modified parameters shown in Table 2.3, to investigate the impacts of the voltage reference settings and the controller implementations on the transient performance of voltage margin control. Simulations of the loss of the voltage slack bus GSC3 were conducted for these scenarios, with the results shown in Figure 2.36.

The behaviour of Case 3a is satisfactory as the transition of the voltage regulating role is smooth and a new equilibrium operating point is quickly restored. Because the two upper voltage references V_H^* are designed to be close to each other in Case 3b, the DC voltages are controlled by the voltage controllers of GSC1 and GSC2 simultaneously and this results in a relatively long settling time. The converter powers behave in a ramping fashion when the GSCs employ identical bandwidth and both of them operate in voltage control mode, as shown in Case 3b and 3c. Unlike the other cases, the new voltage regulating role is taken by GSC1 instead of GSC2 in Case 3c. The transitions of the voltage control between GSCs for the hysteresis-based implementation in Case 3d are

faster than the adaptive limit method but with more high-frequency oscillations. Care has to be taken in setting the hysteresis band; since a low value will lead to frequent switching between controllers, while a large hysteresis threshold could cause multiple PI voltage controllers to be activated simultaneously. For an insufficiently large voltage margin setting, both of the two controller structures cannot deal with the severe voltage transients without experiencing long term interferences between converters.

In essence, regulating the DC system voltage using multiple PI controllers simultaneously should be avoided, as a steady-state power flow solution under such scenarios may not exist. The voltage margin between two converters should be configured at least larger than the maximum possible steady-state voltage drop across the two DC buses.

2.4 Chapter Summary

This chapter has discussed the MTDC modelling and control methodologies that will be employed to conduct further analysis into steady-state and dynamic characteristics of MTDC systems in the rest of this thesis.

Modelling and the hierarchical control structure of GSCs have been described. Key dynamics of the control systems for current control, PLL, active and reactive power control, AC and DC voltage control have been derived, and a number of tuning approaches have been applied to achieve reasonable dynamic performance and stability. Furthermore, critical trade-offs regarding the parameterisation of the controllers have been discussed. In addition, modelling of a simplified wind farm and control of an offshore WFC with a basic fault ride-through functionality have been presented.

Control implementations of various types of voltage margin and voltage droop characteristics have been presented. Furthermore, key features and transient performance of these voltage coordination strategies have been evaluated by a comparative study. Generally, droop control has superior reliability, stability and power sharing capability, and therefore it will be analysed further in the following chapters.

Chapter 3 Steady-State Analysis of MTDC

This chapter focuses on the power flow algorithm and linear analysis of the quasi-steady-state behaviours of MTDC systems. A generalised DC power flow algorithm is proposed in the first section to obtain an accurate power flow profile when complex DC voltage control characteristics are employed. This is followed by a brief discussion of the key factors which determine the PQ capability of VSC-HVDC. To provide a clearer understanding of the power flow variations after a disturbance or reference change, the analysis of the linearised power flow equations based upon droop control is presented in Section 3.3. In Section 3.4 a possible DC voltage control hierarchy consisting of three stages is presented for future DC grids, with the droop control acting as the primary stage.

3.1 Power Flow Algorithms for MTDC

Droop control is likely to be employed in the interests of MTDC reliability and stability, however the use of the droop characteristics could significantly increase the complexity of power flows. Under such situations, the operating point and power sharing of the system vary with power disturbances such as those imposed by wind farm power fluctuations and converter outages. Since a grid supervisory control relying on telecommunications may not be available, and in any case this control would be likely to update the converter set-points only periodically in a very slow manner, the impact of the quasi-steady-state droop lines on the DC power flow needs to be fully understood by the grid operators. Moreover, computation of the optimised set-points by the supervisory control may require such power flow techniques incorporating droop characteristics.

Most of previous research has focused on solving MTDC power flow without taking detailed DC voltage control into consideration. A unified power flow method for integrated AC/MTDC systems is proposed in [105] by solving the AC and DC power flow equations simultaneously. In the AC/DC power flow algorithm discussed in [106, 107], the AC and DC network equations are solved sequentially in each iteration. Research on power flow of DC networks is provided in [98, 108-110]. Basic DC power flow analysis has been applied in [109] and [110] to represent the DC transmission losses and to optimise the voltage references. DC slack bus voltage control has been used by most papers examining power flow analysis. The sequential AC/MTDC method is updated by including the V-P droop in [111]. V-P droop is assessed in detail using linear

analysis in [98], however a nonlinear power flow is not performed. Both AC and DC power flow algorithms are normally based upon Newton iteration method. Strong negative-sequence-harmonic interactions between LCC-HVDC and weak AC systems may result in divergence issues when fixed point iteration is employed [112, 113]. This potential problem is not investigated here for VSC-HVDC systems because the low-order harmonic content of MMC converter is sufficient low and the resulting AC/DC harmonic interaction is insignificant. Furthermore, the focus of this section is DC power flow rather than AC/DC harmonic load flow. This section aims to provide a range of power flow solutions for MTDC systems with different voltage control techniques.

3.1.1 Integration of AC/DC Power Flow

Since MTDC systems essentially serve AC networks, a methodology for the integration of the AC and DC power flow models is presented in this section, with the associated flow chart illustrated in Figure 3.1. The AC and DC power flow are computed separately, as the power flow of the DC system is intrinsically determined by the converter DC voltage/power control setting. This method utilises the fact that for DC side V-I/V-P droop control of VSC-HVDC, the power flows within the DC system can be solved separately from the AC power flows. The approach starts by solving the DC power flow, and the computed DC side powers will then be utilised for the initialisation of AC power flow. The power loss is calculated iteratively according to the results obtained from the up-to-date AC power flow, with the convergence indicated by appropriate active power at the PCC.

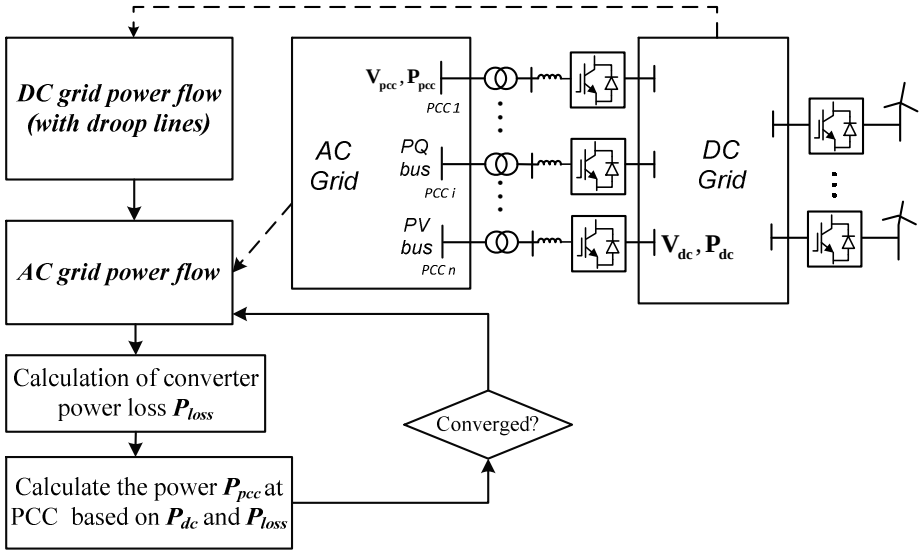


Figure 3.1: Integration of MTDC power flow with AC power flow.

Unlike the unified AC/DC power flow algorithms, this method allows existing AC power flow models to incorporate the MTDC models with no significant modification. The key step of this algorithm is the DC system power flow with droop lines, which will be analysed in detail in the following sections.

From the DC power flow point of view, the converter DC bus can be represented by a fixed or variable V_{dc} bus or P_{dc} bus, or more generally, the droop DC voltage characteristics. To facilitate AC power flow calculation, the PCC bus of the converter station can be described as a PV or PQ bus, depending on the reactive power control design.

A simplified power loss model is provided here to link the converter DC side power with the power injection into the AC grid at the PCC bus. According to the detailed power loss analysis for MMC performed in [114], the conduction loss of upper arm (UA) and lower arm (LA) can be represented by:

$$P_{cond}^{UA} = V_o N_s \cdot \left| \frac{I_{ac}(\omega t)}{2} + \frac{I_{dc}}{3} \right| + \frac{R_o N_s}{N_p} \cdot \left[\frac{I_{ac}(\omega t)}{2} + \frac{I_{dc}}{3} \right]^2 \tag{3.1}$$

$$P_{cond}^{LA} = V_o N_s \cdot \left| \frac{I_{ac}(\omega t)}{2} - \frac{I_{dc}}{3} \right| + \frac{R_o N_s}{N_p} \cdot \left[\frac{I_{ac}(\omega t)}{2} - \frac{I_{dc}}{3} \right]^2 \tag{3.2}$$

where N_s and N_p represent the number of sub-modules in series and in parallel in each arm respectively, and V_o and R_o denote the on-state slope voltage and resistance of IGBT/diode. The assumption that the IGBT and diode have similar on-state characteristics is made to greatly simplify the power loss calculation with only a slight degradation on the accuracy with appropriate parameter choice. The total conduction loss for the converter valve can then be computed by (3.3).

$$P_{cond} = 3 \cdot \frac{1}{2\pi} \cdot \int_0^{2\pi} \left(P_{cond}^{UA} + P_{cond}^{LA} \right) d(\omega t) \tag{3.3}$$

Switching loss is derived based on the general form [115]:

$$P_{switch} = 6 N_s N_p \cdot f \cdot \sum_{cycle} \left(E_{on}(I) + E_{off}(I) + E_{rec}(I) \right). \tag{3.4}$$

The result in [114] suggests that the switching loss only corresponds to a fraction of the total MMC valve loss. Accurate switching loss calculation requires complex nonlinear modelling however this level of modelling fidelity may not be necessary for power flow

calculations. The average phase current is used in (3.4) for simplification, as suggested in [116].

By combining (3.3) and (3.4), the total loss of the converter station can be represented as:

$$P_{loss} = K_1 \cdot |I_{ac}| + K_2 \cdot |I_{dc}| + (K_3 + 3R) \cdot I_{ac}^2 + K_4 \cdot I_{dc}^2 \tag{3.5}$$

where R is the aggregated resistance of converter transformer and the equivalent converter reactor, and $K_{1\text{-}4}$ are constants. More detailed derivations are provided in Appendix B.1.

3.1.2 Power Flow of MTDC with a Slack Bus

Power flow analysis of an MTDC system aims to obtain the operating point of every DC terminal in the grid, with provided generation, loading and control conditions. The problems are usually represented by a series of nonlinear relationships between voltages and currents. The power flow algorithms proposed here are based on the well-known Newton-Raphson (NR) method [117, 118].

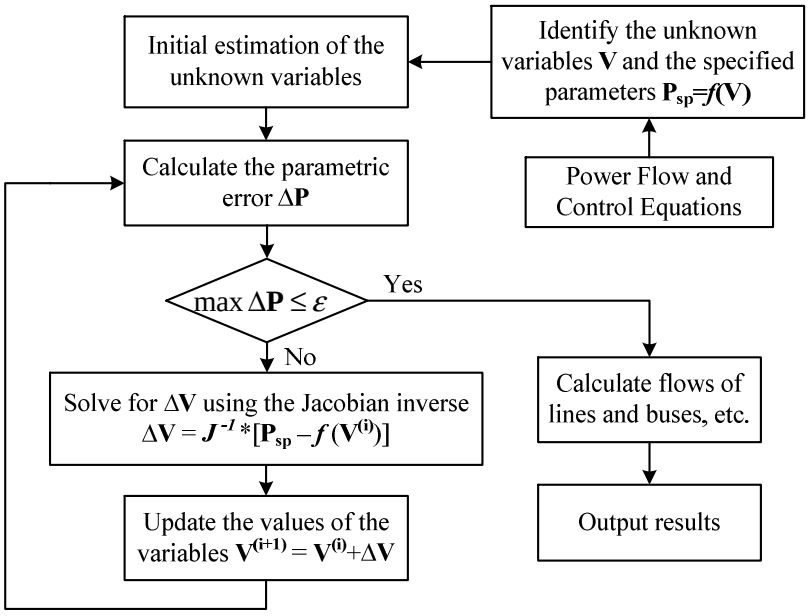


Figure 3.2: Flow chart of the NR method for MTDC power flow.

A simplified flow chart of the numerical iterative procedure for solving a generic MTDC power flow is shown in Figure 3.2. Firstly, with the system represented by the power flow and control equations, the unknown variables **V** and the specified parameters $\mathbf{P_{sp}}$ need to be selected. In MTDC studies, normally, DC voltages are selected as the variables, and the power quantities are chosen to be the specified parameters, which can be represented using the nonlinear parametric functions $\boldsymbol{f}$ **(V)**.

Based upon the existing estimates of the unknown voltages, the Jacobian matrix **J** is composed of partial derivatives of the functions ***f* (V)**:

$$\mathbf{J} = \frac{\partial \mathbf{P}_{sp}}{\partial \mathbf{V}} = \frac{\partial \mathbf{f}(\mathbf{V})}{\partial \mathbf{V}}. \tag{3.6}$$

Based on the inverse of the Jacobian matrix, the new set of the voltage estimates are calculated by

$$\mathbf{V}^{(i+1)} = \mathbf{V}^{(i)} + \mathbf{J}^{-1} \cdot \left[\mathbf{P}_{sp} - \mathbf{f}\left(\mathbf{V}^{(i)}\right) \right] \tag{3.7}$$

where $\mathbf{V}^{i}$ and $\mathbf{V}^{(i+1)}$ are the *i*th and (*i+1*)th estimates respectively. The estimated voltages are updated iteratively until an acceptable tolerance has been achieved for the mismatch between the specified parameters and those computed using the estimated variables.

In a DC system containing *n* terminals, the steady-state relationship between the DC voltages and currents can be written as

$$\mathbf{I}_{dc} = \mathbf{Y} \cdot \mathbf{V}_{dc} \tag{3.8}$$

where $\mathbf{I}_{dc}$ is the vector of DC currents flowing from converters into the DC network, $\mathbf{V}_{dc}$ is the DC voltage vector and **Y** is the admittance matrix of the network.

For a symmetrical monopole HVDC system, if $\mathbf{V}_{dc}$ is comprised of pole-to-pole DC voltages, the admittance matrix needs to be calculated based on the series resistance of the positive-pole and negative-pole cables. Per unit (pu) values are used for the power flow studies here, and the differences between the bipolar and monopolar configurations can thus be disregarded.

As analysed by the majority of previous literature, in a basic power flow problem for a DC grid of *n* buses, the DC voltage of the slack bus is provided. The vector of the (*n*-1) specified parameters are comprised of given nodal power injections or line branch power flows. Wind farm terminals are assumed to be power buses, since they are normally not equipped with proper DC voltage control capability.

The power injected to the MTDC system by the *i*th terminal can be represented as

$$P_i = V_i \cdot \left(\sum_{j=1}^{n} Y_{ij} V_j \right). \tag{3.9}$$

The branch power flow from the *i*th terminal to the *j*th terminal is:

$$P_{ij} = V_i \cdot Y_{ij}\left(V_j - V_i\right). \tag{3.10}$$

Accordingly, the elements of the Jacobian matrix associated with (3.9) and (3.10) can be derived as (3.11) and (3.12), respectively. With the (*n*-1) nonlinear equations tackled by the NR method, this basic power flow with the slack bus is solved.

$$\frac{\partial P_i}{\partial V_i} = 2Y_{ii}V_i + \sum_{j=1, j\neq i}^{n} Y_{ij}V_j, \quad \left.\frac{\partial P_i}{\partial V_j}\right|_{j\neq i} = V_i Y_{ij} \tag{3.11}$$

$$\frac{\partial P_{ij}}{\partial V_i} = Y_{ij}V_j - 2Y_{ij}V_j, \quad \frac{\partial P_{ij}}{\partial V_j} = Y_{ij}V_i, \quad \left.\frac{\partial P_i}{\partial V_k}\right|_{k\neq i, k\neq j} = 0 \tag{3.12}$$

In an MTDC system with large power flows and long transmission distances, the voltages might be significantly different from each other. From the system planning point of view, it might be more reasonable to specify the mean voltage of all the buses instead of that of the slack bus. However, this may present a new problem, i.e. how to solve the power flow with the given powers and the mean voltage. An algorithm has been developed from the former power flow method to solve this problem.

Under this circumstance, all the *n* voltages are configured to be the variables and an additional equation is built to represent the average voltage. The supplementary parametric equations and the associated Jacobian element are

$$V_{av}(\mathbf{V}) = \frac{1}{n}\sum_{i=1}^{n} V_i, \quad \frac{\partial V_{av}}{\partial V_i} = \frac{\partial}{\partial V_i}\left(\frac{1}{n}\sum_{i=1}^{n} V_i\right) = \frac{1}{n} \tag{3.13}$$

where V_{av} is the specified average voltage of the grid. The other Jacobian elements can be computed according to (3.11) and (3.12), as the power flow equations remain as (3.9) and (3.10). If the power injections are specified for all terminals except for the terminal *m*, this bus can be seen as a "floating slack bus" aiming to achieve the given mean voltage. This power flow does not stand for any DC grid control strategy, but it could be very useful for system planning and converter reference setting.

From the control perspective, the two methods discussed in this section can be employed to configure the nominal voltage and power/current references for the droop line set.

3.1.3 Power Flow of MTDC with Droop Control

The DC voltage-power (V-P) and voltage-current (V-I) characteristics are the two most widely proposed droop control approaches. Grid operators need to understand how the power flow works if the communication is lost; furthermore, they need to understand the primary voltage and power variations after a disturbance, since the non-standardised higher level control is not likely to update the droop references very frequently.

3.1.3.1 Voltage Power (V-P) Droop

Generally, if the V-P droop is employed by a DC grid of *n* buses, the power flow problem can be described as how to solve the operating point of the system with a series of *m* specified V-P characteristics and (*n*-*m*) given nodal or branch powers.

If V-P droop is used for terminal *i*, the converter rectifying power would be controlled according to[4]:

$$P_i = K_i(V_i^* - V_i) + P_i^* \tag{3.14}$$

where the voltage and power references of the droop line are denoted by V_i^* and P_i^*. The droop control gain K_i indicates the sensitivity of the converter power to the local DC voltage. Note that rectifier orientation is used in this chapter for the direction of DC power and current[5].

By setting *K* to zero, a VSC terminal in power control mode or with known power generation can also be represented by (3.14). This feature of V-P droop makes it easier to analyse the power flow of the grid in a more generalised way.

Voltages of all DC buses are selected as the variables to be solved. The vector of the specified parameters is comprised of the power references of the converters in droop control and the given power profile related to other converters:

$$\mathbf{P}_{sp} = [P_1^* \quad P_2^* \quad \cdots \quad P_n^*]^T. \tag{3.15}$$

[4] The droop gain and droop constant that are normally represented by K_{droop} and R_{droop} in other chapters, are written as *K* and *R* in this chapter, since a number of other subscripts and superscripts need to be employed in this chapter.

[5] **Please note that only in this chapter, converter power is defined to be positive under rectifier operation. In the other chapters, inverter orientation is used instead (i.e. P>0 for inverter operation).**

The nonlinear functions related to the given nodal and branch powers are shown in (3.9) and (3.10). By combining the power flow equation (3.9) and the control equation (3.14), the parametric functions are computed as:

$$f_i(\mathbf{V}) = V_i^2 Y_{ii} + V_i \sum_{j=1, j\neq i}^{n} Y_{ij} V_j - K_i V_i^* + K_i V_i = P_i^*. \tag{3.16}$$

The corresponding Jacobian elements can thus be obtained:

$$\frac{\partial P_i}{\partial V_i} = 2Y_{ii}V_i + \sum_{j=1, j\neq i}^{n} Y_{ij} V_j + K_i, \quad \left.\frac{\partial P_i}{\partial V_j}\right|_{j\neq i} = V_i Y_{ij}. \tag{3.17}$$

The offline converters can be considered as a specific V-P droop with both the gain K and the power reference P^* equal zero. If there are no branch power flows specified, all the nonlinear equations and the Jacobian elements can be written as (3.16) and (3.17) respectively.

3.1.3.2 Voltage-Current (V-I) Droop

The rectifying power of terminal i equipped with a typical V-I droop can be represented as:

$$P_i = V_i \cdot \left[K_i (V_i^* - V_i) + I_i^* \right] \tag{3.18}$$

where the current reference is represented by I_i^*. Considering that the power P_i can also be derived as (3.9), the following parametric function is obtained for terminals in V-I droop:

$$f_i(\mathbf{V}) = \left(Y_{ii} + K_i\right) V_i^2 + V_i \left(\sum_{j=1, j\neq i}^{n} Y_{ij} V_j - \left(I_i^* + K_i V_i^* \right) \right) = 0. \tag{3.19}$$

Accordingly, the specified parameters are obtained as:

$$\mathbf{P}_{sp} = [\underbrace{0 \quad 0 \quad \cdots \quad 0}_{V-I \text{ droop control}} \quad \underbrace{P_{m+1} \quad P_{m+2} \quad \cdots \quad P_n}_{P \text{ control}}]^T \tag{3.20}$$

where zero is chosen to indicate the effectiveness of the droop control, while the other (n-m) parameters are comprised of the specified nodal or line powers. The Jacobian elements associated with (3.19) are derived as:

$$\frac{\partial f_i}{\partial V_i} = 2(Y_{ii} + K_i)V_i + \sum_{j=1, j\neq i}^{n} Y_{ij} V_j - \left(I_i^* + K_i V_i^* \right) \tag{3.21}$$

$$\left.\frac{\partial f_i}{\partial V_j}\right|_{j\neq i} = V_i Y_{ij}. \tag{3.22}$$

So far, the steady-state equations for converters in slack bus control, constant power control, basic V-P and V-I droop control, and off-line operations have been addressed. Therefore, generalised MTDC power flow can be solved for DC grids with a mixture of these control strategies by appropriately integrating these equations using the NR method.

3.1.4 Power Flow with Generalised V-P/V-I Characteristics

In the algorithms discussed previously, the operating mode of a converter is fixed and the converter limits have not been considered in detail. Furthermore, the droop control used in Section 3.1.3 has not been sufficiently generic. Realistically, the droop characteristics could be a combination of multiple linear or nonlinear functions of DC voltage.

An algorithm is proposed here to solve the MTDC power flow involving more complex V-P/V-I characteristics with multiple control modes, such as voltage margin control or voltage droop with deadband. This generalised approach can be applied to most types of VSC power and DC voltage control. Converter limit checking is included by enabling an additional outer iteration loop. The key procedure of this method is to iteratively update the parameters of V-P or V-I functions according to the newly estimated voltages.

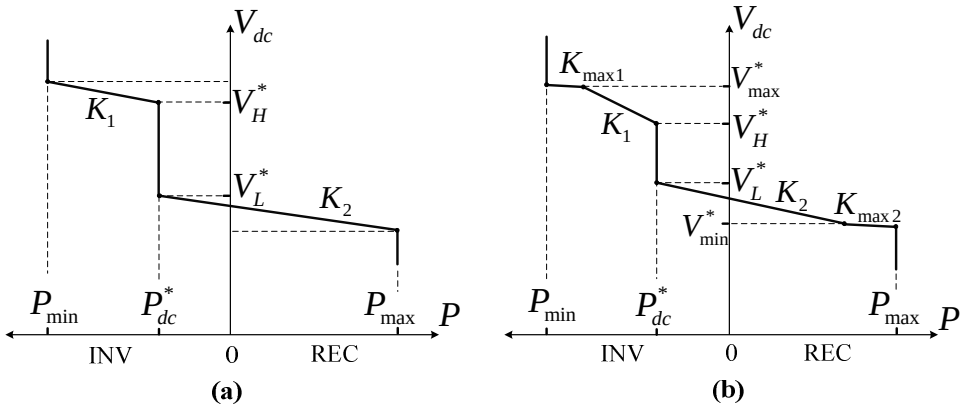


Figure 3.3: (a) V-P droop with deadband; (b) V-P droop with deadband and voltage limits

Each voltage droop line is essentially a function between the voltage and the desired current/power output. For example, the voltage droop with a deadband and voltage limit is comprised of multiple linear functions, as shown in Figure 3.3. Differentiated by the voltage level, these linear functions of the converter power can all be represented in the form of typical droop lines:

$$P_{dc}\left(V_{dc}\right)=\begin{cases} K_{\max 1}\left(V_{\max}^{*}-V_{dc}\right)+\left[K_1\left(V_H^{*}-V_{\max}^{*}\right)+P_{dc}^{*}\right], \text{ for } V_{dc}\geq V_{\max}^{*} \\ K_1\left(V_H^{*}-V_{dc}\right)+P_{dc}^{*}, \qquad \text{for } V_H^{*}<V_{dc}<V_{\max}^{*} \\ 0\cdot\left(V_H^{*}-V_{dc}\right)+P_{dc}^{*}, \qquad \text{for } V_L^{*}\leq V_{dc}\leq V_H^{*} \\ K_2\left(V_L^{*}-V_{dc}\right)+P_{dc}^{*}, \qquad \text{for } V_{\min}^{*}<V_{dc}<V_L \\ K_{\max 2}\left(V_{\min}^{*}-V_{dc}\right)+\left[K_2\left(V_L^{*}-V_{\min}^{*}\right)+P_{dc}^{*}\right], \text{ for } V_{dc}\leq V_{\min}^{*}. \end{cases} \tag{3.23}$$

In fact, like the constant power control of an effective K of zero, the slack bus control can be modelled as another extreme case of droop:

$$P(V_{dc})=K\left(V^{*}-V_{dc}\right), \quad K\to\infty. \tag{3.24}$$

With the gain of the slack bus approximated by a sufficiently large number, a good accuracy can be achieved. Based on this, the voltage margin characteristic can be considered as a specific case of the voltage droop with a power deadband. Basically, all the linear stages of different voltage control methods can be represented in the form of the droop function. This will significantly facilitate the power flow programming.

More generally, if the steady-state V-I function $I_i(V_i)$ or V-P function $P_i(V_i)$ is discontinuous at some stages, the power flow equation representing the ith terminal can be written as:

$$f_i=V_i\cdot I_i(V_i)-V_i\cdot\sum_{j=1}^{n}Y_{ij}V_j=0 \tag{3.25}$$

$$f_i=P_i(V_i)-V_i\cdot\sum_{j=1}^{n}Y_{ij}V_j=0 \tag{3.26}$$

In the kth iteration, using the estimated voltages $\mathbf{V}^{(k)}$, the associated Jacobian elements can be derived as:

$$\frac{\partial f_i}{\partial V_i^{(k)}}=I_i(V_i^{(k)})+V_i^{(k)}\cdot\frac{dI_i(V_i^{(k)})}{dV_i^{(k)}}-2Y_{ii}V_i^{(k)}-\sum_{j=1,j\neq i}^{n}Y_{ij}V_j^{(k)} \tag{3.27}$$

$$\frac{\partial f_i}{\partial V_i^{(k)}}=\frac{dP_i(V_i^{(k)})}{dV_i^{(k)}}-2Y_{ii}V_i^{(k)}-\sum_{j=1,j\neq i}^{n}Y_{ij}V_j^{(k)}\,. \tag{3.28}$$

With the equations derived for each control scheme, the generalised algorithm can then be utilised to integrate them together, with the corresponding flow chart illustrated in Figure 3.4. The algorithm consists of an outer iteration loop to check converter limits and an inner iteration loop to perform NR calculations. Two important features of the inner

loop are to select the correct V-I or V-P functions and to ensure a non-singular Jacobian matrix. The Jacobian matrix is indirectly verified by comparing the power flow results obtained from this algorithm and the DSPF simulation results.

The control modes and the corresponding parameters of the ***I***(**V**) and ***P***(**V**) functions will be kept up-to-date in each iteration according to the newest set of voltage estimates. Specifically, if the voltage characteristics are linear, the DC voltages act as an indication of the values of the gain K and the references (V^*, P^*, I^*) which need to be used for the next iteration. If the converter limit mode is activated by the outer iteration loop, the parameters need to be fixed to the limit throughout the inner NR iteration loop.

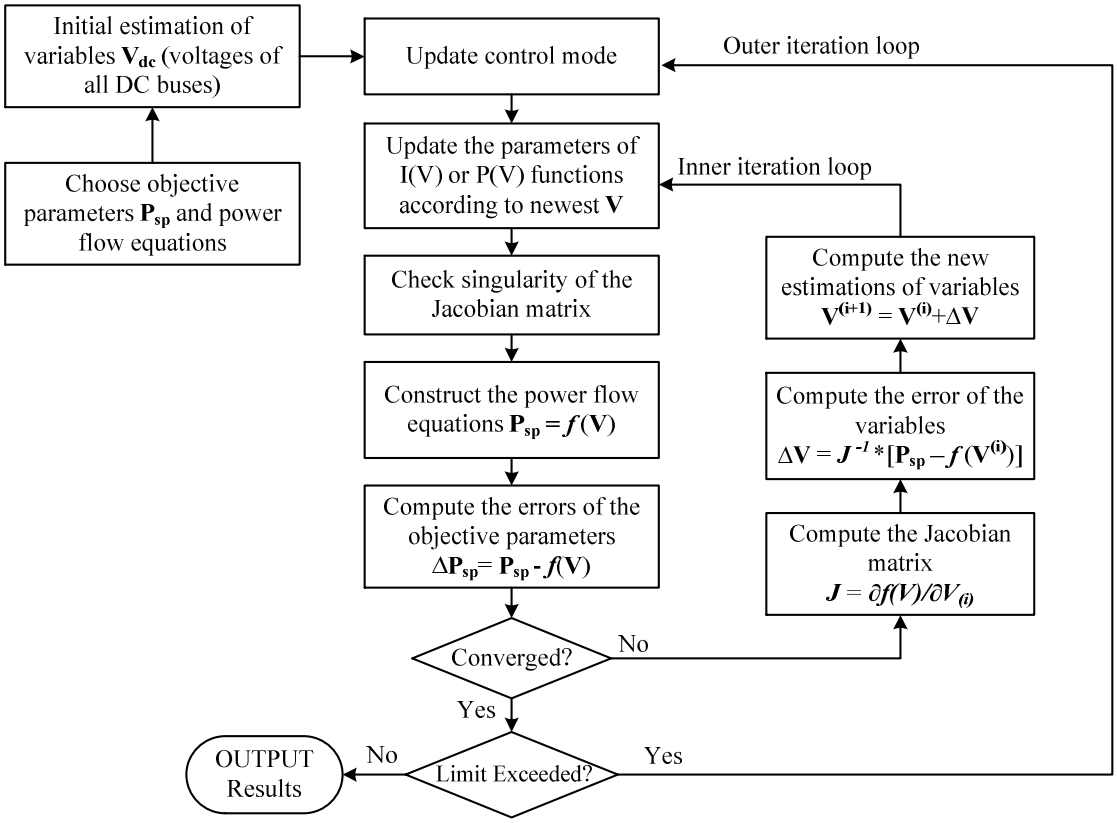


Figure 3.4: Flow chart of the DC power flow with generic droop lines.

Under certain situations where the voltage estimates indicate that all the terminals ought to be in deadband mode or constant power/current mode, the corresponding Jacobian matrix will not be invertible as the voltages will effectively become unsolvable. In this case, a temporary approximation is used to modify the effective K of the deadband control mode from zero to a small value such as 0.5. This will therefore avoid the singularity of the Jacobian and allow the iteration to continue. When the voltage estimates correspond to a system state where at least one converter is in voltage control mode ($K \neq 0$), the gains for all the deadband modes will be set back to zero. This problem

will not occur if no deadband is involved in the droop lines. The approximation will not affect the final power flow results.

After the convergence of the inner iteration, the resulting converter powers or currents will be examined, as it is noted that the converter limits are not considered in the inner iteration loop. If the limits are exceeded, the related terminals will be switched to constant power or constant current mode, and the calculation will enter another series of inner NR iterations. Either DC power or DC current limit, or a combination of both, can be implemented. It may be more reasonable to employ a power limit under an overvoltage condition, while a current limit could be required under an undervoltage circumstance. The iteration stopping criteria is $|\boldsymbol{P}_{sp}-\boldsymbol{P}(\boldsymbol{V})|<\epsilon$, where ϵ is the tolerance indicating the convergence of the iteration.

3.1.5 Case Studies and Simulations

This section demonstrates the performances of the proposed power flow methods, and it evaluates the quasi-steady-state behaviours of various DC voltage control techniques after transient events including wind power changes and converter outages. The power flow algorithms and the case studies are implemented in MATLAB.

3.1.5.1 Test System and Set of Droop Lines

A five-terminal VSC-HVDC network, shown in Figure 3.5, is established as the candidate DC grid model. All the converter stations are rated at 1000 MW, ± 320 kV, with symmetrical monopole topology. This model is configured to enable a primary power flow from GSC1 to GSC2 and GSC3, with the integration of two offshore wind farms. The aggregated resistance of the positive-pole and negative-pole submarine cables is provided.

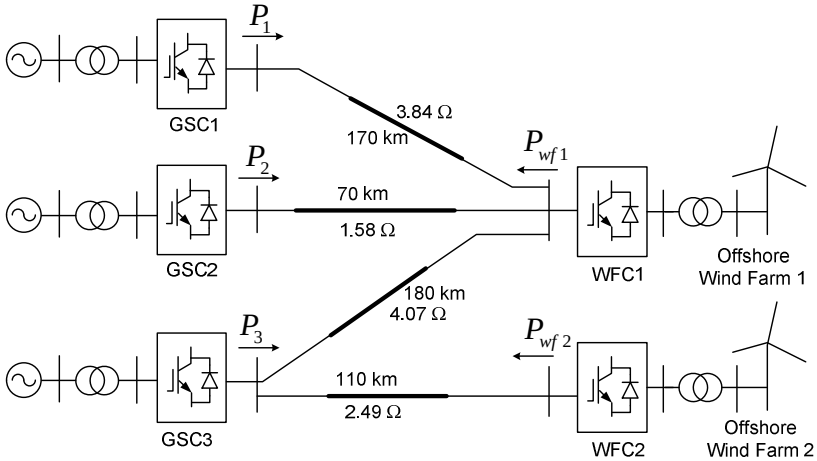


Figure 3.5: Five-Terminal test network for power flow studies.

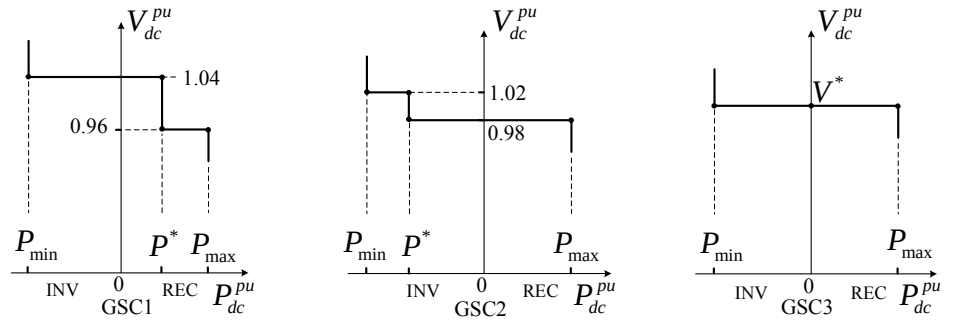
Presented in Figure 3.6, the five control scenarios comprising various combinations of V-P/V-I characteristics, are designed for the three GSCs. All the parameters are shown in per unit. DC power and current limits of 1.05 pu are employed in the five scenarios. The nominal operating point of the system, shown in Table 3.1, is obtained via the method shown in Section 3.1.1, with specified powers for all the converters except GSC3 and an average DC voltage of 0.995 pu. These power flow results are employed as the references (V^*, P^*, I^*) for all the five sets of droop lines [119].

Table 3.1: Power flow results of the nominal operating point.

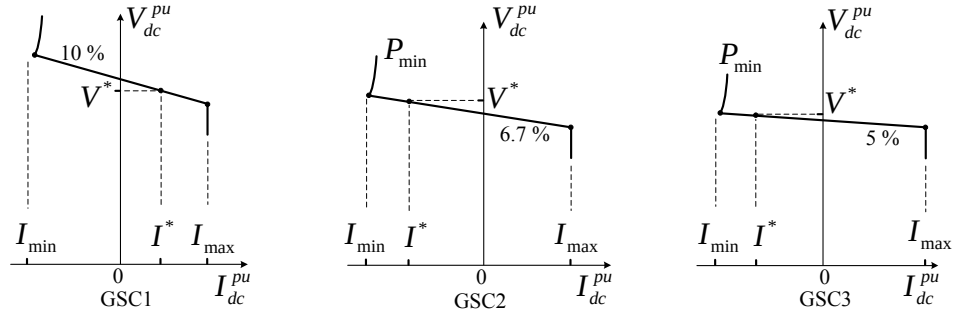
Converter	*GSC1*	*GSC2*	*GSC3*	*WFC1*	*WFC2*
V_{dc} *(pu)*	0.9999	0.9921	0.9923	0.9953	0.9954
P_{dc} *(pu)*	0.5000	-0.8000	-0.7927	0.6000	0.5000
I_{dc} *(pu)*	0.5000	-0.8063	-0.7989	0.6029	0.5023

The voltage margin between the GSCs in Case 1 is configured to be relatively large in order to avoid unwanted control interactions. For each VSC, identical droop constants are utilised in the V-I droop in Case 2 and the V-P droop in Case 3. In Case 2, the maximum power is limited instead of maximum current under inverter operation. Unlike the margin control, the deadbands for GSC1 and GSC2 in Case 4 are arranged to be close to each other. The voltage limits in Case 5 allow a tighter control of the post-transient voltage.

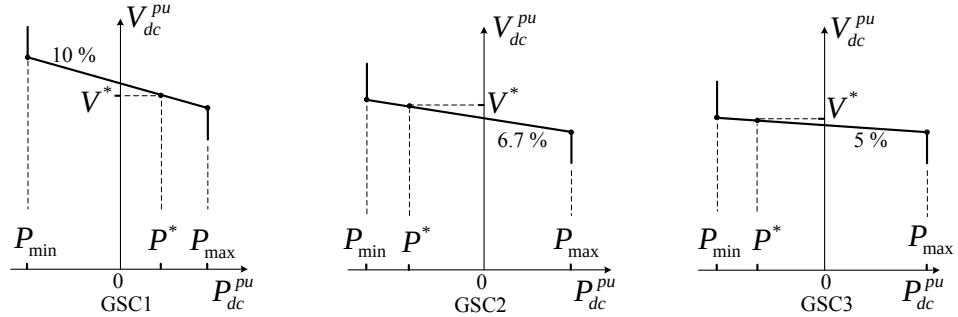
The generalised procedure proposed in Section 3.1.4 is employed in all the scenarios, integrating the power flow equations listed in sections 3.1.2 to 3.1.4. An equivalent droop gain of 10^8 is used for the voltage margin control. It has been tested that the errors due to this approximation are within 10^{-8} for DC voltages and are less than 10^{-10} for powers.



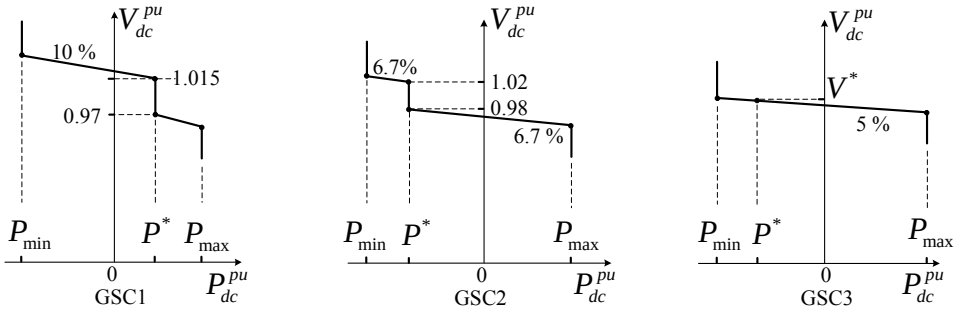
(a) Case 1: voltage margin characteristics



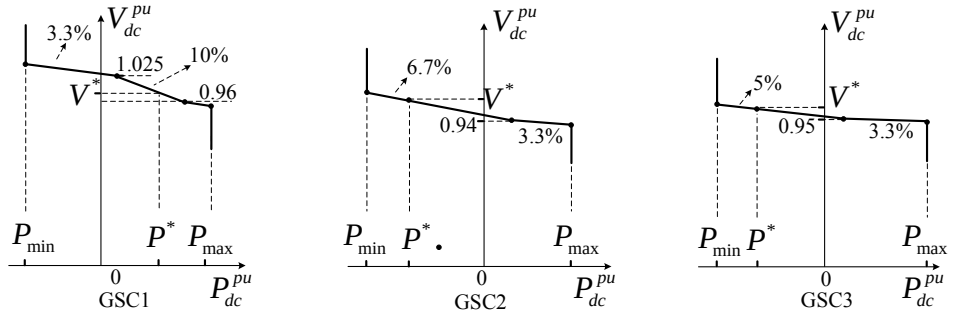
(b) Case 2: V-I droop characteristics



(c) Case 3: V-P droop characteristics



(d) Case 4: V-P droop with deadband



(e) Case 5: V-P droop with voltage limits

Figure 3.6: DC voltage characteristics of the three GSCs.

3.1.5.2 Wind Farm Power Variations

A series of power flows are solved with the five control cases implemented, as the rectifying power of WFC2 varies from 0 to 1.0 pu while the power injection of WFC1 remains fixed at 0.9 pu. The steady-state variations of the converter powers and the average voltage of the four terminals for Case 1, 2, 4, 5 are solved as shown in Figure 3.7. In addition, with the error tolerance of 10^{-8} applied, the iteration number required by each control case is also presented as a function of the power of WFC2 in Figure 3.8.

It is clearly demonstrated in Figure 3.7 that for the voltage margin control there is only one converter at a time responding to DC voltage variation. The average voltage increases slightly even without change of the slack bus, since the WFC2 bus voltage rises as more power is injected to the grid.

The results for Case 2 and 5 demonstrate that the differences between the steady-state behaviours of the V-I and V-P droop lines with identical slopes are almost negligible until the voltage limit control of Case 5 is activated. Unlike the margin control in Case 1, the steady-state voltage response with droop control is continuous. The voltage rises with the increase of the wind generation due the negative-feedback nature of the droop control.

As shown by the power flow solutions of Case 4, the powers of both GSC1 and GSC2 are not perturbed in the deadband range until the droop slack bus reaches its limit. The transitions of the power sharing role are clearly indicated, and that the priorities in response to the power disturbances are determined by the configuration of the deadband ranges is demonstrated.

It is found in Figure 3.8 that the total number of iterations required by the power flow computation is determined by the number of outer iterations. Generally, longer computation time is required for a system state with more converters in limit mode. If all the converters remain in normal operation mode, no more than three iterations are required for a strict tolerance of 10^{-8}. In addition, more iterations are demanded if there are more abrupt changes of control modes, such as the voltage margin control and the deadband control.

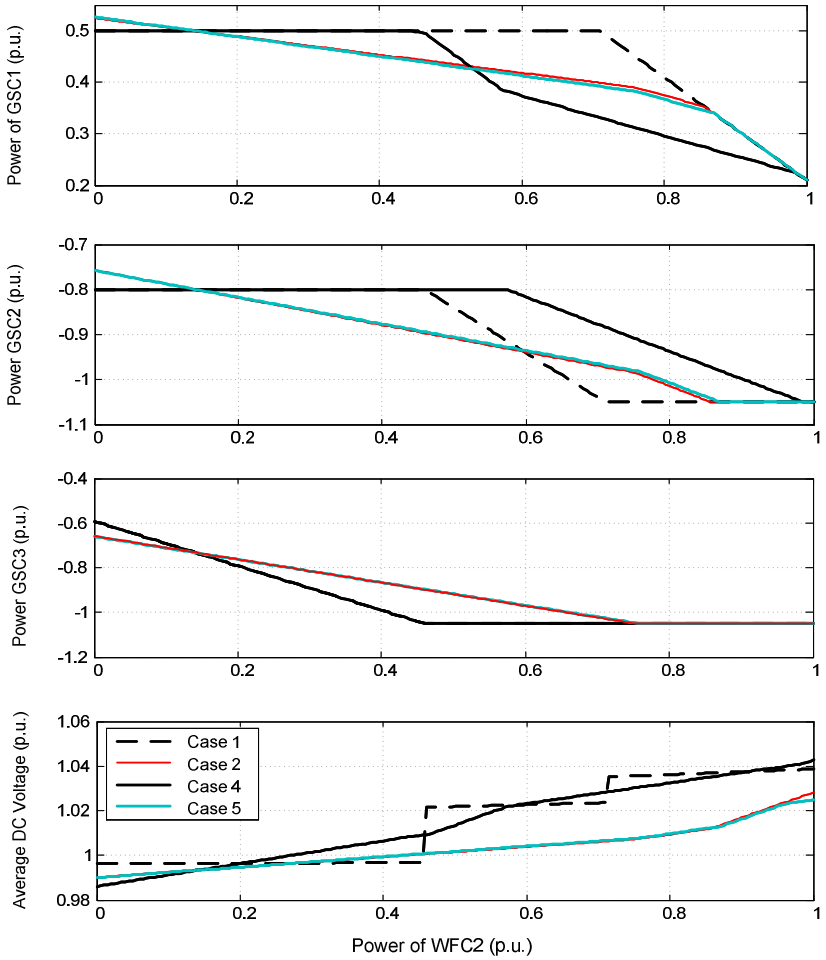


Figure 3.7: Steady-State variations of the power generations of the GSCs and the average DC voltage.

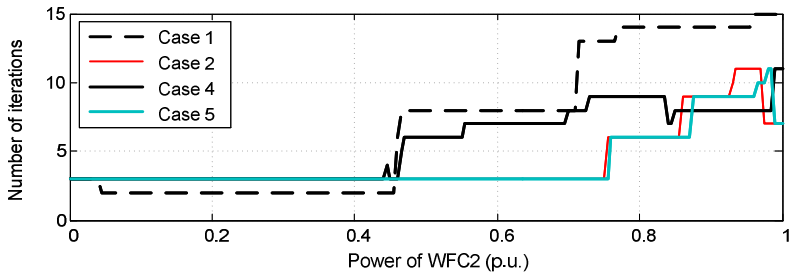


Figure 3.8: Number of iterations for the five control cases for a series of wind farm generations.

3.1.5.3 Converter Outages

Generally, for an MTDC system based on droop control, loss of a rectifier will result in the drop of DC voltage and the increase of rectifying power (or reduction of inverting power) for the remaining terminals in droop control. Loss of an inverter will cause the rise of DC voltage and the decline of rectifying power of the VSCs in droop control. The power flow method is employed here to evaluate the impact of converter outages. It is assumed that the loss of the VSC is caused by the disconnection of the converter AC side. Two converter outage scenarios are studied. The resulting DC voltage and power profiles of the remaining GSCs are presented in Table 3.2 and Table 3.3.

When GSC2 goes offline, acting as the only remaining inverter, GSC3 is not capable to absorb all the wind farm power and the voltage regulation role is taken over by GSC1. Power reversal is experienced by GSC1. The impact of the voltage limit control can be observed from the results of Case 5 in Table 3.2. The new system state is dominated by the characteristic of GSC1 as eventually it becomes the only terminal that has DC voltage control capability.

As shown in Table 3.3, for Case 2, 3 and 5, the power imbalance resulting from the loss of WFC1 is shared by the three GSCs, according to the settings of droop constants. The deadband control in Case 4 enables the powers of GSC2 and GSC1 to be less perturbed or even unchanged. However this could imply a relatively large drift of the DC voltage.

Table 3.2: Power flow results of the outage of GSC2 (in pu).

Converters		*Case 1*	*Case 2*	*Case 3*	*Case 4*	*Case 5*
GSC1	V_{dc}	1.0400	1.0543	1.0545	1.0696	1.0382
	P_{dc}	-0.0458	-0.0459	-0.0459	-0.0460	-0.0457
GSC3	V_{dc}	1.0351	1.0495	1.0497	1.0649	1.0333
	P_{dc}	-1.0500	-1.0500	-1.0500	-1.0500	-1.0500

Table 3.3: Power flow results of the outage of WFC1 (in pu).

Converters		*Case 1*	*Case 2*	*Case 3*	*Case 4*	*Case 5*
GSC1	V_{dc}	0.9940	0.9863	0.9863	0.9751	0.9863
	P_{dc}	0.5000	0.6278	0.6364	0.5000	0.6364
GSC2	V_{dc}	0.9861	0.9780	0.9779	0.9678	0.9779
	P_{dc}	-0.8000	-0.5815	-0.5869	-0.6172	-0.5869
GSC3	V_{dc}	0.9923	0.9799	0.9798	0.9715	0.9798
	P_{dc}	-0.1926	-0.5396	-0.5426	-0.3770	-0.5426

3.1.5.4 Case Study for AC/DC Power Flow

In the previous test cases, the DC power flow methods have been evaluated across a range of control scenarios and disturbance conditions. The integrated AC/DC algorithm discussed in Section 3.1.1 has also been implemented on a 29-bus AC test network [120-122], with the single line diagram shown in Figure 3.9. The converters GSC 1-3 are connected to the 400 kV AC buses 7, 10 and 16 respectively. The control case 4 in Figure 3.6 is adopted for the GSCs in this case study. The converter power loss parameters were derived based on data from [123] (see Appendix B.1).

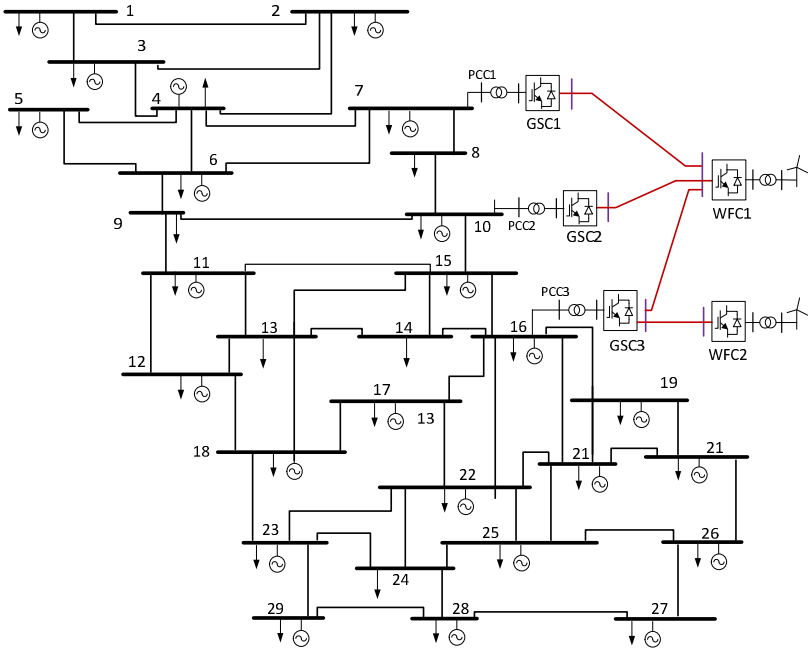


Figure 3.9: Test system for integrated AC/DC power flow.

The combined AC/DC power flow is performed under weak and strong wind scenarios, with the results illustrated in Table 3.4. The AC system power flows are calculated by the open-source package MATPOWER [124]. The voltage magnitude V_g and angle θ_g at the PCC bus, and the real and reactive power injection into the AC grid from the PCC bus are illustrated. Due to the scale and the limited number of variables of the DC grid, the DC power flow requires much less computation time than the AC power flow iterations. Reduced calculation time might be achieved by the unified AC/DC power flow however that requires significant modifications to existing AC models by the user and will reduce the flexibility of both AC and DC grid settings. It also suggests that the DC system power flow is predominantly influenced by the configurations of the droop and the power sources of uncertainty (e.g. wind farms), with the AC power flow only imposing limited auxiliary impact.

Table 3.4: Power flow results for GSCs.

	Case 1: P_{wf1}=200 MW, P_{wf2}=200 MW			*Case 2:* P_{wf1}=950 MW, P_{wf2}=850 MW		
	GSC1	GSC2	GSC3	GSC1	GSC2	GSC3
PCC bus type	*PV*	*PQ*	*PV*	*PQ*	*PQ*	*PQ*
P_{pcc} *(MW) (INV)*	-504.679	601.593	303.650	-259.718	1014.246	1067.270
Q_{pcc} *(MVAr)*	-33.540	100.000	102.840	0.000	0.000	0.000
V_{pcc} *(pu)*	0.9980	1.0045	1.0050	0.9999	1.0037	0.9986
δ_{pcc} *(deg)*	28.680	24.923	18.237	34.678	30.741	23.881
V_{dc} *(pu)*	0.9735	0.9663	0.9667	1.0393	1.0332	1.0350
P_{dc} *(MW) (REC)*	500.000	-595.232	-300.462	257.130	-998.508	-1050.000
Iteration time (s)	0.3475 (AC) 0.0215 (DC)			1.9639 (AC) 0.0216 (DC)		

3.2 VSC Transmission Limit

The PQ transmission limit acts as an important constraint for a VSC-HVDC system. Based on a simplified AC system, this section develops the analytical representations that define the VSC PQ capability, and identifies the associated key impact factors.

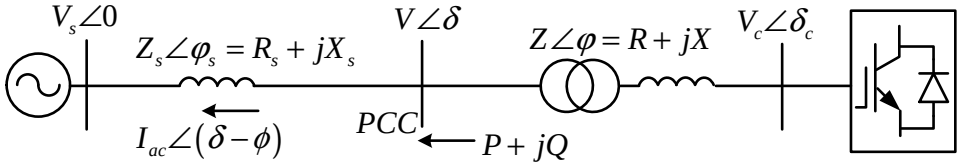


Figure 3.10: Power transfer between a VSC and a simplified AC system.

The equivalent AC system can be represented by the voltage source $\boldsymbol{V_s}$ in series with the network impedance $\boldsymbol{Z_s}$, as shown in Figure 3.10. Normally the AC system strength is indicated by the short-circuit ratio (SCR), which is equal to the reciprocal of the per unit impedance Z_s when V_s equals 1 pu and the converter MVA rating is used as the power base.

$$SCR = \frac{V_s^2}{Z_s}\frac{1}{S_{VSC}^{rated}} \approx \frac{1}{Z_s^{pu}} \tag{3.29}$$

Assuming the network impedance and converter transformer impedance are predominantly inductive, the active and reactive power into the AC system from the VSC can be represented by the converter internal voltage $V_c\angle\delta_c$ and the PCC voltage $V\angle\delta$ as:

$$P = \frac{V_c V}{X}\sin(\delta_c - \delta), \quad Q = \frac{V_c V\cos(\delta_c - \delta) - V^2}{X} \tag{3.30}$$

where X represents the combined reactance of the converter reactor and transformer. By scaling the phasor diagram describing the relationship between $V_c\angle\delta_c$ and $V\angle\delta$ by a factor of V/X, the active and reactive power can be obtained as shown in Figure 3.11(b). This clearly demonstrates that, for an ideal AC system where the PCC voltage is fixed, the PQ capability is defined by the locus of maximum AC current I_{acmax} and internal AC voltage V_{cmax}, shown in Figure 3.11(b) as the locus of AB and OB respectively.

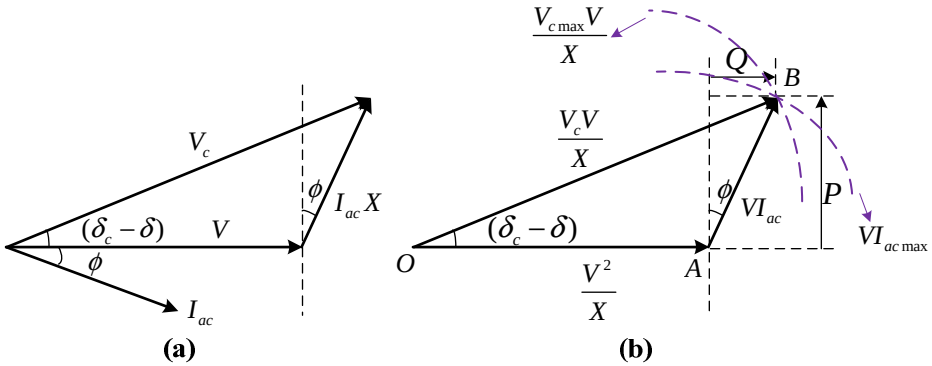


Figure 3.11: (a) Simplified lagging power factor diagram; (b) Scaled lagging power factor diagram.

According to Figure 3.10, regarding the voltages across the network impedance $\boldsymbol{Z_s}$, the active and reactive power injected by the VSC station can also be represented as:

$$P=\frac{V_sV}{X_s}\sin\delta,\quad Q=\frac{V^2-V_sV\cos\delta}{X_s}. \tag{3.31}$$

The magnitude of the PCC voltage can then be derived as a function of P and Q:

$$V(P,Q)=\sqrt{\left(2QX_s+V_s^2+\sqrt{V_s^4+4QX_sV_s^2-4P^2X_s^2}\right)/2}. \tag{3.32}$$

By reconsidering the limits imposed by the maximum voltage and current of the converter, the PQ capability can be described as (3.33) and (3.34), according to (3.32) and Figure 3.11(b).

$$\sqrt{\left(Q+\frac{V^2(P,Q)}{X}\right)^2+P^2}\le\frac{V_{c\max}V(P,Q)}{X} \tag{3.33}$$

$$\sqrt{Q^2+P^2}\le V(P,Q)\cdot I_{ac\max} \tag{3.34}$$

By solving the equations above under boundary conditions, the VSC PQ capability curve can be defined by the following equations:

$$\left[Q(X_s+X)^2+V_s^2X-V_{c\max}^2X_s\right]^2+P^2(X_s+X)^2(X_s-X)^2=V_s^2V_{c\max}^2(X_s-X)^2 \tag{3.35}$$

$$\left(Q - I_{ac\max}^2 X_s\right)^2 = V_s^2 I_{ac\max}^2 - P^2 . \tag{3.36}$$

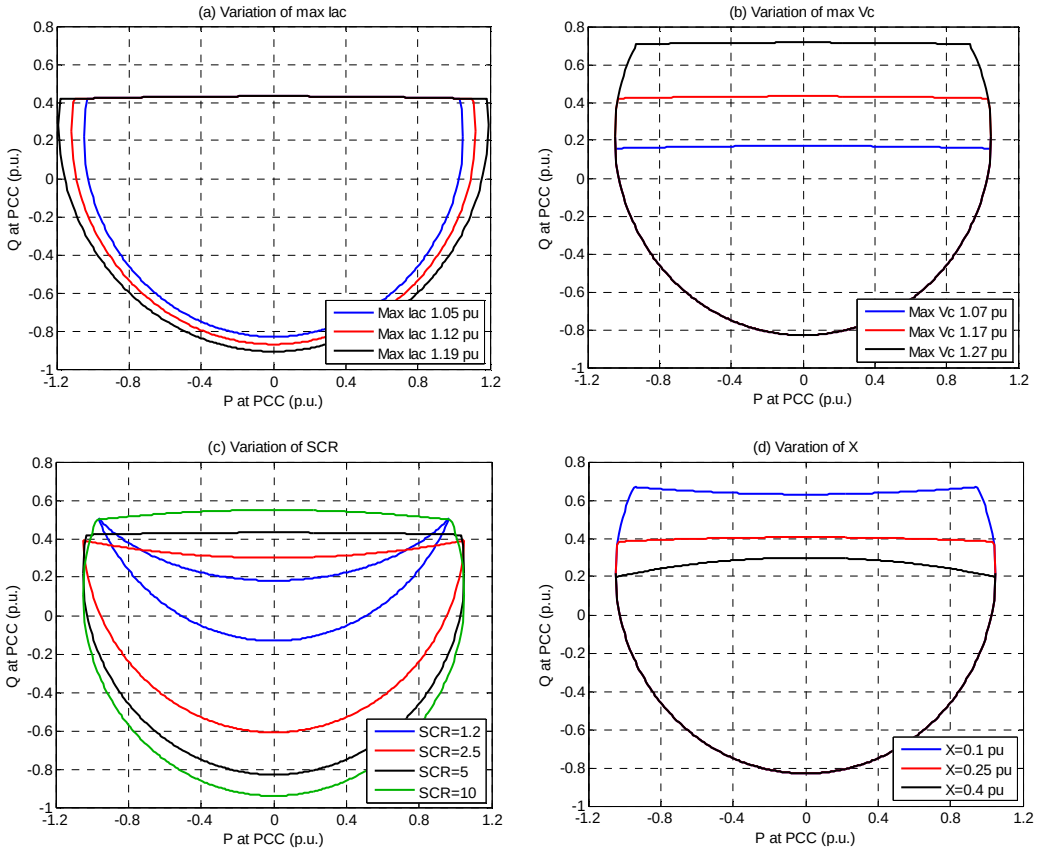


Figure 3.12: Impact of the key factors on the VSC PQ capability curve.

The PQ characteristic is mainly affected by four quantities: the valve current limit, the SCR, the converter transformer/reactor impedance, and the maximum AC voltage, which is determined by the DC voltage and the modulation limit. The impacts of these factors on the VSC PQ capability are demonstrated in Figure 3.12, with the nominal parameters given as $V_{c\max}$*=1.17 pu*, $I_{ac\max}$*=1.05 pu*, X_s*=0.2 pu*, *X=0.225 pu*. Note that the directions of active and reactive power of the converter are defined using the generator rule.

As shown in Figure 3.12, the valve current limit impacts on both active and reactive power capability. The maximum internal AC voltage V_{cmax} that is determined by the DC voltage has a significant impact on the reactive power that can be generated by the VSC. Moreover, a larger transformer or converter reactor indicates that less reactive power can be injected into the AC system by the VSC, due to the increased reactive power consumption within the converter station. Interestingly, the convexity of the capacitive Q limit curve is determined by the relative difference between X_s and X.

As the SCR decreases, less reactive power can be injected into the PCC by the VSC; however, more reactive power is required to support the PCC voltage in order to achieve the maximum active power. Therefore, for a very weak system, the VSC station may not be able to transfer the rated power, due to the insufficient reactive power support. Furthermore, as shown in Figure 3.12(c), reducing the AC system strength also degrades the maximum reactive power that can be absorbed from the AC system by the VSC.

The previous discussion has not considered the network resistance. Nonetheless, the angle of the network impedance φ_s could affect the power transfer capability of inverters and rectifiers in different directions, as suggested in [125] where the impact of the variation of PQ transfer on the PCC voltage is however not considered. By incorporating the impedance angle, the active and reactive power injected into the system can be represented as:

$$P = \frac{V^2 \cos\varphi_s - V_s V \cos(\delta + \varphi_s)}{Z_s}, \quad Q = \frac{V^2 \sin\varphi_s - V_s V \sin(\delta + \varphi_s)}{Z_s} \tag{3.37}$$

Without considering the converter current and voltage limitations, theoretically, the maximum power that can be transferred is shown by (3.38) for inverter and rectifier operations. These equations demonstrate that increasing the impedance angle has a positive contribution to the power transfer capability of an inverter while it has a negative effect on the rectifier operation. The equation (3.38) also implies that, for a AC system with larger impedance angle, a larger amount of reactive power is required to achieve the theoretical maximum power.

$$P_{\max}^{INV} = \frac{V^2 \cos\varphi_s + V_s V}{Z_s}, \; P_{\max}^{REC} = \frac{V^2 \cos\varphi_s - V_s V}{Z_s}, \; \textit{when} \; Q = \frac{V^2 \sin\varphi_s}{Z_s} \tag{3.38}$$

However, the limits shown in (3.38) are usually much larger than the limits imposed by the valve current and the DC voltage, and therefore would not affect the PQ capability curve except for very weak AC systems with SCR close to 1.

3.3 Linear Analysis and Equivalent Circuit[6]

In Section 3.1, the equations describing the power flow of the DC system are nonlinear and have to be solved iteratively. However, the generalised steady-state response of a droop-controlled DC grid to the unanticipated events such as wind power variations and converter outages cannot be directly observed from the nonlinear characteristics. To provide a clearer insight into the impact of the change of droop references and power disturbances on the deviations of the system operating point, analytical studies based upon the linearised power flow equations are conducted in this section.

Excellent work on this subject has been done in [94, 98] and [30]. The influence of non-uniform DC voltage drops is studied in [94, 98], where an analytical expression for estimation of the power sharing in a V-P droop-controlled system has been derived based on the Jacobian matrix. In [30], with respect to the power variations after a converter outage, the impacts of the droop settings and network topologies are discussed and an steady-state optimisation method is developed for the droop gain design.

3.3.1 Voltage-Current Droop

The DC current injected by a GSC in V-I droop control mode can be represented by:

$$I = K\left(V^* - V\right) + I^* = \frac{1}{R}\left(V^* - V\right) + I^*. \tag{3.39}$$

The nodal current of the terminals in active power control or wind farm control mode can be approximated by the equation above, by setting $K=0$ or $R=\infty$. In a generic MTDC system of n buses, the nodal DC current vector can be written as:

$$\begin{pmatrix} I_{1o}+\Delta I_1 \\ I_{2o}+\Delta I_2 \\ \vdots \\ I_{no}+\Delta I_n \end{pmatrix} = \mathbf{Y}\begin{pmatrix} V_{1o}+\Delta V_1 \\ V_{2o}+\Delta V_2 \\ \vdots \\ V_{no}+\Delta V_n \end{pmatrix} = \begin{pmatrix} K_1[(V_{1o}^*+\Delta V_1^*)-(V_{1o}+\Delta V_1)]+I_{1o}^*+\Delta I_1^* \\ K_2[(V_{2o}^*+\Delta V_2^*)-(V_{2o}+\Delta V_2)]+I_{2o}^*+\Delta I_2^* \\ \vdots \\ K_n[(V_{no}^*+\Delta V_n^*)-(V_{no}+\Delta V_n)]+I_{no}^*+\Delta I_n^* \end{pmatrix}. \tag{3.40}$$

The voltage deviation in response to the change of the droop current/voltage references or the power change of other terminals can then be derived as:

$$\Delta\mathbf{V} = \left[\mathbf{Y} + diag(\mathbf{K})\right]^{-1} \cdot \left[\Delta\mathbf{I}^* + diag(\mathbf{K}) \cdot \Delta\mathbf{V}^*\right] \tag{3.41}$$

[6] This has been independently developed by author but some work similar to part of this section has since been published by J. Beerten and T. M. Haileselassie in [30] and [94].

where the subscript 'o' refers to the nominal operating point (OP), *diag*(**K**) is the diagonal matrix formed by the *n* droop gains, $\Delta \boldsymbol{I}^*$ is the vector of current references (for GSCs in droop control) and current disturbances (for GSCs power control and WFCs). The resulting vector of the nodal current deviations is subsequently solved as:

$$\Delta \mathbf{I} = \mathbf{Y}\left[\mathbf{Y} + diag(\mathbf{K})\right]^{-1} \cdot \left[\Delta \mathbf{I}^* + diag(\mathbf{K}) \cdot \Delta \mathbf{V}^*\right]. \tag{3.42}$$

The equations (3.41) and (3.42) clearly demonstrate that the droop gains effectively modify the diagonal elements of the network admittance matrix, and the sharing of the current imbalance is jointly determined by the droop setting and the network impedances.

3.3.2 Voltage-Power Droop

With respect to the utilisation of the V-P droop control in a DC grid of *n* terminals, the quasi-steady-state DC current injected by the *j*th terminal to the DC grid can be written as:

$$I_j = \frac{K_j\left(V_j^* - V_j\right) + P_j^*}{V_j} = \frac{K_j V_j^* + P_j^*}{V_j} - K_j . \tag{3.43}$$

In order to perform further analysis, the equation above is linearised to:

$$I_j = I_{jo} + \Delta I_j = \frac{K_j V_j^* + P_j^*}{V_{jo}} - K_j - \frac{K_j V_{jo}^* + P_{jo}^*}{V_{jo}^2}\Delta V_j + \frac{1}{V_{jo}}\left(K_j \Delta V_j^* + \Delta P_j^*\right). \tag{3.44}$$

Subsequently, the DC current deviation of this terminal can be associated with the variations of the voltage and power references as:

$$\Delta I_j = -\frac{K_j V_{jo}^* + P_{jo}^*}{V_{jo}^2}\Delta V_j + \frac{1}{V_{jo}}\left(K_j \Delta V_j^* + \Delta P_j^*\right) = \sum_{i=1}^{n} Y_{ji}\Delta V_i . \tag{3.45}$$

By defining the new equivalent droop gain and droop constant as shown in (3.46), the equation (3.45) can then be written in matrix form as shown in (3.47).

$$K_j^{'} = \frac{K_j V_{jo}^* + P_{jo}^*}{V_{jo}^2}, \quad R_j^{'} = \frac{V_{jo}^2}{K_j V_{jo}^* + P_{jo}^*} . \tag{3.46}$$

$$diag\left(\mathbf{K}^{'}\right) \cdot \Delta \mathbf{V} + diag\left(\frac{1}{\mathbf{V}_o}\right) \cdot \left[diag\left(\mathbf{K}\right) \cdot \Delta \mathbf{V}^* + \Delta \mathbf{P}^*\right] = \mathbf{Y} \cdot \Delta \mathbf{V} \tag{3.47}$$

The equation above can be further derived as (3.48) to represent the quasi-steady-state relation between the variations of voltage/power references and the resulting deviations of the node voltages of the DC grid. It should be noted that change of wind farm power can be viewed here as equivalent to change of a power reference.

$$\Delta \mathbf{V} = \left[\mathbf{Y} + diag\left(\mathbf{K}^{'}\right) \right]^{-1} \cdot diag\left(\frac{1}{\mathbf{V}_o} \right) \cdot \left[diag\left(\mathbf{K}\right) \cdot \Delta \mathbf{V}^{*} + \Delta \mathbf{P}^{*} \right] \tag{3.48}$$

Subsequently, the vector of the power deviations can be derived as:

$$\Delta \mathbf{P} = \left\{ \mathbf{I} - diag\left(\mathbf{K}\right) \left[\mathbf{Y} + diag\left(\mathbf{K}^{'}\right) \right]^{-1} diag\left(\frac{1}{\mathbf{V}_o} \right) \right\} \cdot \left[diag\left(\mathbf{K}\right) \cdot \Delta \mathbf{V}^{*} + \Delta \mathbf{P}^{*} \right]. \tag{3.49}$$

The power sharing based on V-P droop differs from the current sharing based on V-I droop mainly due to its reliance on operating point, as shown by the comparison of (3.42) and (3.49). If $P_o=0$ and $V_o=V_o^*=1$ for all the terminals, the power sharing shown in (3.49) will be identical to the current sharing shown in (3.42). However, as indicated in (3.46) and (3.49), the impact of the voltage and power operating point on the power sharing is usually very limited since the droop gain is normally much larger than the power reference in pu.

Regarding the 100 MW and -500 MW power variations of WFC1 in the test system shown in Figure 3.5, the power deviations of the GSCs estimated according to (3.49) and the accurate power deviations calculated by the iterative power flow are compared in Table 3.5, assuming the V-P droop control shown as Case 1 in Figure 3.6 is adopted by the three GSCs. The results show that the linearised derivations are sufficiently accurate to perform detailed analysis of distribution of the imbalanced power. Increasing the wind power deviation though degrades the accuracy of the linearised estimation.

Table 3.5: Comparison of the actual and estimated power flow results.

	ΔP_{wf1}=100 MW			ΔP_{wf1}=-500 MW		
Terminal	ΔP_{est} (MW)	ΔP (MW)	Error (%)	ΔP_{est} (MW)	ΔP (MW)	Error (%)
GSC1	-45.388	-45.361	0.058	113.469	113.640	0.150
GSC2	-70.871	-70.819	0.074	177.178	177.515	0.190
GSC3	-83.293	-83.268	0.030	208.233	208.396	0.078

Another method based on the Jacobian matrix can also be used to estimate the voltage and power deviations. As shown in Section 3.1.3, the nodal power vector can be represented as:

$$\mathbf{P} = diag(\mathbf{K}) \cdot (\mathbf{V}^* - \mathbf{V}) + \mathbf{P}^* = diag(\mathbf{V}) \cdot (\mathbf{YV}) . \tag{3.50}$$

The reference variations can be accordingly arranged as a function of the voltage vector as:

$$\mathbf{f}(V_1, V_2, \cdots, V_n) = diag(\mathbf{V}) \cdot (\mathbf{YV}) + diag(\mathbf{K}) \cdot \mathbf{V} = diag(\mathbf{K}) \cdot \mathbf{V}^* + \mathbf{P}^* . \tag{3.51}$$

In analogy to the power flow algorithm shown in 3.1.3, the DC voltage deviations can then be estimated according to the following equation:

$$\Delta\mathbf{V} = \left(\frac{\partial \mathbf{f}}{\partial \mathbf{V}} \right)^{-1} \cdot \left(diag(\mathbf{K}) \cdot \Delta\mathbf{V}^* + \Delta\mathbf{P}^* \right) \tag{3.52}$$

where the elements of the partial derivative matrix are derived as:

$$\frac{\partial f_i}{\partial V_i} = 2Y_{ii}V_{io} + \sum_{j=1, j\neq i}^{n} Y_{ij}V_{jo} + K_i = Y_{ii}V_{io} + \sum_{j=1, j\neq i}^{n} Y_{ij}(V_{jo} - V_{io}) + K_i , \quad \frac{\partial f_i}{\partial V_{j(j\neq i)}} = V_{io}Y_{ij} . \tag{3.53}$$

It is found that this matrix can be related to the power flow Jacobian shown in (3.11) as:

$$\frac{\partial \mathbf{f}}{\partial \mathbf{V}} = \mathbf{J} + diag\left(\mathbf{K}\right) . \tag{3.54}$$

Accordingly, the resulting power sharing vector can be represented by:

$$\begin{aligned} \Delta\mathbf{P} &= -diag\left(\mathbf{K}\right) \cdot \Delta\mathbf{V} + \left(diag(\mathbf{K}) \cdot \Delta\mathbf{V}^* + \Delta\mathbf{P}^* \right) \\ &= \mathbf{J} \cdot \left(\mathbf{J} + diag\left(\mathbf{K}\right) \right)^{-1} \cdot \left(diag(\mathbf{K}) \cdot \Delta\mathbf{V}^* + \Delta\mathbf{P}^* \right) \end{aligned} \tag{3.55}$$

which is similar to the result shown in [98]. Unlike the form shown in (3.49) where the voltage and power operating point is explicitly presented, this effect is implicitly incorporated in the Jacobian matrix in (3.55). The equations (3.42), (3.49) and (3.55) demonstrate that the power sharing within a MTDC system is not only determined by the droop gain setting, but also relies on the impedances of the DC system. If V-P/V-I characteristics with shallower droop are employed, the post-disturbance operating condition of the MTDC system will be more severely affected by the network impedance.

3.3.3 Steady-State Equivalent Circuit for Droop Control

The linear analysis provided in 3.3.1 and 3.3.2 describes the generalised relations between DC voltage/power deviations and the droop gains in matrix forms. To provide a clearer understanding of this and to identify the key steady-state interactions between the droop settings and the system admittances, the equivalent circuits of V-I and V-P droop characteristics are developed.

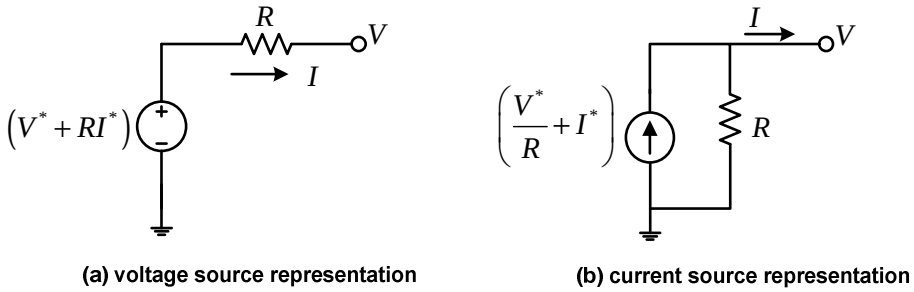


Figure 3.13: Equivalent circuits of V-I droop characteristic.

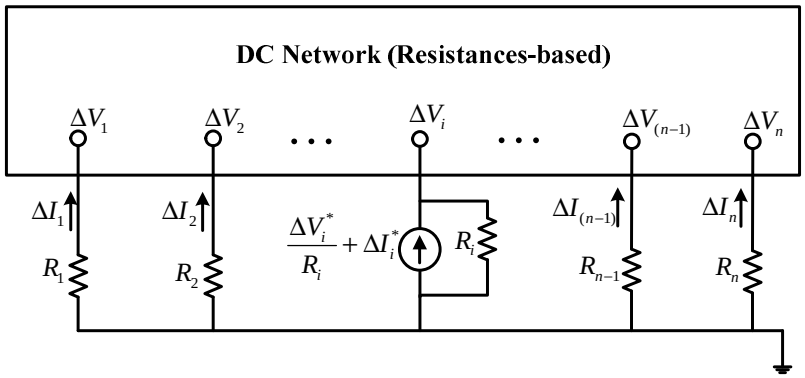


Figure 3.14: Linearised equivalent circuit for a generalised DC network with V-I droop control.

The Thevenin and Norton equivalent circuits for a typical V-I droop control are represented as shown Figure 3.13, according to the basic droop equation (3.39). To understand the current sharing after wind power variations or converter outages, it is more convenient to utilise the current-source-based circuit, as shown in Figure 3.14.

The droop constants *R* effectively act as nodal shunt resistances to modify the network impedance to achieve the distribution of the current imbalance. For systems with relatively short transmission distances, typical values of the droop constants are much larger than the per unit line resistances. Therefore, the current sharing in this case is determined by the ratios between droop constants, according to Figure 3.14. For multiple DC current perturbations, steady-state deviations of the voltage and current of each

terminal can be calculated using the superposition rule by calculating the deviations caused by each current perturbation separately, based on the linear equivalent circuit.

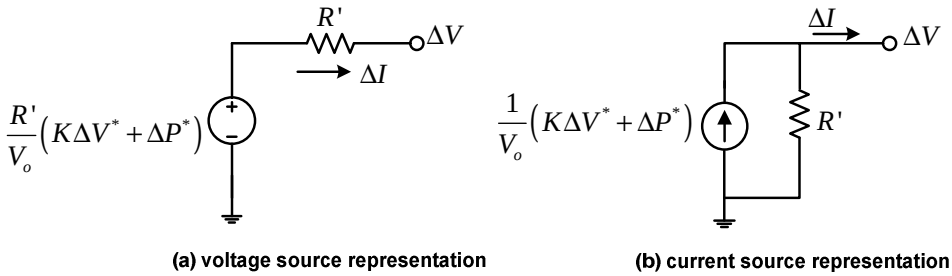


Figure 3.15: Equivalent circuit of V-P droop control.

The equivalent circuits for the V-P droop are derived based upon (3.45) and presented as shown in Figure 3.15. Unlike the V-I droop, the equivalent resistance *R* for the V-P droop differs from the droop constant because it is also dependent on the converter operating point, particularly when a small droop gain is adopted.

Regarding the wind farm power variations of the five-terminal DC network shown in Figure 3.5, the droop-based equivalent circuit is presented as shown in Figure 3.16, assuming that V-P droop control is adopted by the GSCs. Four scenarios of different droop settings and line lengths, as parameterised in Table 3.6, are used to exemplify the key impact factors of the distribution of the wind farm power in a radial MTDC network. The ratios between the droop gains are kept unchanged in the four cases. As the power of wind farm 1 P_{wf1} ramped from 0 to 1.0 pu, the corresponding GSC power deviations from the original power flow were solved through accurate power flow and shown in Figure 3.17.

For relatively small droop gains, the distribution of the wind power surplus is roughly in proportion to the droop gains, as shown in Case 1. However, the results of Case 2, 3 and 4 show that the droop settings have a reduced impact on the wind power distribution if higher gains are employed. In Case 3 and 4, the power deviation of GSC2 is larger than that of GSC1, in spite of the droop gain of GSC1 being much higher, due to the shorter cable length between GSC2 and WFC1. Generally, for a radial MTDC system where identical droop are configured for each converter, the one with longer impedance path to the disturbance terminal will experience less drift of steady-state power, especially when relatively large droop gains are employed.

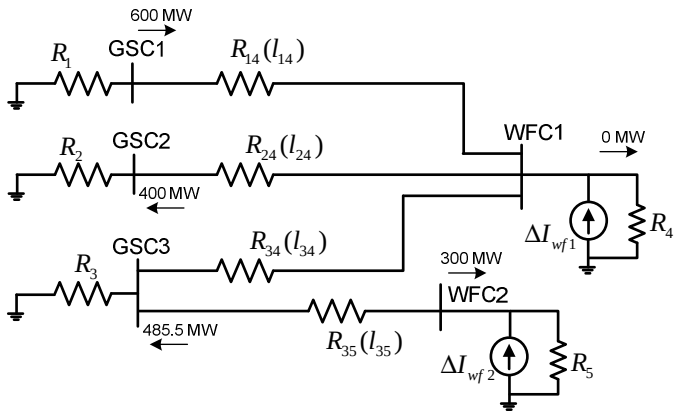


Figure 3.16: Equivalent circuit of the droop controlled five-terminal test system.

Table 3.6: Four test cases for power sharing demonstration.

	K_1	K_2	K_3	l_{14} (km)	l_{24} (km)	l_{34} (km)	l_{35} (km)
Case 1	16	12	12	170	70	180	110
Case 2	32	24	24	170	70	180	110
Case 3	32	24	24	340	70	360	110
Case 4	48	36	36	340	70	360	110

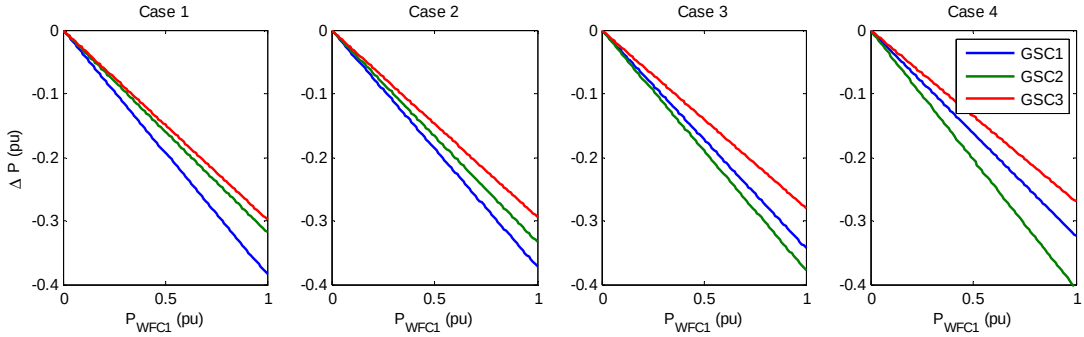


Figure 3.17: Power deviations of the GSCs in response to the power ramp of WFC1 from 0 to 1 pu.

With identical droop gains applied to the GSCs in the five-terminal model, the power and voltage deviations in response to a 0.7 pu power increase of WFC2 for a series of droop gains are calculated as shown in Figure 3.18 (a) and (b). With the droop gains fixed at 10, the deviations with respect to the power change of WFC2 for a series of the scaling of line lengths are also presented in Figure 3.18 (c) and (d).

High-gain droop control implies that the power sharing could be highly dependent on the grid topology and on the location of the disturbance terminal, particularly for large DC grids. Furthermore, high-gain droop may not significantly reduce voltage deviations a beyond a certain point, as shown in Figure 3.18 (b). Increasing the transmission lengths enlarges the differences between the GSCs with respect to both power and voltage deviations. Unlike the frequency droop, the DC voltage droop with identical gains may

impose significantly different burdens on the GSCs. These power flow results agree well with the previous analysis based upon linear equations and the droop equivalent circuit.

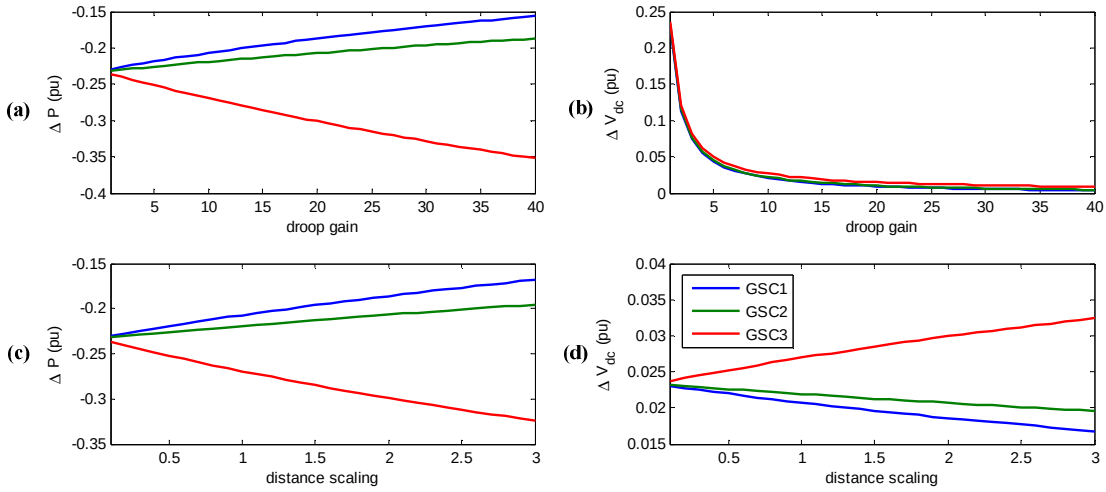


Figure 3.18: Power and voltage deviations of the GSCs in response to 0.7 pu power increase of WFC2, with identical droop gain applied to the GSCs.

3.4 Secondary Control and DC Dispatch

Most of the existing literature regarding DC voltage control in MTDC systems focuses on the primary control stage where the control actions are performed locally and automatically. For a primary control based upon the DC voltage droop, voltage and power control errors of the GSCs in droop control mode are unavoidable in case of a power disturbance. Therefore, further outer scheduling control is necessary to achieve the desired power flow. However, the high-level hierarchy beyond the primary DC voltage control remains unclear.

Hierarchical control schemes based on droop primary control are briefly discussed in [126] and [127]. The existing literature on centralised control mainly analyses the optimal power flow (OPF), particularly regarding the minimisation of transmission losses [109, 128, 129]. In [130, 131], OPF models based on cost-benefit analysis have been developed for integrated AC/DC systems. A generic three-stage DC voltage control structure, which is developed based on the frequency control in AC system, will be briefly described in this section.

3.4.1 Control Structure Description

A possible control hierarchy for future HVDC grids is envisaged here as depicted in Figure 3.19, where the dashed line indicates the requirement of a telecommunication link. The priority of the droop-based primary control is to ensure transient stability of the DC

grid. The communication link is not critical for this fast dynamic control; however, it is required by both of the secondary and the tertiary control for power flow scheduling. The three control stages are likely to have significantly different time constants.

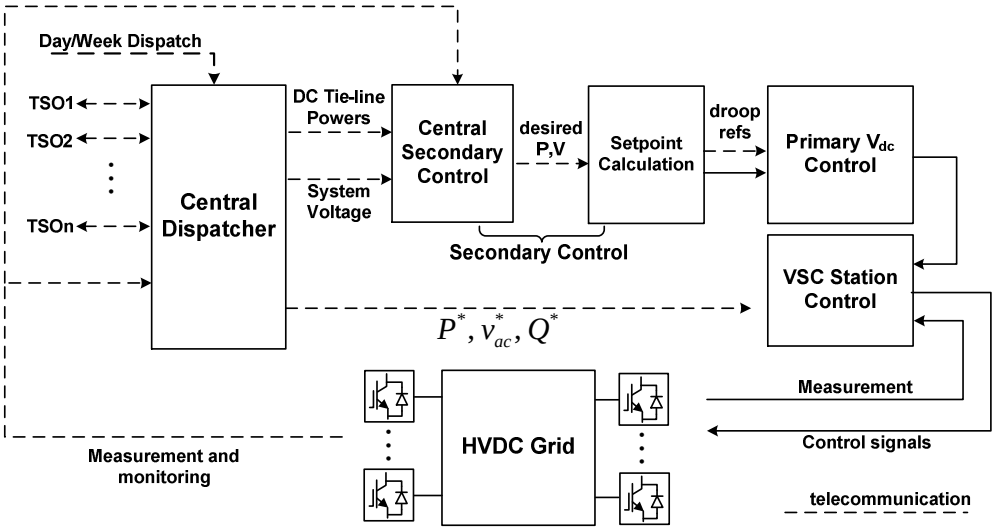


Figure 3.19: Hierarchical MTDC control structure.

The central dispatcher (tertiary control), which is based on complex optimisations regarding both economic and technical aspects, may be activated manually and periodically in a very slow manner. For a large DC grid involving multiple transmission system operators (TSOs), the interests of the AC-TSOs need to be well coordinated with the operation of the DC grid through the central dispatcher by the DC-TSO. The tertiary control is likely to be depending on AC/DC OPF schemes if both the DC and AC grids are owned by the same TSO. For small-scale MTDC systems, the central dispatcher may be merged with the central secondary control for more efficient operation.

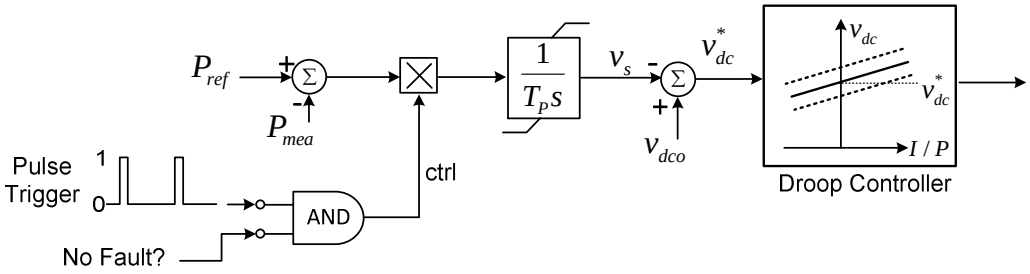
The secondary frequency control in a conventional AC system, which usually adopts the automatic generation control (AGC) scheme, is used to compensate the frequency error and the changes of tie-line power flows caused by the primary control. The DC secondary control, which is possibly comprised of the central secondary control and the setpoint calculation, is expected to fulfil similar purposes: to restore the DC voltage and the power transfer between areas. However, the AGC type control cannot be directly applied to MTDC systems, since the DC voltage is not a global variable like the system frequency. A secondary control scheme is proposed in [94] to assign power compensation to each converter, according to the area control error (ACE) and the participation factor. In this scheme, the DC voltage is however not restored and the update of power references based on the linear analysis may not be sufficiently accurate.

More advanced secondary control based upon modification of the AGC requires further investigation.

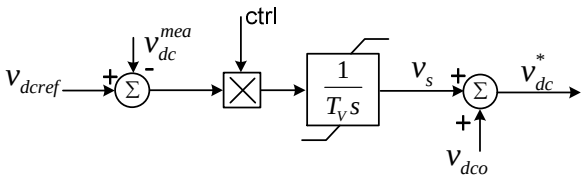
3.4.2 Setpoint Calculation

The setpoint calculation is used to update the voltage and power references of the droop control in order to achieve the demands given by the central secondary control or directly given by the dispatcher for a MTDC system consisting of a small number of converters. This section introduces two setpoint calculation methods: an integrator-based setpoint calculation (ISC) method and a direct setpoint calculation (DSC) method.

The voltage reference of the droop control is used as the control variable by the ISC to compensate the power or voltage errors, once new system references are sent periodically from the higher control layers, as shown in Figure 3.20. In a DC grid, the ISC for most converters will be configured in active power mode. For a MTDC system without a AGC-type secondary control, the desired voltage reference can also be restored utilising the ISC. The integrator controllers are placed locally at converter stations. This control will be deactivated under severe transient conditions.



(a) Secondary control, active power mode



(b) Secondary control, DC voltage mode

Figure 3.20: Integrator-Based setpoint control (ISC) structure.

In the DSC method, the desired voltage and power operating point of all GSCs, which are solved by power flow calculations, are directly sent to individual converters as the references of the droop characteristics. Filters with slow time constants are required for the update of the references to avoid the interaction with the inner primary control. The complexity of the secondary control structure can be reduced by using the DSC method

instead of the ISC method. However, after a disturbance, the resulting power flow based on the DSC may not be as close to the desired dispatch as the integrator-based control, as the errors of the power flow calculation caused by parameter uncertainty are unavoidable.

The dynamic performances of the two setpoint calculation approaches are compared by employing the four-terminal test system shown in Figure 2.32, with the initial operating point shown in Table 3.7. In the simulations conducted for three scenarios and shown in Figure 3.21, the power of the WFC ramped from 500 MW to 200 MW, and the new set of power references was sent to the GSCs at 4 s. In the third scenario, the active-power-mode ISC was adopted by GSC1 and GSC2, while the DSC was employed by GSC3.

After the wind power variation, the desired operating points shown in Table 3.7 were determined through minimisation of DC line losses. In the basic optimisation process, the power of GSC2 and DC voltage of GSC3 were used as manipulated variables, while the power of GSC1 was fixed at -0.8 pu. For each iteration process, firstly the power flow algorithm discussed in 3.1.2 was used to solve the terminal voltages, and then optimisation was performed regarding the objective function shown in (3.56) which represents the total transmission loss.

$$P_{loss} = \frac{1}{2}\sum_{i=1}^{n}\sum_{j=1}^{n}(-Y_{ij})\left(V_i - V_j\right)^2 \tag{3.56}$$

As shown in (3.57), the limits of DC voltages, converter currents and line currents, were used as the constraints for the optimisation. The process was carried out using Matlab based upon the interior point algorithm (see Appendix B.2 for details).

$$V_{\min} \le V_i \le V_{\max}, \quad I_{\min} \le I_i \le I_{\max}, \quad I_{line\_\min} \le -Y_{ij}\left(V_i - V_j\right) \le I_{line\_\max} \tag{3.57}$$

Table 3.7: Optimised operating points for the WFC power of 0.5 pu and 0.2 pu (P_{GSC1} fixed at 0.8 pu).

		GSC1	GSC2	GSC3	WFC	Network Loss
Initial OP	V_{dc}	1.0001	0.9890	0.9890	0.9926	10.73 MW
	P_{dc}	0.800	-0.928	-0.361	0.500	
Updated OP	V_{dc}	0.9973	0.9870	0.9870	0.9898	8.84 MW
	P_{dc}	0.800	-0.714	-0.277	0.200	

All the three scenarios based upon the ISC or DSC schemes demonstrate satisfactory dynamic performance in achieving the new operating point, as shown in Figure 3.21. The bandwidth of the setpoint calculation has been designed to be much lower than the droop control for system security. The steady-state error of the ISC scenario is slightly smaller

than the DSC due to the integral action. However the damping of the ISC response is slightly worse than that of the other two scenarios, since GSC3 acts as the virtual "DC slack bus" during the reference updating process and the bandwidth of the ISC is slightly higher than the other scenarios. The virtual slack bus role can be removed from the ISC scheme if an advanced AGC-type secondary control is used to restore the DC voltage of a large DC grid. Realistically, the secondary control could be much slower than the simulation shown here as ramped change rather than stepped change of the references are more likely to be applied in practice. If the secondary control is designed to have a time constant in the range of tens of seconds, very similar performance will be provided by the ISC and DSC methods.

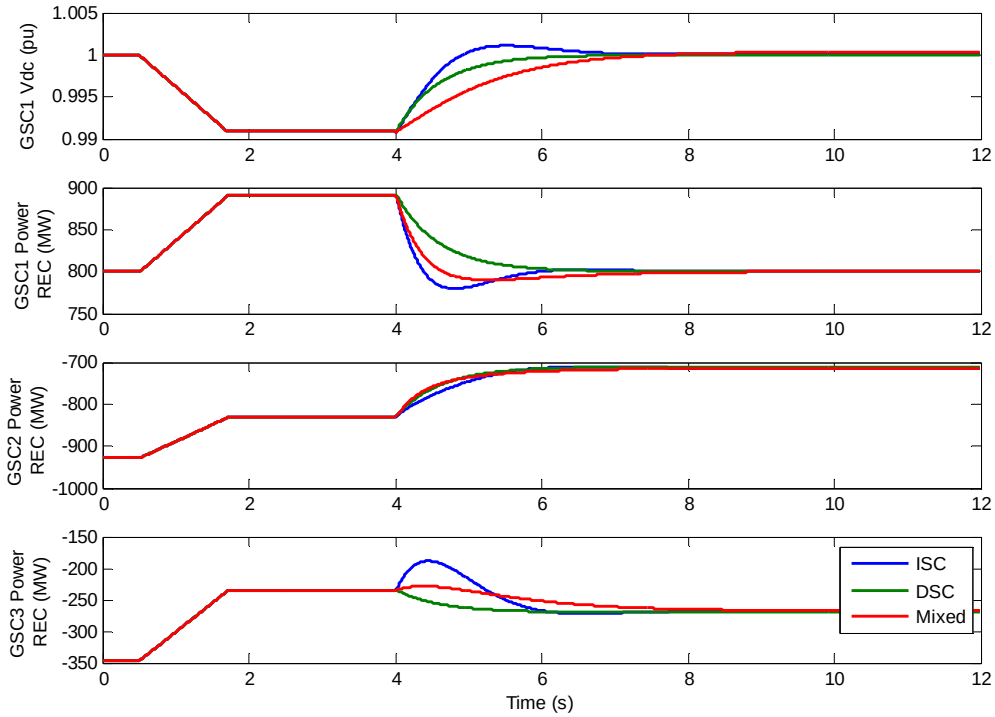


Figure 3.21: Dynamic performance of the ISC and DSC schemes in response to the power change of WFC.

3.5 Chapter Summary

A new generalised power flow approach with two iteration layers has been presented for MTDC systems to enable the power flow calculation for MTDC systems where various voltage characteristics containing multiple control stages are employed. The method to integrate this DC power flow with a conventional AC power flow has been provided. This procedure has been applied to a series of test scenarios and shown satisfactory performance.

The analytical expressions defining the VSC PQ capability have been derived based upon a simplified system model. The impacts of the DC voltage, the current limit, the AC system strength and the transformer impedance on the VSC operating limit have been identified.

Based upon the linearised power flow equations and V-I/V-P droop characteristics, the analytical representations of the deviations of the system operating point in response to power disturbances have been derived. The equivalent circuit of the droop control provides an intuitive way to assess the impact of the droop gains, the network topology and impedances, and the location of the power disturbance, on the voltage and current/power variations of the overall DC system.

A generic control structure consisting of three DC voltage control stages has been briefly presented to achieve desired steady-state power flow of DC grids. Additionally, two methods have been developed to help the DC system to reach the scheduled power flow by varying the droop references.

Chapter 4 Analysis of Active Power Control of VSC-HVDC

Active power control based on vector current control for VSC-HVDC systems can be categorised into voltage disturbance control [96, 102, 132-136] (in effect a type of feedforward control) and power feedback (FB) control [31, 91, 98, 99] as shown in Figure 4.1. For the voltage disturbance feedforward (FF) control, the current setpoint is directly calculated from the power reference and transformed voltage. However, the stability, performance and robustness of these key active power control principles have not been assessed using detailed analytical models. The limitations imposed by the converter plant model and the controller structure have not been examined, which often leads to the AC system strength and the fast current loop dynamics being neglected. Furthermore, the interactions between the widely-proposed V-P droop control and the active power control have not been addressed in the previous literature.

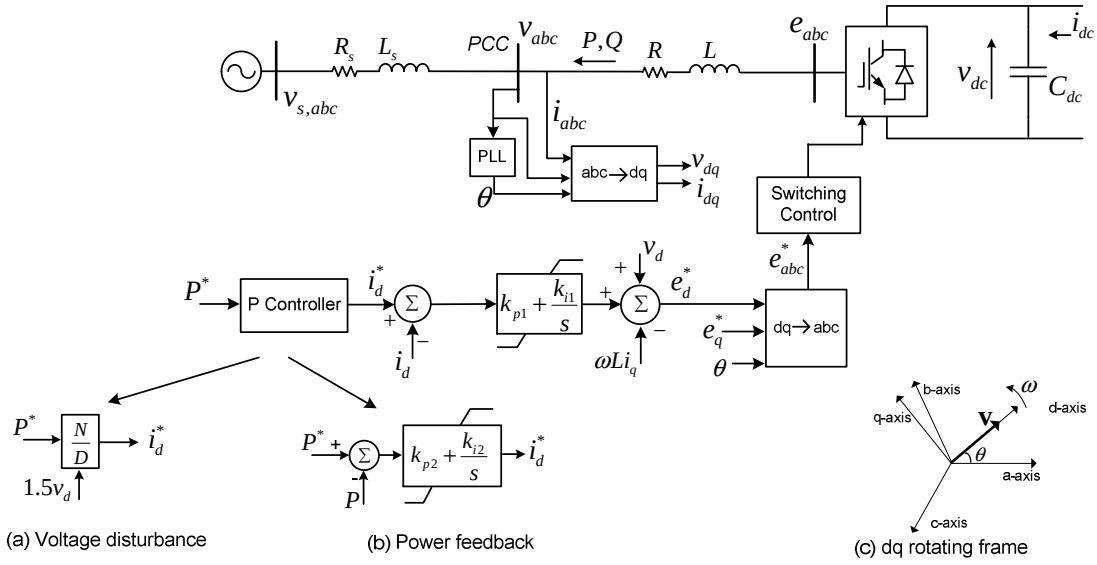


Figure 4.1: Active power controllers employing vector current control: (a) voltage disturbance/feedforward; (b) power feedback.

This chapter aims to comprehensively analyse closed-loop behaviours of active power control for VSC-HVDC systems, to provide insight into the key limitations imposed by the VSC plant model and its control designs, and to offer a framework for analysis of the dynamics associated with power control loops for future research. In order to perform such analysis, in Section 4.1, mathematical models are derived for the plant and closed-loop systems of the active power control as well as outer DC voltage droop control. Based on the linearised analytical models, frequency domain tools are then used to fully

understand the impact that a particular controller has on the closed-loop performance and robustness, with the associated results shown in Section 4.2, along with the verifications by simulation results generated in DSPF. Please note that the active power control strategies discussed in this chapter has also been tested utilising a high-fidelity point-to-point MMC-HVDC model in [137]. Finally, the effect of using the active power control structures on the performance of MTDC systems is analysed using a four-terminal model in Section 4.3.

4.1 Two Types of Controllers

The schematic diagram of the active power control and the vector current control is illustrated in Figure 4.1. The inner current control is implemented in the dq-coordinate system. A feedforward current term is used to reduce the cross coupling effects between the two current control loops. A feedforward voltage term is used to compensate the grid voltage disturbance.

The fast-responding feedforward power controller assumes that the PLL angle always aligns with the PCC voltage. This open-loop controller, shown in Figure 4.1(a), is based on system inversion. Existing literature assumes the converter AC current has little impact on the system voltage v_d, thus this power control loop would have very similar dynamics to the d-axis current loop. However, this assumption may not be valid for a relatively weak AC system. In addition, steady-state error may not be fully avoided for this feedforward design.

For the feedback controller shown in Figure 4.1(b), fast active power regulation could not be achieved without a sufficiently high-bandwidth current loop. Unlike the FF structure, unknown disturbances are expected to have less effect on the control performance and more accurate regulation of active power can be achieved.

4.1.1 More Detailed Current Loop

The traditional plant of the dq current loop is established according to the following equations:

$$e_d - v_d = L\frac{di_d}{dt} + Ri_d - \omega Li_q, \quad e_q - v_q = L\frac{di_q}{dt} + Ri_q + \omega Li_d. \tag{4.1}$$

With $L_t=L+L_s$ and $R_t=R+R_s$, the difference between the d-axis converter voltage e_d and the d-axis AC source voltage v_{sd} can be modelled as:

$$e_d - v_{sd} = L_t \frac{di_d}{dt} + R_t i_d - \omega L_t i_q \,. \tag{4.2}$$

For the derivations in this section, v_{sd} and i_q are considered as disturbances of the i_d current control. The converter voltage reference e_d^* is the input to be manipulated. By combining (4.1) and (4.2), the d-axis voltage at the PCC can be written as

$$v_d = \frac{L_s}{L_t} e_d + \frac{L}{L_t} v_{sd} + \frac{LR_s - L_s R}{L_t} i_d . \tag{4.3}$$

Similarly, the q-axis PCC voltage can be represented as:

$$v_q = \frac{L_s}{L_t} e_q + \frac{L}{L_t} v_{sq} + \frac{LR_s - L_s R}{L_t} i_q . \tag{4.4}$$

The equation (4.3) indicates that the d-axis PCC voltage could be very sensitive to the variation of the converter voltage e_d with respect to weak AC system connections (large L_s). By combining (4.2) and (4.3), the following transfer functions can be derived for i_d and v_d:

$$\Delta i_d = \frac{1}{L_t s + R_t}\left(\Delta e_d - \Delta v_{sd} + \omega L_t \Delta i_q\right) \tag{4.5}$$

$$\Delta v_d = \frac{L_s s + R_s}{L_t s + R_t}\Delta e_d + \frac{Ls + R}{L_t s + R_t}\Delta v_{sd} + \frac{\omega\left(LR_s - L_s R\right)}{L_t s + R_t}\Delta i_q . \tag{4.6}$$

The plant model of the d-axis current control is formed from (4.1) and (4.6), as shown in Figure 4.2. The disturbances and the associated transfer functions are illustrated in (4.7).

$$\Delta d = \begin{bmatrix} \Delta v_{sd} & \Delta i_q \end{bmatrix}^T, \quad G_d(s) = \begin{bmatrix} \dfrac{Ls + R}{L_t s + R_t} & \dfrac{\omega(LR_s - L_s R)}{L_t s + R_t} \end{bmatrix} \tag{4.7}$$

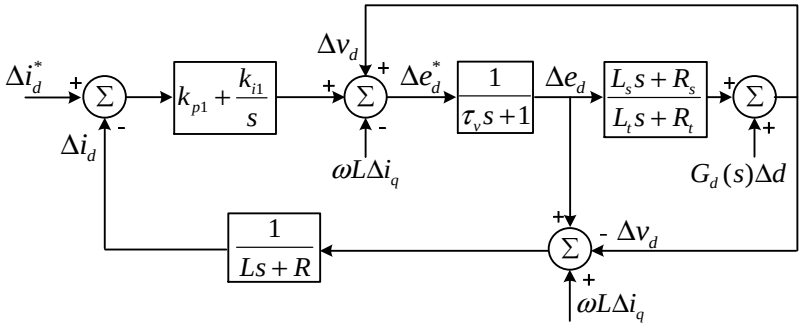


Figure 4.2: Model of the d-axis current loop.

The converter AC voltage modulation is approximated using a first-order system with time constant τ_v, according to the methodology shown in [87, 138]. Ideal measurements are assumed for the feedforward terms v_d and i_q.

4.1.2 Models for Feedforward and Feedback Power Control

The feedforward power controller, which assumes that the synchronisation is maintained by the PLL, can be linearised as:

$$i_d^* = \frac{P^*}{v_d} \;\Rightarrow\; \Delta i_d^* = \frac{\Delta P^*}{v_{do}} - \frac{P_o^*}{v_{do}^2}\Delta v_d \tag{4.8}$$

By employing per unit values, the factor of 1.5 can be eliminated in the representation of the instantaneous power injection into the AC system:

$$P = v_d i_d + v_q i_q \,. \tag{4.9}$$

Substituting (4.3) for v_d in (4.9), the active power can be found as (4.10), assuming v_q to be 0 pu. Considering the equation (4.11) that is derived based on (4.1) and (4.2), the equation (4.10) can be linearised and simplified as shown in (4.12). The general condition that $R \ll 1$ pu is assumed. The subscript "o" refers to the operating point (OP).

$$P = \frac{L_s}{L_t} e_d i_d + \frac{L}{L_t} v_{sd} i_d + \frac{LR_s - L_s R}{L_t} i_d^2 \tag{4.10}$$

$$\begin{bmatrix} e_{do} \\ v_{sdo} \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \end{bmatrix} \cdot v_{do} + \begin{bmatrix} R \\ -R_s \end{bmatrix} \cdot i_{do} + \begin{bmatrix} -\omega L \\ \omega L_s \end{bmatrix} \cdot i_{qo} \tag{4.11}$$

$$\begin{aligned} \Delta P &= \frac{L_s i_{do}}{L_t}\Delta e_d + \frac{L i_{do}}{L_t}\Delta v_{sd} + \left(\frac{L_s}{L_t} e_{do} + \frac{L}{L_t} v_{sdo} + 2 i_{do}\frac{LR_s - L_s R}{L_t}\right)\Delta i_d \\ &= \frac{L_s i_{do}}{L_t}\Delta e_d + \frac{L i_{do}}{L_t}\Delta v_{sd} + \left(\frac{L + L_s}{L_t} v_{do} + \frac{LR_s - L_s R}{L_t} i_{do} + \frac{\omega L_s L - \omega L L_s}{L_t}\right)\Delta i_d \\ &\approx \frac{L_s i_{do}}{L_t}\Delta e_d + \frac{L i_{do}}{L_t}\Delta v_{sd} + v_{do}\Delta i_d \end{aligned} \tag{4.12}$$

Substituting Δi_d in (4.12) with (4.5), and assuming $R_t L_s i_{do}/L_t \ll v_{do}$, the plant models of the converter voltage and the output disturbances are obtained as:

$$\begin{aligned} \Delta P &\approx \frac{L_s i_{do}}{L_t}\Delta e_d + \frac{L i_{do}}{L_t}\Delta v_{sd} + v_{do}\cdot\frac{1}{L_t s + R_t}\left(\Delta e_d - \Delta v_{sd} + \omega L_t \Delta i_q\right) \\ &\approx \frac{L_s i_{do} s + v_{do}}{L_t s + R_t}\Delta e_d + \frac{L i_{do} s - v_{do}}{L_t s + R_t}\Delta v_{sd} + \frac{\omega L_t v_{do}}{L_t s + R_t}\Delta i_q \end{aligned} \tag{4.13}$$

$$G_{d2}(s) = \begin{bmatrix} \dfrac{Li_{do}s - v_{do}}{L_t s + R_t} & \dfrac{\omega L_t v_{do}}{L_t s + R_t} \end{bmatrix} \tag{4.14}$$

By incorporating the current loop model, the block diagram of the feedforward loop is then structured as shown in Figure 4.3. The feedback controller employs a typical cascaded structure, shown in Figure 4.4, with the outer PI controller typically designed to enable the secondary loop to be at least four to ten times slower than the inner loop [1]. However, higher-order controllers can be incorporated into the methodology and the closed-loop system models presented here.

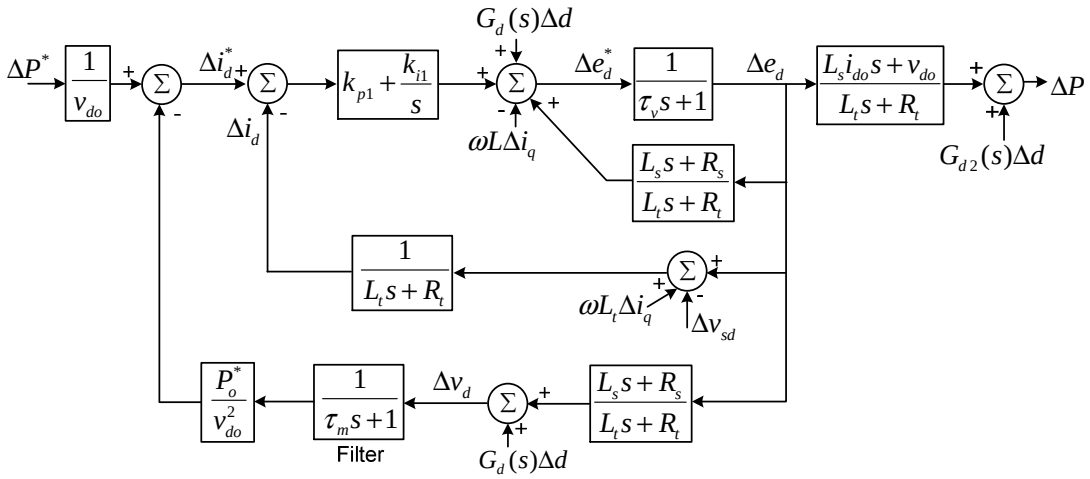


Figure 4.3: Linearised model of the feedforward active power control.

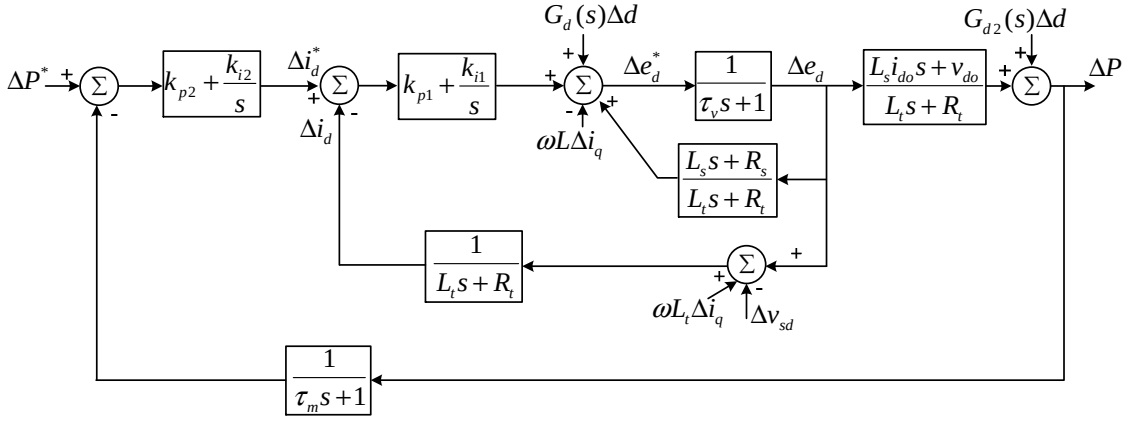


Figure 4.4: Linearised model of the feedback active power control.

It should be noted that, in the models presented above, the d-axis grid voltage v_{sd} and the q-axis current i_q have been treated as external disturbances, and the dynamic relations between the d-axis converter voltage e_d and these disturbances are ignored. However, realistically, as shown in (4.1), the change of e_d and i_d will transiently disturb the current i_q, and this will further cause the variations of the e_q if i_q is to be maintained. Consequently, this will lead to a non-zero v_q, as shown in (4.4), and cause coupling

between the active and reactive power control. The PLL with its relatively low-bandwidth will correct the drift of the voltage v_q by providing a new reference angle and this will result in the further change of v_{sd}.

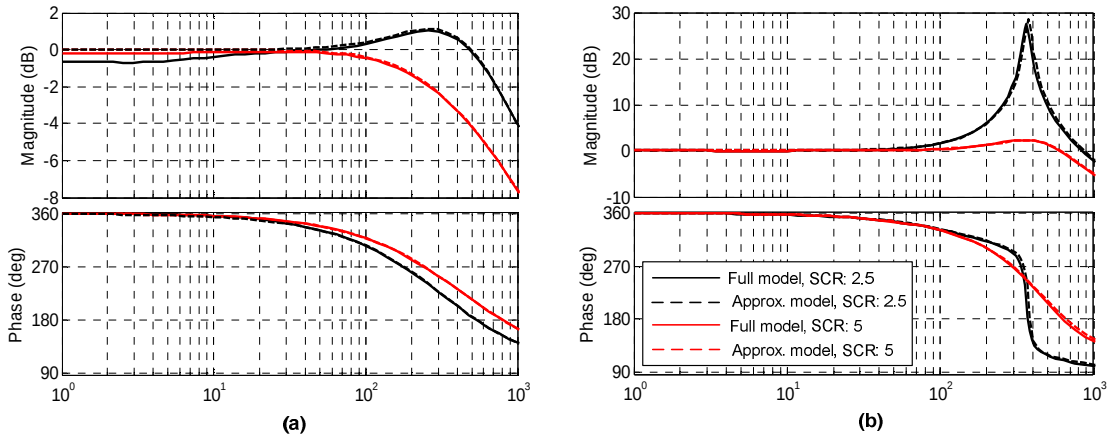


Figure 4.5: Frequency response comparisons for (a) the transfer function P(s)/i_d^*(s) and (b) the FF tracking transfer function P(s)/P*(s), (P_o=-0.6 pu rectifier, i_d loop bandwidth=200 Hz).

In order to verify the feasibility of the approximated models shown in Figure 4.3 and Figure 4.4, a full analytical model considering the dynamics of the q-axis and the PLL control was developed. The derivation of this more detailed model will be presented in Chapter 5. The frequency responses of the open-loop transfer function $P(s)/i_d^*(s)$ and the reference tracking transfer function for the FF control $P(s)/P^*(s)$ of the full model and the approximated model are compared in Figure 4.5, with two SCR settings.

Generally, the two models agree very well across the frequency range of interest and this confirms that the approximation of treating v_{sd} and i_q as exogenous disturbances for this active power stability study is reasonable. There is, though, a slightly larger steady-state difference between the transfer functions $P(s)/i_d^*(s)$ of the two models, for the scenario with the lower SCR. This is due to the fact that, for weaker AC systems, the same amount of d-axis current change causes larger variations of v_{sd} and i_q, and consequently the low-frequency interactions between the active and reactive loops become stronger.

4.1.3 Stability Criterions of the Active Power Control

A key insight revealed in Figure 4.3 is that, for a non-ideal AC grid model, the PCC voltage v_d is inherently affected by the current loop dynamics; and therefore, an indirect feedback is effectively formed between the VSC d-axis voltage e_d and the current reference i_d^*. An inverter operation with $P_o^* > 0$ introduces a negative feedback, while a rectifier operation with $P_o^* < 0$ leads to an undesired positive feedback. Hence, the

converter operating point can have a profound impact on the stability of the FF active power control.

The closed-loop transfer function that describes the reference tracking of the FF control is derived as (4.15), with the dynamics of the switching converter voltage control assumed to be beyond the frequency range of interest ($\tau_v \approx 0$).

$$\frac{\Delta P(s)}{\Delta P^*(s)} \approx \frac{\left(\frac{i_{do}}{v_{do}} L_s s + 1\right)\left(k_{p1} s + k_{i1}\right)}{\left(L + \frac{P_o^*}{v_{do}^2} k_{p1} L_s\right) s^2 + \left(k_{p1} + R + \frac{P_o^*}{v_{do}^2}\left(k_{p1} R_s + k_{i1} L_s\right)\right) s + \left(\frac{P_o^*}{v_{do}^2} R_s + 1\right) k_{i1}} \quad (4.15)$$

Therefore, to ensure two left-half plane poles, the stability criterion of the feedforward control loop is approximated as:

$$\frac{P_o^*}{v_{do}^2} > \max\left(-\frac{L}{k_{p1} L_s},\ -\frac{k_{p1} + R}{k_{p1} R_s + k_{i1} L_s}\right) \quad (4.16)$$

where inverter orientation is used for power flow (P>0 for inverter). As observed from (4.16), the key factors that affect the stability of the closed-loop FF power control include: the AC system strength (L_s and R_s), the current controller design (k_{p1} and k_{i1}), the converter impedance (R and L) and the operating point (P_o and v_{do}).

The stability of the FF power control can be improved by employing a filter $1/(\tau_m s+1)$ for the feedforward voltage v_d. The closed-loop transfer function $P(s)/P^*(s)$ can then be written as:

$$\frac{\Delta P(s)}{\Delta P^*(s)} \approx \frac{\left(\frac{i_{do}}{v_{do}} L_s s + 1\right)\left(k_{p1} s + k_{i1}\right)\left(\tau_m s + 1\right)}{D(s)}, \quad where \ \ D(s) = L\tau_m s^3 + \left(k_{p1} + R\right)\tau_m s^2 + \left(L + \frac{P_o^*}{v_{do}^2} k_{p1} L_s\right) s^2 + \left(k_{i1}\tau_m + k_{p1} + R + \frac{P_o^*}{v_{do}^2}\left(k_{p1} R_s + k_{i1} L_s\right)\right) s + \left(\frac{P_o^*}{v_{do}^2} R_s + 1\right) k_{i1} \quad (4.17)$$

According to the Routh's stability criterion [139], the operating point of the converter system should satisfy the following condition:

$$\frac{P_o^*}{v_{do}^2} > \max\left(-\frac{L + \tau_m\left(k_{p1} + R\right)}{k_{p1} L_s},\ -\frac{k_{p1} + R + \tau_m k_{i1}}{k_{p1} R_s + k_{i1} L_s}\right). \quad (4.18)$$

Using a larger filtering time constant τ_m results in smaller values of the limiting factors shown in the right-hand side of (4.18), and therefore the stability criterion can be more easily satisfied. The bandwidth of the filter should be reduced if the converter is connected to a weaker AC system or the bandwidth of the current loop is increased.

As demonstrated in Figure 4.3 and Figure 4.4, a right-half-plane (RHP) zero exists due to the term ($L_s i_{do} s + v_{do}$) in the loop transfer function, for a converter in rectifier operation ($i_{do} < 0$), despite the controller design. This RHP-zero could impose severe stability limitations, including inverse response, high-gain instability and restricted closed-loop bandwidth [1]. Particularly, for weaker AC systems (larger L_s) and converters operating in higher rectifying power (larger P_o and i_{do}), the RHP-zero migrates closer to the origin and results in stricter limitations on the achievable bandwidth of the active power control. According to [1], to achieve relatively satisfactory performance and stability margins (frequency peak of the sensitivity transfer function no larger than 2), the bandwidth of the active power control should be approximately limited as:

$$\omega_B^P < \frac{1}{2} \cdot \frac{-v_{do}}{L_s i_{do}} \approx \frac{1}{2} \cdot \frac{-v_{do}^2}{L_s P_o}, \quad for\ i_{do} < 0 \tag{4.19}$$

For low-order controllers such as PI controllers, to ensure a positive phase margin, the bandwidth of the power control loop is also limited by the phase lag of the plant model [1]:

$$\omega_B^P < \omega_u^P \quad \left(where\ \angle G_P\left(j\omega_u^P \right) = -180^\circ \right). \tag{4.20}$$

The two conditions above are solid for most of the active power control designs. Usually, the limitation shown in (4.19) is tighter than that in (4.20) for VSCs under rectifier operations. Provided with identical current loop settings, the FF control is more severely affected by these constraints as the bandwidth of the FF control is always higher than that of the FB control,.

4.1.4 Impact on the Voltage Droop Control

For V-P droop control, the active power control is presented as an actuator, denoted by the transfer function $T_P(s)$ in Figure 4.6. Note that $T_P(s)$ is depicted graphically in Figure 4.3 or Figure 4.4.

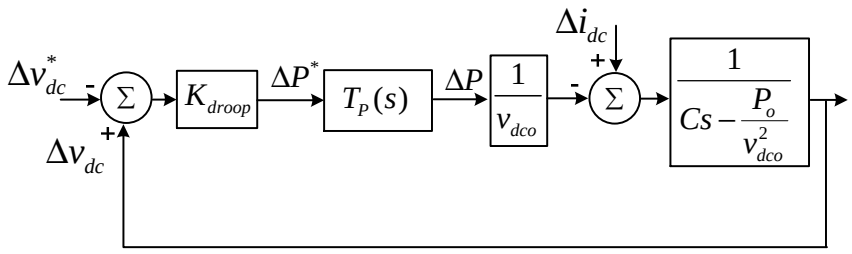


Figure 4.6: Linearised V-P droop control employing the power loop.

With reference to Figure 4.1, by considering the DC current injection as the disturbance and assuming the AC power at PCC to be nearly identical with the converter DC side power, the dynamics of the DC link can be approximated as (4.21). The closed-loop transfer function diagram of the droop control loop can then be derived as shown in Figure 4.6.

$$C_{dc}\frac{dv_{dc}}{dt} = i_{dc} - \frac{P}{v_{dc}} \quad \Rightarrow \quad \Delta v_{dc} = -\frac{1}{v_{dco}\left(C_{dc}s - \frac{P_o}{v_{dco}^2}\right)}\Delta P + \frac{1}{C_{dc}s - \frac{P_o}{v_{dco}^2}}\Delta i_{dc} \qquad (4.21)$$

In terms of stability, there are two limitations that need to be considered: the limitation imposed by the right-half plane (RHP) zero under rectifier operation and the limitation imposed by the RHP-pole under inverter operation.

Classical root locus analysis suggests that closed-loop poles migrate towards open-loop zeros as the controller gain increases [1]. Therefore, for VSCs under rectifier operation, as the droop gain K_{droop} increases, one pole of the DC voltage loop migrates to the RHP-zero and this leads to instability. This high-gain instability feature implies a fundamental limitation imposed by the converter active power plant model on the maximum achievable droop gain.

The inverter operation with $P_o>0$ results in a RHP-pole, and thus indicates an unstable DC link plant model, shown in Figure 4.6. Stabilisation of this system requires active power control to respond sufficiently fast, and this implies a lower bound on the bandwidth of the power loop. If the power loop is simplified as a first-order system with bandwidth of ω_B^P, the DC voltage reference tracking transfer function can be approximated as:

$$\frac{\Delta v_{dc}(s)}{\Delta v_{dc}^*(s)} = \frac{K_{droop}\omega_B^P}{C_{dc}v_{dco}} \cdot \frac{1}{s^2 + \left(\omega_B^P - \frac{P_o}{v_{dco}^2 C_{dc}}\right)s + \frac{\omega_B^P}{C_{dc}}\left(\frac{K_{droop}}{v_{dco}} - \frac{P_o}{v_{dco}^2}\right)}. \qquad (4.22)$$

The stability requirement of the power loop bandwidth ω_B^P is then approximated as:

$$\omega_B^P > P_o / (v_{dco}^2 C_{dc}) \tag{4.23}$$

The damping ratio of the transfer function shown in (4.22) can be derived as:

$$\zeta = \frac{\sqrt{\omega_B^P} - \frac{1}{\sqrt{\omega_B^P}} \frac{P_o}{C_{dc} v_{dco}^2}}{2\sqrt{\frac{K_{droop}}{v_{dco} C_{dc}} - \frac{P_o}{C_{dc} v_{dco}^2}}} \tag{4.24}$$

It is shown in (4.22) and (4.24) that decreasing the bandwidth ω_B^P degrades damping of closed-loop droop control. The rise of the droop gain K_{droop} leads to reduced steady-state DC voltage error and the increase of the droop gain however worsens the damping of the system. The transfer function models derived in Figure 4.3, 4.4 and 4.6 provide a useful framework for the analysis of droop control regarding local terminal dynamics.

4.2 Frequency-Response Analysis and Simulations

In this section, performance and robustness of the two types of active power control strategies discussed in Section 4.1 are evaluated using electromagnetic simulations in DSPF. The average-value VSC-HVDC model used in the simulations is rated at ±500 kV, 2000 MVA. Selected robustness and performance measures of closed-loop behaviours are computed in frequency domain using the analytical models presented in Section 4.1.

The i_d current controllers are designed analytically according to the desired bandwidth and damping, using the tuning method presented in Chapter 2. The feedback power controllers are tuned based upon the Skogestad IMC method [1], to achieve a reasonable trade-off between robustness and disturbance rejection performance.

4.2.1 Impact of Controller Bandwidth

For a step change of the power reference from 1000 MW to 1020 MW, the responses of the d-axis converter voltage e_d and the rectifying power are shown in Figure 4.7, for a FF control case and three FB control cases configured with different bandwidth (BW) settings. The magnitude of the manipulated input e_d for the FF control is larger and more oscillatory than the ones for the three FB scenarios. Considering that this is only 1% step change of the power reference, the converter voltage limit could be easily violated by the FF control scheme, and this will lead to saturated performance during severe transients.

The presence of the RHP zero implies an initial undershoot, as demonstrated in the power responses for both FF and FB control. Much smoother but slower responses are provided using the FB control structure. The frequency domain peaks, such as the maximum values of the sensitivity function $S(s)$ and complementary sensitivity function $T(s)$, denoted as M_S (or $\|S\|_\infty$) and M_T (or $\|T\|_\infty$) respectively, are effective indicators of the quality of the closed-loop system behaviour. Typically larger values of M_S and M_T suggest poorer transient performance, and poorer robustness to plant uncertainties and unmodelled dynamics [1]. Specifically, both M_S and M_T correlate well with the closed-loop robustness and the reference tracking performance, and M_S is also a very effective measure of the disturbance rejection capability. The peak of the transfer function $CS(s)$ $[\Delta e_d(s)/\Delta P^*(s)]$ relating the controller output and the setpoint, denoted as M_{CS} (or $\|CS\|_\infty$), correlates well with the input usage, which in this case refers to the utilisation of the converter current and voltage. Larger values of M_{CS} indicate higher possibilities of saturation of converter AC voltage and current.

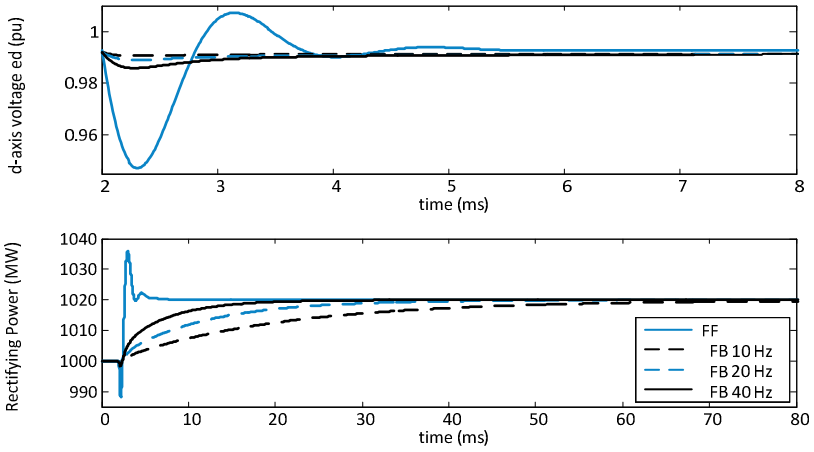


Figure 4.7: Step responses of the power loops of different bandwidths (i_d loop bandwidth=250 Hz, SCR=5).

Table 4.1: Frequency domain measures for the controls simulated in Figure 4.7.

Controller	M_T (dB)	M_S (dB)	M_{CS} (dB)	*GM* (dB)	*PM* (deg)
FF	8.65	8.71	19.2	3.38	Inf
FB 40 Hz	0	1.56	-2.28	16.3	97.1
FB 20 Hz	0	0.77	-8.96	22.2	93.9

Selected frequency domain measures of the analytical models corresponding to the simulation models in Figure 4.7 are presented in Table 4.1. These include gain margin (GM), phase margin (PM), and the key frequency domain peaks M_S, M_T and M_{CS}. The results in Table 4.1 agree well with the simulations shown in Figure 4.7. An increase in

the power loop bandwidth results in poorer robustness and higher demand of the VSC voltage, demonstrated by the increase of M_S and M_{CS}. For the FF control, the GM and PM are calculated using the equivalent loop transfer function shown in (4.25), which is obtained from graphical inspection of Figure 4.3.

$$L_{FF}(s) = \frac{\Delta e_d(s)}{\Delta i_d^*(s)} \cdot \frac{L_s s + R_s}{L_t s + R_t} \frac{P_o^*}{v_{do}^2} \tag{4.25}$$

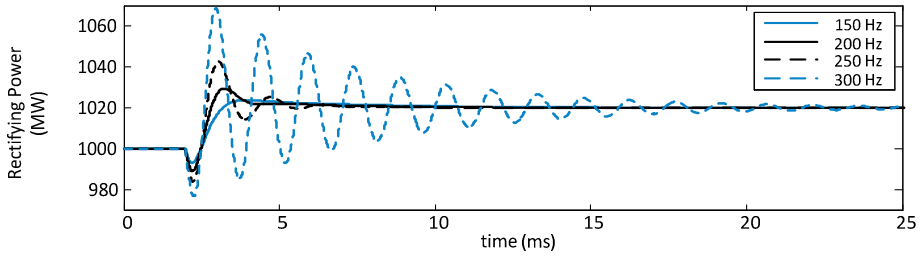


Figure 4.8: Step responses of FF control systems with various current loop bandwidths (SCR=4).

Table 4.2: Impact of current loop bandwidth on the FF Control and the FB control (feedback power loop bandwidth=12.5Hz, SCR=4)

i_d loop BW	FB Control 12.5Hz			FF Control		
	M_S (dB)	M_{CS} (dB)	GM (dB)	M_S (dB)	M_{CS} (dB)	GM (dB)
150	0.68	-16.7	29	6.29	11.1	6.34
225	0.52	-13.4	25.4	12.7	20.9	2.61
300	0.38	-10.7	22.9	24.8	35	0.59

The impact of the inner current loop bandwidth (BW) on the behaviours of the FF control is clearly shown in Figure 4.8 and Table 4.2. High-bandwidth current control can result in an oscillatory behaviour, and therefore the FF control structure imposes an upper bound on the current loop bandwidth. In contrast, the current loop dynamics have much less impact on the slow FB control with a bandwidth of 12.5 Hz.

4.2.2 Sensitivity Analysis

Sensitivity studies regarding the AC system strength, the converter operating point (OP) and the PCC bus voltage were undertaken.

For an SCR of the AC system ranging from 2 to 5, responses to a 50 MW power reference step from the converter d-axis voltage and the power are shown in Figure 4.9. As the strength of the AC system decreases and the equivalent source impedance increases, the PCC bus voltage becomes more sensitive to the variation of the converter AC terminal voltage. In that case, the change of the active converter current for VSCs in

rectifier operation could induce a strong positive feedback effect, and therefore may lead to poor stability.

It is demonstrated in Table 4.3 that the SCR could significantly affect both the stability and the output performance of the FF control, especially for a SCR less than 3. In contrast, the slow FB control loop shows sufficient robustness for weak AC networks and should be adopted in those cases.

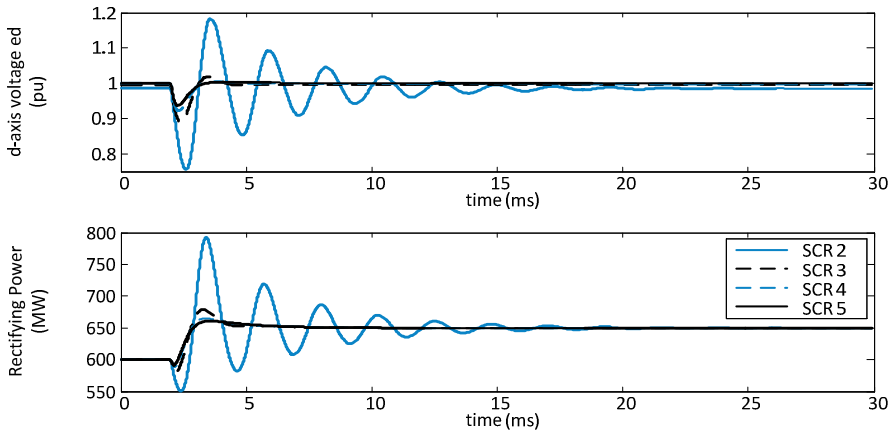


Figure 4.9: Impact of SCR on the performance of FF control (i_d loop bandwidth=200 Hz).

Table 4.3: Impact of SCR on the frequency domain measures (i_d loop BW=200 Hz, P_o=0.3 pu INV)

SCR	FB Control (20Hz)		FF Control	
	M_S (dB)	*GM* (dB)	M_S (dB)	*GM* (dB)
2	1.09	19.3	21.1	0.94
3	0.72	23.2	8.59	4.62
4	0.54	25.9	5.93	7.20

Another important factor that affects the dynamics of the active power control is the power setpoint, as shown in Figure 4.10 and Table 4.4. Satisfactory performance is shown for inverter operation. However, the increase of the rectifying power moves the RHP-zero closer to the origin, and degrades the controllability, regardless of the power controller designs. For the FF control, it also amplifies the positive feedback effect of the FF control and deteriorates dynamic performance. Thus, it appears that the FB control could be the preferred option for converters with large power variations.

Under rectifier operation, the dynamics of the FF control with fast current loop are also sensitive to the system bus voltage, as shown in Figure 4.11. Decreasing the voltage OP has a similar effect as increasing the rectifying power, as demonstrated in (4.15). This feature of FF control implies its vulnerability to AC voltage sags. Therefore, the FF

active power control may have to reduce its bandwidth in order to achieve a satisfactory AC fault ride-through performance.

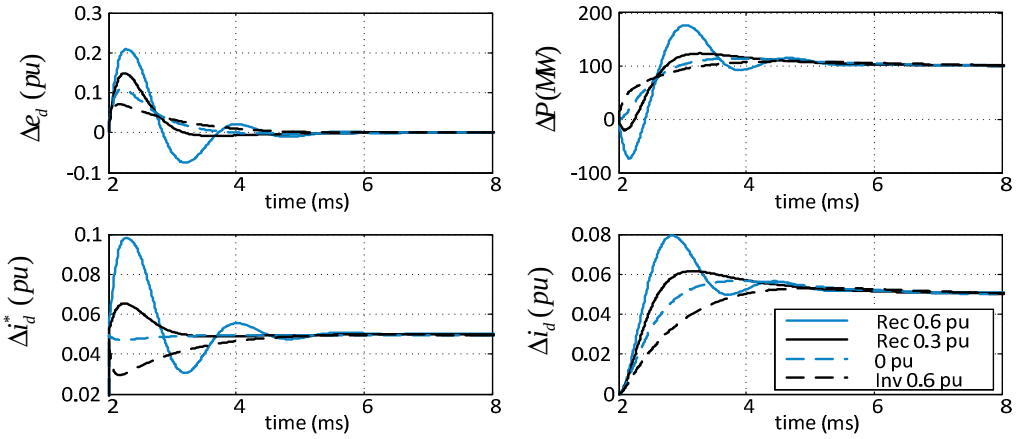


Figure 4.10: Step responses of the FF power control under a series of power operating points (SCR=5, i_d loop bandwidth=250 Hz).

Table 4.4: Impact of the power OP on the frequency domain indicators (for SCR=5, i_d loop BW=250 Hz)

P_o^* (pu)	FB Control (20 Hz)		FF Control	
	M_S (dB)	*GM* (dB)	M_S (dB)	*GM* (dB)
REC 0.6	0.816	21.5	12.51	2.64
REC 0.3	0.447	27.5	4.81	8.67
0	0.122	Inf	1.02	Inf
INV 0.6	0.060	Inf	0	Inf

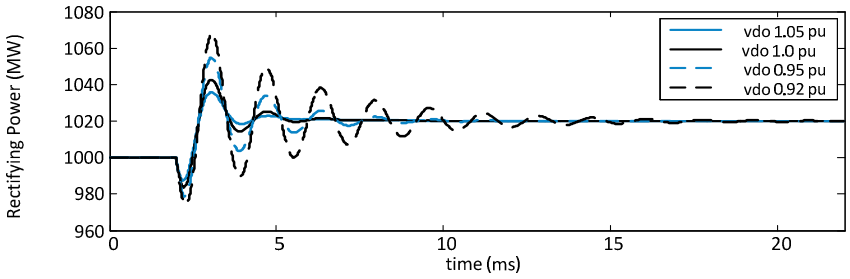


Figure 4.11: Impact of the PCC voltage on the step response of the FF power control (SCR=4, i_d loop bandwidth=250 Hz).

4.2.3 Simulations of SISO Droop Control

Simulations for a single-terminal VSC-HVDC model with DC voltage droop control are presented in this part. A DC current disturbance model is used to represent the power variations of the DC grid. The frequency domain analysis of the single-input single-output (SISO) DC voltage loop is provided to reveal the limitations imposed by the active power control design on the droop setting.

Responses of the DC voltage, the converter power and the d-axis voltage e_d, to a 0.2 kA step of the DC current disturbance are shown in Figure 4.12. The droop control gain K_{droop} of 20 is applied for the four active power control scenarios[7]. Best disturbance rejection response is provided by the fast feedforward control, which can rapidly respond to the DC power disturbance. However, such rapid response does come at the cost of requiring large converter voltage, which may lead to overmodulation of the converter.

The findings from Figure 4.12 indicate that a trade-off has to be made between the DC disturbance rejection performance of MTDC systems and the robustness of the power control loop. The maximum allowed droop gain calculated from root locus analysis for the FF control and the 20 Hz FB control are shown in Table 4.5. This demonstrates the high-gain instability induced by the RHP-zero stated in Section 4.1. Larger capacitor size usually corresponds to a stiffer DC voltage plant, better stability margins, and smoother and more stable transient responses. The increase of the rectifying power induces a decrease of the maximum gain and a tighter upper bound on the droop control bandwidth. The results show that the FB control allows a larger degree of freedom in choosing the droop gain.

The frequency domain analysis for the droop voltage loop employing the 25 Hz and 12.5 Hz FB power control is shown in Table 4.6. Larger values of the gain K_{droop} result in a higher bandwidth ω_B^{vdc} of the closed-loop DC voltage control and therefore faster responses to power variations in the DC grid. However, this has a negative impact on the robustness of the droop control, indicated by the *GM*, the *PM* and the sensitivity peak M_S. Furthermore, increasing K_{droop} could also reduce the quality of the transient performance, shown by the decrease of the damping ratio ζ of the dominant complex poles and the increase of the sensitivity peak.

[7] All the droop gains used in this thesis are dimensionless, since system parameters including voltages, currents and powers are configured based upon per unit values.

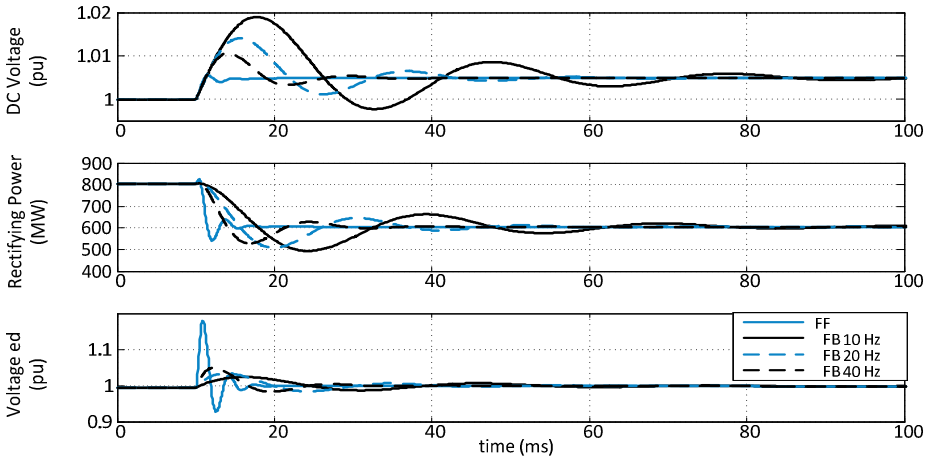


Figure 4.12: Simulations of a 0.1pu step of DC current disturbance for droop control based on different power control modes.

Table 4.5: Maximum droop gain K_{droop} allowed for the FF and the 20 Hz FB power control, with SCR=4 and current BW=200 Hz (rectifier OP).

	FF control			20 Hz FB control		
P_o	-0.2 pu	-0.5 pu	-0.8 pu	-0.2 pu	-0.5 pu	-0.8 pu
C_{dc}=30 µF	41.4	18.9	2.19	148	71.6	46.5
C_{dc}=60 µF	82.7	37.7	4.80	293	127	89.6
C_{dc}=90 µF	125	55.5	7.08	420	196	124
C_{dc}=180 µF	249	112	14.0	853	392	244

Table 4.6: Frequency domain measures for the droop control with C_{dc}=66 µF and P_o=-0.8 pu REC, SCR=4.

	25 Hz FB power control					12.5 Hz FB power control				
K_{droop}	M_S (dB)	ζ	GM (dB)	PM (deg)	ω_B^{vdc} (Hz)	M_S (dB)	ζ	GM (dB)	PM (deg)	ω_B^{vdc} (Hz)
10	3.97	0.42	20.4	45.7	21.9	5.08	0.34	23.5	38.3	15.9
20	6.18	0.32	14.4	32.8	31.7	7.23	0.26	17.5	27.7	22.5
40	9.80	0.22	8.35	20.8	46.2	10.1	0.19	11.5	19.0	32.3

4.3 Simulations Studies Using a Four-Terminal Model

A four-terminal VSC-HVDC model built in DSPF was employed to evaluate the performance of the two active power control structures and their impact on the behaviours of the outer droop control, under AC fault and converter outage conditions. The network diagram and V-P droop characteristics for each grid side converter stations (GSCs) are shown in Figure 4.13. An identical droop constant of 5% (K_{droop}=20) is used for all the three GSCs.

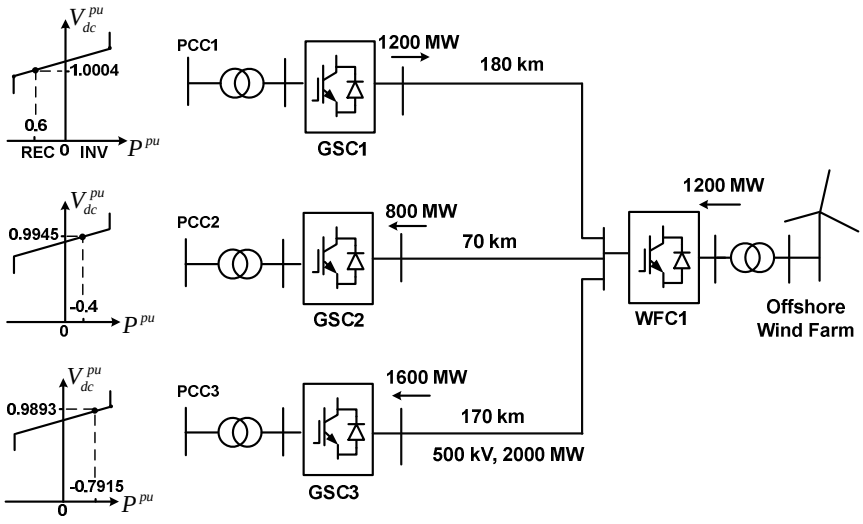


Figure 4.13: Four-Terminal test network and droop characteristics.

Simulation of an AC system fault has been performed, for the control scenarios where FF or 20-Hz FB power control is adopted by the droop control for GSC1. The responses of the DC voltage and power of GSC1 are shown in Figure 4.14. A fault causing a 30% voltage sag at the PCC1 occurs at 0.1 s and is cleared after 150 ms. Severe transients are experienced by the FF case. This is mainly due to the insufficient robustness of the FF control to the AC system voltage. The other reason is that the FF control highly relies on the synchronous frame provided by the PLL. During severe fault circumstances, the PLL is not capable to maintain its alignment, and this could result in severe power oscillations due to the adverse interactions between the active and reactive power control.

In order to investigate the impact of the power control on the interoperability of MTDC systems, simulations of the loss of GSC3 are performed for three control scenarios. The result associated with GSC1 is shown in Figure 4.15. In scenario 1, a 20-Hz FB power control is utilised by all GSCs. In scenario 2, the FF controller is applied to GSC1, while FB design is used by GSC2. An identical FF controller is used by all GSCs in scenario 3. The FF control shows a more damped performance to the FB control in this case. In a

multi-vendor system where a combination of the FF and FB control is applied for the droop control, the terminals with FF control take more responsibilities in stabilising the DC voltage, with their powers responding more actively and aggressively to DC grid disturbances.

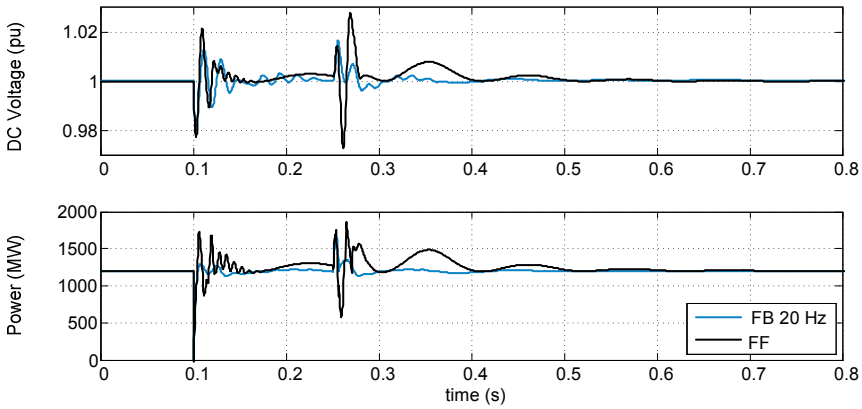


Figure 4.14: Responses of the DC voltage and power of GSC1 to 30% voltage sag at PCC1 (i_d loop bandwidth=200 Hz; SCR=4).

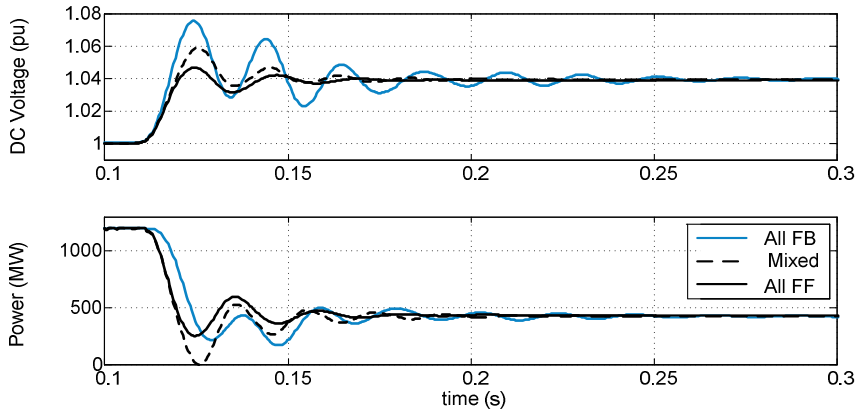


Figure 4.15: Responses of the DC voltage and power of GSC1 to the outage of GSC3.

4.4 Chapter Summary

The frequency domain responses and time domain simulations in this chapter reveal the fundamental stability and robustness issues of active power control for converters in rectifier operations. The controllability limitations imposed by the current control bandwidth, the AC system strength and the power operating point on the active power loop have been evaluated analytically. The results can be used to establish initial guidelines for controller structure design and bandwidth setting for active power control.

Limitations imposed by the active power control systems on the stability and performance of the voltage-power droop control have been analysed. For rectifiers connected to a weak AC system, a fast feedforward power loop could imply high-gain instability and restricted stability margins for the voltage droop control. High-gain droop control is not recommended from the perspective of robustness and transient performance. Better disturbance rejection performance of the droop control can be achieved by employing a faster power controller.

Generally the feedback approach is recommended due to its superior stability and robustness. However, when fast control of active power is required, a feedforward design may be preferred for the VSCs normally operating as inverters, provided that a relatively strong AC network exists.

Chapter 5 Small-Signal Modelling of VSC-MTDC

Multi-Terminal VSC-HVDC is a highly nonlinear multi-input-multi-output (MIMO) system. Linearised small-signal models, which are usually in state-space form, are commonly used in power systems to investigate dynamic characteristics. This type of model is required by analytical techniques including modal analysis, frequency-response analysis and advanced controller designs for the study of large-scale MIMO systems.

Frequency-domain analysis based upon small-signal analytic models were widely used to identify the stability issues associated with LCC-HVDC [140-142]. Transfer function models of LCC systems based upon describing function [143] were derived in [140, 144] where the LCC converter was represented by a multi-port network. A small-signal LCC model which uses a piecewise representation of distorted DC and AC waveforms was presented in [145].

Some good work has been provided in the previous literature with respect to the analytical modelling of VSC systems [85, 100, 133, 134, 146-150]. State-Space modelling methods of VSCs for microgrid applications are provided in [148, 149]. Small-Signal models are constructed in [134, 150] for VSC-HVDC systems regarding the study of weak AC system connection. However, the PLL model is not incorporated in [100, 133, 147], and the DC voltage control is not considered in detail in [134, 146, 148, 150]. Further work is required to construct the state-space model for an up-to-date AVM with a variety of control configurations. Moreover, the experience in developing an analytical DC network model and integrating such a model with a flexible number of converter terminals is limited. Sensitivity studies based on modal analysis with the focus on DC system parameterisation have not been carried out in detail in previous literature.

This chapter aims to provide generalised analytical models that capture the key dynamics of the MTDC systems within the frequency range for slow-transient stability studies.

5.1 Modelling of Grid Side Converter (GSC)

The state-space model of the grid side converters (GSCs) is developed here according to the converter model and controllers discussed in Chapter 2. Based upon the notations shown in Figure 5.1 for the AVM model, the complete closed-loop GSC model, which includes the AC and DC system plant, the detailed current controller and the PLL, and various outer controllers will be constructed by interconnecting several sub-systems. The main focus of this section is to provide the linearised dynamic equations and the model formulation for the grid side VSC system, subjected to an equilibrium point of the system.

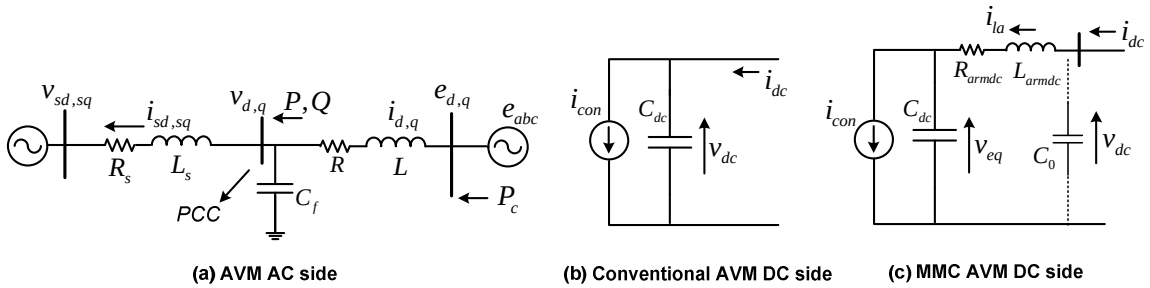


Figure 5.1: VSC-HVDC system for analytical modelling.

5.1.1 Modelling of AC Side Dynamics and PLL

The system dynamics of the currents across the equivalent converter reactor and the network impedance can be derived as:

$$\frac{d\Delta i_d}{dt} = \frac{\Delta e_d}{L} - \frac{\Delta v_d}{L} - \frac{R}{L}\Delta i_d + \omega\Delta i_q, \quad \frac{d\Delta i_q}{dt} = \frac{\Delta e_q}{L} - \frac{\Delta v_q}{L} - \frac{R}{L}\Delta i_q - \omega\Delta i_d \tag{5.1}$$

$$\frac{d\Delta i_{sd}}{dt} = \frac{\Delta v_d}{L_s} - \frac{\Delta v_{sd}}{L_s} - \frac{R_s}{L_s}\Delta i_{sd} + \omega\Delta i_{sq}, \quad \frac{d\Delta i_{sq}}{dt} = \frac{\Delta v_q}{L_s} - \frac{\Delta v_{sq}}{L_s} - \frac{R_s}{L_s}\Delta i_q - \omega\Delta i_{sd} \tag{5.2}$$

where e_{dq}, v_{dq} and v_{sdq} represent the VSC AC terminal voltage, the PCC bus voltage and the AC source voltage in dq domain, respectively. Including the filter capacitance C_f enables v_d and v_q to be state variables, as shown in (5.3), and therefore facilitates the small-signal modelling.

$$\frac{d\Delta v_d}{dt} = \frac{\Delta i_d}{C_f} - \frac{\Delta i_{sd}}{C_f} + \omega\Delta v_q, \quad \frac{d\Delta v_q}{dt} = \frac{\Delta i_q}{C_f} - \frac{\Delta i_{sq}}{C_f} - \omega\Delta v_d \tag{5.3}$$

It is noted that v_{sd} and v_{sq} are neither state variables nor known inputs in (5.2). However, they can be related to the PLL dynamics based on the following equation:

$$\begin{pmatrix} v_{sd} \\ v_{sq} \end{pmatrix} = \begin{pmatrix} \cos\theta_m & \sin\theta_m \\ -\sin\theta_m & \cos\theta_m \end{pmatrix} \begin{pmatrix} \hat{V}_s \cos\theta_s \\ \hat{V}_s \sin\theta_s \end{pmatrix} = \begin{pmatrix} \hat{V}_s \cos(\theta_s - \theta_m) \\ \hat{V}_s \sin(\theta_s - \theta_m) \end{pmatrix} \tag{5.4}$$

where θ_s and $\hat{V}_s$ are the angle and magnitude of the voltage vector v_s respectively, and θ_m is the reference angle produced by the PLL. The equation (5.4) is also valid if θ_s and θ_m are not instantaneous angles but relative angles with respect to a synchronous reference rotating at nominal speed ω_o:

$$\theta_s = \omega_s t - \omega_o t + \theta_{so}, \quad \theta_m = \omega_m t - \omega_o t + \theta_{mo}. \tag{5.5}$$

Assuming that the magnitude and frequency of the voltage v_s do not vary, the equation (5.4) can be further linearised as:

$$\begin{aligned} \Delta v_{sd} &= \hat{V}_{so} \sin(\theta_{so} - \theta_{mo})(\Delta\theta_m - \Delta\theta_s) \approx v_{sqo}\Delta\theta_m \\ \Delta v_{sq} &= \hat{V}_{so} \cos(\theta_{so} - \theta_{mo})(\Delta\theta_s - \Delta\theta_m) \approx -v_{sdo}\Delta\theta_m \end{aligned} \tag{5.6}$$

where

$$\Delta\theta_m = (\omega_m - \omega_o)t = \Delta\omega_m t, \quad \Delta\theta_s = (\omega_s - \omega_o)t = 0. \tag{5.7}$$

The relative angles are used for the small-signal modelling since a instantaneous angle does not have a equilibrium point. Furthermore, the terms Δv_{sdq} in (5.2) need to be substituted by (5.6), since they are intermediate variables and are not defined explicitly for initial conditions.

More complex AC networks can be conveniently incorporated in the small-signal model, given that the differential equations representing the electromagnetic dynamics of the AC system are derived within the dq-coordinate frame provided by the PLL.

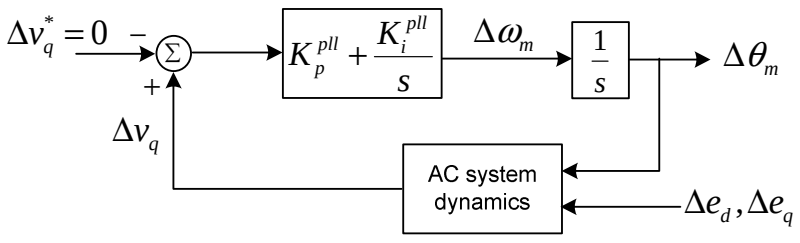


Figure 5.2: Closed-Loop SRF PLL.

The most commonly used synchronous reference frame (SRF) PLL [56], with its small-signal model linearised as shown in Figure 5.2, is employed here. The dynamics of the reference angle and the PI loop filter are:

$$\frac{d\Delta\theta_m}{dt} = K_p^{pll}\Delta v_q + \Delta x_{pll}, \quad \frac{d\Delta x_{pll}}{dt} = K_i^{pll}\Delta v_q . \tag{5.8}$$

5.1.2 Modelling of the DC Side Dynamics

According to the AVM shown in Figure 5.1(b), the dynamics of the conventional DC link model can be linearised as:

$$\frac{d\Delta v_{dc}}{dt} = \frac{\Delta i_{dc}}{C_{dc}} + \frac{P_{co}}{C_{dc}v_{dco}^2}\Delta v_{dc} - \frac{1}{C_{dc}v_{dco}}\Delta P_c . \tag{5.9}$$

In [39], it is suggested that an equivalent arm inductance should be modelled on the DC side for the MMC, as shown in Figure 5.1(c). For improved accuracy, the following equations might be adopted instead of (5.9).

$$\frac{d\Delta i_{la}}{dt} = \frac{\Delta v_{dc}}{L_{armdc}} - \frac{\Delta v_{eq}}{L_{armdc}} - \frac{R_{armdc}}{L_{armdc}}\Delta i_{la}, \quad \frac{d\Delta v_{dc}}{dt} = \frac{\Delta i_{dc}}{C_0} - \frac{\Delta i_{la}}{C_0} \tag{5.10}$$

$$\frac{d\Delta v_{eq}}{dt} = \frac{\Delta i_{dc}}{C_{dc}} + \frac{P_{co}}{C_{dc}v_{eqo}^2}\Delta v_{eq} - \frac{1}{C_{dc}v_{eqo}}\Delta P_c \tag{5.11}$$

In this case, the voltage v_{dc} across the equivalent capacitance C_{dc} and inductance L_a is the DC voltage to be measured. A small equivalent capacitance C_0 is incorporated to enable v_{dc} to be a state variable to facilitate the generalised modelling. The converter AC power deviation ΔP_c in (5.9) and (5.11) needs to be substituted by (5.12), which is derived based upon AC/DC power balance principle, with the converter valve loss ignored.

$$P_c = e_d i_d + e_q i_q \quad \Rightarrow \quad \Delta P_c = i_{do}\Delta e_d + e_{do}\Delta i_d + i_{qo}\Delta e_q + e_{qo}\Delta i_q \tag{5.12}$$

5.1.3 Modelling of Current Control

A first-order transfer function with a small time constant τ_v is used here to represent VSC modulation control. This enables the converter AC terminal voltages e_d and e_q to become variables and therefore reduce the complexity of the state-space model. The dynamics related to this state variable can then be described as:

$$\frac{d\Delta e_d}{dt} = \frac{1}{\tau_v}\left(\Delta e_d^* - \Delta e_d\right), \quad \frac{d\Delta e_d}{dt} = \frac{1}{\tau_v}\left(\Delta e_q^* - \Delta e_q\right). \tag{5.13}$$

The dynamics of the integrators in the two current controllers can be described by:

$$\frac{d\Delta x_{id}}{dt} = K_i^{id}\left(\Delta i_d^* - \Delta i_d\right), \quad \frac{d\Delta x_{iq}}{dt} = K_i^{iq}\left(\Delta i_d^* - \Delta i_q\right) \tag{5.14}$$

where x_{id} and x_{iq} are defined as the state variables of the two integrators. Considering that typically feedforward decoupling is employed for the dq current controllers, as shown in Figure 2.4, the differential equations regarding the VSC AC terminal voltage are further derived based on (5.13) as:

$$\begin{aligned}\frac{d\Delta e_d}{dt} &= \frac{1}{\tau_v}\left[K_p^{id}\left(\Delta i_d^* - \Delta i_d\right) + \Delta x_{id} + \Delta v_d - \omega L \Delta i_q - \Delta e_d\right] \\ \frac{d\Delta e_q}{dt} &= \frac{1}{\tau_v}\left[K_p^{iq}\left(\Delta i_q^* - \Delta i_q\right) + \Delta x_{iq} + \Delta v_q + \omega L \Delta i_d - \Delta e_q\right].\end{aligned} \tag{5.15}$$

5.1.4 Modelling of Outer Control Loops

The equations (2.32) and (2.33), which represent the per unit active and reactive power injected into the PCC bus from the converter, can be linearised as:

$$\Delta P = v_{do}\Delta i_d + i_{do}\Delta v_d + v_{qo}\Delta i_q + i_{qo}\Delta v_q \tag{5.16}$$

$$\Delta Q = v_{qo}\Delta i_d + i_{do}\Delta v_q - v_{do}\Delta i_q - i_{qo}\Delta v_d \tag{5.17}$$

The dynamics regarding to the state variables of the integrator in the PQ controllers are:

$$\frac{d\Delta x_P}{dt} = K_i^P\left(\Delta P^* - \Delta P\right), \quad \frac{d\Delta x_Q}{dt} = K_i^Q\left(\Delta Q - \Delta Q^*\right). \tag{5.18}$$

The dq current references can then represented by:

$$\Delta i_d^* = K_p^P\left(\Delta P^* - \Delta P\right) + \Delta x_P, \quad \Delta i_q^* = K_p^Q\left(\Delta Q - \Delta Q^*\right) + \Delta x_Q \tag{5.19}$$

The quantities ΔP and ΔQ in (5.18) and (5.19) need be substituted by (5.16) and (5.17), in order to form the state-space model. The current references in (5.14) and (5.15) should then be replaced by the updated (5.19). The linearised form of the instantaneous voltage of the PCC bus is derived as:

$$v_{ac} = \sqrt{v_d^2 + v_q^2} \;\Rightarrow\; \Delta v_{ac} = \frac{v_{do}}{\sqrt{v_{do}^2 + v_{qo}^2}}\Delta v_d + \frac{v_{qo}}{\sqrt{v_{dco}^2 + v_{qo}^2}}\Delta v_q. \tag{5.20}$$

The linearised equations related to the PI AC voltage controller are shown as:

$$\frac{d\Delta x_{vac}}{dt} = K_i^{vac}\left(\Delta v_{ac} - \Delta v_{ac}^*\right), \quad \Delta i_q^* = K_p^{vac}\left(\Delta v_{ac} - \Delta v_{ac}^*\right) + \Delta x_{vac} \tag{5.21}$$

When the droop V_{ac}-Q control discussed in Section 2.1.7 is employed, the following equations should be adopted for the modelling of the AC voltage controller:

$$\begin{aligned} \frac{d\Delta x_Q}{dt} &= -K_i^Q \left[K_{VQ} \left(\Delta v_{ac}^* - \Delta v_{ac} \right) + \Delta Q^* - \Delta Q \right] \\ \Delta i_q^* &= -K_p^Q \left[K_{VQ} \left(\Delta v_{ac}^* - \Delta v_{ac} \right) + \Delta Q^* - \Delta Q \right] + \Delta x_Q . \end{aligned} \tag{5.22}$$

Please note that Δv_{ac} in (5.21) and (5.22) needs to be substituted by (5.20), and the i_q reference in (5.14) and (5.15) should be replaced by the representation in (5.21) or (5.22).

The equations representing the typical PI DC voltage controller are shown as:

$$\frac{d\Delta x_{vdc}}{dt} = K_i^{vdc} \left(\Delta v_{dc} - \Delta v_{dc}^* \right), \quad \Delta i_d^* = K_p^{vdc} \left(\Delta v_{dc} - \Delta v_{dc}^* \right) + \Delta x_{vdc} . \tag{5.23}$$

Regarding a typical V-P droop control, the following equations should be adopted:

$$\begin{aligned} \frac{d\Delta x_P}{dt} &= K_i^P \left[K_{droop} \left(v_{dc} - v_{dc}^* \right) + P_{ac}^* - \Delta P_{ac} \right] \\ \Delta i_d^* &= K_p^P \left[K_{droop} \left(v_{dc} - v_{dc}^* \right) + P_{ac}^* - \Delta P_{ac} \right] + \Delta x_P . \end{aligned} \tag{5.24}$$

The dynamics of a V-I droop controller are represented as:

$$\begin{aligned} \frac{d\Delta x_{vdc}}{dt} &= K_i^{vdc} \left[\Delta v_{dc} - \Delta v_{dc}^* + R_{droop} \left(\Delta i_{dc}^* - \Delta i_{dc} \right) \right] \\ \Delta i_d^* &= K_p^{vdc} \left[\Delta v_{dc} - \Delta v_{dc}^* + R_{droop} \left(\Delta i_{dc}^* - \Delta i_{dc} \right) \right] + \Delta x_{vdc} . \end{aligned} \tag{5.25}$$

Depending on the VSC control configuration, appropriate differential equations should be selected to describe the outer converter controllers.

5.1.5 Integration of Sub-Systems for GSC

By combining the differential equations discussed above, a generalised state-space model can then be constructed for a GSC terminal. This model is formulated by interconnecting the sub-systems, based on the closed-loop structure shown in Figure 5.3 where the state variables of each sub-system are explicitly presented. The detailed model derivations and the resulting state-space matrices are provided in Appendix C.2 and C.3. The small-signal model is sensitive to the system operating conditions. Therefore, power flow results are required to calculate the initial condition of this dynamic model, with detailed derivations provided in Appendix C.5.

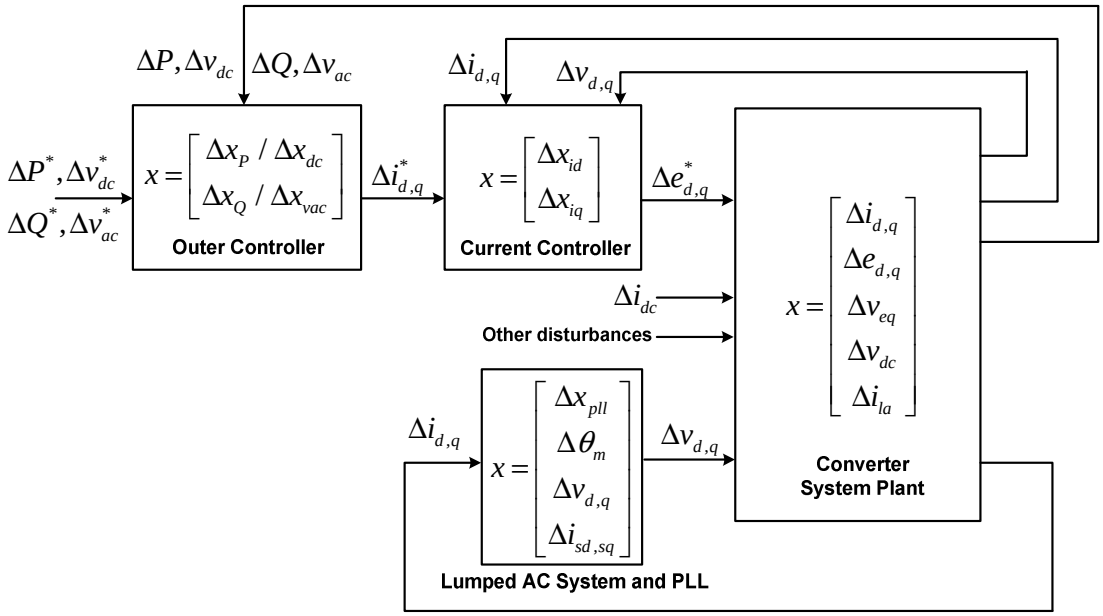


Figure 5.3: Generalised state-space model for grid side VSC-HVDC.

The model structure based upon Figure 5.3 can be conveniently modified into different open-loop and closed-loop models to suit various studies, such as controllability analysis with respect to the system plant, analysis of system stability and disturbance rejection performance, and analytical comparison of different controller designs.

5.2 Modelling of Wind Farm Side Converter Terminal

The simplified wind farm model (SWF) and the WFC model discussed in Chapter 2 can be briefly described by the single-line diagram shown in Figure 5.4. As detailed in Section 2.2.2, the simplified wind farm (SWF) is approximated by an aggregated VSC model in active and reactive control mode to represent the electrical dynamics of the fully rated converter. The AC voltage of the wind farm is maintained by the WFC through the manipulation of the modulation index P_m. The fault-ride-through capability is not considered here for small-signal modelling.

The analytical model of the wind farm side terminal is formed by three sub-systems: the WFC model, the SWF model and the PLL of the SWF, as shown in Figure 5.5, where the state variables of each sub-systems are clearly illustrated. The SWF can be modelled in a similar approach as a GSC model in PQ control mode, but, it is assumed to have an ideal DC link voltage and therefore the DC capacitance of the SWF is not modelled here. PCC2 voltages $v_{d2,q2}$ provided by the WFC model.

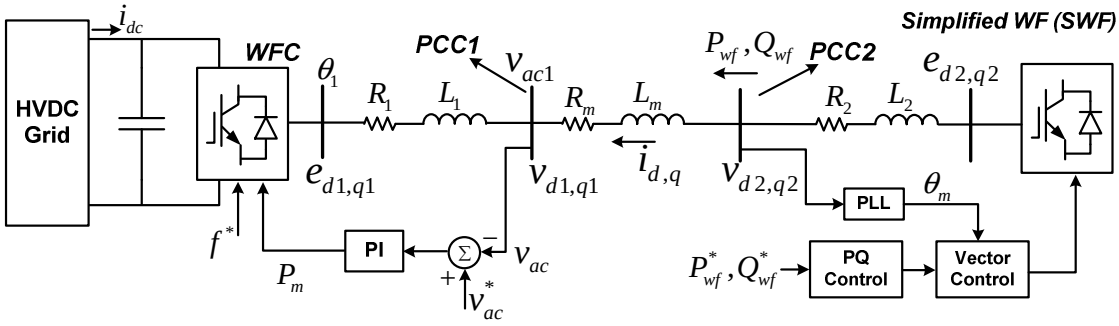


Figure 5.4: Control block diagram of the WFC and the simplified wind farm (SWF) model.

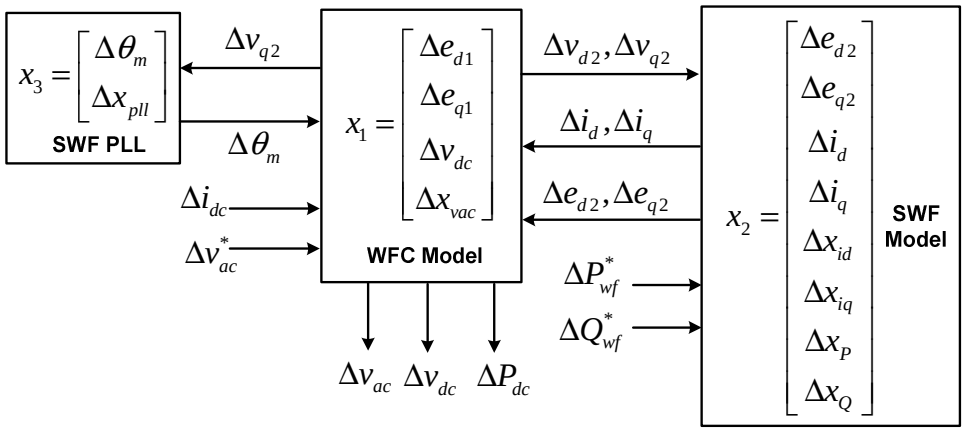


Figure 5.5: State-Space formulation of the wind farm side terminal.

The DC side model of the WFC is identical to that of the GSC. The AC side of the WFC in V_{ac}-f control is modelled as a voltage source with a controllable magnitude. The AC voltage at PCC1 is controlled by manipulating the WFC's modulation index P_m:

$$\Delta P_m = K_p^{vac}\left(\Delta v_{ac}^* - \frac{v_{d1o}}{\sqrt{v_{d1o}^2+v_{q1o}^2}}\Delta v_{d1} - \frac{v_{q1o}}{\sqrt{v_{dco}^2+v_{q1o}^2}}\Delta v_{q1}\right) + \Delta x_{vac} \tag{5.26}$$

$$\Delta x_{vac} = K_i^{vac}\left(\Delta v_{ac}^* - \frac{v_{d1o}}{\sqrt{v_{d1o}^2+v_{q1o}^2}}\Delta v_{d1} - \frac{v_{q1o}}{\sqrt{v_{dco}^2+v_{q1o}^2}}\Delta v_{q1}\right) \tag{5.27}$$

where K_p^{vac}, K_i^{vac} and Δx_{vac} are the proportional gain, integral gain and state variable of the PI AC voltage controller respectively.

The magnitude of the WFC AC terminal voltage in per unit $\hat{e}_1$ can be derived as:

$$\hat{e}_1 = \frac{\sqrt{3}}{2\sqrt{2}V_{ac}^{base}} \cdot P_m \cdot v_{dc} V_{dc}^{base} = k_o P_m v_{dc} \tag{5.28}$$

where $k_o = \sqrt{3}V_{dc}^{base} / (2\sqrt{2}V_{ac}^{base})$.

Equation (5.28) can be further linearised into:

$$\Delta\hat{e}_1 = k_o P_{mo}\Delta v_{dc} + k_o v_{dco}\Delta P_m \tag{5.29}$$

where ΔP_m need to be further substituted by the representation shown in (5.26).

The dq representations of the AC terminal voltage of the WFC are subsequently derived as:

$$\begin{pmatrix} e_{d1} \\ e_{q1} \end{pmatrix} = \begin{pmatrix} \hat{e}_1 \cos(\theta_1 - \theta_m) \\ \hat{e}_1 \sin(\theta_1 - \theta_m) \end{pmatrix} \Rightarrow \begin{pmatrix} \Delta e_{d1} \\ \Delta e_{q1} \end{pmatrix} = \begin{pmatrix} e_{d1o} \\ e_{q1o} \end{pmatrix}\Delta\hat{e}_1 + \begin{pmatrix} e_{q1o} \\ -e_{d1o} \end{pmatrix}\Delta\theta_m + \begin{pmatrix} -e_{q1o} \\ e_{d1o} \end{pmatrix}\Delta\theta_1 \tag{5.30}$$

Where the reference angle provided by the PLL is denoted by $\Delta\theta_m$, and the deviation of the WFC voltage angle $\Delta\theta_1$ is considered to be 0, based on the assumption that the frequency is fixed by the open-loop control. Based on the AC voltages $e_{d2,q2}$ and $e_{d1,q1}$ provided by the two converter models, the PCC2 voltages required by the SWF model are derived as:

$$\begin{pmatrix} \Delta v_{d2} \\ \Delta v_{q2} \end{pmatrix} = \begin{pmatrix} \Delta e_{d2} \\ \Delta e_{q2} \end{pmatrix} \cdot \frac{L_1}{L_t} + \begin{pmatrix} \Delta e_{d1} \\ \Delta e_{q1} \end{pmatrix} \cdot \frac{L_2 + L_m}{L_t} + \begin{pmatrix} \Delta i_d \\ \Delta i_q \end{pmatrix} \cdot \frac{(L_2 + L_m)R_1 - (R_2 + R_m)L_1}{L_t}. \tag{5.31}$$

where $L_t = L_1 + L_2 + L_m$ and L_m is the impedance between the PCC buses of the SWF and the WFC. The complete representation of the analytical model for the overall WFC terminal is detailed in Appendix C.4.

However, this level of modelling complexity might not be necessary in some scenarios. From the perspective of the stability of the overall DC grid, a wind farm side terminal has a similar behaviour as a GSC in active power control mode, provided no significant wind power oscillation occurs. Hence, alternatively, for simplicity, the AC side of the WFC and the SWF can be modelled by a controlled DC power source with a time constant τ_{wf} representing the approximate time frame of the wind turbine converters:

$$P_{wf} = \frac{1}{\tau_{wf} s + 1} P_{wf}^{*} \tag{5.32}$$

5.3 DC Network Modelling

The transient behaviours and stability of a MTDC system are heavily affected by the dynamic characteristic of the DC network. This section presents a generalised analytical model for HVDC circuits based upon a number of cascaded π models.

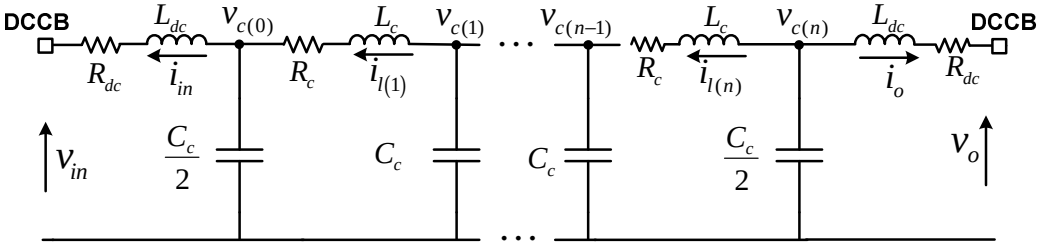


Figure 5.6: Circuit of a multi-π cable model with DC inductors at two ends.

For most of the state-of-the-art HVDC circuit breakers (DCCB), a relatively large DC reactor is required to limit the rate of rise of the fault current [23, 24]. The DC reactors are likely to be located at the ends of each line in the DC switchyard of the converter station. For a DC line modelled by n π sections, as illustrated in Figure 5.6, the dynamics of the DC reactors and the π sections can be represented by the following ($2n+3$) differential equations:

$$\begin{aligned}
&\left.\frac{dv_{c(j)}}{dt}\right|_{j=1,2,\cdots,n-1} = \frac{1}{C_c}\left(i_{l(j+1)} - i_{l(j)}\right) \\
&\frac{dv_{c(0)}}{dt} = \frac{2}{C_c}\left(i_{l(1)} - i_{in}\right), \quad \frac{dv_{c(n)}}{dt} = \frac{2}{C_c}\left(-i_{l(n)} - i_o\right)
\end{aligned} \tag{5.33}$$

$$\begin{aligned}
&\left.\frac{di_{l(j)}}{dt}\right|_{j=1,2,\cdots,n} = \frac{1}{L_c}\left(v_{c(j)} - v_{c(j-1)} - R_c i_{l(j)}\right) \\
&\frac{di_{in}}{dt} = \frac{1}{L_{dc}}\left(v_{c(0)} - v_{in} - R_{dc} i_{in}\right), \quad \frac{di_o}{dt} = \frac{1}{L_{dc}}\left(v_{c(n)} - v_o - R_{dc} i_o\right)
\end{aligned} . \tag{5.34}$$

Subsequently, according to the equations presented above, the ($2n+3$)th-order state-space model of the jth line and the associated DC breaking reactors can be written as:

$$\begin{aligned}
\dot{x}_j^{line} &= A_j^{line} x_j^{line} + B_j^{line} u_j^{line} \\
y_j^{line} &= C_j^{line} x_j^{line}
\end{aligned} \tag{5.35}$$

$$\begin{aligned}
x_j^{line} &= [\underbrace{v_{c0} \quad v_{c2} \quad \cdots \quad v_{c(n)}}_{n+1} \quad \underbrace{i_{in} \quad i_{l1} \quad \cdots \quad i_{l(n)} \quad i_o}_{n+2}]^T \\
y_j^{line} &= [i_{in} \quad i_o]^T, \; u_j^{line} = [v_{in} \quad v_o]^T
\end{aligned} \tag{5.36}$$

where the DC voltages at the two ends are used as input and the DC currents out of the line are produced as output. The detailed parametric representation is provided in Appendix C.1.

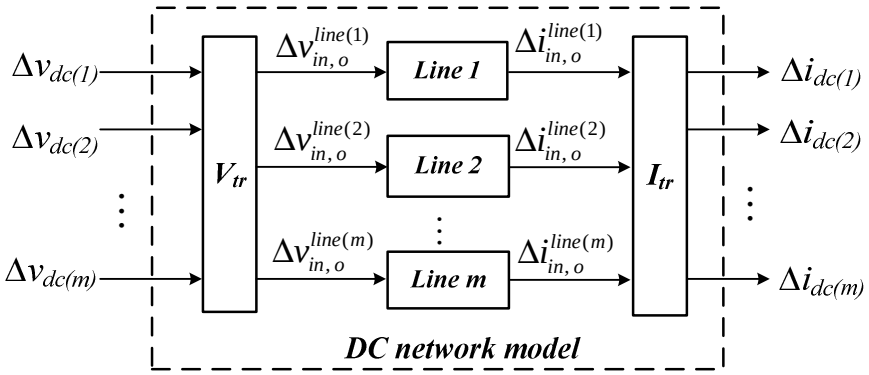


Figure 5.7: DC network model integrating multiple DC line models.

For a DC grid with *n* converter terminals and *m* DC lines, based on the modelling structure illustrated in Figure 5.7, the DC line models in the form of (5.35) can then be interconnected to form the state-space model of the overall HVDC circuit:

$$\begin{bmatrix} \dot{x}_1^{line} \\ \dot{x}_2^{line} \\ \vdots \\ \dot{x}_m^{line} \end{bmatrix} = \begin{bmatrix} A_1^{line} & & & \\ & A_2^{line} & & \\ & & \ddots & \\ & & & A_m^{line} \end{bmatrix} \cdot \begin{bmatrix} x_1^{line} \\ x_2^{line} \\ \vdots \\ x_m^{line} \end{bmatrix} + \begin{bmatrix} B_1^{line} & & & \\ & B_2^{line} & & \\ & & \ddots & \\ & & & B_m^{line} \end{bmatrix} \cdot V_{tr} \begin{bmatrix} v_{dc(1)} \\ v_{dc(2)} \\ \vdots \\ v_{dc(n)} \end{bmatrix}$$
$$\begin{bmatrix} i_{dc(1)} \\ i_{dc(2)} \\ \vdots \\ i_{dc(n)} \end{bmatrix} = I_{Tr} \begin{bmatrix} y_1^{line} \\ y_2^{line} \\ \vdots \\ y_m^{line} \end{bmatrix} = I_{tr} \cdot \begin{bmatrix} C_1^{line} & & & \\ & C_2^{line} & & \\ & & \ddots & \\ & & & C_m^{line} \end{bmatrix} \begin{bmatrix} x_1^{line} \\ x_2^{line} \\ \vdots \\ x_m^{line} \end{bmatrix} \quad (5.37)$$

where $v_{dc(j)}$ denotes the DC terminal voltage of the *j*th converter, and $i_{dc(j)}$ is the DC current flowing into the *j*th converter from the DC grid. The matrix $\mathbf{V}_{tr}$ is used to transform the vector of the VSC terminal DC voltages to the voltage vector suitable for the input of line models, and $\mathbf{I}_{tr}$ is used to obtain the vector of the converter DC current by aggregating the outputs of the respective line models, as shown in (5.38).

$$\begin{bmatrix} v_{dc(1)} & \cdots & v_{dc(n)} \end{bmatrix}^T = V_{tr}^{-1} \cdot \begin{bmatrix} v_{in}^{line(1)} & v_o^{line(1)} & \cdots & v_{in}^{line(m)} & v_o^{line(m)} \end{bmatrix}^T$$
$$\begin{bmatrix} i_{dc(1)} & \cdots & i_{dc(n)} \end{bmatrix}^T = I_{tr} \cdot \begin{bmatrix} i_{in}^{line(1)} & i_o^{line(1)} & \cdots & i_{in}^{line(m)} & i_o^{line(m)} \end{bmatrix}^T \quad (5.38)$$

5.4 Model Interconnection for MTDC Systems

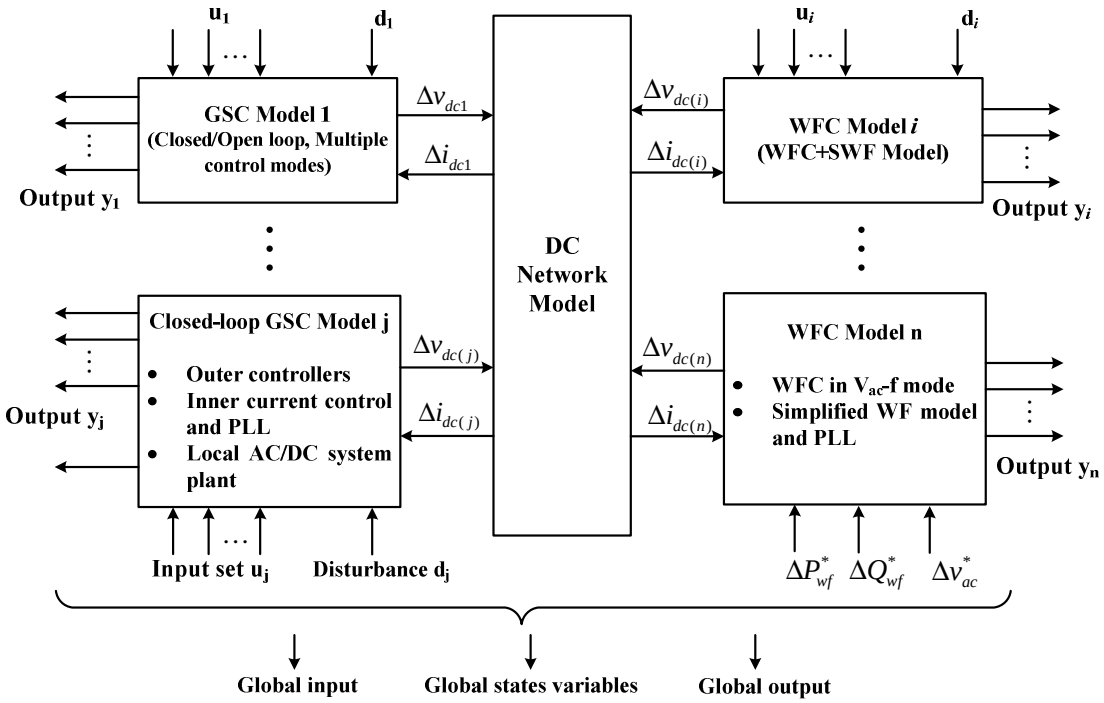


Figure 5.8: Formulation of the state-space model for MTDC systems.

The overall multi-input-multi-output (MIMO) model of a MTDC system that includes the key electromagnetic transients for DC grid studies is formulated by interconnecting the sub-systems including GSC models, the WFC models and the DC network model, based upon the generalised structure shown in Figure 5.8. The converter models are integrated with the DC network models through exchanging DC voltages and currents. Please note that an initial condition solution based upon the overall AC/DC power flow results needs to be performed for parameterisation, which is detailed in Appendix C.5. The independent AC systems could be replaced by a meshed system through interconnecting the AC network model with the converter models based upon the exchange of AC voltages and currents.

Depending on the interest of the studies, the closed-loop or open-loop converter models of different modelling fidelities and control configurations can be incorporated using this model interconnection approach. Various analytical techniques including frequency-response analysis, modal analysis and advanced controller designs are then ready to be applied to the resulting MIMO model.

The generic state-space model for the *j*th VSC terminal can be written in the following form:

$$\begin{aligned}
\dot{x}_j &= A_j x_j + \begin{bmatrix} B_{jG} & B_j \end{bmatrix} \begin{bmatrix} u_{jG} \\ u_j \end{bmatrix} \\
y_{jG} &= C_{jG} x_j \\
y_j &= C_j x_j + \begin{bmatrix} D_{jG} & D_j \end{bmatrix} \begin{bmatrix} u_{jG} \\ u_j \end{bmatrix}, \quad where \;\; u_{jG} = i_{dc(j)}, \; y_{jG} = v_{dc(j)}
\end{aligned} \tag{5.39}$$

where x_j is the vector of state variables of the *j*th converter model, u_j is the local input vector of the *j*th converter, B_{jG} is the column vector of the input matrix corresponding to the DC current input, B_j is input matrix corresponding to the local converter input, C_{jG} is the row vector of the output matrix with respect to the converter DC voltage, y_j contains the output of interest of the *j*th converter, D_{jG} is the vector of the D matrix corresponding to the DC current input, and D_j is the D matrix with D_{jG} excluded. Please note that the disturbances of interest can be incorporated as part of the input vector.

$$\begin{aligned}
\dot{x}_G &= A_G x_G + B_G \Delta \mathbf{v}_{dc} \\
\Delta \mathbf{i}_{dc} &= C_G x_G
\end{aligned} \tag{5.40}$$

For a MTDC system with n converter terminals, by combining the analytical models of all the converter terminals shown in the form of (5.39) and the DC network model shown in (5.40), which is equivalent to (5.37), the overall state-space model for the MTDC system can be derived as:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \vdots \\ \dot{x}_n \\ \dot{x}_G \end{bmatrix} = \begin{bmatrix} A_1 & & & & B_{1G}C_{G1} \\ & A_2 & & & B_{2G}C_{G2} \\ & & \ddots & & \vdots \\ & & & A_n & B_{nG}C_{Gn} \\ B_{G1}C_{1G} & B_{G2}C_{2G} & \cdots & B_{Gn}C_{nG} & A_G \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \\ x_G \end{bmatrix} + \begin{bmatrix} B_1 & & & \\ & B_2 & & \\ & & \ddots & \\ & & & B_n \\ 0 & & \cdots & 0 \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ \vdots \\ u_n \end{bmatrix} \tag{5.41}$$

$$\begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_n \end{bmatrix} = \begin{bmatrix} C_1 & 0 & \cdots & 0 & D_{1G}C_{G1} \\ 0 & C_2 & & 0 & D_{2G}C_{G2} \\ \vdots & & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & C_n & D_{nG}C_{Gn} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \\ x_G \end{bmatrix} + \begin{bmatrix} D_1 & 0 & \cdots & 0 \\ 0 & D_2 & & 0 \\ \vdots & & \ddots & \vdots \\ 0 & & \cdots & D_n \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ \vdots \\ u_n \end{bmatrix} \tag{5.42}$$

where B_{Gj} is the *j*th column of the input matrix B_G of the DC network model, and C_{Gj} is the *j*th row of the output matrix C_G of the DC network model. Please note that the zeros in (5.41) and (5.42) are matrices with appropriate dimensions.

5.5 Modal Analysis

Modal analysis based upon the aforementioned state-space model is performed in this section to assess the dynamic characteristics of MTDC systems, using a four-terminal system as an example. The base-case power flow scenario and control configurations of the candidate system are illustrated in Figure 5.9. All the controllers used for the following sensitivity studies are designed based on the tuning methods discussed in Chapter 2. V-P droop control is employed by GSC2 and GSC3, while constant power control is applied to GSC1.

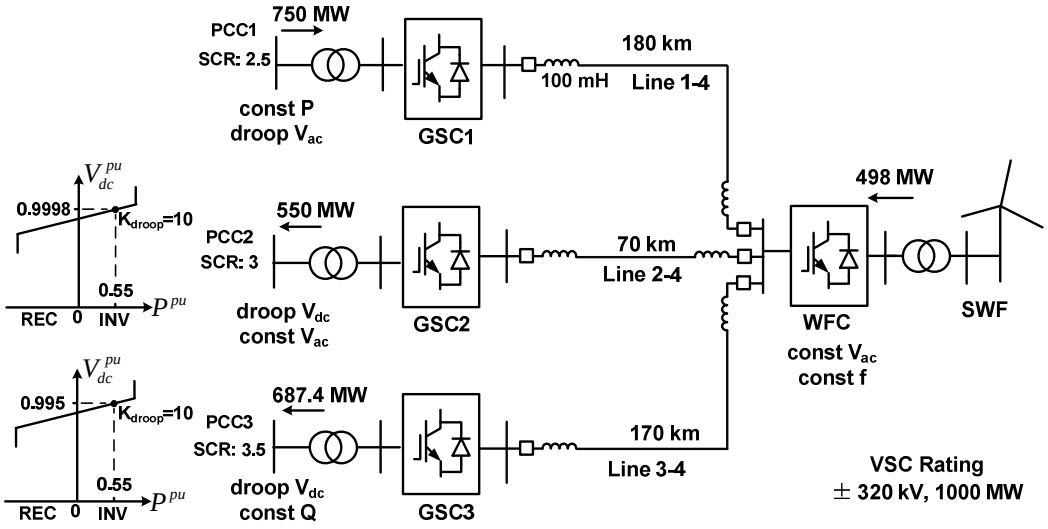


Figure 5.9: The nominal power flow and control modes of the four-terminal test system.

The dynamic responses of the vector of state variables $\Delta\mathbf{x}(t)$ and the vector of system modes $\Delta\mathbf{z}(t)$ can be related to each other as [151]:

$$\Delta\mathbf{x}(t) = \begin{bmatrix}\phi_1 & \phi_2 & \cdots & \phi_n\end{bmatrix}\Delta\mathbf{z}(t), \quad \Delta\mathbf{z}(t) = \begin{bmatrix}\psi_1^T & \psi_2^T & \cdots & \psi_n^T\end{bmatrix}^T \Delta\mathbf{x}(t) \tag{5.43}$$

where n is the number of modes, and the right eigenvector ϕ_i and the left eigenvector ψ_i corresponding to the ith eigenvalue are termed as:

$$\mathbf{A}\phi_i = \lambda_i\phi_i, \quad \psi_i\mathbf{A} = \lambda_i\psi_i. \tag{5.44}$$

To be more specific to time domain, the free motion response of the states can be represented by the eigenvalues as [151]:

$$\Delta\mathbf{x}(t) = \sum_{i=1}^{n} \phi_i \left(\psi_i \Delta\mathbf{x}(0)\right) e^{\lambda_i t} \tag{5.45}$$

where λ_i is the ith eigenvalue and $\Delta\mathbf{x}(0)$ is the initial condition vector of the states.

The participation factor matrix, which is defined as (5.46), represents the combination of the right and left eigenvectors. The element p_{ji} effectively reflects the relative participation of the jth state in the ith mode [151, 152].

$$\begin{aligned}\mathbf{P} &= [\mathbf{p}_1 \quad \mathbf{p}_2 \quad \cdots \quad \mathbf{p}_n] \\ \mathbf{p}_i &= [p_{1i} \quad p_{2i} \quad \cdots \quad p_{ni}]^T = [\phi_{1i}\psi_{i1} \quad \phi_{2i}\psi_{i2} \quad \cdots \quad \phi_{ni}\psi_{in}]^T\end{aligned} \tag{5.46}$$

The state-space model can be re-written using the modes instead of the state variables in the following form to allow the modes to be directly linked to the input and output of the system:

$$\begin{aligned}\dot{\mathbf{z}} &= \Lambda\mathbf{z} + \Phi^{-1}\mathbf{B}\Delta\mathbf{u} \\ \Delta\mathbf{y} &= \mathbf{C}\Phi\mathbf{z} + \mathbf{D}\Delta\mathbf{u}\end{aligned} \tag{5.47}$$

where $\boldsymbol{\Lambda}$ is the diagonal matrix comprised of eigenvalues, and the matrices $\boldsymbol{\Phi^{-1}B}$ and $\boldsymbol{C\Phi}$ are termed as controllability matrix and observability matrix respectively [151].

Participation factor analysis has been implemented on the four-terminal model to identify the associations between the state variables and the critical eigenvalues, with the selected results shown in Figure 5.10 and Table 5.1. More detailed results are provided in the Appendix C.7. As depicted in Figure 5.10 (a), the eigenvalues of the MTDC system can be mainly categorised into fast current loop modes, outer converter control modes and the DC circuit modes.

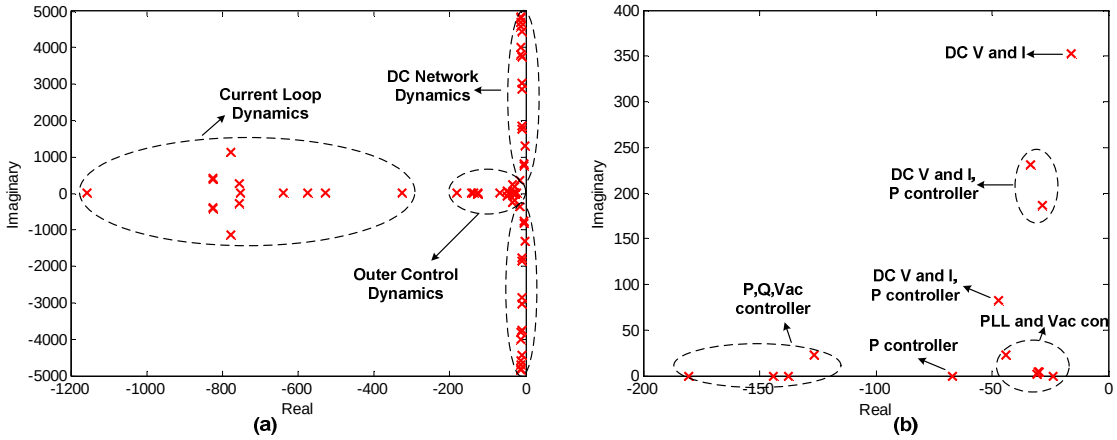


Figure 5.10: Eigenvalues and their dominant state variables.

Table 5.1: Selected eigenvalues and the corresponding dominant participant variables.

Eigenvalues	ζ	Freq (Hz)	Participant variables	Participant factors
-15.97±j353.05	0.05	56.19	v_{dc4}, v_{dc2}, i_{in} $Line_{2\text{-}4}$, i_o $Line_{2\text{-}4}$	1.00, 0.467, 0.340, 0.315
-23.68	1.00		x_{pll1}, θ_{m1}, x_{vac1}, i_{q1}	1.00, 0.531, 0.047, 0.018
-28.55±j186.77	0.15	29.73	v_{dc1}, v_{dc3}, x_{P3}, i_o $Line_{1\text{-}4}$	1.00, 0.828, 0.519, 0.423
-30.18±j3.82	0.99	0.61	x_{pll2}, θ_{m2}, x_{pll3}, θ_{m3}	1.00, 0.982, 0.134, 0.132
-33.60±j231.1	0.14	36.78	v_{dc2}, v_{dc3}, x_{P2}, x_{P3}	1.00, 0.736, 0.501, 0.339
-44.01±j22.47	0.89	3.58	θ_{m1}, x_{vac1}, x_{pll1}, x_{P1}	1.00, 0.440, 0.426, 0.138
-47.159±j82.173	0.50	13.08	x_{P2}, v_{dc1}, x_{P3}, v_{dc4}	1.00, 0.870, 0.850, 0.560
-67.27	1.00		x_{P2}, x_{P3}, θ_{m3}, x_{Q3}	1.00, 0.998, 0.312, 0.272
-126.5±j22.72	0.98	3.62	x_{P4}, x_{vac4}, x_{Q4}, θ_{m4}	1.00, 0.859, 0.745, 0.096
-137.76	1.00		x_{Q3}, i_{q3}, θ_{m3}, x_{iq3}	1.00, 0.082, 0.080, 0.057
-144.03	1.00		x_{P1}, x_{vac1}, i_{d1}, θ_{m1}	1.00, 0.205, 0.150, 0.064

The participation factors suggest that, the high-frequency modes which have significantly lower damping than the rest of modes are determined by the intrinsic characteristics of the DC lines and usually out of the frequency range of the DC voltage control. The analysis of the observation matrix in (5.47) and the linear combination of these high-frequency modes in (5.45) demonstrate that these poorly damped modes generally have a insignificant impact on the low-frequency response of the outputs and states of interest. Additionally, the frequencies of the DC circuit modes will decrease if a reduced number of π sections are used for the cable modelling.

The low-frequency dominant modes, which are depicted in the enlarged view in Figure 5.10 (b), are predominantly affected by the state variables associated with the outer control loops. The modes associated with the converter DC voltages and currents generally have lower time constants and higher oscillating frequencies than the modes associated with the control loops for active and reactive power, due to their interactions with the relatively poorly damped DC network modes. Unlike the scenario for a typical AC system where most of the eigenvalues are determined by individual generator systems, the dominant modes for the MTDC system are usually sensitive to the state variables of multiple converters. Due to the fast-response nature of the VSC control, the interactions between the states of different converters in the MTDC system are much stronger than those of different generators in the conventional AC system.

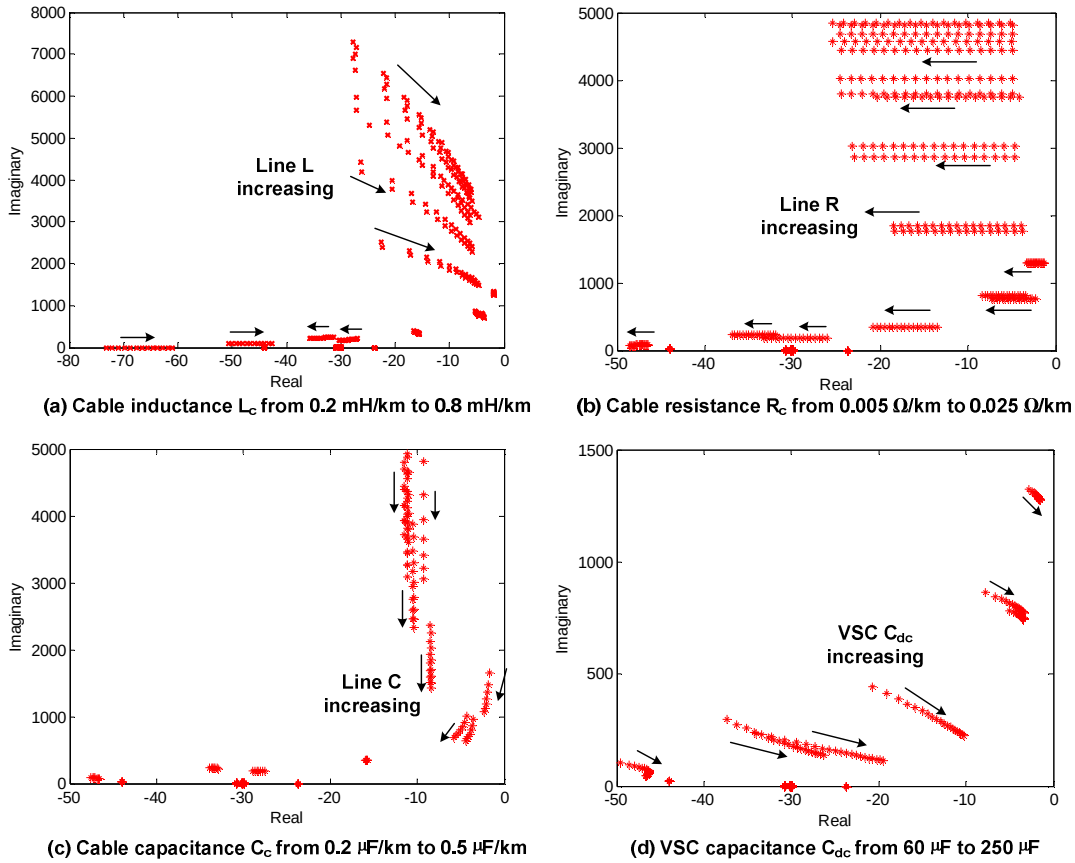


Figure 5.11: Trajectories of eigenvalues as a function of different DC system parameters (nominal parameters: L_c=0.466 mH/km, R_c=0.0113 Ω/km, C_c=0.28 μF/km, C_{dc}=98 μF).

Based on the base-case scenario shown in Figure 5.9, a series of sensitivity studies have been performed by evaluating the trajectories of the modes of interest with respect to the variations of different DC system parameters, with the results illustrated in Figure 5.11.The increase of the cable inductance reduces the damping as well as the oscillating frequency of the poles associated with the DC network. This implies that the MTDC system could be exposed to high-frequency instability if excessive DC inductances are inserted into network. Increasing the cable resistance clearly shows a stabilising impact on the overall system, as most of the modes, particularly the DC network modes, migrate horizontally towards the left-half plane. The effect of the resistance on the oscillating frequencies of the poles is however negligible. Increasing the cable capacitance has a positive impact on the damping of the high-frequency modes, whereas it has a very limited impact on the converter control modes. The converter equivalent capacitance C_{dc} has a significant impact on the low-frequency critical modes, as indicated in Figure 5.11 (d). A system with larger converter capacitors is expected to have slower response speed and enhanced stability.

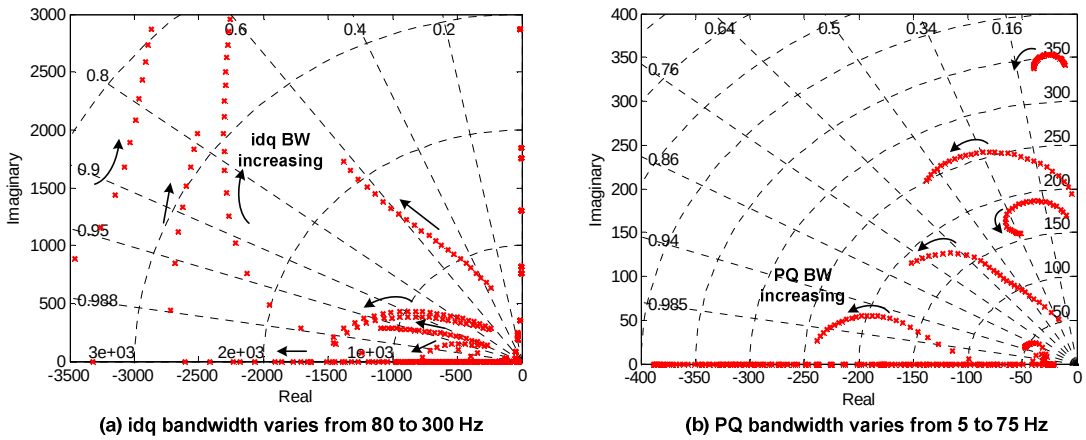


Figure 5.12: Trajectories of eigenvalues corresponding to the variations of controller settings.

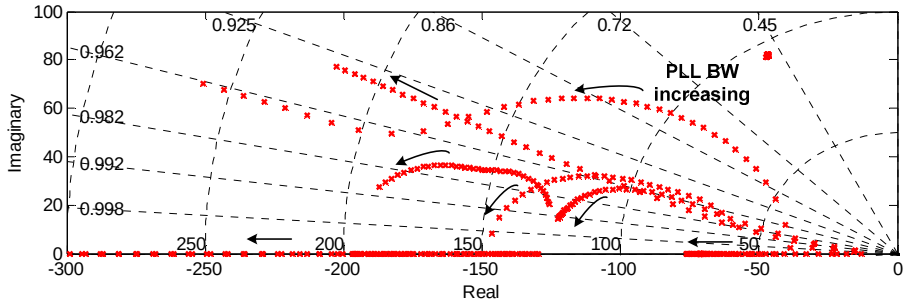


Figure 5.13: Trajectories of eigenvalues as the PLL bandwidth varies from 5 to 100 Hz.

Sensitivity analyses regarding the bandwidths of the current control, the active and reactive power control and the PLL have also been conducted, with the trajectories of the modes of interest shown in Figure 5.12(a), Figure 5.12(b) and Figure 5.13 respectively.

The increase of the current control bandwidth affects most of the slow dominant modes in an insignificant manner, however, this shifts the fast current modes further to the LHP and also reduces the damping of the these modes. The critical modes that determine the MTDC transient behaviour are greatly affected by the real and reactive power controllers. As shown in Figure 5.12(b), using a larger gain for the power controllers may improve the dynamic performance of this droop-controlled system. However, the high-gain power control may result in degraded stability of the local VSC system. It should be noted that the power controller parameterisation could have a dissimilar impact for a scenario with a different droop configuration or a different power flow condition. The PLL controller setting mainly influences the low-frequency modes, which are typically well damped and also affected by the power and AC voltage control system dynamics. The bandwidth of the PLL however has a limited impact on the DC voltage dynamics when the VSC is connected to a relatively strong AC system.

Table 5.2: Four power flow operating points (OP) for the four-terminal system.

	GSC1	GSC2	GSC3	WFC
Power OP1 (pu)	-0.750	0.550	0.687	-0.498
Power OP2 (pu)	-0.300	0.250	0.248	-0.200
Power OP3 (pu)	0.850	-0.900	0.974	-0.943
Power OP4 (pu)	0.990	-0.500	-0.407	-0.100

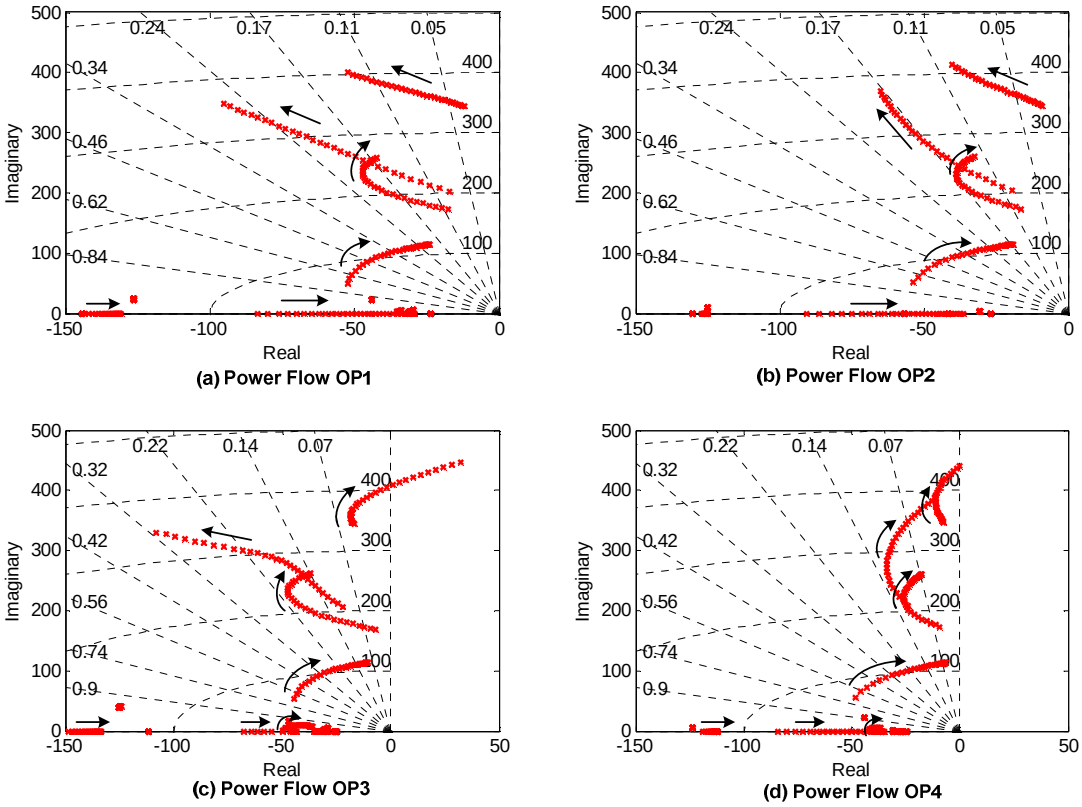


Figure 5.14: Trajectories of the dominant modes as the droop gain of GSC2 and GSC3 varies from 5 to 36 (GSC1: constant power control, GSC2 and GSC3: V-P droop control).

The effect of droop gain on the system stability can be observed from the trajectories of the dominant modes shown in Figure 5.14. Sensitivity studies were carried out with respect to the four power flow operating points (OPs) shown in Table 5.2. V-P droop controllers with identical gains are applied to GSC2 and GSC3 while constant power control is used by GSC1. The variation of the droop has a similar impact on the modes for the scenarios OP1 and OP2, within which the directions of power transfer of the converters are identical. The modes with relatively high frequencies migrate towards the left-half plane (LHP), while the low-frequency modes migrate towards the right-half plane (RHP) as the droop gain increases for OP1 and OP2. As one or both of the converters in droop control mode change to rectifier operation in OP3 and OP4, the increase of the droop gain may initially enhance the damping of the high-frequency modes, however, a further increment of the droop gain could significantly deteriorate the

damping and even cause instability. This phenomenon clearly shows that the impact of droop gains on the MTDC stability depends on the power flow of the system. This serious robustness issue will be analysed in further detail in the next two chapters.

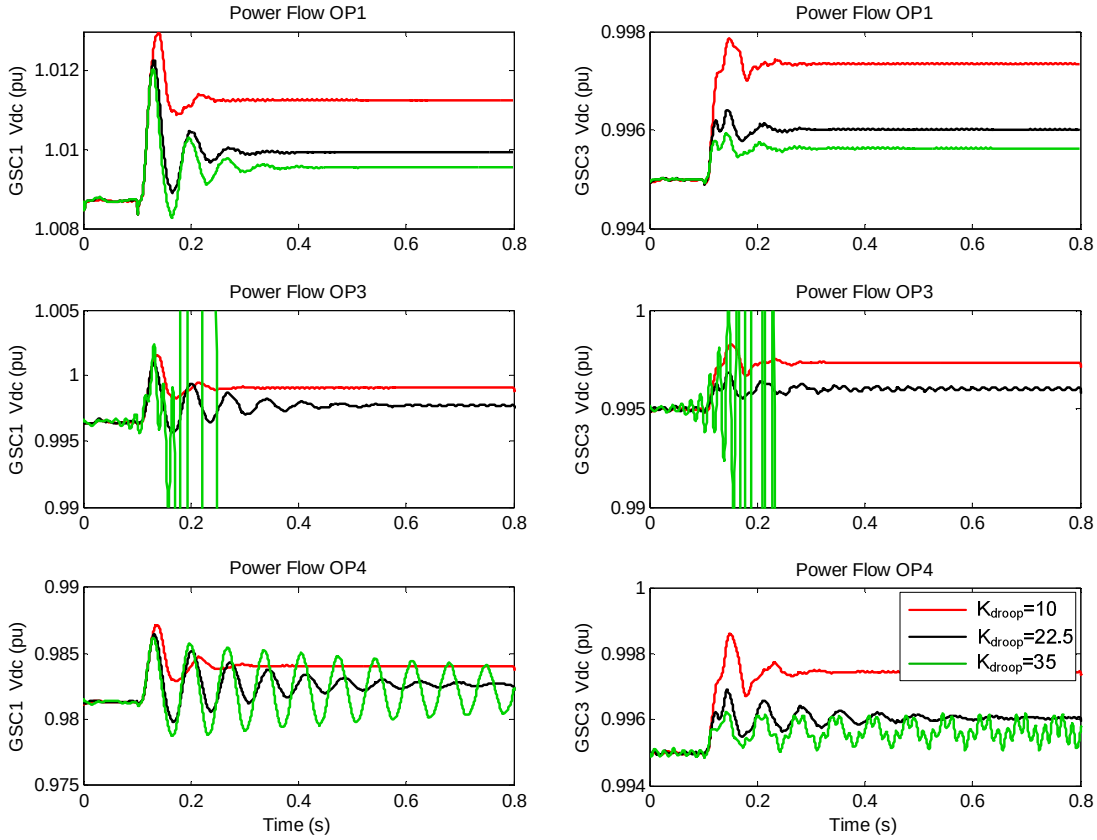


Figure 5.15: DC voltage responses to 100 MW change of wind farm power under three OP scenarios.

The modal analysis results in Figure 5.14 are verified by the time domain simulations in Figure 5.15, where the DC voltage responses of GSC1 and GSC3 to a 100 MW increase of wind farm power at 0.1 s are shown for the scenarios OP1, OP3 and OP4. In OP1, increasing the droop gain reduces the steady-state error, while slightly degrades the damping of the low-frequency modes. In the other two scenarios, applying the gain of 22.5 results in poor damping, and using the large gain of 35 leads to the system instability in OP3 and causes marginal instability in OP4. Practically, an appropriate droop setting should be carefully assessed across all possible power flow scenarios.

5.6 Chapter Summary

This chapter presents a systematic procedure for the mathematical modelling of a VSC-MTDC system, incorporating the key dynamics of the VSC stations and DC network.

The overall analytical MTDC model is formulated based upon interconnections between the following linearised sub-systems: the GSC model, the WFC model and the DC network model. Each of these sub-systems is developed by combining the state-space models of smaller scale, depending on the control scenarios and the AC/DC plant. This modelling technique gives a good degree of flexibility with respect to the variations of network topology and control configuration, and can be conveniently extended to larger MTDC systems.

Participation factor analysis has been applied to identify the state variables that strongly correlate to the eigenvalues of interest, utilising a four-terminal candidate model. Sensitivity studies based upon modal analysis have been conducted to investigate the impact of the DC system parameters, the current and power controller design, the droop gains and the DC power flow on the MTDC stability and dynamics.

Modal analysis is advantageous in terms of addressing the small-signal stability issues and identifying the key factors that influence the dynamics of a large system. This analytic approach however has the following drawbacks with MTDC applications:

- It is not very effective in examining the transient performance of the MTDC system. For example, the bandwidth and overall damping of the control systems of interest cannot be directly observed from the modal results.
- The impact of the zeros, which could impose serious limitations of the control design, are usually ignored in modal analysis.
- It is less effective for a MTDC system than for a conventional AC system, mainly due to the fact that the coupling between the states in the DC system is much stronger than those in the AC system. It is difficult to find the equivalent “inter-area mode” of a DC grid system.
- It is less effective in terms of assessing the stability margins and evaluating the dynamic responses (including tracking and disturbance rejection performances) than frequency-response methods.

The modelling methodology presented here forms the basis of the analysis developed in the next two chapters.

Chapter 6 Stability Analysis of DC Voltage Control of VSC-HVDC

This chapter aims to identify and analyse key stability issues with respect to the control of DC voltage in VSC-HVDC systems. DC voltage controllers including constant DC voltage control, V-P droop control and V-I droop control need to react sufficiently fast to cope with the DC current/power disturbances imposing on the VSC-HVDC system, by manipulating the active current between the converter and the AC system. The closed-loop DC voltage control is a complex system in which both the detailed dynamics of the AC and DC sides ought to be considered.

Previous literature regarding droop control has been focused on the steady-state and dynamic operation of the droop control from the MTDC perspective. Typically, interactions between the droop control and the other converter controllers have been neglected. For most of the previous analytical work for DC voltage control, only the dynamics of the converter capacitor are considered, while the impact of the DC line dynamics has been ignored or assumed to be cancelled by feedforward measurement [84, 85, 87]. Furthermore, the constraints imposed by the AC system strength and converter operating point on the DC voltage stability have not been investigated in most of the previous studies. Some good work has however been presented in [34, 125, 134, 137] regarding the steady-state and dynamic limitations imposed by weak AC systems on active and reactive power control for VSC-HVDC.

DC voltage is controlled based on local measurement instead of wide-area measurement. In this chapter frequency-response analysis based upon detailed converter control models with appropriately modelled DC disturbances is employed to deliver an intuitive understanding into the system stability and performance. Moreover, this generalised approach can be used to investigate design limitations of the droop controller and provide a solid foundation for a more complex multivariable analysis.

This chapter is organised as follows. Section 6.1 addresses the stability limitations imposed on the DC voltage stability by weak AC systems, large DC inductance and the interactions with other controllers. A novel compensator-based droop controller is proposed in Section 6.2 to improve the stability margins as well as the transient performance of V-P droop control. The stability of V-I droop is briefly evaluated in

Section 6.3. The implications of using a feedforward of DC power for DC voltage control are investigated in Section 6.4.

6.1 Key Dynamic Limitations for DC Voltage Control

Regarding V-P droop control, this section focuses on revealing and analysing the key limitations imposed by weak AC systems, variation of converter operating point, and interactions with other control loops. Frequency response is used here to provide insightful information on the associated performance and stability issues.

6.1.1 Formulation of the Plant Model

Three types of DC link models, as shown in Figure 6.1, are analysed. The type 1 model is based on the local terminal dynamics, where the DC current disturbance i_{dc} coming from the DC grid directly affects the converter DC terminal voltage.

The type 2 model is effectively a basic point-to-point model, with simplified modelling of DC line impedance and a DC power disturbance P_2, to give a degree of perspective on the impact of DC resonance on the controllability of DC voltage. The current i_{dc} in the type 2 model however does not represent the DC current into the converter, since the converter capacitance is lumped together with the cable capacitance. Therefore, for studies of the control systems involving the use of the converter DC current, such as V-I droop control, the type 3 model is employed instead. The DC reactor dynamics are also included in the type 3 model. The converter capacitances used in the type 1 and type 3 models are purely based on the AVM, while the capacitance used in the type 2 model is also dependent on the DC line parameters.

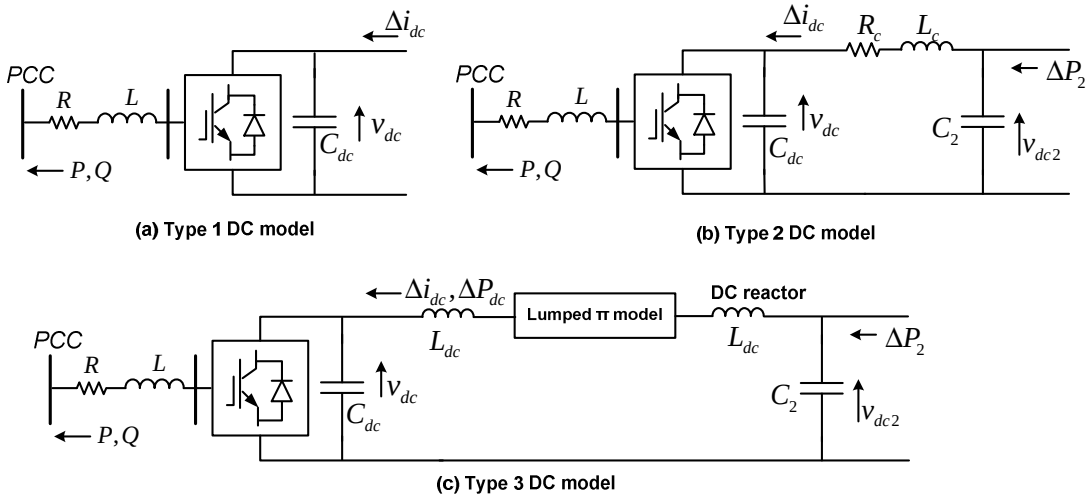


Figure 6.1: The three types models for DC side.

Based on the differential equations described in Chapter 5, the small-signal models including dynamics of the current controller, the PLL and the AC/DC systems can be derived for the type 1, type 2 and type 3 models. The active and reactive power/AC voltage controllers are also connected with such models. The formulation of the open-loop and closed-loop models regarding V-P droop control is shown in Figure 6.2.

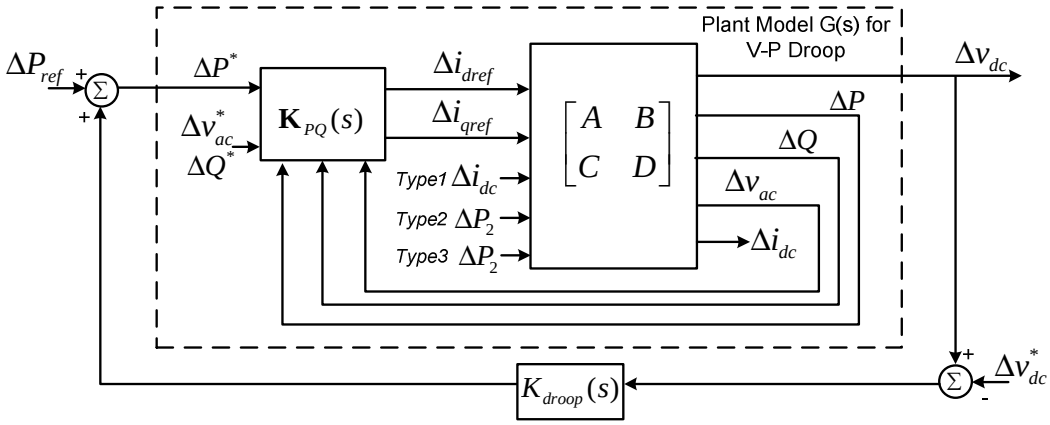


Figure 6.2: Formulation of the plant model for V-P droop control.

The plant transfer function $G(s)$, the loop transfer function $L(s)$ and the sensitivity transfer function $S(s)$ with respect to the V-P droop control, as shown in (6.1), will be frequently used in Sections 6.1 and 6.2.

$$G(s)=\frac{P^*(s)}{v_{dc}(s)},\ L(s)=K_{droop}(s)G(s),\ S(s)=\frac{1}{1+L(s)}. \tag{6.1}$$

6.1.2 Constraints Imposed by Weak AC System

When a VSC-HVDC system is connected to a relatively weak AC network, the voltage and frequency of the local AC system are likely to be largely affected by the variation of the active and reactive powers injected by the VSC. The AC frequency variation is very slow and beyond the scope of EMT-level converter transients. However, the AC voltage can change sufficiently fast and interact with the dynamics of converter control.

With the active and reactive power controllers excluded, frequency responses of the open-loop transfer functions $v_{dc}(s)/i_{dref}(s)$ and $v_{dc}(s)/i_{qref}(s)$ are shown in Figure 6.3. As the SCR decreases, the gain between DC voltage and the d-axis current decreases while the correlation between DC voltage and the q-axis current increases dramatically. This indicates that, for weak AC systems, it can be very difficult to maintain the DC voltage by manipulating the active current, and that the DC voltage is likely to be affected significantly by the reactive power control of the VSC. This strong coupling effect

between v_{dc} (or P) and the q-axis current is highly undesirable. Furthermore, the low-gain characteristic of $v_{dc}(s)/i_{dref}(s)$ shows that, for very weak AC systems, i_d current may have to be utilised excessively by DC voltage control and this can cause severe saturation of converter current.

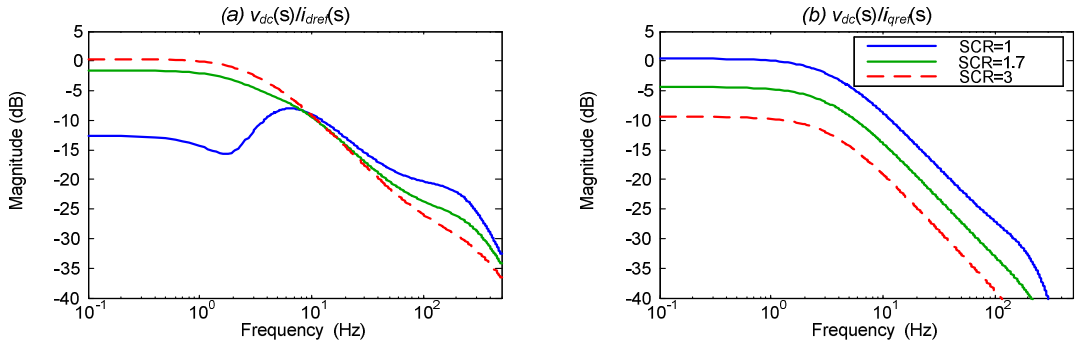


Figure 6.3: Bode plots of the open-loop transfer functions $v_{dc}(s)/i_{dref}(s)$ and $v_{dc}(s)/i_{qref}(s)$ (P_o=0.9 pu INV, type 1 model).

With respect to the weak AC system connection, the impact of the power operating point on the frequency responses of $v_{dc}(s)/i_{dref}(s)$ and $v_{dc}(s)/i_{qref}(s)$ is demonstrated in Figure 6.4. The results indicate that increasing the power transfer of the VSC reduces the low-frequency gain of $v_{dc}(s)/i_{dref}(s)$, increases the interactions between the q-axis current and DC voltage, and therefore deteriorates the controllability of the DC voltage.

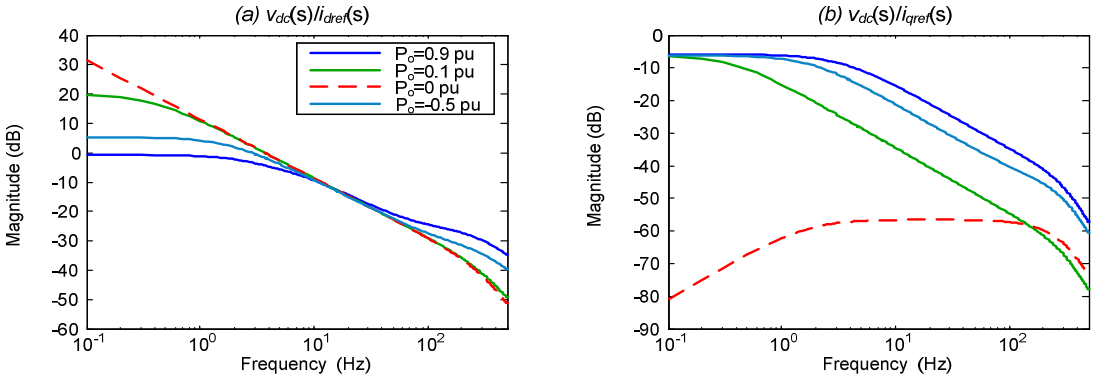


Figure 6.4: Frequency responses of the open-loop transfer functions $v_{dc}(s)/i_{dref}(s)$ and $v_{dc}(s)/i_{qref}(s)$ (SCR=2, type 1 model).

The main reason causing the limitations shown in Figure 6.3 and Figure 6.4 is that the PCC bus voltage is not sufficiently robust with respect to the variation of the active and reactive power flows of the VSC, due to the large impedance between the PCC bus and the AC source voltage. Assuming that the steady-state q-axis PCC voltage is controlled to be 0 pu, by setting the differential terms to 0 in equation (5.2) and replacing Δv_{sd} and Δv_{sq} using equation (5.6), the variation of the d-axis voltage can be solved as:

$$\Delta v_d = (R_s + \frac{v_{sqo}}{v_{sdo}}\omega L_s)\Delta i_d + (\frac{v_{sqo}}{v_{sdo}}R_s - \omega L_s)\Delta i_q \tag{6.2}$$

where

$$\frac{v_{sqo}}{v_{sdo}} = \frac{-\omega L_s i_{do} - R_s i_{qo}}{v_{do} + \omega L_s i_{qo} - R_s i_{do}}. \tag{6.3}$$

Assuming that the steady-state q-axis PCC voltage is controlled to be 0 pu, the steady-state variation of the DC power can be approximated as:

$$\Delta P \approx i_{do}\Delta v_d + v_{do}\Delta i_d = (R_s i_{do} + \frac{v_{sqo}}{v_{sdo}}\omega L_s i_{do} + v_{do})\Delta i_d + (\frac{v_{sqo}}{v_{sdo}}R_s - \omega L_s) i_{do}\Delta i_q. \tag{6.4}$$

Assuming $\omega L_s \gg R_s$, this equation above can be further simplified as:

$$\Delta P \approx (\frac{v_{sqo}}{v_{sdo}}\omega L_s i_{do} + v_{do})\Delta i_d - \omega L_s i_{do}\Delta i_q \approx (\frac{\omega^2 L_s^2 i_{do}^2}{v_{do}} + v_{do})\Delta i_d - \omega L_s i_{do}\Delta i_q. \tag{6.5}$$

This equation conceptually shows that larger AC network impedance (ωL_s) and higher power transfer (larger i_{do}) imply a weaker $\Delta P/\Delta i_d$ relation and a stronger $\Delta P/\Delta i_q$ relation. This demonstrates a fundamental flaw of applying conventional active power control or DC voltage control based on dq current control for very weak AC system integration, namely a potentially substantial interaction between active and reactive power control.

6.1.3 Constraints Imposed by Power Operating Point (OP)

The plant model of DC voltage control is sensitive to the power operating point (OP) of the VSC. This section analyses two severe constraints that are imposed by the combining effects of converter power OP and AC system strength and DC circuit resonance.

From the AC system perspective, according to the active power control model presented in Chapter 4, a right-half plane (RHP) zero $-v_{do}/(L_s i_{do})$ exists in the loop transfer function of active power control for a converter in rectifier operation ($P_o<0$, $i_{do}<0$). Since, physically, the change of DC voltage relies on the variation of active power, this RHP zero remains in the DC voltage plant model, in spite of the v_{dc} control strategy. The RHP zero will migrate towards the origin as the SCR decreases and the rectifying power increases, and this will imply high-gain instability and restricted bandwidth.

From the DC system perspective, a converter in constant power control can be viewed as a DC power source. The DC current absorbed by this power source can be represented as:

$$i_{dc} = \frac{P_{dc}}{v_{dc}} \quad \Rightarrow \quad \Delta i_{dc} = \frac{\Delta P}{v_{dco}} - \frac{P_{dco}}{v_{dco}^2} \Delta v_{dc} \,. \tag{6.6}$$

Accordingly, the nonlinear and linearised forms of the power source in a simplified DC link model can be depicted as shown in Figure 6.5. The converter in constant power control behaves like a negative admittance in parallel with a DC current source for inverter operation [84, 153-155]. Increasing the inverting power enlarges the negative admittance and deteriorates the DC link controllability. For a point-to-point system, this phenomenon implies that it is likely more stable to use the inverter, rather than the rectifier, for DC voltage regulation.

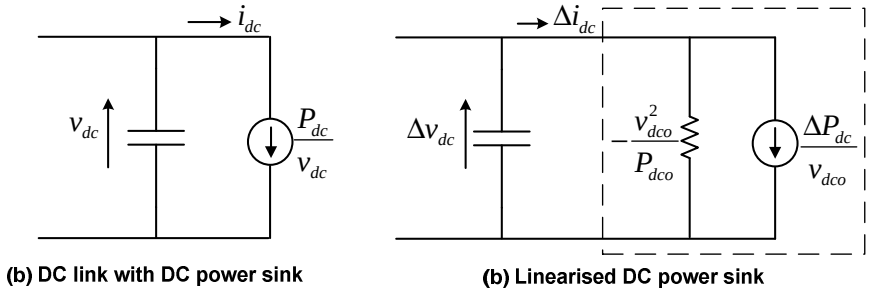


Figure 6.5: Simplified DC link model with DC power sink.

The closed-loop DC voltage droop control for the type 2 model can be approximated using the diagram shown in Figure 6.6. The closed-loop reference tracking transfer function for active power control, based on the derivation in [137], is denoted as $T_p(s)$. The disturbance transfer function $G_d(s)$ is used to represent the open-loop dynamics between P_2 and v_{dc}, and $G_{mv}(s)$ represents the voltage measurement filter.

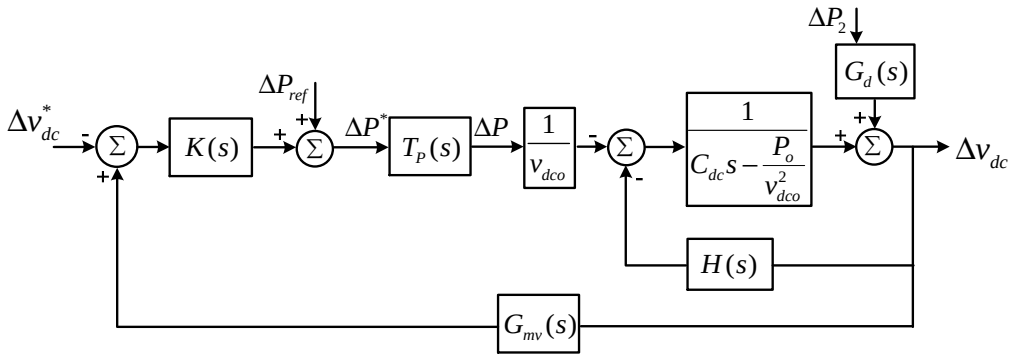


Figure 6.6: Linearised DC voltage control loop (type 2 model).

The key dynamics of the line inductance and the equivalent capacitance of the power disturbance terminal are captured in the following transfer function:

$$H(s)=\frac{\frac{1}{L_c}s+\frac{P_{2o}}{L_cC_2v_{2o}^2}}{s^2+(\frac{R_c}{L_c}+\frac{P_{20}}{C_2v_{20}^2})s+\frac{1}{L_cC_2}(\frac{R_cP_{2o}}{v_{2o}^2}+1)} \tag{6.7}$$

It is observed from (6.7) that a large amount of rectifying power transfer could result in a pair of RHP poles of *H(s)*, when the following equation is satisfied:

$$P_{20}<-\frac{R_c}{L_c}C_2v_{2o}^2\,. \tag{6.8}$$

The RHP poles in $H(s)$ will be reflected in the DC voltage loop transfer function as RHP zeros. Unlike the previous RHP zero, which is determined by the dynamics of the VSC AC side, this pair of RHP zeros result from the negative admittance effect. This is the second constraint imposed by the power operating point on the DC voltage controllability. It should be noted that the type 1 model does not contain the information of this RHP-zero pair due to the oversimplified model of the DC side.

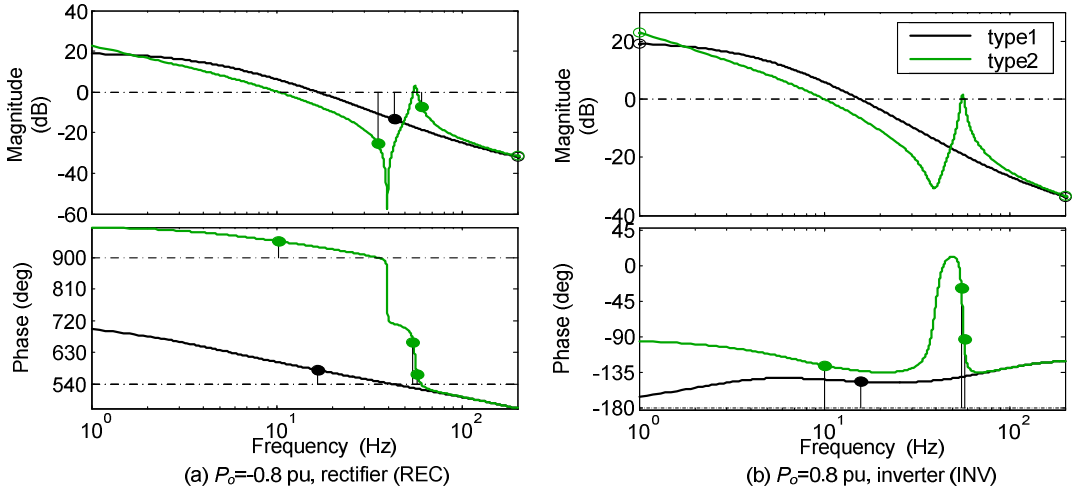


Figure 6.7: Frequency responses of the loop transfer functions L(s) regarding V-P droop control, with P_o=-0.8 pu REC in (a) and P_o=0.8 pu INV in (b) (K_{droop}=7.5, SCR=2.5).

Table 6.1: Frequency domain indicators as converter power varies.

	Type 1		*Type 2*	
P_o *(pu)*	-0.8 REC	0.8 INV	-0.8 REC	0.8 INV
ω_B *(Hz)*	13.6	11.7	8.7	8.3
GM (dB)	11.0	84.2	4.6	84.2
PM (deg)	32.6	32.7	15.3	50.6
$\|\|S\|\|_\infty$ *(dB|)*	6.97	5.44	13.4	2.72

Regarding two operating points of active power transfer, the frequency responses of the loop transfer functions $L(s)$ for DC voltage control are presented in Figure 6.7, for both the type 1 and type 2 model. A droop gain K_{droop} of 7.5 is adopted for both scenarios. The quantified frequency-response measurements, including closed-loop bandwidth ω_B, gain margin (GM), phase margin (PM) and peak of sensitivity transfer function $\|S\|_\infty$, are shown in Table 6.1.

When the type 1 model is applied to the two OP scenarios, due to the RHP zero caused by the converter AC side dynamics, the gain margin for the rectifier case is much lower than that for the inverter case. The differences between the two OP scenarios, with respect to the sensitivity peak $\|S\|_\infty$ and GM, are expected to rise significantly as the SCR decreases.

The utilisation of the type 2 model improves the stability margins of the inverter scenario however deteriorates both the stability and performance of the rectifier scenario. The constraints caused by the RHP zeros lead to undesired levels of the GM, PM and $\|S\|_\infty$ for the rectifier operation. The DC circuit dynamics together with the negative admittance effect result in a resonance peak of the loop transfer function. In order to reduce the implications caused by such peaks, the droop gain has to be reduced or a more advance controller structure needs to be used to shape the loop transfer function. It should be noted that the limitations imposed by low-SCR systems and converter power OP exist, regardless of the DC voltage controller design.

6.1.4 Constraints Imposed by Other Control Loops

The active power control loop effectively acts as part of the plant model for V-P droop control. The impact of the active power loop bandwidth ω_B on the frequency response of the sensitivity transfer function is shown in Figure 6.8 and Figure 6.9, with the results generated by the type 1 model and type 2 model respectively.

Normally, for a system without RHP zeros, a faster actuator improves the transient performance of the closed-loop system [1]. The result of the inverter operation suggests that an increased power loop bandwidth reduces the sensitivity peak and thus enhances both the robustness and performance of the droop DC voltage control.

However, for rectifier operations, increasing power loop bandwidth results in a larger loop gain, and could significantly reduce the stability margins of the droop control, due

to the high-gain instability effect discussed in Section 6.1.3. The difference between the results for the type 1 and type 2 models is mainly caused by the pair of RHP zeros resulting from the DC side model. A trade-off has to be made between the performance of inverter operations and the stability of rectifier operations in terms of the selection of the power loop bandwidth.

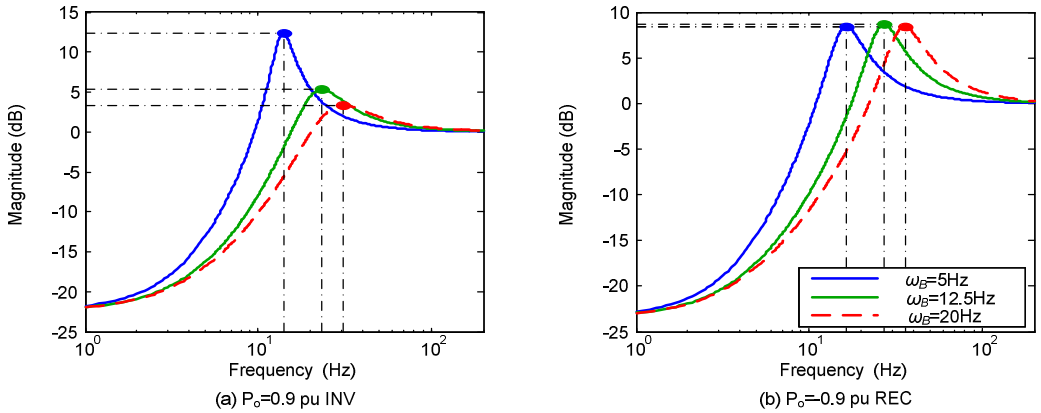


Figure 6.8: Frequency response of the sensitivity transfer function |S(*jω*)| (type 1 model, SCR=2.5, K_{droop}=12.5).

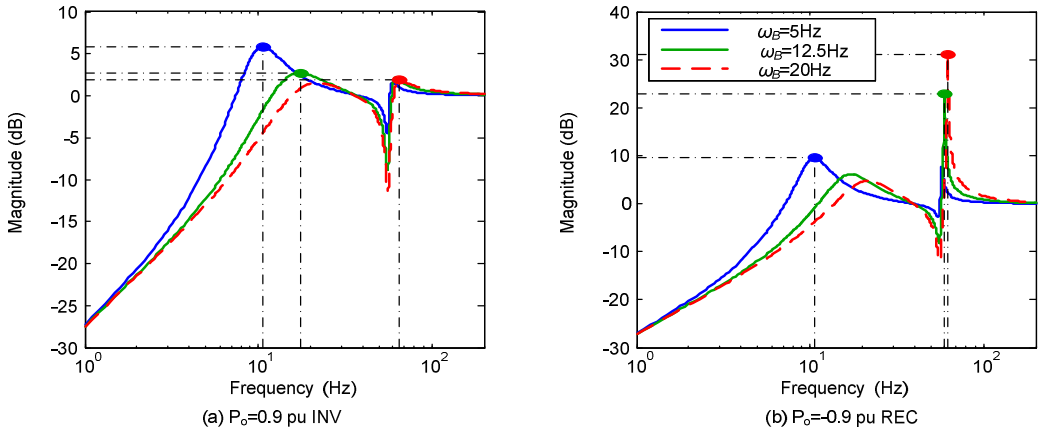


Figure 6.9: Frequency response of the sensitivity transfer function |S(*jω*)| (type 2 model, SCR=2.5, K_{droop}=12.5).

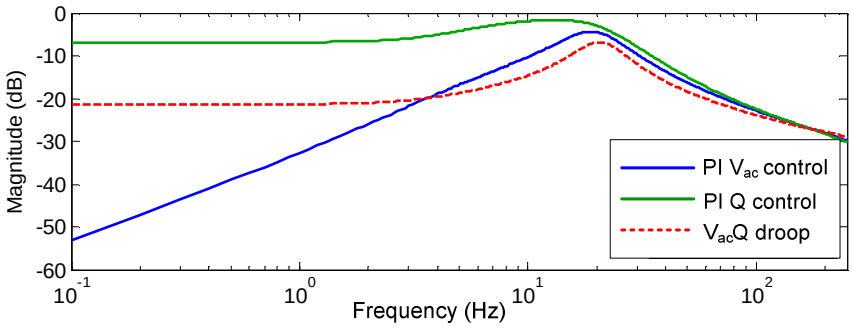


Figure 6.10: Frequency response of the closed-loop transfer function $v_{ac}(s)/i_{dc}(s)$ for three AC voltage/reactive power control designs (K_{droop}=12.5, SCR=1.65, P_o=0.9 pu INV).

For a weak AC system with SCR of 1.8 and droop gain of 7.5, frequency responses of the transfer function between the PCC bus voltage and the DC current variation in the type 1 model are compared in Figure 6.10, with three types of reactive power or AC voltage control controllers applied. When the PI AC voltage control or V_{ac}-Q droop control described in Chapter 2 is employed, the PCC bus voltage is relatively robust to the DC current variation. However, the AC voltage of a weak system can be quite sensitive to the DC side transients when the PI reactive power control is adopted, and this may lead to undesired AC voltage oscillations. Furthermore, it will limit the maximum power that can be manipulated by DC voltage control, and this could further result in the saturation of the droop controller. This analysis suggests that AC voltage control should be adopted for the application of VSC-HVDC in weak AC systems, in the interest of the stability of both the AC and DC sides of the converter system, unless the PCC bus voltage is supported by other devices with reactive power capability.

The frequency characteristics of the loop transfer function $L(s)$ produced by the type 2 model are presented in Figure 6.11, for four reactive power flow scenarios. The result shows that increasing the reactive power transfer into the converter side (decreasing Q_o) enhances the phase of $L(s)$ and therefore improves the gain margin and phase margin. However, a VSC is supposed to provide reactive power support for a weak AC system rather than absorbing reactive power. For a relatively weak AC system, an additional reactive power compensation device close to the PCC bus is desirable to reduce the reactive power transfer from the VSC to the AC system. But if the VSC is connected to a strong AC system, the variation of the reactive power operating point may have negligible impact on the stability of the DC voltage control.

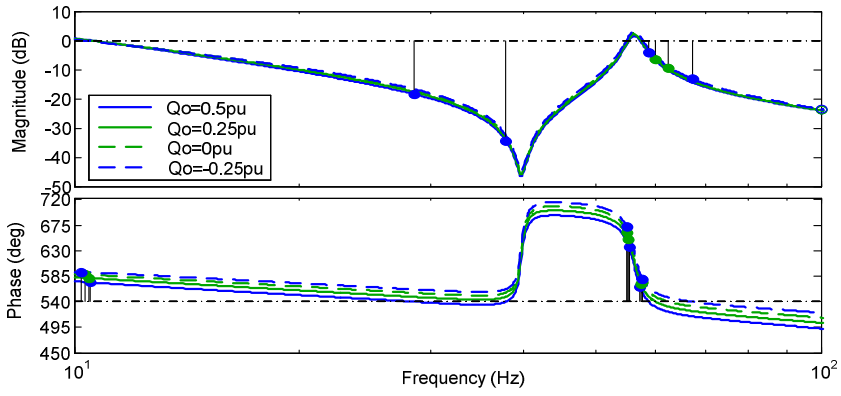


Figure 6.11: Frequency response of the loop transfer function *L(s)* for four reactive power operating point (SCR=1.8, P_o=-0.5 pu REC, K_{droop}=7.5, type 2 model).

6.2 Droop Control with Transient Compensation

The analysis presented in Section 6.1 suggests that conventional proportional-type droop may not be able to simultaneously provide sufficient robustness and satisfactory performance, especially for rectifiers connected to weak AC systems. A modified droop controller based upon transient compensation is proposed here to tackle this issue.

6.2.1 Transient Gain Reduction

Transient gain reduction (TGR) has been widely used in hydro governors and certain generator voltage regulators to achieve more stable control performance [151]. The proposed TGR design for DC voltage droop control is shown in Figure 6.12, where K_T represents the transient gain to be reduced from the steady-state gain K_C and the time constant T_R determines the frequency range of the TGR. The TGR enables a lower droop gain during transients, and therefore enhances the stability and robustness of the DC voltage loop without degrading the steady-state performance. The range of feasible droop gains can be extended via this compensator-based modification.

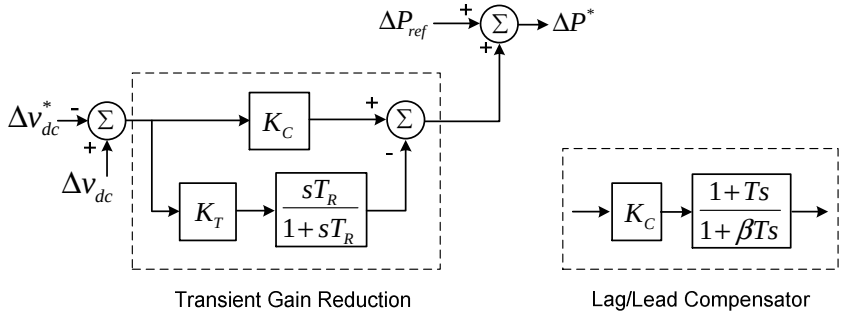


Figure 6.12: Droop controllers modified with transient compensation.

The droop control with the TGR can be represented in the form of a classic lag compensator shown in Figure 6.12, with equivalent parameters of the compensator described as:

$$T = \frac{K_C - K_T}{K_C} T_R,\ \beta = \frac{K_C}{K_C - K_T},\ (K_T < K_C) \tag{6.9}$$

A design methodology of lag compensators can therefore be readily applied for this TGR-based droop controller. The frequency-response based procedure discussed in [156] is adopted to achieve specifications of stability and robustness. In the design scheme, the gain K_C is determined by steady-state requirements of DC voltage deviations, β is calculated based on the additional magnitude reduction required to achieve the specified

stability margins, and T is selected to enable the corner frequency of the compensator to be eight to ten times lower than the new cut-off frequency. It is the attenuation characteristic, rather than the phase lag, that is utilised to reduce the high-frequency peak of L(s) and to improve the stability margins [156], particularly the phase margin. Therefore, a lag-compensator-based droop control always has a lower bandwidth than a proportional-type droop with identical gain. TGR-based droop control may however result in slightly larger DC voltage transient and longer settling time due to the reduced bandwidth.

6.2.2 Time-Domain Simulations

A four-terminal model constructed in DSPF, with the steady-state droop characteristics and the power flow operating point shown in Figure 6.13, is employed for the simulation test of the dynamic performance of the improved droop control. V-P droop control is used for GSC2 and droop with deadband control is applied to GSC3. Three droop controller designs are applied for GSC1, with the associated parameters shown in Table 6.2.

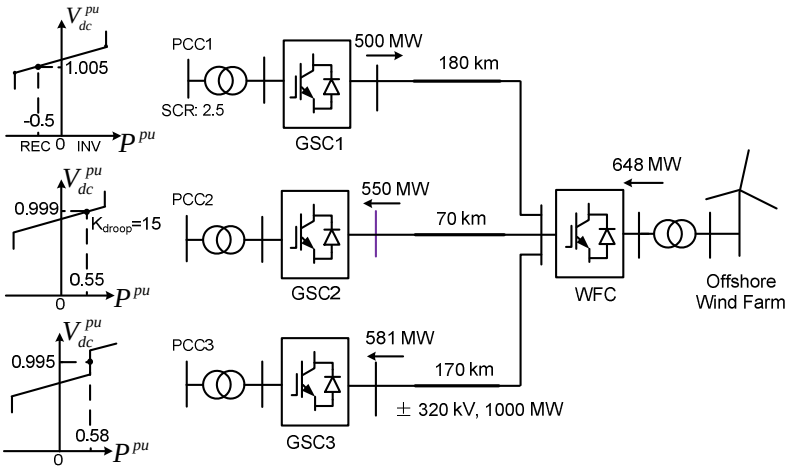


Figure 6.13: Four-Terminal test network and droop lines for GSCs.

Table 6.2: Parameters of the droop controllers.

	Droop	*TGR/Lag 1*	*TGR/Lag 2*
K_C	12.5	12.5	18
T	0	0.18	0.10
β	0	2.29	3.35
e_{ss}	0.08	0.08	0.06

Comparisons of the selected frequency domain indicators, as shown in Table 6.3, clearly demonstrate the superiority of the TGR-based droop controller over the proportional

controller. By including the appropriately designed compensation, the GM, PM and the sensitivity peak have been significantly improved, implying not only improved robustness but also enhanced damping performance, for both the type 1 and type 2 analytical models. The transient and stability measures for the two compensators are almost identical, while TGR/lag compensator 2 is preferred if the steady-state error e_{ss} is the key concern.

Table 6.3: Frequency domain measure of the droop controllers.

	Type 1 Model			*Type 2 Model*		
	Droop	*TGR/Lag1*	*TGR/Lag2*	*Droop*	*TGR/Lag1*	*TGR/Lag2*
ω_B *(Hz)*	14.8	9.4	9.1	9.3	5.4	5.2
GM (dB)	11.3	18.3	18.1	7.9	14.9	14.7
PM (deg)	28.1	47.1	44.8	20.3	51.8	47.8
$\|S\|_\infty$	4.6	4.4	7.8	10.7	4.8	4.8

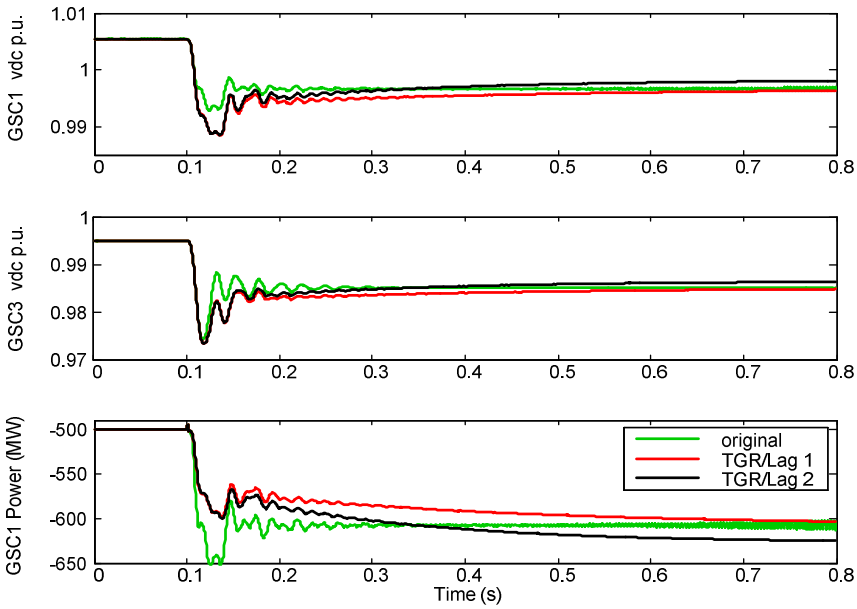


Figure 6.14: Simulation of loss of 250 MW wind power and comparison of performance of the three types of droop design for GSC1.

Transient responses of DC voltages of GSC1 and GSC3, and the inverting power of GSC1 to a sudden loss of 250 MW wind generation are shown in Figure 6.14. The simulations correlate well with the frequency-response analysis. The system with the proportional-type droop control struggles to deal with high-frequency oscillations and maintain acceptable performance. The active power responses with much higher damping and less high-frequency oscillations are provided by the scenarios where the transient compensations are employed. Practically, this reduces the stress on the AC system caused by DC side transients. Furthermore, the transient behaviour of the DC voltage at

GSC3 is enhanced. The scenario with the TGR/lag compensator 2 has the best steady-state performance, indicated by the lowest post-disturbance deviation of the DC voltage.

A slightly higher DC voltage peak occurs for the compensator cases, since the bandwidth is reduced in exchange for better stability. The simulation also verifies the feasibility of applying the droop controller designed based on the local terminal dynamics for the more complicated MTDC system. However, further investigation is required to develop a more robust design of the compensator-based droop control.

6.3 Stability Analysis of V-I Droop Control

The preceding DC voltage stability studies have focused the analysis with the emphasis on V-P droop control. This section aims to briefly address some parameterisation and stability issues associated with V-I droop control.

For a typical V-I droop implementation, the DC voltage reference is modified by a supplementary signal in proportion to the converter DC current, as illustrated in the closed-loop diagram in Figure 6.15, where $i_{dc}(s)/i_d^*(s)$ and $v_{dc}(s)/i_d^*(s)$ are the open-loop transfer functions that depend upon the overall dynamics of the DC network. The feedforward of the converter DC power could be used to reduce the impact of the power imbalance on the local DC voltage.

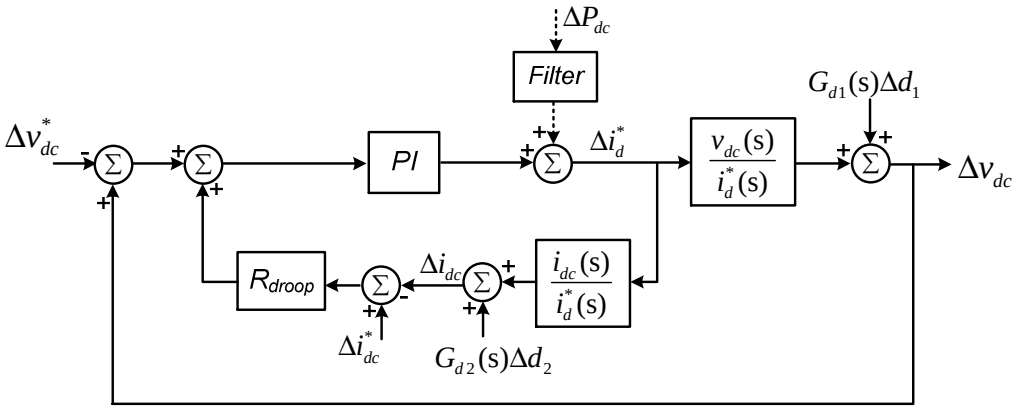


Figure 6.15: A generalised closed-loop diagram for V-I droop control.

A mathematical model based on the detailed converter model and the type 3 DC model, with its schematic formulation illustrated Figure 6.16, was constructed and employed for the frequency domain analysis of the V-I droop, with respect to the impact of the power OP, the DC voltage control bandwidth and the droop constant R_{droop}, which is the steady-state slope of the droop line. The SCR is selected to be 2.5 and the cable length of 150

km is used in the analysis undertaken in this section. The feedforward DC power is not used here, however detailed discussion of this method will be provided in next section.

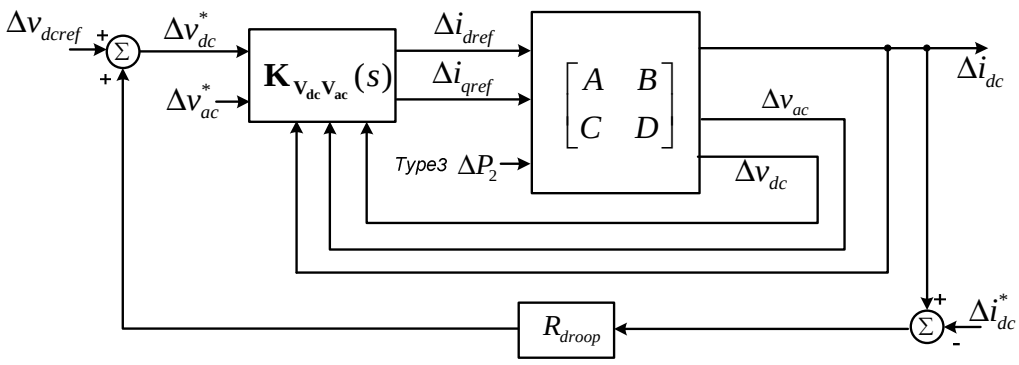


Figure 6.16: Formulation of the open-loop/closed-loop model for V-I droop control (type 3 model).

With the system linearised at P_o=-0.8 pu (REC), the resulting frequency responses of the closed-loop disturbance transfer function $v_{dc}(s)/P_2(s)$, the sensitivity transfer function S(s) and the dominant eigenvalues of the closed-loop models are depicted in Figure 6.17 for three settings of the droop constants.

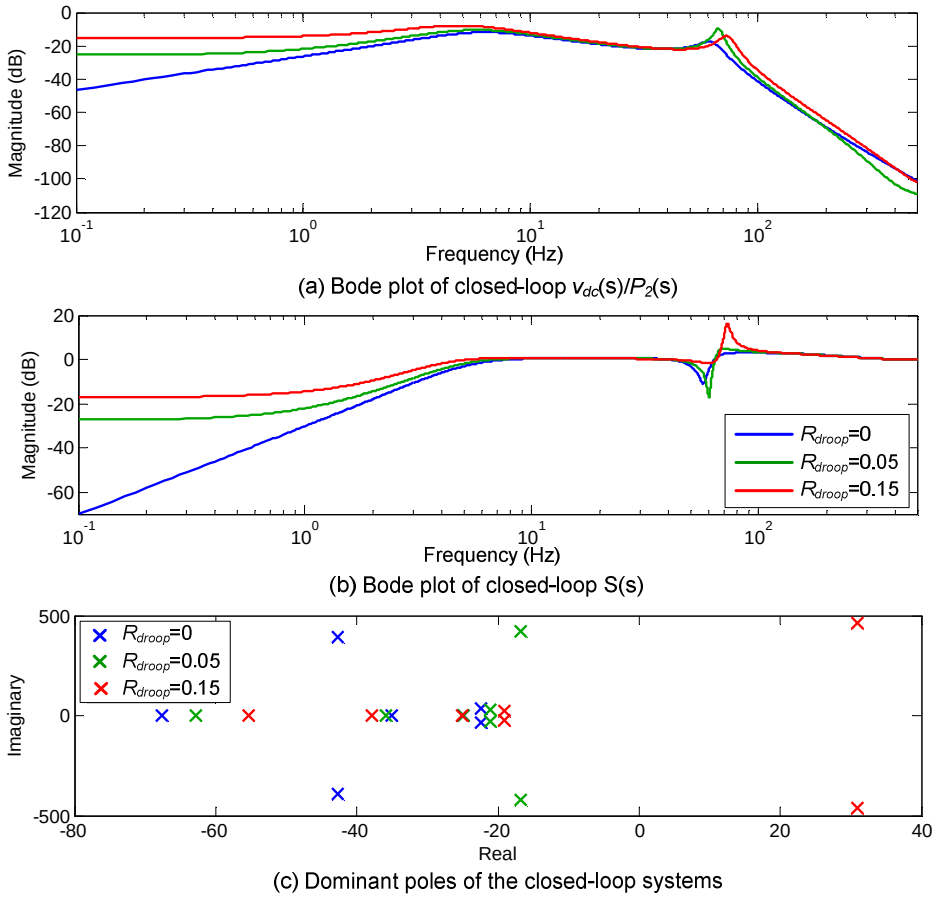
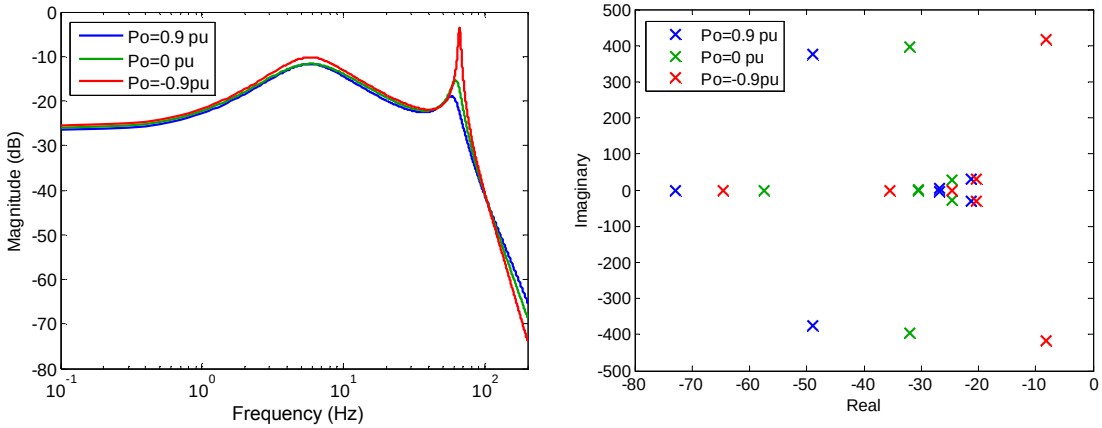


Figure 6.17: Analytical results of the type 3 model with respect to three V-I droop settings (cable length=150 km, P_o=-0.8 pu REC, type 3 model).

Increasing R_{droop} degrades the disturbance rejection capability of the DC voltage control at low frequencies, as shown in Figure 6.17(b). The high sensitivity peak for R_{droop}=0.15 around 75 Hz in Figure 6.17(a) indicates poor robustness and stability. Using a larger droop constant reduces the damping of the high-frequency modes and could eventually cause instability, as shown in Figure 6.17(c). Considering that the droop constant can be seen as the reciprocal of the droop gain in steady-states, better steady-state DC voltage error can probably be achieved by V-I droop rather than the more conventional V-P droop. A smaller droop constant typically indicates better stability; however, it also implies that the power sharing between converters is more dependent on the network topology, according to the analysis in Chapter 3.

The impact of the power operating point on the frequency response of $v_{dc}(s)/P_2(s)$ and the closed-loop eigenvalues is demonstrated in Figure 6.18. Like V-P droop control, the robustness issue with respect to the power operating point also exists for V-I droop control. The DC voltage becomes more sensitive to the power disturbance around 60-70 Hz, and the associated modes become less damped as the converter injects more power into the DC system. In fact, the limitations identified in Section 6.1 based on the open-loop analysis can be directly applied for the V-I droop control, as essentially it is still the d-axis current that is used as the manipulated input.

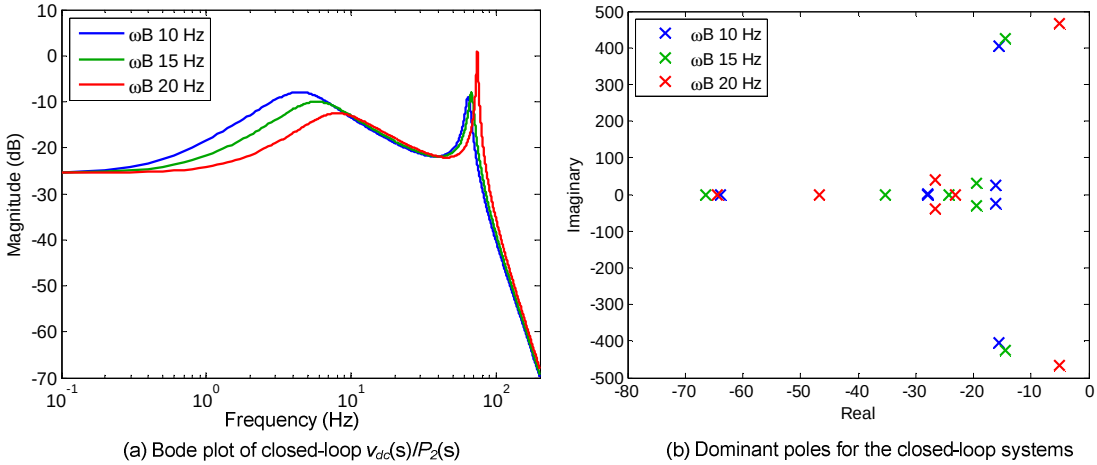


(a) Bode plot of closed-loop $v_{dc}(s)/P_2(s)$ (b) Dominant poles for the closed-loop systems

Figure 6.18: Analytical results of the type 3 model with respect to three power operating points (cable length=150 km, R_{droop}=0.05, type 3 model).

The frequency-response and the eigenvalue plots are provided in Figure 6.19 to assess the impact of the DC voltage controller gain on the performance of the V-I droop. More damping can be provided for the DC voltage at low frequencies by the PI controllers with higher gains. However, the increase of the DC voltage control bandwidth could result in poor damping at relatively high frequencies (65 to 75 Hz in this case) and even instability

of the V-I droop control, when the converter is in rectifier operation. The design of the PI v_{dc} controller and the droop constant should therefore be coordinated for weak AC system connection to avoid such potential instability.



(a) Bode plot of closed-loop $v_{dc}(s)/P_2(s)$ (b) Dominant poles for the closed-loop systems

Figure 6.19: Analytical results of the type 3 model with respect to three PI v_{dc} controllers (cable length=150 km, R_{droop}=0.05, P_o=-1.0 pu REC, type 3 model).

In order to demonstrate the performance of the V-I droop and its interaction with the V-P droop, four control scenarios configured as shown in Table 6.4 were compared using the four-terminal model shown in Figure 6.13. The SCR of 2.5 was applied to all GSC terminals. Figure 6.20 shows the simulation results of a sudden loss of 250 MW wind farm power. The typical V-P droop without transient compensation was employed in this study.

Table 6.4: Four control cases for the four-terminal test system.

	GSC1		GSC2		GSC3	
Scenario	Mode	Gain	Mode	Gain	Mode	Gain
Case 1	V-P droop	K_{droop}=10	V-P droop	K_{droop}=10	V-P droop	K_{droop}=10
Case 2	V-I droop	R_{droop}=0.08	V-I droop	R_{droop}=0.08	V-I droop	R_{droop}=0.08
Case 3	V-I droop	R_{droop}=0.02	V-I droop	R_{droop}=0.02	V-I droop	R_{droop}=0.02
Case 4	V-I droop	R_{droop}=0.02	V-I droop	R_{droop}=0.02	V-P droop	K_{droop}=10

The lowest transient excursion of the DC voltage is provided by the V-P droop scenario as the active powers of the GSCs respond to the DC voltage deviation more abruptly in Case 1 than the V-I droop in Case 2 and 3, since the power reference is quickly modified by the V-P droop controller due to its high gain. The low-frequency active power transients for the two V-I droop cases are very similar; however, high-frequency instability occurs for Case 3 where the more steeper droop (larger R_{droop}) is employed for the rectifier GSC1, as increasing the droop constant effectively enlarges the loop gain

and this can cause instability for systems with RHP zeros. Steep droop is normally not desired from the perspective of steady-state DC voltage error either.

It takes a much longer time for the system to reach the new post-transient operating point when the V-I droop is utilised jointly with the V-P droop in Case 4. Similar behaviour has been observed in Chapter 2 when V-P droop is employed in conjunction with constant DC voltage control. During transients, the terminal equipped with V-P droop takes more responsibility in regulating the DC voltage, because V-P droop control is more sensitive to the DC voltage error than V-I droop and the closed-loop bandwidth of V-P droop is usually higher.

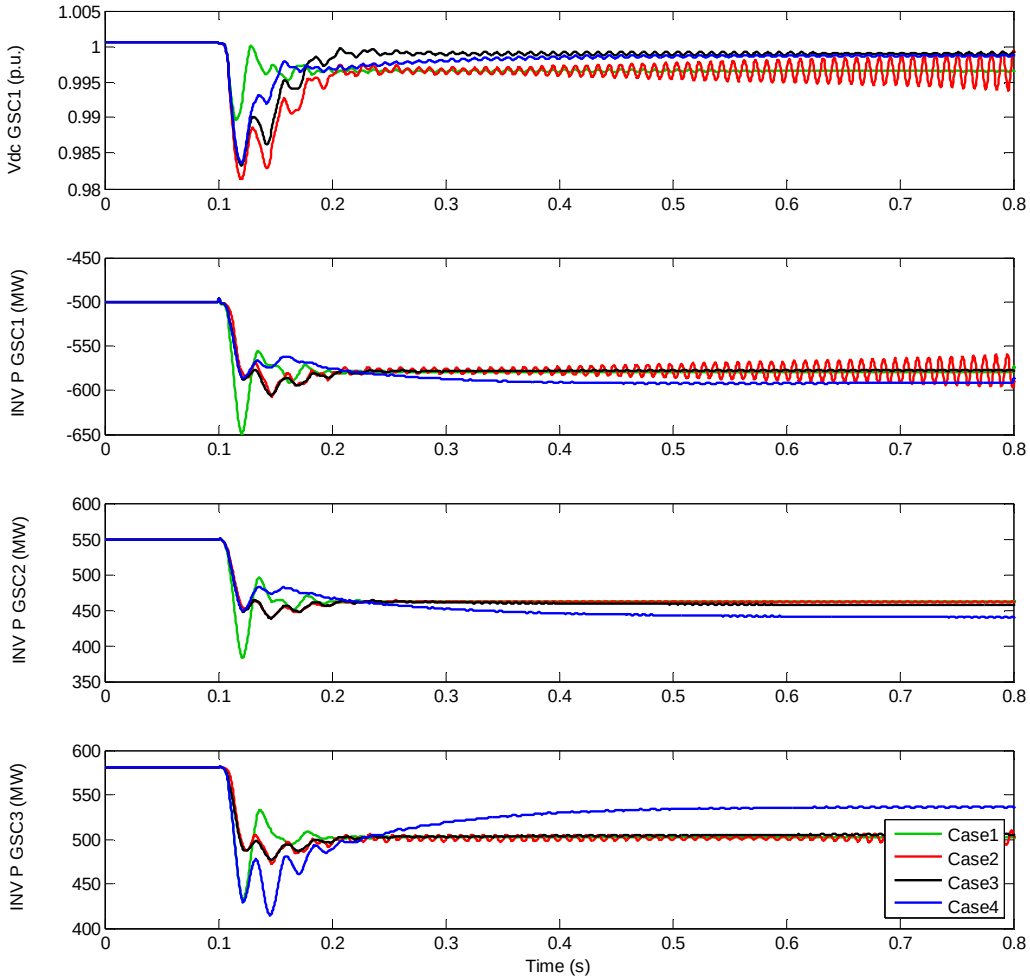


Figure 6.20: Dynamic responses of the four-terminal test system to sudden loss of 250 MW wind farm power, under four control scenarios.

The majority of the limitations identified in Section 6.1 for V-P droop are also applicable to V-I droop control. In essence, irrespective to the form of the controller, the DC voltage has to be controlled through the active current, which is directly related to the converter power, given that vector current control is employed. The droop constant R_{droop} for V-I

droop control should be sufficiently low in order to avoid interactions between the high-frequency component of DC current and the AC side active power control. Additionally, similar to V-P droop, the stability margins for V-I droop can also be improved by applying the TGR technique to reduce the transient droop constant.

6.4 Impact of the Feedforward DC Current

Both voltage margin control and V-I droop control are formed based upon constant DC voltage control. It is suggested in [66, 84, 85] to use the feedforward of the converter DC power or DC current to compensate the power disturbance coming from the DC system, as shown in Figure 2.22 and Figure 6.21. Through this approach, the d-axis current is modified rapidly by the feedforward power to improve the disturbance rejection performance of the DC voltage control. Another important purpose of this control structure is to allow the v_{dc} controller to be designed independently from the DC network dynamics, provided that the current loop is sufficiently fast to enable the DC power to be well compensated by the feedforward term.

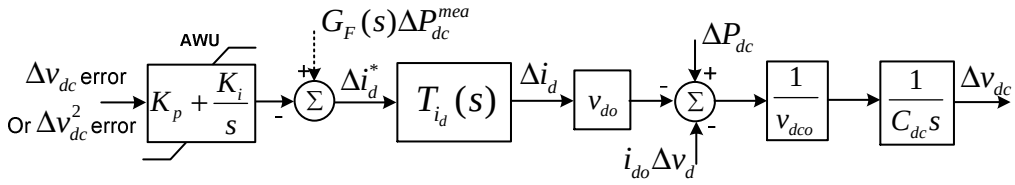


Figure 6.21: DC voltage control with feedforward DC power.

However, the impact of this control modification on the stability of the VSC system has not been addressed in the previous literature. This section aims to identify the stability constraints associated with the utilisation of this disturbance cancellation technique for the DC voltage control. A point-to-point DSPF test model depicted in Figure 6.22 is used to illustrate the dynamic issues with respect to such control. The associated frequency response results produced using the type 3 model are presented for analytical verification.

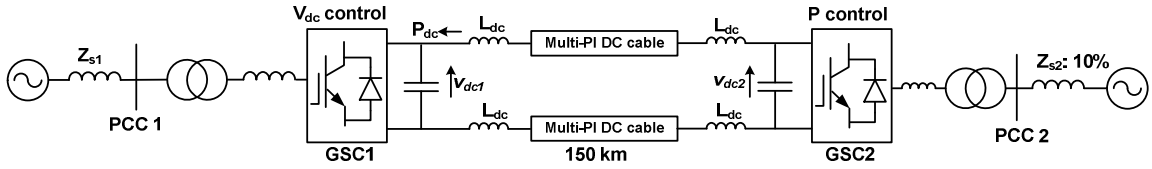


Figure 6.22: Point-To-Point test system.

The dynamic responses of the DC voltage and power of GSC1 to the 50 MW power reference change of GSC2 are compared for three v_{dc} controller designs in Figure 6.23,

considering the impact of the bandwidth of the low-pass filter (LPF) $G_F(s)$ for the feedforward P_{dc}. The corresponding frequency responses of the transfer function $v_{dc1}(s)/P_{ref2}(s)$ and $P_1(s)/P_{ref2}(s)$ are shown in Figure 6.24. The transient peak of the DC voltage is significantly reduced by employing the feedforward term, because the current reference is modified much faster by the feedforward power than by the PI v_{dc} controller. The use of the feedforward power results in the fact that the active power response is much more sensitive to the DC side transients. The best overall performance is provided by the case where the 25 Hz LPF is used for the filtering of the DC power. The damping performance for the scenario where 150 Hz $G_F(s)$ is employed is extremely poor at 42 Hz. This shows that a LPF with an appropriate bandwidth, which has normally been neglected, is necessary if the feedforward DC power is used for the v_{dc} control.

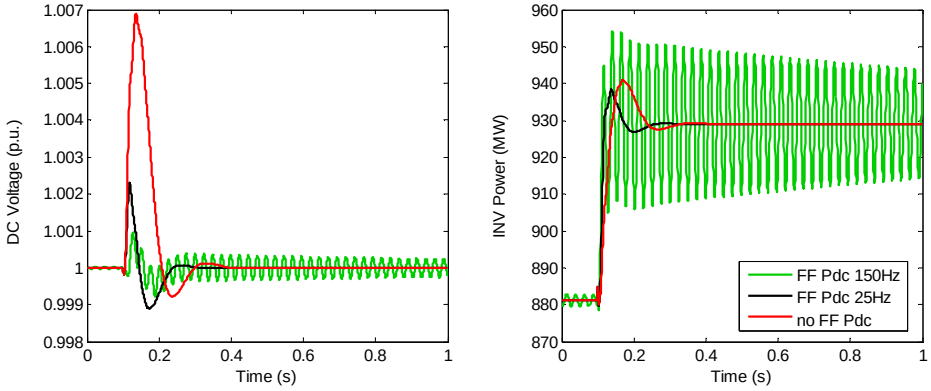


Figure 6.23: Responses of GSC1 to a 50-MW power reference change of GSC2 for three types of DC voltage controller at GSC1 (L_{dc}=0 mH, Z_{s1}=0.4 pu).

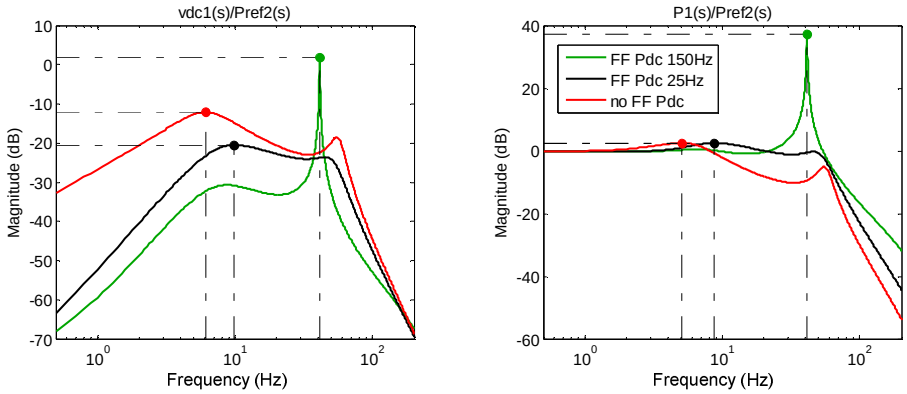


Figure 6.24: Frequency responses of the closed-loop transfer function $v_{dc1}(s)/P_{ref2}(s)$ and $P_1(s)/P_{ref2}(s)$ (P_o=0.93 pu INV, L_{dc}=0 mH, Z_{s1}=0.4 pu, type 3 model).

One controversial reason for using fast feedforward power for the v_{dc} control is to improve the robustness of the closed-loop system to DC system uncertainties. By including DC reactors of 125 mH in the test system, simulations similar to the previous study have been performed with the results presented in Figure 6.25, which clearly

demonstrates that the use of the feedforward DC power could worsen the system robustness at high frequencies if the LPF $G_F(s)$ is not well designed. Injecting high-frequency DC power/current dynamics into the DC voltage controller output cannot perfectly cancel the disturbance, which can in contrast result in adverse interaction with the AC side dynamics. The weaker the AC system is, the more such interactions are likely to be severe.

When the GSC1 is in rectifier operation (P_o=-1.0 pu), the dynamic performances of the three controller designs in response to a 50 MW power reference change of GSC2 are compared in Figure 6.26. In contrast to the results shown previously for the inverter operation, the conventional PI control without the feedforward power suffers from the high-frequency instability due to the combination effect of the low SCR and the rectifier operation, while stability is maintained with the use of the feedforward power. Increasing the filtering bandwidth of the feedforward power reduces the transient DC voltage peak however it also degrades the damping and stability.

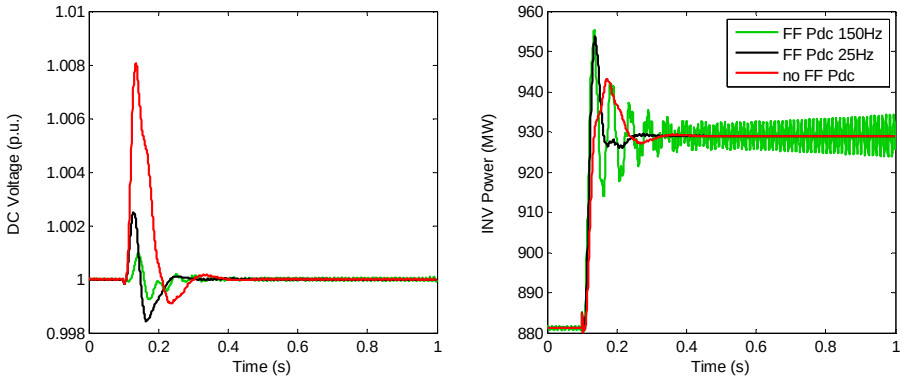


Figure 6.25: Responses of GSC1 to the 50 MW power reference change of GSC2 for three types of DC voltage controller at GSC1 (Inverter, L_{dc}=125 mH, Z_{s1}=0.4 pu).

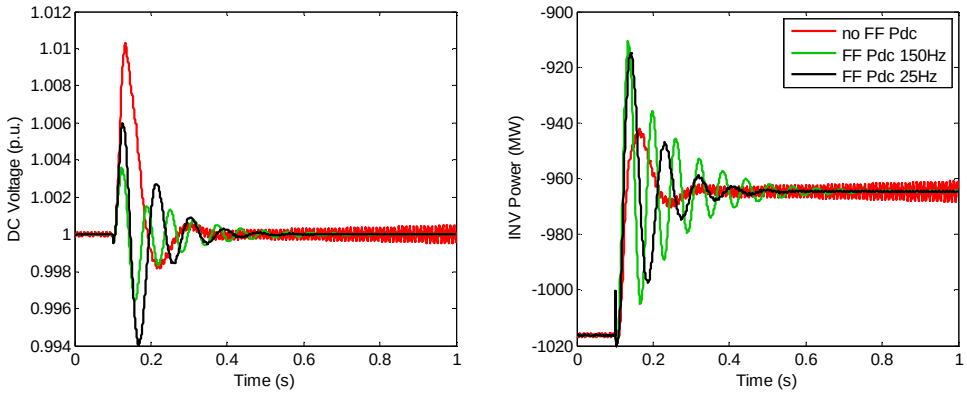


Figure 6.26: Responses of GSC1 to a 50-MW power reference change of GSC2 for three types of DC voltage controller at GSC1 (Rectifier, L_{dc}=125 mH, Z_{s1}=0.4 pu).

In the previous two study cases, relatively low SCRs of 2.5 were employed for GSC1. When GSC1 is operating as a rectifier and the SCR of 10 is configured, the dynamic

responses of GSC1 to a power reference change of GSC2 are shown in Figure 6.27. The utilisation of the 150 Hz LPF for the feedforward power leads to poorly damped DC transient performance, and the resulting system is marginally stable. This phenomenon, which is predominantly caused by the negative admittance effect of constant power control, is verified analytically by the large frequency domain peaks at low frequencies within 20 Hz, as shown in Figure 6.28. Clearly, using the feedforward modification is not a reliable solution for the negative admittance instability issue.

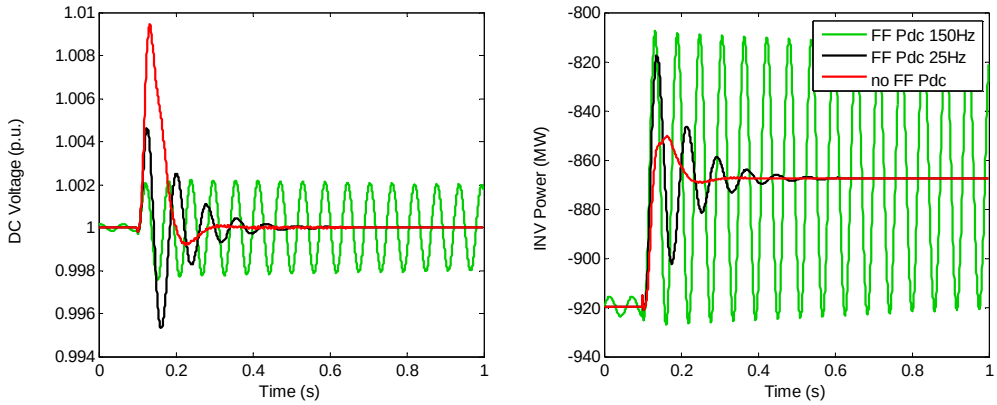


Figure 6.27: Responses of GSC1 to a 50-MW power reference change of GSC2 for three types of DC voltage controller at GSC1 (P_o=-0.87 pu REC, L_{dc}=125 mH, SCR1=10).

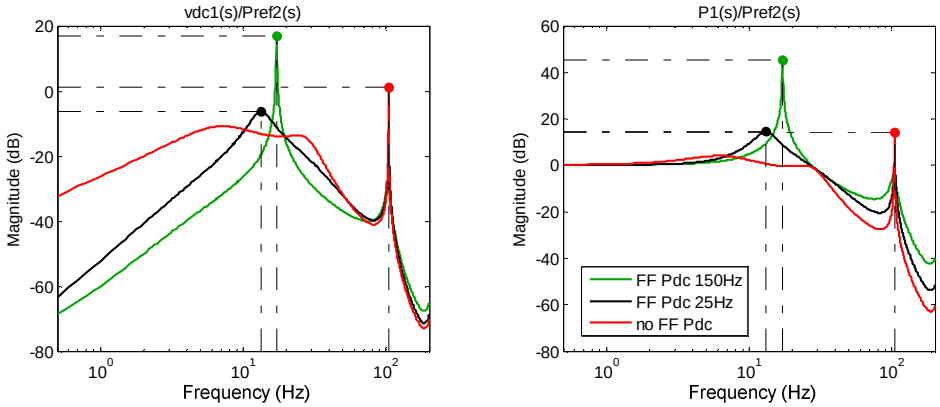


Figure 6.28: Frequency responses of the closed-loop transfer function v_{dc1}(s)/P_{ref2}(s) and P_1(s)/P_{ref2}(s) (P_o=-0.87 pu REC, L_{dc}=125 mH, SCR1=10, type 3 model)

6.5 Chapter Summary

Stability limitations of the VSC-HVDC DC voltage control, particularly V-P droop control, have been analysed using frequency-response techniques based upon a detailed converter system model and three types of DC system models. Fundamental robustness issues of the conventional droop controller regarding weak AC systems, converter operating point and controller design of other control loops, including the active/reactive power control and AC voltage control, have been identified. Key trade-offs in the design of the droop gain have been addressed. It is shown that it could be quite challenging to use a rectifier connected to a weak AC system to control the voltage of a DC system which has large reactors.

A droop controller with transient compensation has been proposed to enhance its robust stability without compromising its power sharing capability, the performance of which is demonstrated by both frequency and time domain simulations.

The impact of the droop constant, the power operating point and the DC voltage control bandwidth on the stability of V-I droop control has been analysed. Most of the limitations identified for V-P droop control also restrict the performance and stability of V-I droop control. Large droop constants and high-bandwidth DC voltage control are not recommended for the use with V-I droop. More comprehensive assessment of the V-I and V-P droop control is required for future studies.

The impact of using the feedforward of the DC power as part of the DC voltage controller on stability and disturbance rejection performance of DC voltage control has been assessed. A low-pass filter with carefully selected bandwidth is recommended for the DC power measurement in order to avoid instability, especially when the converter is connected to a high-impedance AC system and a high-inductance DC system.

Chapter 7 Impact of DC Reactor on MTDC Stability and Damping Enhancement

At present, fault clearance for point-to-point systems is undertaken by AC side breakers. For large DC grids, this will be impractical since the entire DC grid would need to be de-energised. The disruption caused by such an event would most likely be prohibitive. HVDC circuit breakers (DCCB) to isolate faulted lines individually would be needed, such as the design shown in Figure 7.1. Thus, substantial research has been undertaken by major manufacturers in developing DC breakers, and very good progress is being made in developing full-scale commercial devices [23, 24].

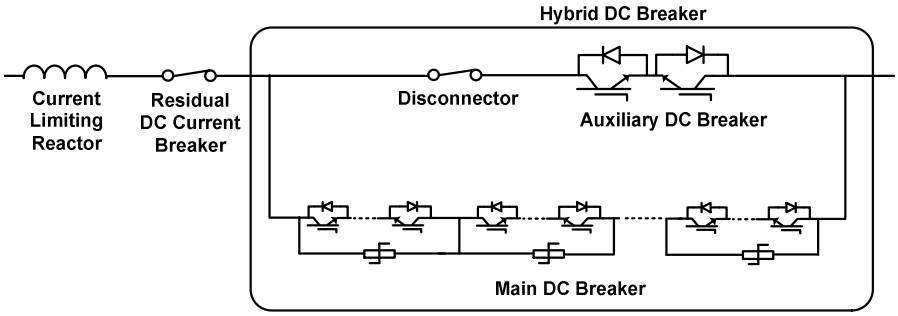


Figure 7.1: ABB proactive HVDC circuit breaker [23].

All such devices to date however rely on a relatively large DC reactor to help limit the rate of rise of faulted current and the rate of reduction of DC voltages. This reactor is also likely to be required for fault location algorithms [157]. The minimum size of the DC reactor depends on the breaking time of the DCCB and its maximum current breaking rating, which is directly linked with the cost of the breaker. On the other hand, the DC reactor size is also limited by its cost and, possibly, by the extra conduction loss it causes and the stability requirements of the DC grid. Values in the order of 100 mH per pole for ±320 kV systems are typically used in previous published work [23, 158].

However, the utilisation of large DC reactors can have a detrimental effect on the DC voltage control and even affect the stability of HVDC grids. A number of excellent papers exist analysing dynamics of multi-terminal grids [43, 67, 75, 147, 159], but none yet examines the impact of this new component. The stability in the level of DC grid can be interpreted as DC voltage stability. Droop control will be used as the benchmark control in this chapter for the study of the impact of the DC reactor on MTDC dynamics.

The purpose of this chapter is to address the limitations imposed by the DC reactor on the stability and dynamic performance of MTDC systems, and show how control can be improved to cope with such issues. Detailed analysis of the stability and performance issues caused by the DCCB system are provided in Section 7.1. In Section 7.2, a new DC voltage damping control is proposed to enhance the transient behaviour of systems with large DC reactors. The selection of the controller location and the performance of this damping control are demonstrated using a seven-terminal MTDC system. Two types of active stabilising control are developed in Section 7.3 to counteract the negative admittance effect caused by constant power control and to improve the controllability and damping of the DC system.

7.1 Stability Issues Caused by DC Reactor

This section approaches the problems associated with the DC reactor by analysing the poles, zeros and frequency responses of the open-loop and closed-loop DC voltage control systems. The constraints imposed by the DC reactor on stability, controllability and dynamic performance of MTDC systems are demonstrated and analysed using a generic four-terminal model.

7.1.1 Description of Analytical Models

A schematic diagram of the multi-input-multi-output (MIMO) plant model used for the MTDC voltage stability analysis is shown in Figure 7.2. For V-P droop control, the power references of the GSCs in DC voltage control mode are employed as the manipulated inputs. The power variations of the WFCs and the GSCs in active power control mode act as disturbances to the DC voltage control. The power “reference” for the WFC can be seen as the mechanical power captured by the turbine system. For a relatively strong AC system, the q-axis current and reactive power control are likely to have a very limited impact on the DC voltage dynamics. The q-axis related controllers and dynamics are not included here in the mathematical model for DC voltage stability study, as weak AC system connection is not the main concern of this chapter.

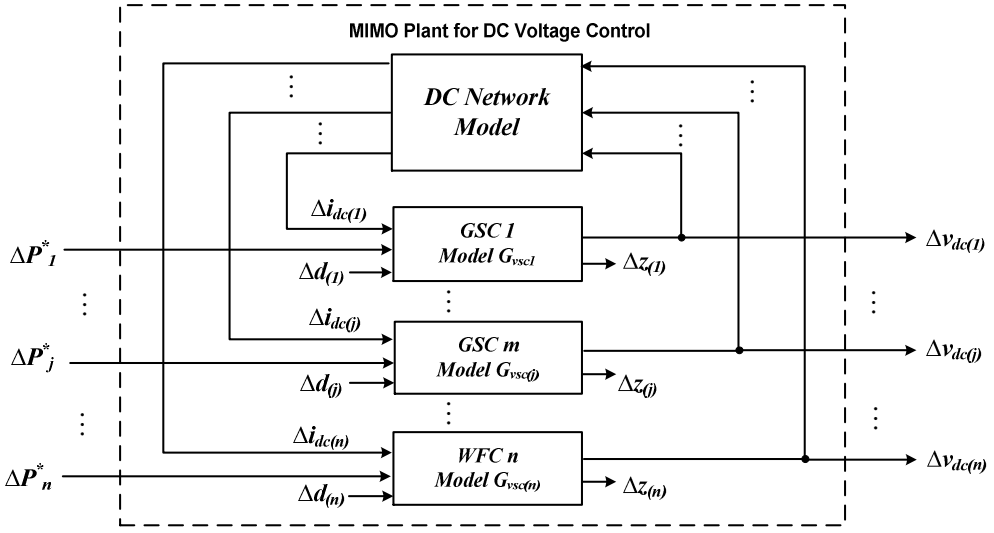


Figure 7.2: Formulation of plant model for DC voltage control.

V-P droop control is employed here for the GSCs under investigation to form a closed-loop model. For the common implementation of V-P droop control, the active power reference P^* is modified by the droop controller output; therefore, the active power control is treated here as part of the plant model of the droop control. Based on the modelling methodology explained in Chapter 5, a state-space model is constructed for the *j*th GSC, in the form of (7.1), where P_j^* is the power reference of the *j*th converter, $i_{dc(j)}$ is the DC current injected into the *j*th converter from the DC grid, d_j denotes the disturbance vector ($[v_{sd}\ v_q\ i_q\ i_{sq}]^T$ in this case). Please see [160] for more detailed model description.

$$\begin{aligned} \dot{x}_j &= A_j x_j + \begin{bmatrix} B_{jG} & B_j \end{bmatrix} \begin{bmatrix} \Delta i_{dc(j)} \\ \Delta P_j^* \end{bmatrix} + B_{dj} d_j \\ \Delta v_{dc(j)} &= C_{jG} x_j \end{aligned} \tag{7.1}$$

The mathematical DC network model is constructed by interconnecting all the state-space line models, according to the approach presented in Section 5.3. The resulting form of the overall network model is shown as (7.2), where the converter DC voltages are used as input and the DC currents into the converter from the DC system are produced as output.

$$\begin{aligned} \dot{x}_G &= A_G x_G + B_G \Delta \mathbf{v}_{dc} \\ \Delta \mathbf{i}_{dc} &= C_G x_G \end{aligned} \tag{7.2}$$

By combining the analytical models of all the converter terminals shown in the form of (7.1) and the DC network model shown in (7.2), the overall open-loop state-space model

for the DC voltage stability studies can be derived as shown in (7.3), where x_j is the state variables of the jth converter model, B_{Gj} is the jth column of B_G, and C_{Gj} is the jth row of C_G, n is the total number of converter terminals, n_G is the number of state variables of x_G.

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \vdots \\ \dot{x}_n \\ \dot{x}_G \end{bmatrix} = \begin{bmatrix} A_1 & & & & B_{1G}C_{G1} \\ & A_2 & & & B_{2G}C_{G2} \\ & & \ddots & & \vdots \\ & & & A_n & B_{nG}C_{Gn} \\ B_{G1}C_{1G} & B_{G2}C_{2G} & \cdots & B_{Gn}C_{nG} & A_G \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \\ x_G \end{bmatrix} + \begin{bmatrix} \mathbf{diag}\left(B_j \big|_{j=1,\ldots,n} \right) \\ \mathbf{0}_{n_G \times n} \end{bmatrix} \begin{bmatrix} \Delta P_1^* \\ \Delta P_2^* \\ \vdots \\ \Delta P_n^* \end{bmatrix} \tag{7.3}$$

$$\Delta \mathbf{V}_{dc} = \begin{bmatrix} \mathbf{diag}\left(C_{jG} \big|_{j=1,\ldots,n} \right) & \mathbf{0}_{n \times n_G} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \\ x_G \end{bmatrix}$$

In the following studies, the relevant open-loop transfer functions are extracted from this multivariable model. The closed-loop MTDC model will be formed by interconnecting droop controllers with this MIMO model.

7.1.2 Stability and Controllability Issues

A four-terminal VSC-HVDC system, with its topology and the nominal power flow shown in Figure 7.3, is employed to demonstrate the stability and performance issues revealed in this section. The nominal DC reactor of 100 mH per pole is selected for the DC breaker system.

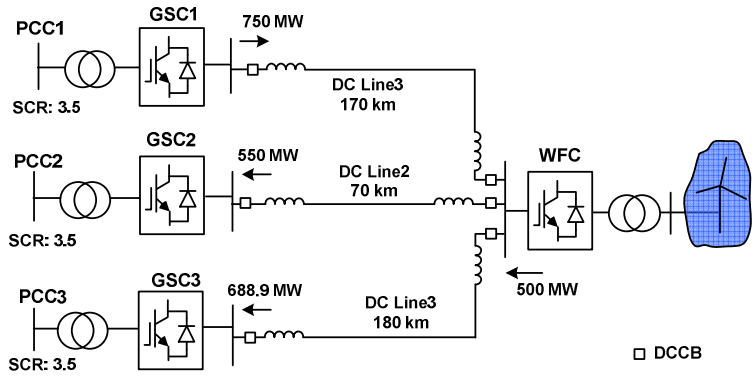


Figure 7.3: Four-terminal VSC-HVDC test model.

The typical V-P droop control is essentially a proportional DC voltage controller. Root locus analysis based on the plant model is very effective to analyse controllability and to determine the appropriate droop gain. For a particular VSC terminal, the plant of its

droop controller is the transfer function between its power reference $P_j^*(s)$ and the local DC voltage $v_{dcj}(s)$, which can be directly extracted from the MIMO model. Controllability analysis is performed based upon the open-loop plant models of the DC voltage control, in order to reveal the general stability issues imposed by the DC reactor, despite the controller form. The limitations imposed by the DC reactor on the DC voltage controllability and stability are investigated by analysing the loci of poles and zeros.

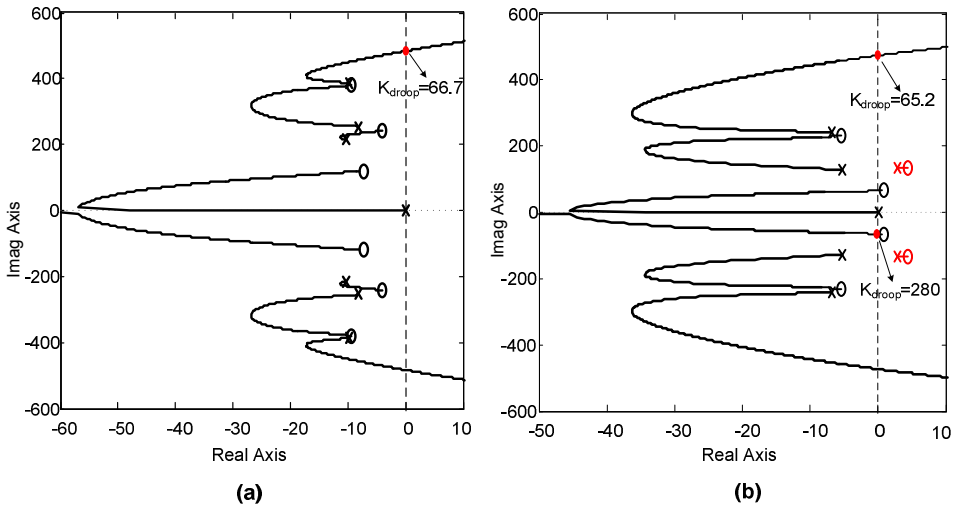


Figure 7.4: Root loci of the open-loop transfer function of $v_{dc1}(s)/P_1^*(s)$ for the four-terminal model in low-frequencies: (a) without DC reactor; (b) with DC reactor of 100 mH.

With respect to DC voltage control using GSC1, the root loci of the plant model $v_{dc1}(s)/P_1^*(s)$ are shown in Figure 7.4 (a) and (b), for the four-terminal model without and with consideration of the DC reactors in the system, respectively. Only the low-frequency dominant poles and zeros out of the hundreds in the system are shown here for clarity. Including the 100 mH DC reactors significantly worsens the controllability of the system, since there are right-half-plane (RHP) poles and zeros located close to each other, as shown in Figure 7.4 (b).

It is acknowledged in [1] that, large peaks of sensitivity in a transfer function are unavoidable when RHP poles are close to RHP zeros. Therefore, such systems are very difficult to stabilise and a high-order controller would have to be used. The root loci in Figure 7.4 (b) suggest that, when there is no other converter in DC voltage control mode, the DC voltage is uncontrollable by GSC1 using droop control, irrespective of the droop gain setting. In fact, the DC reactor imposes a severe constraint for all types of DC voltage control using GSC1, including slack bus control and voltage margin control. An increased number of converters need to be configured in DC voltage control mode in order to stabilise the DC system installed with DC reactors.

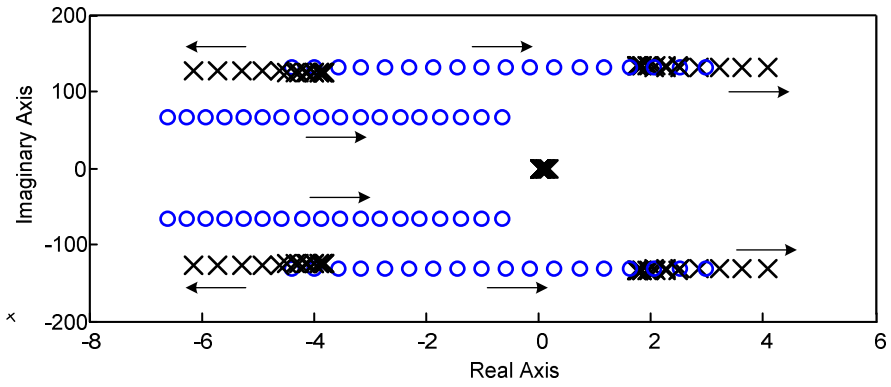


Figure 7.5: Trajectories of the dominant poles and zeros of the open-loop transfer function $v_{dc3}(s)/P_3^*(s)$ as GSC3's inverting power varies from 0.85 pu (INV) to -0.45 pu (REC).

For a MTDC system with DC breaker systems, dynamics are likely to be sensitive to the variations of the power flow condition of the network. This is demonstrated by Figure 7.5 where the trajectories of the dominant poles and zeros of the plant model $v_{dc3}(s)/P_3^*(s)$ of DC voltage control using GSC3 are shown for a range of power flow scenarios, in which the powers of GSC3 and GSC1 are varied while the powers of GSC2 and WFC1 are kept constant.

The dominant poles and zeros migrate towards the RHP as the rectifying power of GSC3 increases. Especially, the low-frequency zeros are highly sensitive to the power flow of the local terminal as well as the DC network. This effect is mainly caused by the underlying nonlinearity of constant power control. This feature also exists for other types of DC voltage controllers as essentially the DC side control of VSC relies on the AC side active current control, which is directly correlated with active power rather than DC current. The RHP poles impose a lower bound of the DC voltage control bandwidth. The RHP zeros however imply high-gain instability and an upper bound of the bandwidth [1].

This robustness issue with respect to the converter power flow exists, even without including large DC reactors in the model. However, the increase of the inductances in the DC system significantly worsens this issue by amplifying the sensitivity of the poles/zeros to the power flow. It is preferable to implement voltage droop control for the converters that usually operate as inverters. For better robustness, droop control is also suggested to be applied to the converters that are likely to experience power reversals. The converter may need to change its control mode in case of extreme power flow changes. More advanced robust controller design may be required to ensure the stability of a DC grid where the power flow could vary significantly and frequently.

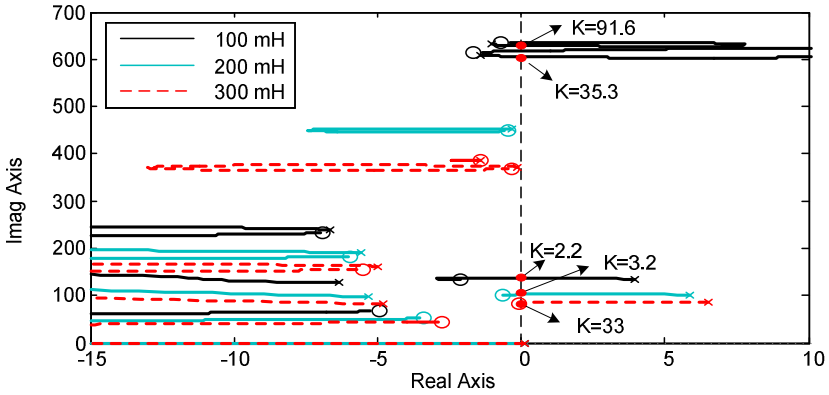


Figure 7.6: Root loci of the open-loop transfer function $v_{dc3}(s)/P_3^*(s)$ of the four-terminal model for three DC inductor sizes.

For three settings of the DC reactor size, root loci of the plant model $v_{dc3}(s)/P_3^*(s)$ are shown in Figure 7.6, which describes DC voltage control using GSC3. This analysis demonstrates that a larger size of DC inductance implies tighter constraints on the boundaries of droop control gain. Since the unstable poles move towards the RHP as the inductance increases, a high-gain controller may have to be employed to obtain a stable system. Furthermore, for the 200 mH and 300 mH scenarios, it is very difficult to achieve a satisfactory dynamic performance since the damping of the dominant closed-loop poles would be excessively low. This clearly shows that the control requirement imposes a bound on the maximum DC reactor size.

It should be noted that, for a HVDC grid that has larger equivalent capacitances and resistances, the DC system will be more stable and better damped, and therefore may allow DC reactors with higher ratings to be utilised.

Generally, to improve the stability of DC grids with large DC reactors, voltage droop control systems with carefully designed bandwidth/gains and selected location, should be adopted by more converters, particularly for inverters.

7.1.3 Dynamic Performance Issues

Frequency-response analysis is employed here to address the dynamic performance issues caused by large DC reactors, since this analytic tool is very useful in interpreting the damping, robust performance and key oscillating frequencies of a complex system.

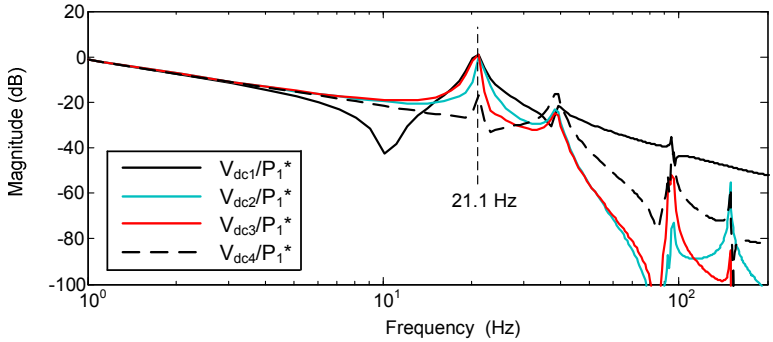


Figure 7.7: Frequency responses of the open-loop transfer functions between the DC voltages of the four terminals and the power reference of GSC1 $P_1^*(s)$, the four-terminal model.

The frequency responses of the open-loop transfer functions between the four DC terminal voltages and the power reference of GSC1 are shown in Figure 7.7. The frequency domain peak at 21.1 Hz implies that the DC voltages of GSC1, GSC2 and GSC3 are sensitive and likely to be oscillatory in response to the power change of GSC1 at this frequency. This low-frequency resonance of the open-loop model will be reflected in the closed-loop model.

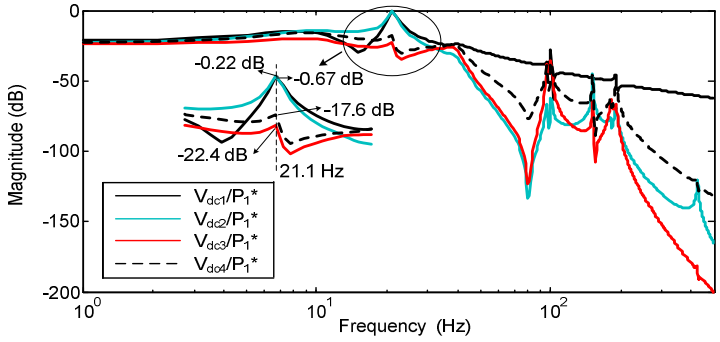


Figure 7.8: Frequency responses of the closed-loop transfer functions between the DC voltages of the four terminals and $P_1^*(s)$, with droop controller at GSC3 (K_{droop}=15), four-terminal model.

The frequency responses of the closed-loop transfer functions between the DC voltages and the power deviation of GSC1 are shown in Figure 7.8. In this closed-loop system, GSC3 uses V-P droop control with a gain of 15, while GSC1 and GSC2 are operating in active power control mode. The dynamic behaviours of DC voltages at different terminals may differ significantly, mainly due to the increase of DC inductances effectively slowing down the propagation of dynamic changes of DC currents. As shown in Figure 7.8, the frequency peaks of the transfer functions associated with GSC1 and GSC2 are much higher than those with GSC3 and GSC4. Larger frequency domain peaks normally indicate poorer transient performance and robustness [1]. This indicates a serious performance issue, that the DC voltages of the terminals in active power control mode can lack damping.

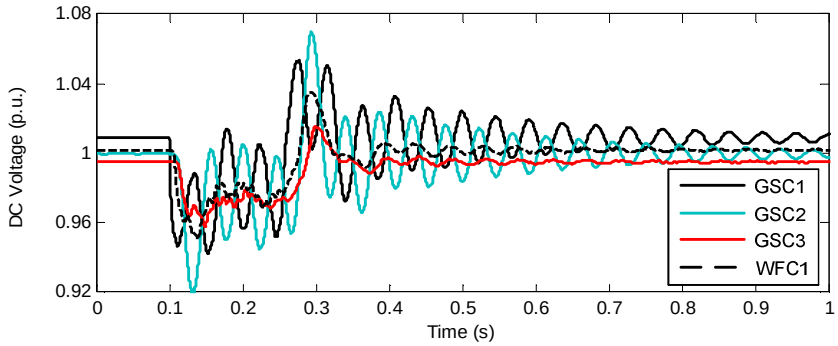


Figure 7.9: Responses of the DC voltages to a 50% AC voltage sag caused by a fault at PCC1 (V-P droop control at GSC3 with K_{droop}=15, four-terminal model)

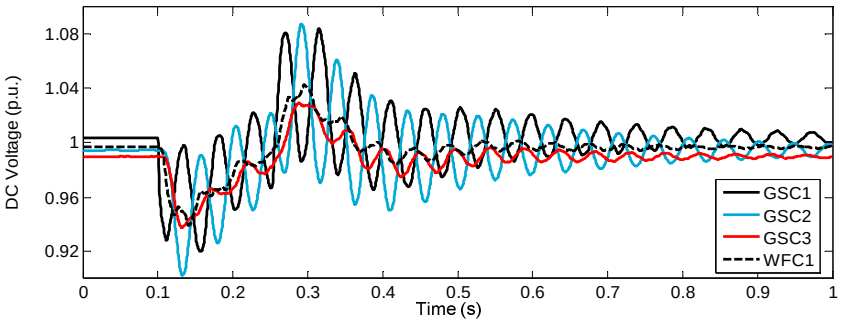


Figure 7.10: Responses of the DC voltages to a 50% AC voltage sag caused by a fault at PCC1 (V-I droop control at GSC3 with R_{droop}=0.05, four-terminal model).

A time domain simulation was performed to verify the frequency-response analysis, with the DC voltage responses to a fault at the PCC bus of GSC1 shown in Figure 7.9. The fault, which results in a 50% sag of the AC voltage at PCC1, occurred at 0.1 s and is cleared after 150 ms. All the EMT simulations are performed on an average-value VSC model using DSPF. In case of the sudden power variation of GSC1, the DC voltages of GSC1 and GSC2 experience severe oscillations. In contrast, the DC voltages of the GSC3 and WFC1 are much better damped, which confirms the frequency responses shown in Figure 7.8. Furthermore, the key oscillation frequency in Figure 7.9 agrees well with frequency domain results. With the V-P droop control of GSC3 replaced by the V-I droop control (R_{droop}=0.05), the DC voltage responses to the same AC fault event are presented in Figure 7.10. The poorly damped voltages of GSC2 and GSC3 in Figure 7.10 demonstrate the generalisation of the transient performance issue and the fact that it cannot be mitigated by employing the V-I droop control.

Please note that, for a more complete analysis of the disturbance rejection performances of the DC voltage control as would be required for an actual implementation, the frequency responses with respect to the transfer functions between the DC voltages and the power variations of all the converters would need to be evaluated.

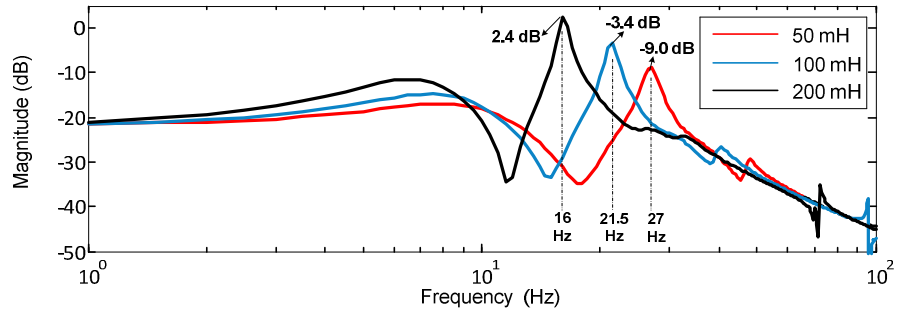


Figure 7.11: Frequency response of the closed-loop transfer function $v_{dc1}(s)/P_1(s)$ for three sizes of DC reactors, with droop controller at GSC3 (K_{droop}=15).

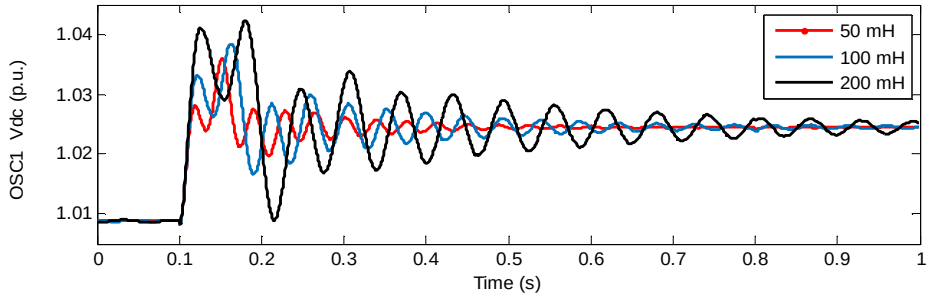


Figure 7.12: Response of the DC voltage of GSC1 to a 0.2 pu step change of the power reference P_1^*, with droop controller at GSC3 (K_{droop}=15).

When GSC3 operates in droop control mode while other GSCs are in power control mode, the impact of the DC reactor size on the frequency response of the transfer function between v_{dc1} and the power deviation of GSC1 is shown in Figure 7.11. For systems with larger DC reactors, the frequency-response peak tends to be larger and located at lower frequency, and this implies that the oscillations of the corresponding DC voltages in case of power imbalance in the DC system are more severe. Similar behaviours can be observed from the transfer functions between DC voltages and power variations of other terminals. The frequency-response analysis is verified by the simulation provided in Figure 7.12, which shows the DC voltage responses to the change of power reference of GSC1. Increasing the DC reactor could significantly deteriorate the dynamic DC voltage performance of the converters that do not participate in DC voltage control. The issue could be alleviated by applying transient DC voltage control to the converters with poorly damped DC voltages, as shown in sections 7.2 and 7.3

7.2 DC Voltage Damping Controller (DCPSS)

A DC damping controller similar to a power system stabiliser (PSS), termed as a DCPSS, is proposed to provide transient damping for DC voltage and improve the stability of the DC network by modifying converter power control using a supplementary stabilising signal. A typical closed-loop MTDC model with such damping controllers is illustrated in Figure 7.13. During transients, the voltages of the DC grid are regulated by the droop control together with the DCPSS to reject the DC power disturbances coming from other terminals. In steady-state, a GSC equipped with the DCPSS behaves like a typical converter in the active power control mode. As the speed deviation is normally used by the PSS in generator systems, the locally measured DC voltage, which is the indicator of power balance in DC system, acts as the input for the DCPSS.

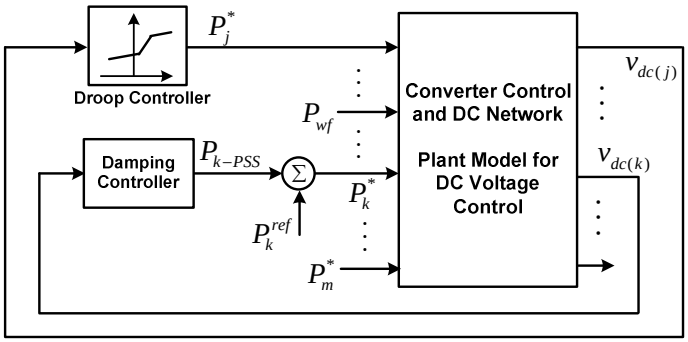


Figure 7.13: Generalised closed-loop model for DC voltage control in MTDC systems with damping controllers.

7.2.1 Location Selection and Control Design

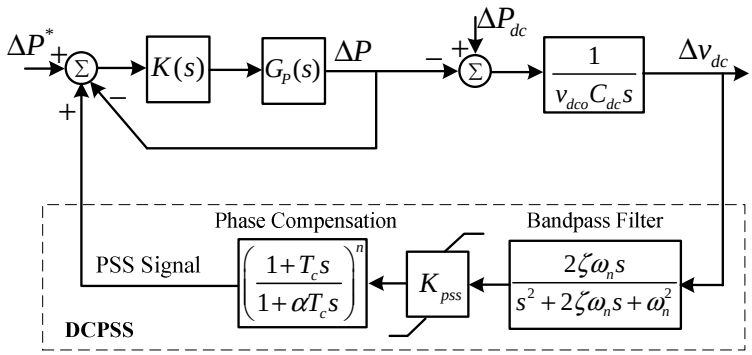


Figure 7.14: DC voltage damping controller (DCPSS) structure.

As shown in Figure 7.14, the DCPSS controller is comprised of a bandpass filter (BPF), a phase compensator, and a stabiliser gain. The bandpass filter should not only allow the key DC voltage oscillations to pass but also prevent the damping controller from reacting to high-frequency noises. The phase compensation is designed to compensate the phase

lag between the PSS output and converter power output, in order to produce a component of DC current roughly in phase with the DC voltage variations.

To demonstrate the generalisation of the modelling method and the analysis approach presented in Section 7.1, a more complex seven-terminal MTDC model, with its schematic diagram shown in Figure 7.15, is built in MATLAB and employed for the studies on the DCPSS. DC reactors of 100 mH per pole are utilised in the model. The system is also built in DSPF to perform time domain simulations.

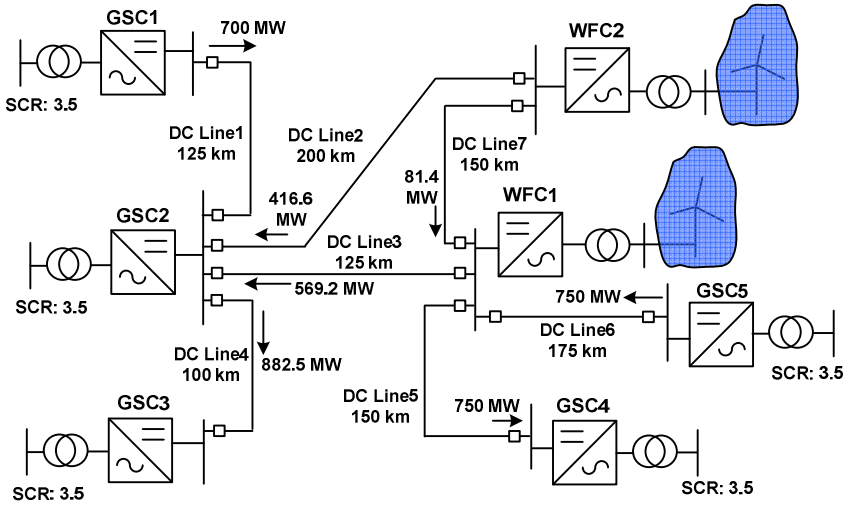


Figure 7.15: Network diagram of the seven-terminal HVDC test model.

Singular value analysis has been used to select the DCPSS location, cross-verified with participation factor analysis. These methods can also be directly applied to identify the appropriate location for DC voltage droop control.

The singular value method, which is the equivalent frequency response for multivariable systems and provides information on the gains between multiple output and input [1], is employed here to assess the gain between the DC voltages of all the terminals and the power reference of a particular VSC terminal. A singular value plot shows the gains between the Euclidean norm of the output vector and that of the input vector in the frequency domain [1]. A GSC with large singular values in the frequency range of interest implies that the DC voltages of the overall system are likely to be sensitive to the power variation of this GSC, and therefore it can be a desirable site for the DCPSS.

When GSC1 and GSC2 operate in droop control mode with droop gains of 7 and 15 respectively, and GSC3-5 operate in active power control mode, the singular values

between the $\boldsymbol{v_{dc}}$ vector and the power set-points of the selected terminals, are shown in Figure 7.16 for this closed-loop model.

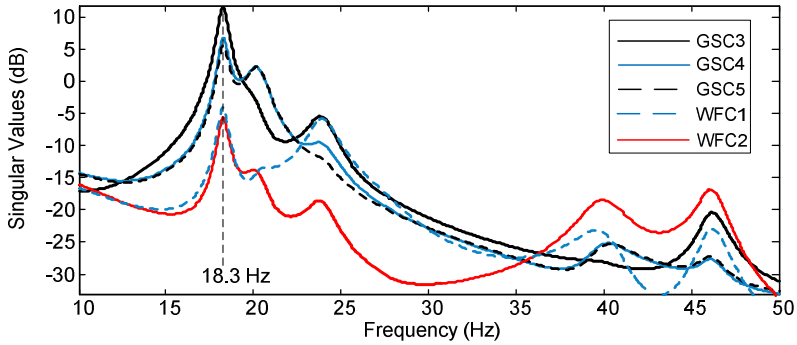


Figure 7.16: Singular value plots of the closed-loop models with all the DC terminal voltages as output and the power of selected terminal as input (GSC1: K_{droop}=7; GSC2: K_{droop}=15).

The singular value of the dynamic model which has all the terminal voltages as output and the power of GSC3 as input has the highest peak. This shows that the GSC3 is suitable for the installation of the DCPSS, because the power of GSC3 generally has a larger impact on the DC voltages around the resonant frequency (18.3 Hz) and this implies that the DC resonance is likely to be more effectively damped by manipulating the power of GSC3. Additionally, Figure 7.16 shows that the two WFCs have a relatively lower impact on the DC voltages at low frequencies, and this indicates a relatively good disturbance rejection capability of the system regarding the wind power changes.

Participation factor analysis has been adopted to identify a suitable location of a PSS in a multi-machine system [161, 162]. In the participation factor method, firstly the dominant oscillating modes need to be identified by computing the eigenvalues. It is observed that the DC terminal voltages are the state variables that generally have large participation factors in the poorly damped eigenvalues, in analogy to the frequency in AC system [162]. Therefore, the participation factors associated with the DC voltages of each converter terminal are calculated for the modes of interest.

Table 7.1: Selected participation factors for the seven-terminal system.

Eigenvalues	GSC1	GSC2	GSC3	GSC4	GSC5
-1.69±*j*115	0.047	0.037	**0.367**	0.101	0.100
-4.07±*j*127	0.005	0.003	0.062	0.229	0.323
-5.35±*j*150	0.068	0.014	0.161	0.051	0.045
-4.84±*j*290	0.030	0.348	0.021	0.003	0.003

For the seven-terminal system, with respect to the DC voltages of the GSCs, the participation factors corresponding to the poorly damped low-frequency modes are

calculated as shown in Table 7.1. GSC3 is selected as the suitable converter station for the installation of DCPSS, due to its significant participation in the most poorly damped mode. The frequency of this mode is identified as identical to the frequency of the singular value peak in Figure 7.16. This participation factor method yields an identical DCPSS location as the singular-value approach.

It should be noted that the candidate terminal which is identified as the suitable site for the DCPSS using the aforementioned methods requires further controllability analysis using root locus or frequency response based on the plant model. The next procedure is the parameterisation for the DCPSS. The frequency range of interest can be identified by observing the frequencies where the singular value peaks occur, such as the 15-25 Hz range shown in Figure 7.16. A wider frequency range is suggested for the bandpass filter as the frequency domain peaks may vary with the operating condition of the system. The phase compensation is preferred to be designed to be effective for a range of frequencies. To compensate the lag of the power control loop, the phase lead can be designed disregarding the control of other terminals. With the BPF and the compensator ready to use, the gain of the DCPSS is selected by performing root locus analysis, to identify the point where sufficient damping is achieved [151].

7.2.2 Test of Damping Controllers

The performance of the proposed damping controllers is evaluated using transient simulations of the seven-terminal model. The configured control modes and droop gains for the GSCs in the two case studies are shown in Table 7.2. In Case 1, GSC1 and GSC2 are selected to operate in droop control mode. In Case 2, another droop controller is added to GSC4 in order to strengthen the DC voltage stability. GSC3 is selected as the site for DCPSS. The parameters of the damping controller are shown in Table 7.3.

Table 7.2: Control modes and droop gains of GSCs for Case 1 and 2.

	GSC1	GSC2	GSC4	GSC5
Case 1	K_{droop}: 7	K_{droop}: 15	P control	P control
Case 2	K_{droop}: 7	K_{droop}: 15	K_{droop}: 10	P control

Table 7.3: DCPSS parameters for two case studies.

Parameter	Case 1	Case 2
Gain K_{pss}	12.1	8.5
T_c	0.0282 s	0.0279 s
α	0.10	0.07
BPF Range	15 – 35 Hz	15 – 35 Hz

For a sudden loss of 250 MW wind generation at WF2 in Case 1, the selected responses of DC voltages and powers are compared in Figure 7.17, with GSC3 operating in three control modes: active power control, V-P droop control and DCPSS control. The transient simulations show the feasibility of the location and design of the DCPSS. The damping of the DC voltage of GSC3 is significantly improved by replacing the conventional active power control with the DCPSS. The performance of the DCPSS is slightly better than the droop control, as shown by the DC voltages of both GSC3 and GSC4 as well as the power variation of GSC3, because the power of GSC3 is utilised more efficiently by the DSPSS to stabilise the poorly damped modes than the droop control. Furthermore, unlike the droop control, the steady-state power of GSC3 remains at the pre-transient level when the DCPSS is adopted.

The damping improvement is however limited for the DC voltage of GSC4, as the oscillations in GSC4 cannot be directly sensed by the damping controller located at GSC3 due to the large electrical distance between the converters. The responses of GSC3 and GSC4 to a fault at the PCC bus of GSC5 are shown in Figure 7.18, with three types of control applied to GSC3. The fault at PCC5, which resulted in a 70% voltage drop, occurred at 0.1 s and was cleared after 200 ms. When GSC3 is in power control mode, and the MTDC stability is maintained by three GSCs out of five, the transient voltage of GSC4 is controlled within an acceptable range however the DC voltage of GSC3 experiences severe oscillations. The comparison of the controllers for GSC3 clearly demonstrates the damping enhancement provided by the DCPSS, as both the amplitude and duration of the DC voltage oscillations are significantly reduced.

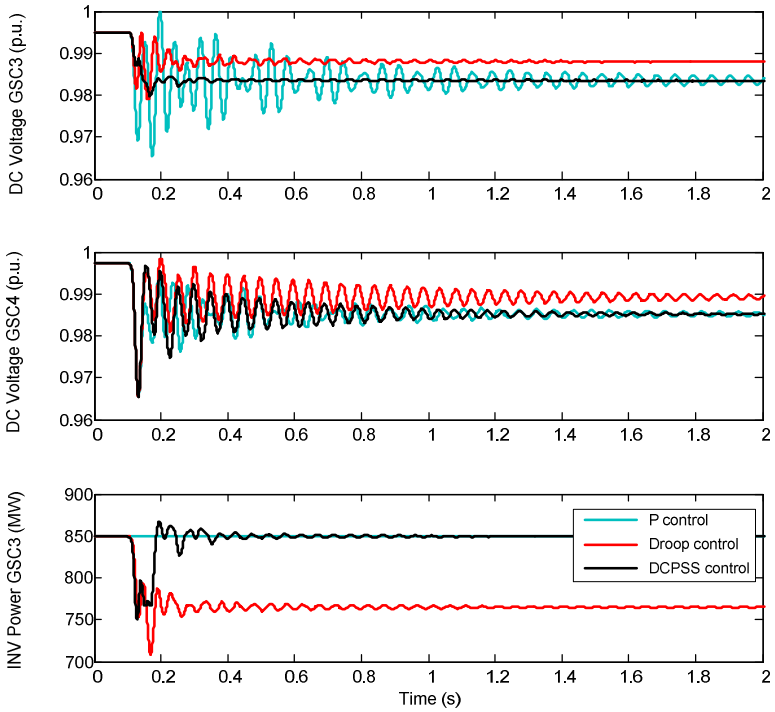


Figure 7.17: Responses of the DC voltage and power of GSC3 and GSC4 to a loss of 250 MW generation in wind farm 2, with three types of control applied to GSC3 (Case 1: GSC1 and GSC2 in droop mode).

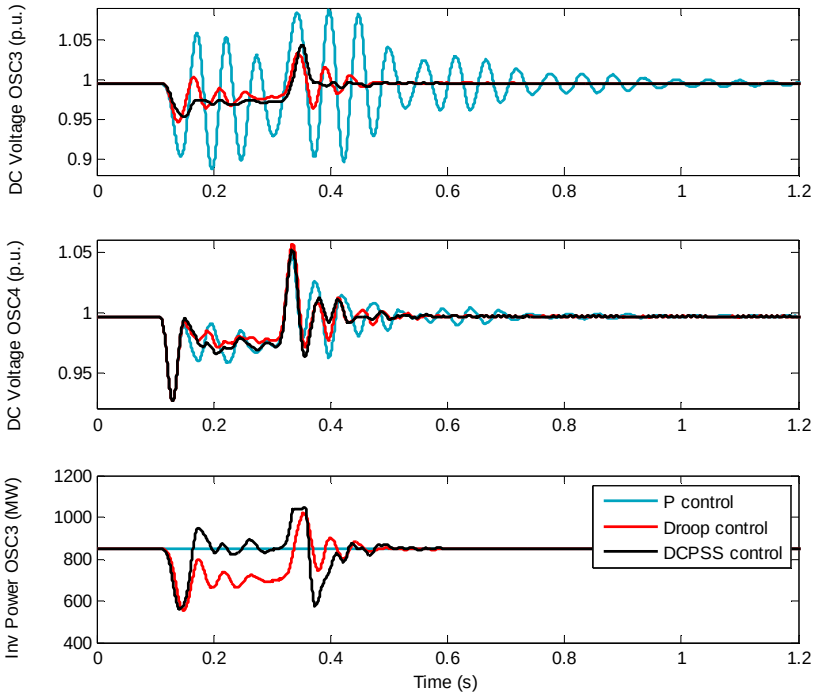


Figure 7.18: Responses of the DC voltage and power of GSC3 and GSC4 to a fault occurring at PCC5, with three types of control applied to GSC3 (Case 2: GSC1, GSC2 and GSC4 in droop control).

Generally, the damping of the system can also be improved by utilising more converters for droop control, as shown by Figure 7.17 and Figure 7.18. However, it is worth noting that merely increasing the number of DC voltage controllers does not necessarily

improve the damping performance as the location and design of these controllers also matter.

The use of the DCPSS has several key advantages over incorporating more terminals in droop control. Firstly, the power transfer for the converter with DCPSS control is only perturbed during DC voltage transients. Therefore, this feature facilitates the power flow scheduling and imposes an reduced stress on the connected AC system. Furthermore, with appropriate location and the phase compensation, the poorly damped poles are more effectively targeted by the DCPSS than droop control, and, therefore, better damping performance can be achieved. Like droop control, DCPSS controllers can also be employed by multiple converters simultaneously.

Table 7.4: Low-frequency modes with and without DCPSS (Case 1).

Without DCPSS		With DCPSS	
Frequency (Hz)	Damping ratio ζ	Frequency (Hz)	Damping ratio ζ
18.31	0.015	22.61	0.117
23.89	0.036	45.22	0.126
46.34	0.017	52.23	0.087

Table 7.5: Low-frequency modes with and without DCPSS (Case 2).

Without DCPSS		With DCPSS	
Frequency (Hz)	Damping ratio ζ	Frequency (Hz)	Damping ratio ζ
18.63	0.041	13.03	0.279
23.09	0.049	22.13	0.125
46.34	0.019	47.29	0.043

The enhancement of the damping on the critical modes is also demonstrated by the analytical results shown in Table 7.4 and Table 7.5 for the application of DCPSS in Case 1 and Case 2, respectively. The oscillating frequency and the damping ratio ζ for the poorly damped modes are calculated for the closed-loop MIMO model with and without the DCPSS in GSC3. As the DCPSS is designed mainly targeting the low-frequency modes with the poorest damping, the damping of such modes is improved most dramatically. Furthermore, the DCPSS also has a very positive impact on the damping for the modes of a range of frequencies. In fact, the DCPSS can not only enhance the dynamic performance but also strengthen the DC system stability. This eigenvalue analysis agrees well with the time domain simulations.

7.3 Active Stabilising Control

The DCPSS is very effective in terms of the enhancement of the dynamic behaviour of MTDC systems for a given system operating point. It is however difficult to ensure a satisfactory performance of the DCPSS across a wide range of operating conditions, as the DC system dynamics are sensitive to the power flow of the DC network. Supplementary control is required for MTDC system to tackle the robustness issue caused by the nonlinearity between converter powers and voltages, particularly for systems with large DC reactors.

Active stabilising control techniques, which have been adopted for the DC link control of practical inverter drive systems [153, 154, 163, 164], are investigated in this section for their application in MTDC systems to counteract the negative admittance effect caused by constant power control, and inherently to improve the robustness and stability of DC voltage control. In [153, 154], the DC link of a drive system is stabilised by dynamically varying the active power or current reference of the inverter using a supplementary signal that contains the information of the DC voltage dynamics.

7.3.1 Two Stabilising Controllers

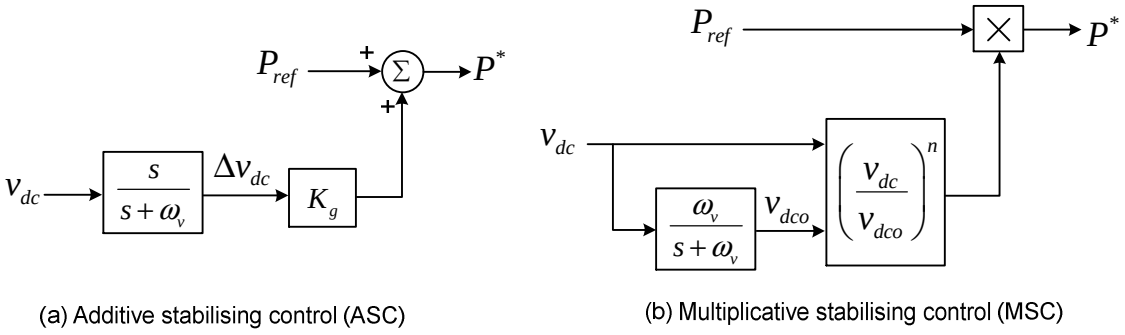


Figure 7.19: Two active DC link stabilising control structures.

In Figure 7.19, two types of active stabilising controllers are shown based upon concepts from drive systems. Additive stabilising control (ASC) [153, 163, 164] and multiplicative stabilising control (MSC) [154, 164], are proposed here to apply to VSC-HVDC, to mitigate the negative admittance issue which is revealed in Section 6.1.3. The key idea is to alter the low-frequency input admittance of the converter in constant power control.

For the ASC, the steady-state active power reference P_{ref} is modified in proportion to the oscillating component of the DC voltage, as shown in (7.4), where the stabilising gain K_g

determines the additional damping provided by this control. Please note that in this chapter the power is defined to be positive for inverters.

$$P^* = P_{ref} + K_g\left(v_{dc} - v_{dco}\right) \quad \Rightarrow \quad \Delta P^* = \Delta P_{ref} + K_g \Delta v_{dc} \tag{7.4}$$

$$P = \frac{\omega_B^P}{s + \omega_B^P} P^* \tag{7.5}$$

With the converter power loss ignored, by modelling the active power control loop using a simplified representation as shown in (7.5), the DC current absorbed by the converter in ASC control can be linearised into:

$$\Delta i_{dc} = \frac{\Delta P}{v_{dco}} - \frac{P_o}{v_{dco}^2}\Delta v_{dc} = \frac{\omega_B^P}{s + \omega_B^P} \cdot \frac{1}{v_{dco}} \cdot \Delta P_{ref} + \left(\frac{\omega_B^P}{s + \omega_B^P} \cdot \frac{K_g}{v_{dco}} - \frac{P_o}{v_{dco}^2} \right) \cdot \Delta v_{dc} . \tag{7.6}$$

The input admittance of the converter can then be derived as shown in (7.7), in comparison to the admittance of $-P_o/v_{dco}^2$ for the constant power control.

$$Y = \frac{\omega_B^P}{s + \omega_B^P} \cdot \frac{K_g}{v_{dco}} - \frac{P_o}{v_{dco}^2} \tag{7.7}$$

The admittance is clearly dependent on the power loop bandwidth. Provided with ideal active power control, the natural damping can be restored by selecting $K_g = P_o/v_{dco}$:

$$Y_{ideal} = \frac{K_g}{v_{dco}} - \frac{P_o}{v_{dco}^2} . \tag{7.8}$$

With the dynamics of the high-pass filter in Figure 7.19 (a) considered, the equivalent input admittance for the ASC can be further derived as:

$$Y = \frac{\omega_B^P s}{s^2 + \left(\omega_B^P + \omega_v\right)s + \omega_B^P \omega_v} \cdot \frac{K_g}{v_{dco}} - \frac{P_o}{v_{dco}^2} \tag{7.9}$$

where the filtering bandwidth ω_v should be sufficiently low to allow the key oscillating frequencies to go through, but not so excessively low as to affect the steady-state power transfer.

For MSC, the original power demand is dynamically modified by multiplying the exponential component of the DC voltage with the exponent $n \geq 1$. The linearised form of the active power reference for MSC can be derived as:

$$P^* = P_{ref}\left(\frac{v_{dc}}{v_{dco}}\right)^n \quad \Rightarrow \quad \Delta P^* = \Delta P_{ref} + n\frac{P_o}{v_{dco}}\Delta v_{dc} \tag{7.10}$$

which is similar to the representation for the ASC shown in (7.4). Considering the simplified power loop dynamics shown in (7.5), the DC current injected into the converter in MSC mode can then be linearised into:

$$\Delta i_{dc} = \frac{\Delta P}{v_{dco}} - \frac{P_o}{v_{dco}^2}\Delta v_{dc} = \frac{\omega_B^P}{s+\omega_B^P}\cdot\frac{1}{v_{dco}}\cdot\Delta P_{ref} + \left(\frac{\omega_B^P}{s+\omega_B^P}n-1\right)\cdot\frac{P_o}{v_{dco}^2}\cdot\Delta v_{dc}. \qquad (7.11)$$

Subsequently, the equivalent input admittance for the converter is modified by MSC into:

$$Y = \left(\frac{\omega_B^P}{s+\omega_B^P}n-1\right)\cdot\frac{P_o}{v_{dco}^2}, \quad Y_{ideal} = (n-1)\cdot\frac{P_o}{v_{dco}^2}. \qquad (7.12)$$

The selection n=1 implies that the converter could provide zero input admittance [154], if the dynamics of the active power control are ignored. This is, however, not usually the case.

The comparison between (7.8) and (7.12) shows that, unlike ASC where the additional admittance is determined by the gain K_g, the equivalent admittance for MSC is largely affected by the power OP. This implies that, if a fixed exponent n is used, MSC may deteriorate the damping of the DC system if the direction of the power transfer is altered.

The analysis suggests that the equivalent input admittance of the converter is still dependent on the power OP with the ASC or MSC control. The ASC/MSC parameters shown in (7.13), which are dependent on the power OP, are recommended if robustness is strictly required. This control is termed as adaptive stabilising control here. Y_{des} is the desired input admittance and increasing Y_{des} usually results in more damped DC voltages.

$$K_g = Y_{des}v_{dco} + \frac{P_o}{v_{dco}}, \quad n = \frac{v_{dco}^2}{P_o}Y_{des} + 1 \qquad (7.13)$$

7.3.2 Analytical Results

This section aims to analytically demonstrate the impact of the active stabilising controllers on the stability and robustness improvement of MTDC systems.

For the four-terminal model illustrated in Figure 7.3, the trajectories of the dominant poles and zeros of the plant model $v_{dc3}(s)/P_3^*(s)$ of DC voltage control using GSC3 are shown in Figure 7.20 for a range of power flow scenarios, in which the powers of GSC1 and GSC3 are varied while the powers of GSC2 and WFC are kept constant. This study has been performed for four control scenarios, in which constant power control or different active stabilising control is applied to GSC1 and GSC2.

The results shown in Figure 7.20 clearly demonstrate the effectiveness of the ASC and MSC designs in improving the controllability and robustness of the DC system. The open-loop zeros have been well restricted within the left-half plane by the active stabilising control. This could significantly improve the controllability of the system, contrary to the constant power scenario, where the RHP poles and zeros are close to each other. The dominant poles and zeros shown in Figure 7.20 (b) and (c) are, however, still sensitive to the variation of the power flow. This robustness issue can be alleviated by employing of the ASC or MSC with adaptive control parameters, as shown in Figure 7.20(d).

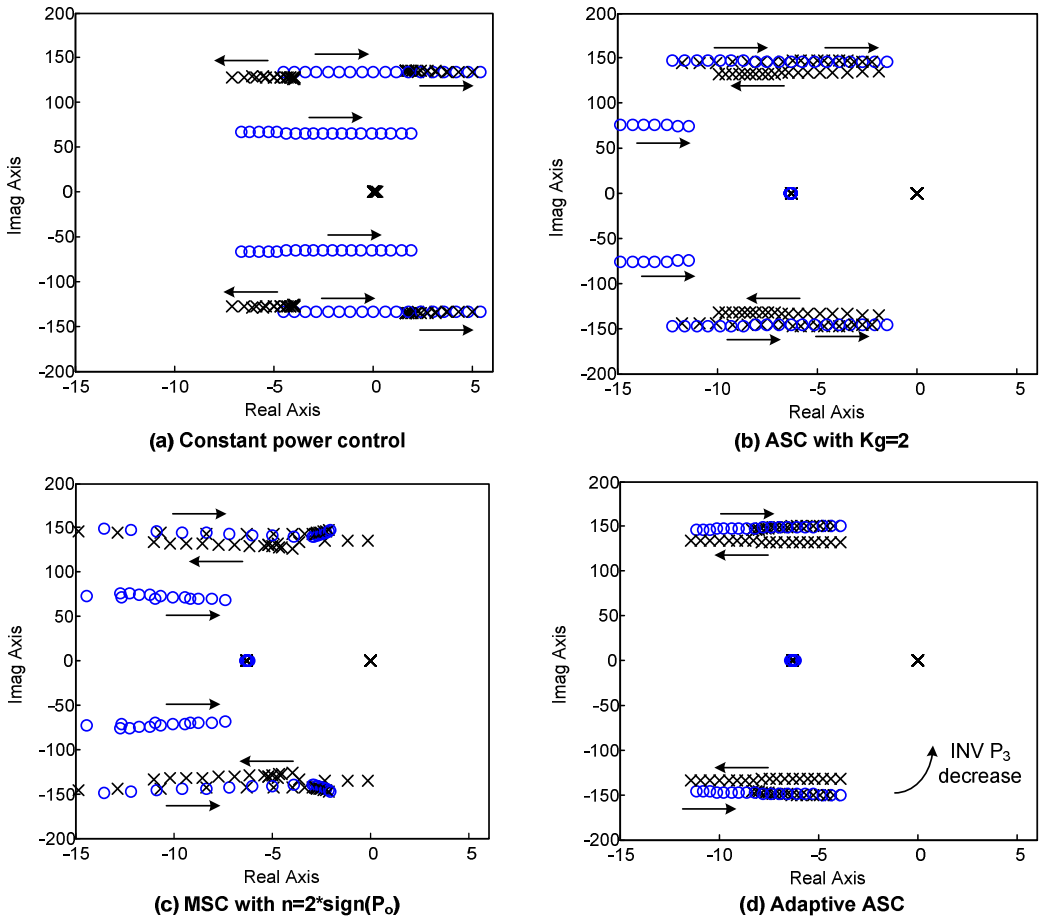


Figure 7.20: Trajectories of the dominant poles and zeros of the open-loop transfer function $v_{dc3}(s)/P_3^*(s)$ as GSC3's inverting power varies from 0.85 pu (INV) to -0.45 pu (REC), seven-terminal model (for the MSC case, sign(P_o)=1 if P_o>0, while sign(P_o)=-1 if P_o<0).

Based upon the mathematical model of the seven-terminal test system, the singular value plots of the closed-loop MIMO system, with the power reference of the respective terminal as input and all the DC terminal voltages as output, are depicted in Figure 7.21 for four control scenarios, to assess the impact of the power loop bandwidth on the performance of the ASC. The ASC is located at GSC3 and GSC5. The low-frequency

peaks of the closed-loop system are significantly reduced by employing the ASC. This implies a much more damped performance of the DC voltages in response to the DC power imbalance. This dynamic performance can be further improved by choosing a higher closed-loop bandwidth for the active power control. However, this action may result in high-gain instability and adverse interactions with weak AC systems.

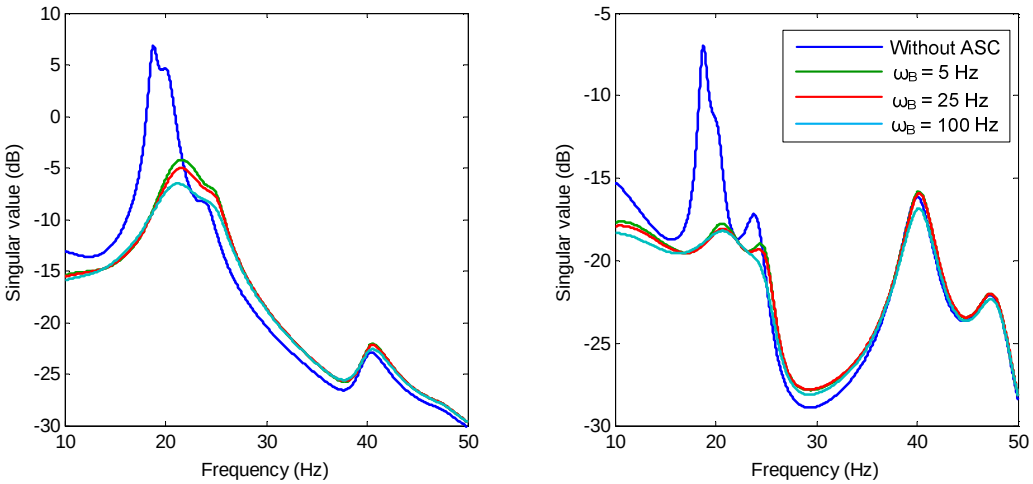


Figure 7.21: Singular value plots of the closed-loop models with all the DC terminal voltages as output and the power of selected terminal as input (seven-terminal model, ASC with K_g=2 for GSC3 and GSC5, GSC1 K_{droop}=7, GSC2 K_{droop}=15, GSC4 in constant power control).

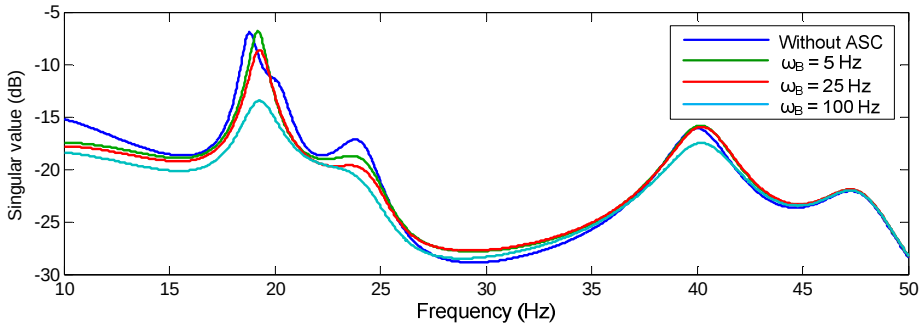


Figure 7.22: Singular value plots of the closed-loop models with all the DC terminal voltages as output and the power of WFC1 as input (seven-terminal model, ASC with K_g=2 for GSC4 and GSC5, GSC1 K_{droop}=7, GSC2 K_{droop}=15, GSC4 in constant power control).

Similar studies have been performed when the ASC control is applied to GSC4 and GSC5 instead of GSC3 and GSC5, with the singular value plot between the seven DC voltages and the power of WFC1 presented in Figure 7.22. In comparison to the previous case shown in Figure 7.21, the ASC control is much less effective in terms of reducing the low-frequency peak, unless an excessively high-bandwidth power control is utilised. This is mainly because no stabilising control is used to target at the negative input admittance caused by the inverter GSC3. Like the DCPSS, the performance of the ASC or MSC is highly dependent on the location of the controller.

With MSC applied to GSC3, GSC4 and GSC5 of the seven-terminal system, the singular value plots between all the DC terminal voltages and the powers of the selected terminals are presented in Figure 7.23, along with the frequency responses regarding the utilisation of the power for the converters in MSC mode. Please note that the exponent is set to be dependent on the sign of the power flow direction to avoid damping deterioration for rectifier operation.

The disturbance rejection capability for the DC voltage control at low resonant frequencies can be improved by increasing the gains of the MSC controllers, as demonstrated by the singular values in Figure 7.23. Realistically, a high-gain MSC or ASC is not necessary as a relatively low gain is usually sufficient counteract the negative admittance and enhance the DC voltage performance efficiently. In response to the DC power perturbations, larger utilisation of the converter power across the wide low-frequency range is demanded by the stabilising control with larger gains, as shown in Figure 7.23 (c) and (d). Increasing the ASC gain K_g has a similar impact on the frequency responses to the MSC scenarios shown in Figure 7.23.

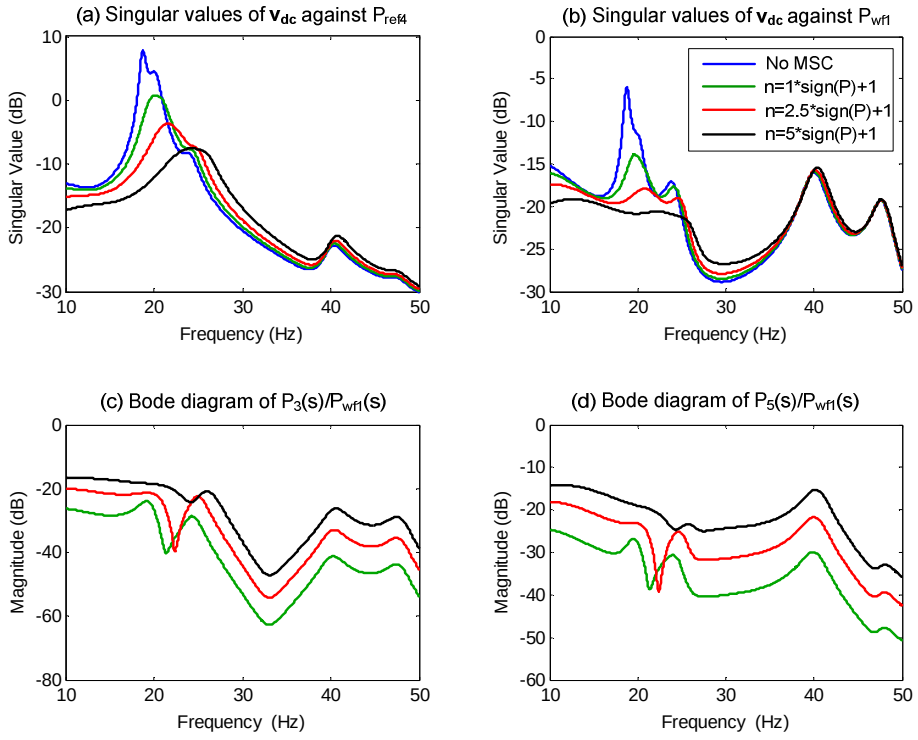


Figure 7.23: Closed-loop frequency responses for different settings of MSC gains (seven-terminal model, GSC1: K_{droop}=7, GSC2: K_{droop}=15; MSC with identical gains applied to GSC3, GSC4 and GSC5).

7.3.3 Simulation Results

In order to evaluate the impact of the active damping control on the robustness of the MTDC system with respect to the variation of the power flow, the simulations of a sudden increase of 100 MW wind farm power of the four-terminal model have been compared in Figure 7.24. The power flow scenarios under investigation are shown in Table 7.6. For the simulations shown in Figure 7.24(a), constant quadratic DC voltage control is applied to GSC1, while constant power control is utilised by GSC2 and GSC3. The simulations shown in Figure 7.24(b) are obtained with the adaptive ASC applied to GSC2 and GSC3.

The simulations shown in Figure 7.24(a) clearly demonstrate that, when constant power control is applied to GSC2 and GSC3, the DC system dynamics and stability are significantly affected by the DC network power flow. Such a high degree of sensitivity to the system power flow may not be acceptable for realistic MTDC networks. The system robustness can be significantly improved by configuring GSC2 and GSC3 into the adaptive ASC mode, as shown in Figure 7.24(b), where the impact of the power flow variation on the dynamic response of the DC voltages and the GSC1's power is substantially reduced.

Table 7.6: Inverting power of the converters in MW for the three power flow scenarios.

INV PCC Power (MW)	Scenario 1	Scenario 2	Scenario 3
GSC1	-650	650	250
GSC2	550	300	-200
GSC3	580.4	-465	864
WFC	-499	-498	-931

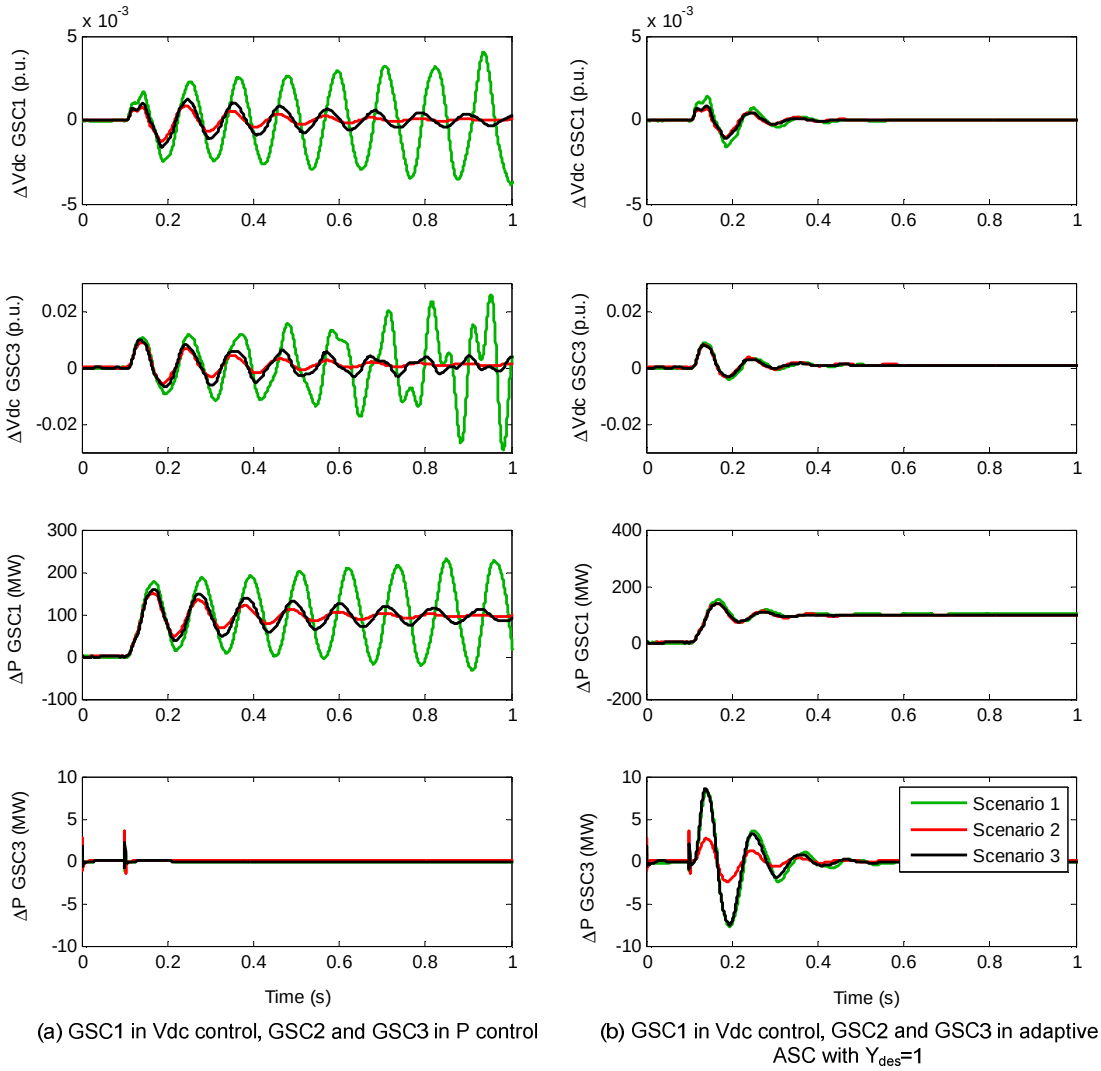


Figure 7.24: Transient responses of GSC1 and GSC3 to the sudden increase of 100 MW wind farm power for each scenario (four-terminal model).

The seven-terminal MTDC model shown in Figure 7.15 was employed to produce the simulations shown in Figure 7.25, Figure 7.26 and Figure 7.27, where V-P or V-I droop control was adopted by GSC1 and GSC2, while constant power control and various active stabilising control were utilised by GSC3, GSC4 and GSC5.

The responses of DC voltages and converter powers for GSC2, GSC3 and GSC4 to a sudden loss of 250 MW generation in wind farm 2 are presented in Figure 7.25 to demonstrate the impact of the ASC gain on the dynamic performance of the system. Conventional active power control cannot provide damping support to the DC voltage, and this leads to severe voltage oscillations. The transient performance is significantly improved by employing the stabilising control. Typically, increasing the ASC gain improves the damping of DC voltages, since a larger amount of converter power is used for stabilising the DC voltage.

Similar simulation studies were conducted for the stabilising control based upon MSC, with the results shown in Figure 7.26. The DC system becomes more stable as the exponent *n* increases, which verifies the frequency responses shown in Figure 7.23. The feedforward (FF) active power control loop, which acts as a much faster actuator than the feedback control, improves the damping performance of the active stabilising control, which verifies the frequency domain analysis shown in Figure 7.21.

To demonstrate the compatibility of the stabilising control, the ASC and MSC were applied to the seven-terminal model, where the V-I droop instead of the V-P droop was implemented to GSC1 and GSC2. The comparative results of an AC fault simulation are illustrated in Figure 7.27, with three types of control applied to GSC3, GSC4 and GSC5. Like the V-P droop, the V-I droop applied to GSC1 and GSC2 cannot provide sufficient damping for the overall DC system equipped with the DC reactors. The active stabilising controls essentially improve the controllability of MTDC voltage control; and therefore, their impact on damping enhancement is applicable to most of the existing DC voltage controller structures.

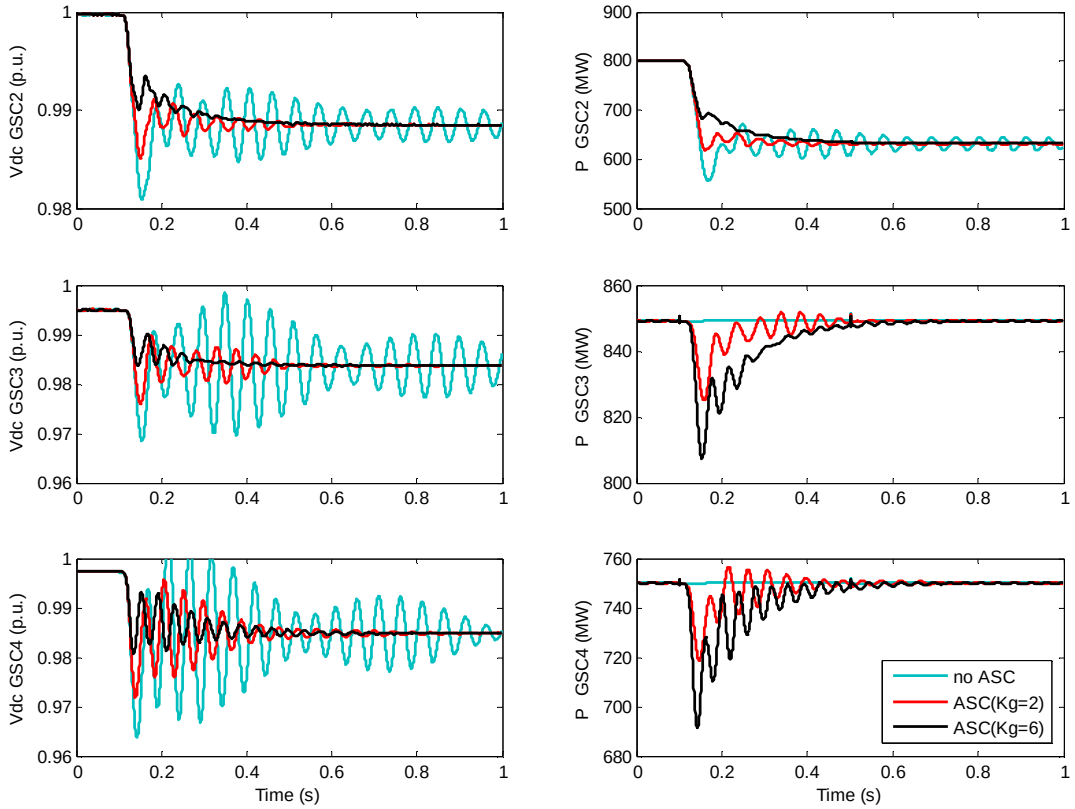


Figure 7.25: Transient responses of GSC2, GSC3 and GSC4 to a loss of 250 MW generation in wind farm 2, with three types of control applied to GSC3, GSC4 and GSC5 (GSC1 K_{droop}=7, GSC2 K_{droop}=15).

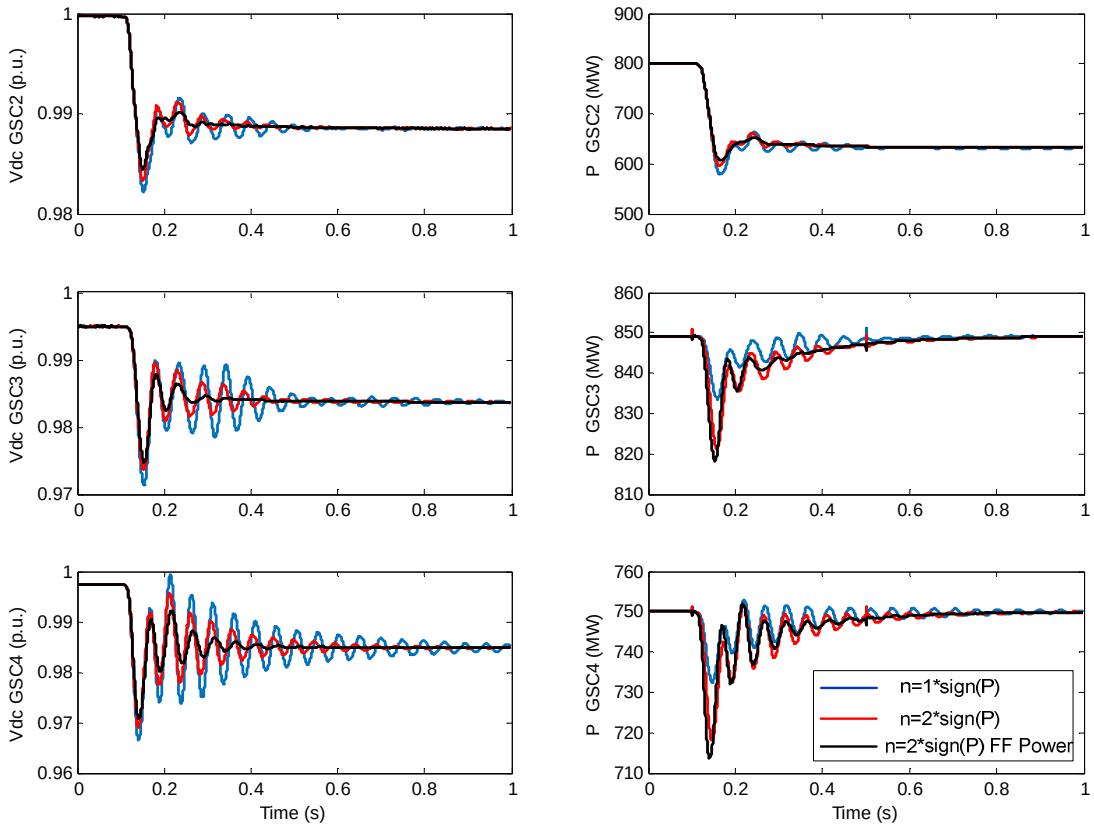


Figure 7.26: Transient responses of GSC2, GSC3 and GSC4 to a loss of 250 MW generation in wind farm 2, with three types of MSC control applied to GSC3, GSC4 and GSC5 (GSC1 K_{droop}=7, GSC2 K_{droop}=15).

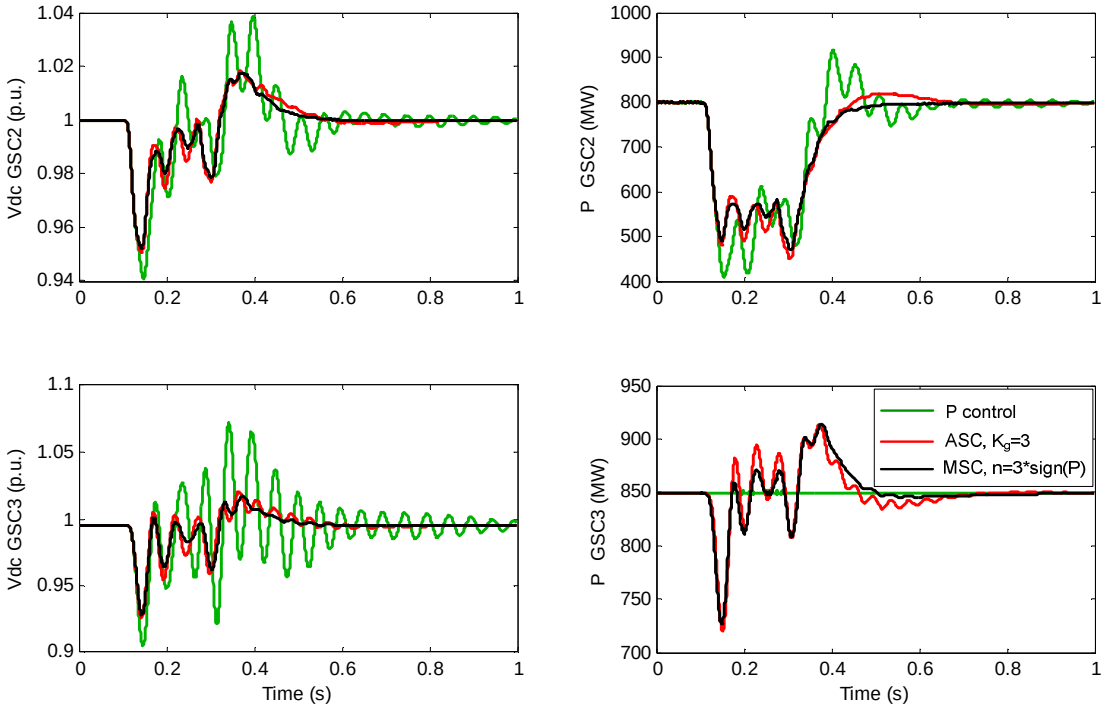


Figure 7.27: Transient responses to the AC fault causing 50% voltage sag at the PCC5, with three control settings applied to GSC3, GSC4 and GSC5, and V-I droop used for GSC1 (R_{droop}=4%) and GSC2 (R_{droop}=2.5%).

7.4 Chapter Summary

Based on the four-terminal analytical model, pole-zero and frequency-response analyses have been adopted to identify the fundamental stability and performance issues related to the DC reactors. The DC voltage controllability can be significantly degraded by the use of DC reactors. This component also has a detrimental effect on the robustness of MTDC dynamics with respect to power flow variation. For a MTDC system where the locations of droop controllers are not carefully selected, the use of a large DC reactor can result in undesired oscillations of DC voltages and even instability.

The DCPSS controller has been proposed to enhance the dynamic performance of the DC voltage control in a DC grid. Two methods have been developed for the selection of the DCPSS location. The transient simulations and eigenvalue analysis for the seven-terminal HVDC model have demonstrated the excellent performance of the damping controller. However, the DCPSS may not be sufficiently robust and may not be helpful for the system stability if large power flow variation occurs.

Two active stabilising controllers have been applied to MTDC systems to replace the constant power control. It is particularly useful if such controllers are applied to inverters to avoid a negative admittance issue at low frequencies and, therefore, to improve controllability and robustness with respect to DC voltage control. The dynamic characteristics of the ASC and MSC are similar to of the V-P droop control; however, typically, a much lower gain is required by the active stabilising controls.

In order to achieve better stability and robustness, this chapter suggests reducing the number of converters in active power control mode, and applying DCPSS control and active stabilising control to more converters, with carefully selected locations for these supplementary controllers.

Chapter 8 Conclusion and Future Work

8.1 Conclusion

This thesis focuses on the control, dynamics and analysis of VSC-based MTDC systems. The main contributions of the thesis can be summarised into the following four aspects:

8.1.1 Modelling and Control of MTDC

Modelling and control methodologies of MTDC systems have been discussed in detail in this thesis, with a focus on the modelling of the hierarchical control of grid-side VSC-HVDC. Dominant dynamics of the main converter inner and outer control loops have been derived. A number of tuning methods have been applied to these systems to achieve reasonable dynamic performance and stability, with the critical trade-offs of the designs described. Simplified modelling of the wind farm and offshore VSC control has been presented, with a degree of basic fault ride-through functionality.

The main candidate strategies for the DC voltage control of MTDC have been examined. Steady-State and dynamic modelling of various voltage margin and voltage droop characteristics have been presented. Key advantages, weaknesses and dynamic features of these control strategies have been identified. With appropriate designs, both voltage margin and voltage droop control could provide a good degree of reliability and stability for MTDC system with a small number of converters. As the scale of the DC system grows, it becomes more difficult to maintain the DC voltage stability using one converter at a time. Hence, droop control is recommended for large DC grids due to its superior scalability, reliability and power sharing capability.

8.1.2 Steady-State Analysis of MTDC

Incorporating various DC voltage control characteristics can significantly increase the complexity of power flow calculations in a MTDC system, especially when the characteristics have multiple control stages. To solve this issue, a new generalised DC power flow approach that contains two iteration layers has been developed and integrated into a conventional AC power flow. This algorithm has been applied to a series of test scenarios and demonstrated satisfactory performance. In addition to this, the analytical representations that define the VSC PQ capability have been derived and the impact

factors including AC system strength, maximum current, DC voltage and transformer impedance have been identified.

Analytical studies based upon linearised equations describing power flow and V-I/V-P droop control have been performed to investigate how the DC system operating point is affected by power disturbances. An equivalent circuit model has been developed according to the steady-state behaviours of droop control, and it has been used to intuitively assess the impact of the droop setting on the power sharing in DC systems. It has been shown that the post-disturbance voltage and power deviations can be significantly affected by the topology and impedance of the DC network if high-gain droop control is employed.

Additionally, a generic DC grid control hierarchy, consisting of the tertiary dispatch control, secondary control and local converter control, has also been briefly described. Two methods have been developed to achieve the desired power flow by varying the droop references.

8.1.3 Stability Studies of Active Power and DC Voltage Control

Detailed mathematical VSC-HVDC models and frequency domain tools have been employed to assess the stability, performance and robustness of active power and DC voltage control.

The limitations imposed by a weak AC system, rectifier operation, a low PCC bus voltage and a high-bandwidth current control on the stability of two types of active power controllers have been identified and evaluated. The interactions between the active power control and typical V-P droop control have also been analysed. For rectifiers connected to a weak AC system, a high-gain droop control and feedforward active power control could imply poor robustness and stability. Generally, the feedback active power is recommended for better stability. However, with careful design, the feedforward approach may be employed to achieve a fast control of active power, provided that the VSC is connected to a relatively strong system and is usually operating as an inverter.

Utilising a detailed analytical VSC model and three types of DC system models, the stability limitations of DC voltage control, particularly V-P droop control, have been identified. There are fundamental issues of employing vector current control for the control of DC voltage if the converter is connected to a very weak AC system.

Furthermore, a high-impedance AC system also imposes an upper bound of the DC voltage loop bandwidth, especially for converters in rectifier operation. Applying constant power control to inverters results in negative input admittance, which could lead to instability of DC systems with large inductances. For typical V-P droop control, high-bandwidth power control is beneficial for fast disturbance rejection performance, while low-bandwidth power control is preferred for stability when there are RHP zeros resulting from AC and DC systems. A droop controller with transient compensation has been developed to improve the robust stability of DC voltage control without compromising steady-state performance.

Stability of V-I droop control has also been analysed. The limitations imposed by a weak AC system and the power operating point also restrict the stability of this controller structure. Large droop constants and high-bandwidth DC voltage control are not recommended for V-I droop. If the feedforward DC power is to be used as part of the DC voltage controller for disturbance cancellation, a carefully designed low-pass filter is required to avoid adverse interactions with high-impedance AC and high-inductance DC systems at high frequencies.

The stability analysis leads to recommendations for the configuration of active power and DC voltage droop control.

8.1.4 MTDC Stability Analysis and Auxiliary Controllers

A generalised and systematic procedure has been developed for the mathematical modelling of MTDC systems in order to perform open-loop and closed-loop analysis of multivariable problems, especially for the control of DC voltage in DC grids. The overall analytical MTDC model is formulated by mathematically interconnecting a number of sub-system models for GSCs, WFCs and the DC network. Participation factor analysis has been applied to identify the state variables that strongly affect the eigenvalues of interest. The dominant modes in a MTDC system are usually determined by a number of state variables of different converter systems. Sensitivity studies based on modal analysis have revealed the impacts of a series of system and controller parameters on MTDC stability and dynamics.

A large DC reactor is required by a DC breaker system to limit the rise of DC fault current. Frequency-response and root-locus analyses have been employed to identify the fundamental stability and performance issues associated with this component. The use of

large DC reactors could significantly degrade the DC voltage controllability as there could be RHP poles and zeros located close to each other. This component could also deteriorate the MTDC robustness with respect to power flow variations and this imposes a serious challenge for control design. The large frequency domain peaks at low frequencies caused by the use of large reactors can result in poorly damped DC voltage oscillations and require supplementary damping control.

The DCPSS controller has been proposed to tackle the transient performance issues caused by the utilisation of large DC reactors. The location of such a controller can significantly affect its performance and hence two methods have been developed for the selection of the location. Satisfactory performance of this new controller has been demonstrated through a seven-terminal MTDC model. However this controller may not be sufficiently robust to provide damping support in case of large power flow changes.

Two active stabilising controllers have been developed to counteract the negative input admittance of constant power control of inverters and, therefore, improve the robustness and stability of the DC system. The performance of such controllers has been verified by singular value analysis and time domain simulations.

8.2 Future Work

Within the context of MTDC control, based upon the work provided in this thesis, the recommended future work could be categorised into the following four aspects:

8.2.1 More Realistic MTDC Models

The time domain simulations presented in this thesis were produced using MTDC models built in DSPF. The functionality of DSPF in terms of DC system modelling has limited the scope of this research. More EMT-focused simulation packages such as PSCAD/EMTDC are recommended for further research on detailed transient studies of DC systems.

Detailed equivalent MMC model, which efficiently represents the sub-modules, would provide more convincing simulations of DC voltage transients, in comparison to the AVM model employed in this research. This would however increase the simulation duration. It would also be useful to improve the existing AVM model for a good balance between simulation time and accuracy. Furthermore, a frequency-dependent DC cable

model, which captures the travelling wave effect, would provide more accurate simulation results than the lumped model used in DSPF, particularly for fast DC transient studies. Additionally, the transformer model may also need to be improved, for instance, by incorporating saturation characteristics to provide more realistic simulation results.

In this thesis, simplified AC system models were employed, and the AC system strength is determined by the network impedance. The impact of inertia was not considered. A meshed generator-based AC system model for simulations would be recommended to perform more realistic AC/DC interaction studies, such as the interaction between the frequency or voltage support provided by VSC and the droop control. For LCC-HVDC systems, low-order harmonic instability issues, which are caused by the interactions AC/DC network and HVDC control at resonant frequencies, attracted extensive research from both industries and academia in 1980s and 1990s [142, 165, 166]. However, similar studies have not conducted in previous literature for multi-terminal VSC-HVDC systems. It would be very useful to analyse the potential AC system resonance issues for VSC-HVDC systems, particularly when there VSC and LCC HVDC links connected close to each other. An AC system model with a more realistic impedance representation would be required to perform such studies. Furthermore, a more detailed wind farm model would be desirable for detailed studies of the WFC control.

8.2.2 Coordinated MTDC Control

Droop control is likely to be employed as the primary control of MTDC systems. The secondary control, which is also referred to as the HVDC grid controller or coordinated system control, is required to achieve the desired system operating point after perturbations by providing new references to the converter local control. This high-level control, which remains unclear, was only briefly discussed in this thesis, and substantially more further work is needed to provide an in-depth understanding. Telecommunication links are required by this control stage, and therefore the impact of the latency and reliability of the communication needs to be analysed in detail.

Like AGC in an AC system, the secondary control in a large DC grid should be able to adjust the converter voltages and powers automatically after disturbances to ensure the scheduled power flow between control areas. Furthermore, the DC grid stability should be well maintained when the droop references are updated by the secondary control. A more complex structure than AGC could be required for this DC coordination control,

since there is no global DC voltage in the DC grid. Advanced controller designs, such as model predictive control (MPC), might be helpful for secondary DC grid control.

8.2.3 Assessment of Droop Control Implementations

The importance of dynamic implementation of droop control appears to be neglected by a majority of the previous literature on MTDC control, and has not received enough attention to date. Different droop control implementations can have very similar or identical steady-state behaviours, and, on the other hand, they may have significantly different transient performance. It would be very useful to conduct a comprehensive assessment study for the leading droop implementations, in order to identify the limitations and advantages of each implementation. This stability and robustness assessment would require multiple open-loop and closed-loop analytical models, as these implementations effectively employ different control structures. Such comparative studies could be helpful to form recommendations for the field of MTDC control.

Another important aspect, worthy of further detailed study is the design and parameterisation of the droop controller, considering the limitations imposed by the system plant and controller structure. Coordinated design for all the converters in droop control may provide a superior overall transient performance. However, in this case, the control will have to be reconfigured if there is any change of the DC grid structure. Independent design is easier to implement in practice. However, it is difficult to take into account the interactive dynamics between the converters. Another difficulty for droop design is the lack of technical specifications and formal requirements due to an absence of practical experience and understanding of constraints. A combination of independent and coordinated designs may be useful to form a framework for droop control parameterisation.

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Appendix A Modelling of MTDC Systems

A.1 Clark and Park Transformations

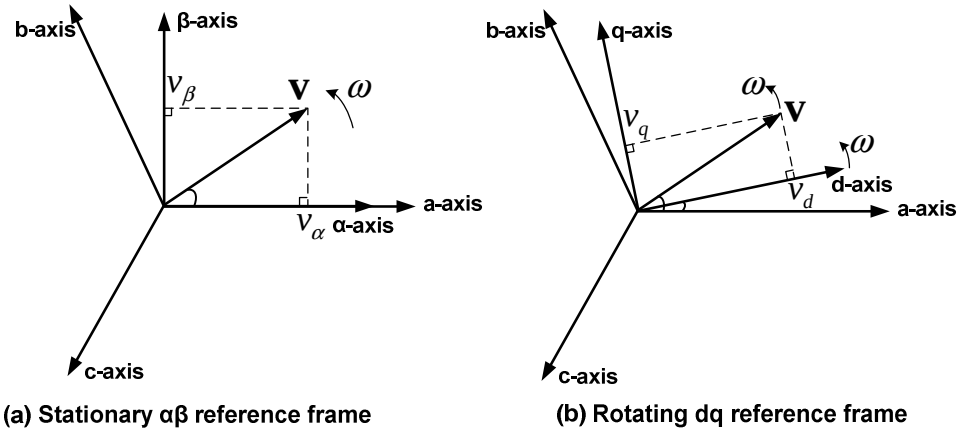

Figure A.1: Stationary and rotating reference frames.

Clark transformation:

$$\begin{pmatrix} v_\alpha \\ v_\beta \\ v_0 \end{pmatrix} = \frac{2}{3} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix} \cdot \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix}. \tag{A.1}$$

Park transformation:

$$\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} = \begin{pmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} v_\alpha \\ v_\beta \\ v_0 \end{pmatrix} = P \cdot \begin{pmatrix} v_\alpha \\ v_\beta \\ v_0 \end{pmatrix}. \tag{A.2}$$

The abc-dq0 transformation:

$$\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{pmatrix} \cdot \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix}. \tag{A.3}$$

Under balanced conditions, the instantaneous αβ components can be derived as:

$$\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} = \frac{2}{3}\begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \cdot \begin{pmatrix} \hat{V}\cos(\omega t+\delta) \\ \hat{V}\cos\left(\omega t+\delta-\frac{2\pi}{3}\right) \\ \hat{V}\cos\left(\omega t+\delta+\frac{2\pi}{3}\right) \end{pmatrix} = \begin{pmatrix} \hat{V}\cos(\omega t+\delta) \\ \hat{V}\sin(\omega t+\delta) \end{pmatrix}. \quad \text{(A.4)}$$

With θ denoting the reference angle used for the Park transformation, the dq components are then obtained as:

$$\begin{pmatrix} v_d \\ v_q \end{pmatrix} = \begin{pmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{pmatrix} \cdot \begin{pmatrix} \hat{V}\cos(\omega t+\delta) \\ \hat{V}\sin(\omega t+\delta) \end{pmatrix} = \begin{pmatrix} \hat{V}\cos(\omega t+\delta-\theta) \\ \hat{V}\sin(\omega t+\delta-\theta) \end{pmatrix}. \quad \text{(A.5)}$$

Therefore, if the angle of the phase A voltage is well locked by the PLL (namely $\theta=\omega t+\delta$), $v_d = \hat{V}, v_q = 0$.

A.2 Differential Equations in DQ Domain

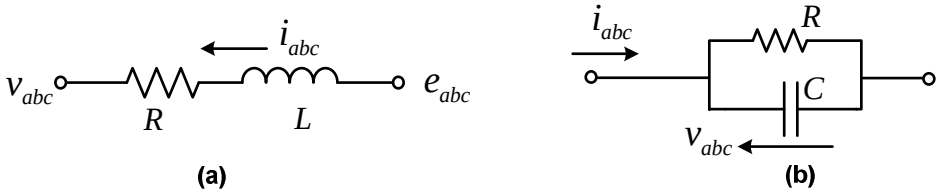

Figure A.2: Basic dynamic inductor and capacitor circuits.

The differential equation with respect to the inductor shown in Figure A.2 (a) is:

$$L\frac{d}{dt}\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} + R\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \begin{pmatrix} e_a \\ e_b \\ e_c \end{pmatrix} - \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \quad \text{(A.6)}$$

Considering that Clark transformation is linear, the dynamic equation in αβ domain is:

$$L\frac{d}{dt}\begin{pmatrix} i_\alpha \\ i_\beta \\ i_0 \end{pmatrix} + R\begin{pmatrix} i_\alpha \\ i_\beta \\ i_0 \end{pmatrix} = \begin{pmatrix} e_\alpha \\ e_\beta \\ e_0 \end{pmatrix} - \begin{pmatrix} v_\alpha \\ v_\beta \\ v_0 \end{pmatrix}. \quad \text{(A.7)}$$

According to the inverse αβ0-to-dq0 transformation, (A.7) can be written as:

$$L\frac{d}{dt}\cdot P^{-1}\begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} + R\cdot P^{-1}\begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} = P^{-1}\begin{pmatrix} e_d \\ e_q \\ e_0 \end{pmatrix} - P^{-1}\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix},\ P^{-1} = \begin{pmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{pmatrix} \quad \text{(A.8)}$$

which can then be further derived into:

$$L \cdot P^{-1} \cdot \frac{d}{dt}\begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} + L \cdot \frac{d\theta}{dt} \cdot \begin{pmatrix} -\sin\theta & -\cos\theta & 0 \\ \cos\theta & -\sin\theta & 0 \\ 0 & 0 & 0 \end{pmatrix}\begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} + R \cdot P^{-1}\begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} = P^{-1}\begin{pmatrix} e_d - v_d \\ e_q - v_q \\ e_0 - v_0 \end{pmatrix} \quad \text{(A.9)}$$

By multiplying the Park transformation matrix on both sides of (A.9),

$$L \cdot \frac{d}{dt}\begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} + R \cdot \begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} + \omega L \cdot P\begin{pmatrix} -\sin\theta & -\cos\theta & 0 \\ \cos\theta & -\sin\theta & 0 \\ 0 & 0 & 0 \end{pmatrix}\begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} = \begin{pmatrix} e_d - v_d \\ e_q - v_q \\ e_0 - v_0 \end{pmatrix}. \quad \text{(A.10)}$$

The equation representing the current dynamic across the inductor can then be obtained as:

$$L \cdot \frac{d}{dt}\begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} + R \cdot \begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} + \omega L \cdot \begin{pmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix}\begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} = \begin{pmatrix} e_d - v_d \\ e_q - v_q \\ e_0 - v_0 \end{pmatrix}. \quad \text{(A.11)}$$

The capacitor dynamics of the circuit shown in Figure A.2 (b) are:

$$C\frac{d}{dt}\begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} + \frac{1}{R}\begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} = \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} \Rightarrow C\frac{d}{dt}\begin{pmatrix} v_\alpha \\ v_\beta \\ v_0 \end{pmatrix} + \frac{1}{R}\begin{pmatrix} v_\alpha \\ v_\beta \\ v_0 \end{pmatrix} = \begin{pmatrix} i_\alpha \\ i_\beta \\ i_0 \end{pmatrix}. \quad \text{(A.12)}$$

Based on the inverse Park transformation, the following equation can be derived:

$$C\frac{d}{dt} \cdot P^{-1}\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} + \frac{1}{R} \cdot P^{-1}\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} = P^{-1}\begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} \quad \text{(A.13)}$$

which is then further derived into:

$$C \cdot P^{-1} \cdot \frac{d}{dt}\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} + C\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} \cdot \frac{d}{dt}P^{-1} + \frac{1}{R} \cdot P^{-1}\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} = P^{-1}\begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix}. \quad \text{(A.14)}$$

By multiplying the Park transformation matrix on both sides of (A.14), the dq-domain representation of the capacitor dynamics is:

$$C \cdot \frac{d}{dt}\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} + \omega C \cdot \begin{pmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix}\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} \cdot + \frac{1}{R} \cdot \begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} = \begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix}. \quad \text{(A.15)}$$

A.3 Justification of the Use of AVM

The MTDC models employed throughout this thesis have been based upon average-value models (AVMs). The AVM has been categorised by CIGRE B4 working group as a solid model for the studies of steady-state and low-frequency dynamic operations of VSC-HVDC systems [29, 38]. The behaviours of the converter are represented using controllable voltage and current sources in the AVM. The AVM used in this thesis assumes that the internal AC voltage generated by the converter is purely sinusoidal, which is likely a reasonable assumption for a modern MMC with most of its harmonic magnitudes below 1% [40]. The submodule capacitor voltages are assumed to be perfectly balanced and the current circulating internally between converter legs are not considered, as the AVM is used here for the studies of the overall converter behaviours rather than the internal MMC control. The AVM, which is widely used for MTDC research, is considered to be sufficiently accurate within the frequency range of interest for most of the studies conducted in this thesis.

Some good work has been done in [37-39] to verify the modelling methodology of the AVM. The simulation comparisons between the AVM and the more complicated MMC models demonstrate that the AVM shows very good accuracy for AC transient studies and it also achieves a good match for low-frequency DC voltage transients. The model used in this thesis has been based on an updated AVM , which has an enhanced accuracy over the AVM shown in [167]. A relatively small DC capacitance is employed for the stability studies in order to give a conservative analysis of DC voltage stability. Simulations using AVM are significantly faster than those using the more detailed MMC models with switching behaviours [37, 39]. A detailed equivalent MMC model was employed in [137] for the verification of the analysis provided in Chapter 4 and showed good agreement with the results obtained from the AVM model. An additional reason of using AVM is due to the limitations of PowerFactory, which is the software specified by the project's sponsor.

However, the AVM should be carefully used with consideration of its limitations. It is very difficult to use the AVM to represent the transient behaviours of MMC-HVDC under DC fault conditions, due to the high-frequency nature of DC protection studies. The AVM cannot be used to study the interaction between the submodule dynamics and the outer loop dynamics. Furthermore, the AVM need to be used with care to study DC system stability issues caused by high-frequency resonances.

A.4 Base Values for AC and DC System Parameters

According to equation (A.5), the base values of the dq voltages are equivalent to the base value of the peak AC voltage:

$$V_d^{base} = \hat{V}^{base} = \sqrt{\frac{2}{3}} V_{ac}^{base}, \quad V_q^{base} = \hat{V}^{base} = \sqrt{\frac{2}{3}} V_{ac}^{base}. \tag{A.16}$$

Similarly, the base values of dq currents are:

$$I_d^{base} = \hat{I}^{base} = \sqrt{2} I_{ac}^{base}, \quad I_q^{base} = \hat{I}^{base} = \sqrt{2} I_{ac}^{base}. \tag{A.17}$$

It should be noted that the converter model in DSPF does not recognise the AC voltage reference as input but instead uses the dq components of the modulation index in EMT simulation mode [168]. The modulation index is related to the per unit voltage reference according to the following equation:

$$\begin{bmatrix} P_{md} \\ P_{mq} \end{bmatrix} = \begin{bmatrix} \dfrac{e_d}{0.5 v_{dc}} \\ \dfrac{e_q}{0.5 v_{dc}} \end{bmatrix} = \begin{bmatrix} \dfrac{e_d^{pu}}{v_{dc}^{pu}} \\ \dfrac{e_q^{pu}}{v_{dc}^{pu}} \end{bmatrix} \cdot \frac{V_d^{base}}{0.5 V_{dc}^{base}} = \begin{bmatrix} \dfrac{e_d^{pu}}{v_{dc}^{pu}} \\ \dfrac{e_q^{pu}}{v_{dc}^{pu}} \end{bmatrix} \cdot \frac{2\sqrt{2} V_{ac}^{base}}{\sqrt{3} V_{dc}^{base}} \tag{A.18}$$

The power base is identical to the MVA base:

$$P^{base} = S^{base} = \sqrt{3} V_{ac}^{base} I_{ac}^{base} = \frac{3}{2} \hat{V}^{base} \hat{I}^{base}. \tag{A.19}$$

The instantaneous power can be represented by dq quantities as:

$$P = \frac{3}{2} \left(v_d i_d + v_q i_q \right). \tag{A.20}$$

The per unit representation of (A.20) however does not contain the coefficient 1.5:

$$P^{pu} = \frac{\frac{3}{2}\left(v_d i_d + v_q i_q \right)}{\frac{3}{2}\left(\hat{V}^{base} \hat{I}^{base} \right)} = v_d^{pu} i_d^{pu} + v_q^{pu} i_q^{pu}. \tag{A.21}$$

$$Q = \frac{3}{2} \left(v_q i_d - v_d i_q \right) \tag{A.22}$$

Similarly, the per unit representation of the instantaneous reactive power is derived as:

$$Q^{pu} = v_q^{pu} i_d^{pu} - v_d^{pu} i_q^{pu}. \tag{A.23}$$

With the converter rated power configured as the DC power base, the DC current base and the DC impedance base shown below are used in the thesis:

$$I_{dc}^{base} = \frac{P_{dc}^{base}}{V_{dc}^{base}}, \quad Z_{dc}^{base} = \frac{V_{dc}^{base}}{I_{dc}^{base}}. \tag{A.24}$$

Please note that the rated pole-to-pole voltage rather than the rated pole-to-ground voltage is used as the DC voltage base.

The base values of inductor and capacitor need to be carefully selected to provide correct per unit representations of AC/DC system dynamic equations. The capacitance base is derived using the basic capacitor dynamic equation shown below:

$$C\frac{dv_{dc}}{dt} = i_{dc}. \tag{A.25}$$

By dividing both sides of (A.25) by the DC current base, the per unit representation of the (A.25) is derived as:

$$i_{dc}^{pu} = \frac{i_{dc}}{I_{dc}^{base}} = C\frac{dv_{dc}}{dt}\cdot\frac{1}{I_{dc}^{base}} = C\frac{dv_{dc}}{dt}\cdot\frac{Z_{dc}^{base}}{V_{dc}^{base}} = CZ_{dc}^{base}\cdot\frac{d}{dt}\left(\frac{v_{dc}}{V_{dc}^{base}}\right) = C^{pu}\frac{dv_{dc}^{pu}}{dt} \tag{A.26}$$

Therefore the following equation is used for calculating per unit DC capacitance in this thesis:

$$C^{pu} = C\cdot Z_{dc}^{base}. \tag{A.27}$$

The inductance base is derived using the basic capacitor dynamic equation shown below:

$$L\frac{di_{dc}}{dt} + Ri_{dc} = v_{dc}. \tag{A.28}$$

By dividing both sides of (A.28) by the DC current base, the per unit representation of the (A.28) is derived as:

$$v_{dc}^{pu} = \frac{v_{dc}}{V_{dc}^{base}} = \frac{L}{Z_{dc}^{base}}\cdot\frac{d}{dt}\left(\frac{i_{dc}}{I_{dc}^{base}}\right) + \frac{R}{Z_{dc}^{base}}\cdot\frac{i_{dc}}{I_{dc}^{base}} = \frac{L}{Z_{dc}^{base}}\cdot\frac{di_{dc}^{pu}}{dt} + R^{pu}i_{dc}^{pu}. \tag{A.29}$$

Therefore the following equation is used for calculating per unit DC capacitance:

$$L^{pu} = L / Z_{dc}^{base}. \tag{A.30}$$

The derivation of the per unit value of the AC side inductance is slightly more complex, as will be illustrated using the following dynamic equation.

$$L\frac{di_a}{dt} = e_a - v_a - Ri_a \tag{A.31}$$

By dividing both sides of (A.31) by the base value of the phase voltage $\sqrt{2}/\sqrt{3}V_{ac}^{base}$, the per unit representation of (A.31) can be derived as:

$$\begin{aligned} e_a^{pu} - v_a^{pu} - R^{pu}i_a^{pu} &= \frac{\sqrt{3}e_a}{\sqrt{2}V_{ac}^{base}} - \frac{\sqrt{3}e_a}{\sqrt{2}V_{ac}^{base}} - \frac{R}{Z_{ac}^{base}}\frac{i_a}{\sqrt{2}I_{ac}^{base}} = \frac{e_a - v_a - Ri_a}{Z_{ac}^{base}\cdot\sqrt{2}I_{ac}^{base}} \\ &= \frac{L}{Z_{ac}^{base}}\cdot\frac{d}{dt}\left(\frac{i_a}{\sqrt{2}I_{ac}^{base}}\right) = \frac{L}{Z_{ac}^{base}}\cdot\frac{di_a^{pu}}{dt}. \end{aligned} \tag{A.32}$$

Therefore, the per unit AC inductance should be calculated by:

$$L_{ac}^{pu} = L / Z_{ac}^{base}. \tag{A.33}$$

Another issue that needs to be taken into account in per unit system representation is the lumped modelling of positive-pole and negative-pole impedances. With respect to the symmetrical monopole DC system shown in Figure 2.19, the DC line dynamics are represented by:

$$v_{dc1+} - v_{dc2+} = R_c\cdot i_{dc+} + L_c\cdot\frac{di_{dc+}}{dt}, \quad v_{dc2-} - v_{dc1-} = R_c\cdot i_{dc-} + L_c\cdot\frac{di_{dc-}}{dt} \tag{A.34}$$

$$\frac{C_c}{2}\cdot\frac{dv_{dc1+}}{dt} = i_{dc1+} - i_{dc+}, \quad \frac{C_c}{2}\cdot\frac{dv_{dc2+}}{dt} = i_{dc+} - i_{dc2+}. \tag{A.35}$$

Under balanced conditions, namely,

$$v_{dc1+} = -v_{dc1-}, \quad i_{dc+} = i_{dc-}, \quad v_{dc2+} = -v_{dc2-} \tag{A.36}$$

the per unit representations of (A.34) and (A.35) can then be derived as:

$$v_{dc1}^{pu} - v_{dc2}^{pu} = \frac{v_{dc1+} - v_{dc2+}}{0.5V_{dc}^{base}} = \frac{2}{Z_{dc}^{base}I_{dc}^{base}}\left(R_c\cdot i_{dc+} + L_c\cdot\frac{di_{dc+}}{dt}\right) = \frac{2R_c}{Z_{dc}^{base}}\cdot i_{dc}^{pu} + \frac{2L_c}{Z_{dc}^{base}}\cdot\frac{di_{dc}^{pu}}{dt} \tag{A.37}$$

$$i_{dc1}^{pu} - i_{dc}^{pu} = \frac{C_c}{2}\cdot\frac{dv_{dc1+}}{dt}\cdot\frac{Z_{dc}^{base}}{V_{dc}^{base}} = \frac{C_c}{2}\cdot\frac{Z_{dc}^{base}}{2}\cdot\frac{d}{dt}\left(\frac{v_{dc1+}}{0.5V_{dc}^{base}}\right) = \frac{C_cZ_{dc}^{base}}{4}\cdot\frac{dv_{dc1}^{pu}}{dt}. \tag{A.38}$$

A.5 VSC-HVDC System Parameters

Table A.1: Base data of AC and DC systems.

AC system base values		*DC system base values*	
MVA base	1000 MVA	DC power base	1000 MW
AC active power	1000 MW	DC voltage base	640 kV
AC voltage base (transformer HV side)	400 kV	DC current base	1.5625 kA
AC voltage base (transformer LV side)	333 kV	DC impedance base	409.6 Ω
AC current base (transformer HV side)	1.44 kA		
AC current base (transformer LV side)	1.73 kA		
AC impedance base (transformer HV side)	160 Ω		
AC impedance base (transformer LV side)	110.89 Ω		
dq current base (measured at PCC)	2.036 kA		
dq voltage base (measured at PCC)	326.60 kV		

Table A.2: Grid side model parameters.

Converter reactor	0.075 pu	Rated DC voltage	640 kV
X/R of converter reactor	30	Rated AC voltage	333 kV
Transformer impedance	0.15 pu	Rated power	1000 MW
X/R of transformer impedance	30	Equivalent converter capacitance	98 µF in Chapters 5, 6, 7
Rated star HV transformer voltage	400 kV		146 µF in Chapters 2, 3
Rated delta LV transformer voltage	333 kV	Arm inductance	53 mH
Modulation time constant τ_v	82 µs	Arm resistance	0.55 Ω

Table A.3: DC cable model parameters.

Rated voltage	320 kV	Resistance per km per pole	0.0113 Ω/km
Rated current	1.5625 kA	Inductance per km per pole	0.466 mH/km
Rated impedance	409.6 Ω	Capacitance per km per pole	0.28 µF/km

Table A.4: Nominal controller data (in per unit) for grid side converters.

Vector current controller	Proportional gain (STFT)	K_p	1.12
	Integral gain (STFT)	K_i	445
	Proportional gain (IMC)	K_p	0.89
	Integral gain (IMC)	K_i	9.24
	Anti-windup gain	K_t	198
	Measurement time constant	τ_m	0.16 ms
PLL controller	Proportional gain	K_p	61
	Integral gain	K_i	932
	Upper frequency limit	ω_{limH}	1.2 pu
	Lower frequency limit	ω_{limL}	0.8 pu

Active/reactive power controller	Proportional gain	K_p	0.128
	Integral gain	K_i	120.3
	Anti-windup gain	K_t	470
	Maximum i_{dref}/i_{qref}	i_{dmax}/i_{qmax}	1.05 pu
	Measurement time constant	τ_m	1.59 ms
AC voltage controller for SCR of 3.5	Proportional gain	K_p	0.228
	Integral gain	K_i	215
	Anti-windup gain	K_t	200
	Maximum i_{qref}	i_{qmax}	1.05 pu
	Gain for V_{ac}-Q droop (if applicable)	K_{VQ}	5
DC voltage controller (for C_{dc} of 97.6 µF)	Proportional gain	K_p	4.61
	Integral gain	K_i	133
	Filtering time constant for the feedforward of P_{dc} (if applicable)	τ_F	10.6 ms
	Anti-windup gain	K_t	66
	Measurement time constant	τ_m	1.0 ms
Quadratic DC voltage controller (for C_{dc} of 97.6 µF)	Proportional gain	K_p	2.3
	Integral gain	K_i	66.5
DC voltage controller (for C_{dc} of 146 µF)	Proportional gain	K_p	6.9
	Integral gain	K_i	199
	Anti-windup gain	K_t	100
Quadratic DC voltage controller (for C_{dc} of 146 µF)	Proportional gain	K_p	3.45
	Integral gain	K_i	99.5
Adaptive current limit control (if applicable)	i_{max} rising rate limit	μ_{lim_rise}	0.01 pu/ms
	i_{max} falling rate limit	μ_{lim_fall}	0.5 pu/ms
	v_q lower hysteresis threshold	v_{q_limL}	0.1 pu
	v_q upper hysteresis threshold	v_{q_limH}	0.4 pu
	Nominal maximum current limit	i_{max_nom}	1.05 pu
	Lookup table x-axis	v_q	(0.1,0.4,0.7,1) pu
	Lookup table y-axis	i_{max}	(0.3,0.2,0.1,0.05) pu
Integrator-Based setpoint controller	Integral time constant for V_{dc}	T_V	1 s
	Integral time constant for P	T_P	3.5 s
	Length of pulse signal	T_{pulse}	7.0 s
	Upper limit for V_{dcref}	V_{dcref_max}	1.05 pu
	Lower limit for V_{dcref}	V_{dcref_min}	0.93 pu

Table A.5: Wind farm side converter model parameters.

Converter reactor	0.075 pu	Rated DC voltage	640 kV
X/R of converter reactor	30	Rated AC voltage	333 kV
Transformer impedance	0.15 pu	Rated power	1000 MW
X/R of transformer impedance	30	Equivalent converter capacitance	98 µF in Chapters 5, 6, 7
Rated transformer HV side voltage	333 kV		146 µF in Chapters 2, 3
Rated transformer LV side voltage	33 kV	Arm inductance	53 mH

Table A.6: Nominal control parameters (in per unit) for wind farm side converters.

AC voltage controller	Proportional gain	K_p	0.074
	Integral gain	K_i	69.5
	Maximum modulation index	P_{m_max}	1.17
Frequency and fault ride-through controller parameters	Reference frequency	f_o	50 Hz
	Lower voltage threshold	V_{limL}	1.07 pu
	Upper voltage threshold	V_{limH}	1.08 pu
	Maximum rate of frequency change	*Grad_max*	0.2 Hz/ms
	Maximum frequency deviation	Δf_{max}	2 Hz
	Gain between Δf and Δv_{dc}	K_{vHz}	15 Hz/pu

Table A.7: Parameters of the simplified wind farm modelled by static generators.

Static generator parameters	Rated AC voltage	V_{rated}	6.9 kV
	Rated MVA	S_{rated}	5 MW
	Reactor impedance	$Z_{reactor}$	0.15 pu
	Reactor resistance	$R_{reactor}$	0.005 pu
Current controller	Proportional gain	K_p	0.75
	Integral gain	K_i	7.86
Active/reactive power controller	Proportional gain	K_p	0.05
	Integral gain	K_i	78.54
	Maximum dq current reference	i_{max}	1.05 pu
PLL controller	Proportional gain	K_p	61
	Integral gain	K_i	932
Power reduction control for fault ride-through	Time constant for filtering frequency	T_{filt}	0.02 s
	Proportional gain (slow PLL)	K_p	40
	Integral gain (slow PLL)	K_i	400
	Upper frequency threshold	f_H	50.3 Hz
	Lower frequency threshold	f_L	50.2 Hz
	Gain between power reduction ratio ΔP_{red} and frequency deviation Δf	K_{fP}	3 pu/Hz
	Maximum rate of power reference change	*Grad_max*	0.2 pu/ms

Table A.8: DC chopper data corresponding to Figure 2.19.

DC braking resistor representation		DC current source representation	
Braking resistor R_{brake}	409.6 Ω	Maximum DC chopper current	1.56 kA
Lower V_{dc} for hysteresis switching v_{limL}	1.075 pu	Lower DC voltage threshold v_{limL}	1.07 pu
Upper V_{dc} for hysteresis switching v_{limH}	1.10 pu	Upper DC voltage threshold v_{limH}	1.15 pu
		Time constant of the current source	8 ms

Table A.9: Vector current controller data corresponding to Table 2.1.

	$\omega_d = 195$ Hz			$\omega_d = 250$ Hz		
Method	STFT	IMC	SIMC	STFT	IMC	SIMC
K_p	1.12	0.88	0.84	1.44	1.12	1.06
K_i	445	9.24	244	731.6	11.69	390.1

Table A.10: DC voltage controller data corresponding to Table 2.2 (C_{dc}=146 µF).

Controller	Tuning parameter	K_p	τ_I	τ_D
1. PI	τ_c=0.0114	4.60	0.052	–
2. PI	τ_c=0.0057	8.17	0.029	–
3. PID	τ_c=0.0114	5.08	0.047	0.001
4. PID	τ_c=0.0057	9.81	0.024	0.001
5. SO	α=4	9.15	0.026	–
6. SO	α=1.96	18.68	0.006	–

Table A.11: Parameters of the GSC model used in Chapter 4.

Converter reactor	0.09 pu	Rated DC voltage	1000 kV
X/R of converter reactor	20	Rated AC voltage	521 kV
Transformer impedance	0.15 pu	Rated power	2000 MW
X/R of transformer impedance	15	Equivalent VSC capacitance	66 µF
Rated star HV transformer voltage	521 kV	Modulation time constant τ_v	80 µs
Rated delta LV transformer voltage	400 kV		

Table A.12: Parameters of the current and active power controllers used in Chapter 4.

	d-axis current control				Feedback power control		
Bandwidth (Hz)	150	200	250	300	12.5	20	40
K_P	0.85	1.13	1.42	1.71	0.05	0.11	0.21
K_i	169.1	300.5	469.4	675.9	54.95	109.2	215.5

Appendix B Power Flow Calculation

B.1 Loss Calculation Parameters

Assuming that the diodes and IGBTs in an MMC converter have the same offset voltages and on-state resistive slopes, the conduction loss of an upper arm (UA) and a lower arm (LA) of an MMC can be approximated as:

$$\begin{aligned} P_{cond}^{UA} &\approx V_o N_s \cdot \left| \frac{I_{ac}(\omega t)}{2} + \frac{I_{dc}}{3} \right| + \frac{R_o N_s}{N_p} \cdot \left[\frac{I_{ac}(\omega t)}{2} + \frac{I_{dc}}{3} \right]^2 \\ &= V_o N_s \cdot \left| \frac{\hat{I}_{ac} \sin(\omega t)}{2} + \frac{I_{dc}}{3} \right| + \frac{R_o N_s}{N_p} \cdot \left[\frac{\hat{I}_{ac} \sin(\omega t)}{2} + \frac{I_{dc}}{3} \right]^2 \end{aligned} \tag{B.1}$$

$$P_{cond}^{LA} \approx V_o N_s \cdot \left| \frac{I_{ac}(\omega t)}{2} - \frac{I_{dc}}{3} \right| + \frac{R_o N_s}{N_p} \cdot \left[\frac{I_{ac}(\omega t)}{2} - \frac{I_{dc}}{3} \right]^2 = P_{con}^{UA} \tag{B.2}$$

where N_s and N_p represent the number of sub-modules in series and in parallel in each arm respectively, V_o and R_o denote the on-state offset voltage and resistance of IGBT/diode, and $\hat{I}_{ac}$ is the peak AC current. The total conduction loss of converter values can then be computed by:

$$\begin{aligned} P_{cond} &= 3 \cdot \frac{1}{2\pi} \int_0^{2\pi} \left(P_{con}^{UA} + P_{con}^{LA} \right) d(\omega t) \\ &= 6 \cdot \frac{1}{2\pi} \int_0^{2\pi} \left\{ V_o N_s \cdot \left| \frac{\hat{I}_{ac} \sin(\omega t)}{2} + \frac{I_{dc}}{3} \right| + \frac{R_o N_s}{N_p} \cdot \left[\frac{\hat{I}_{ac} \sin(\omega t)}{2} + \frac{I_{dc}}{3} \right]^2 \right\} d(\omega t) \end{aligned} . \tag{B.3}$$

The equation (B.3) can be further simplified as:

$$P_{cond} = \frac{3}{\pi} \left[4 V_o N_s \varphi \frac{I_{dc}}{3} + 4 V_o N_s \frac{\hat{I}_{ac}}{2} \cos\varphi + \frac{R_o N_s}{N_p} \left(\frac{\hat{I}_{ac}^2}{8} + \frac{I_{dc}^2}{9} \right) \right] \tag{B.4}$$

where

$$\varphi = \begin{cases} \arcsin\left(\dfrac{2 I_{dc}}{3 \hat{I}_{ac}} \right), & if \quad \dfrac{\hat{I}_{ac}}{2} \geq \dfrac{I_{dc}}{3} \\ \dfrac{\pi}{2}, & if \quad \dfrac{\hat{I}_{ac}}{2} < \dfrac{I_{dc}}{3} \end{cases} . \tag{B.5}$$

Detailed switching loss calculation could be very complex and may require simulations using MMC models, and this may not be necessary for power flow calculation. Alternatively, the switching loss can be derived based on an average current as:

$$P_{switch} \approx 6N_s N_p f_s \cdot \left(E_{on} + E_{off} + E_{rec}\right) \cdot \frac{I_{av}}{N_p} \cdot \frac{1}{I_c} \tag{B.6}$$

where E_{on} and E_{off} denote the turn-on and turn-off switching energy of the IGBT respectively, and E_{rec} is the reverse recovery energy of the diode, f_s is the average switching frequency of the sub-modules, I_c is the rated DC collector current of the IGBT or the rated DC forward current of the diode, I_{av} is the average current flowing through an arm, which can be calculated using the following equation:

$$I_{av} = \frac{1}{2\pi}\int_0^{2\pi}\left|\frac{\hat{I}_{ac}\sin(\omega t)}{2} + \frac{I_{dc}}{3}\right| d\omega t = \frac{1}{2\pi}\left(4\varphi \cdot \frac{I_{dc}}{3} + 4\cos\varphi \cdot \frac{\hat{I}_{ac}}{2}\right). \tag{B.7}$$

By combining (B.4) and (B.6), the total converter valve loss can be approximated by:

$$P_{loss} = P_{cond} + P_{switch} = K_1\hat{I}_{ac} + K_2 I_{dc} + K_3\hat{I}_{ac}^2 + K_4 I_{dc}^2 \tag{B.8}$$

where

$$K_1 = 6N_s f_s \left(E_{on} + E_{off} + E_{rec}\right)\frac{\cos\varphi}{\pi I_c} + \frac{6}{\pi}V_o N_s \cos\varphi \tag{B.9}$$

$$K_2 = N_s f_s \left(E_{on} + E_{off} + E_{rec}\right)\frac{4\varphi}{\pi I_c} + \frac{4}{\pi}V_o N_s \varphi \tag{B.10}$$

$$K_3 = \frac{3R_o N_s}{8\pi N_p}, \quad K_4 = \frac{R_o N_s}{3\pi N_p}. \tag{B.11}$$

Table B.1: IGBT/Diode data used for converter loss calculation [123].

IGBTs in parallel N_p	2	DC collector current I_c	1200 A
Submodules in series per arm N_s	160	DC forward current I_F	1200 A
On-State resistance R_o	0.002 Ω	Turn-On switching energy E_{on}	4.35 J
On-State offset voltage V_o	1.7 V	Turn-Off switching energy E_{off}	6.00 J
Switching frequency per submodule	100 Hz	Reverse recovery energy E_{rec}	2.73 J

B.2 Interior Point Method for Optimisation

A general optimisation problem can be expressed as:

$$\min \quad f(\mathbf{x}) \tag{B.12}$$

subject to the equality and inequality constraints:

$$A\mathbf{x} = b \tag{B.13}$$

$$h_i(\mathbf{x}) \le 0,\ i = 1, 2, \cdots, m. \tag{B.14}$$

In the interior point approach, the original problem with inequality constraints is decomposed into a sequence of equality constrained problems [169]. Then each of these can be handled by the Gradient method or the Newtonian method [118].

The inequality constraints are reformulated by the logarithmic barrier function:

$$\phi(\mathbf{x}) = -\mu \sum_{i=1}^{m} \ln\left(h_i(\mathbf{x})\right) \tag{B.15}$$

This is a form of penalty function that is close to zero when the inequality constraints are met, while becomes very large when the function $h_i(\boldsymbol{x})$ reaches close to zero [118]. Incorporating this barrier function to the objective function, the optimisation problem can be transformed to:

$$\min \quad f_\mu(\mathbf{x}) = f(\mathbf{x}) - \mu \sum_{i=1}^{m} \ln\left(h_i(\mathbf{x})\right) \tag{B.16}$$

subject to the equality constraints shown in (B.13). The solution of this new optimisation problem can be computed using the Newtonian method:

$$\Delta\mathbf{x} = -\left[\frac{\partial}{\partial \mathbf{x}} \nabla L(\mathbf{x})\right]^{-1} \Delta L(\mathbf{x}) \tag{B.17}$$

where $L(\boldsymbol{x})$ is the corresponding Lagrangian equation.

Basically, the general procedure of this interior point method can be described as:

1. Centering step: Calculate $\boldsymbol{x}^*(\mu)$ by minimising $f_\mu(\boldsymbol{x})$ subject to $A\boldsymbol{x} = b$. The solution to the Lagrangian equation is computed by setting the gradient to zero [118]. These nonlinear equations are then solved iteratively via Newton-Raphson method.
2. Update the central path $\boldsymbol{x} := \boldsymbol{x}^*(\mu)$.
3. Terminal the process if the convergence criterion has been met.
4. Increase the penalty factor $u := \alpha\mu$ $(\alpha > 1)$ and repeat the iteration process.

Appendix C State-Space Modelling of MTDC

C.1 State-Space Modelling of DC Lines

The detailed state-space representation for the DC line model shown in Figure 5.6 (DC reactor considered at the two ends of the line; π section number: n):

$$A_{11} = zeros(n+1, n+1), \quad A_{12} = \begin{bmatrix} -\frac{2}{C_c} & \frac{2}{C_c} & & & \\ & -\frac{1}{C_c} & \frac{1}{C_c} & & \\ & & \ddots & \ddots & \\ & & & -\frac{2}{C_c} & \frac{2}{C_c} \end{bmatrix}_{(n+1)\times(n+2)} \tag{C.1}$$

$$A_{21} = \begin{bmatrix} \frac{1}{L_{dc}} & & & \\ -\frac{1}{L_c} & \frac{1}{L_c} & & \\ & -\frac{1}{L_c} & \ddots & \\ & & \ddots & \frac{1}{L_c} \\ & & & -\frac{1}{L_{dc}} \end{bmatrix}_{(n+2)\times(n+1)}, A_{22} = \begin{bmatrix} -\frac{R_{dc}}{L_{dc}} & & & \\ & -\frac{R_c}{L_c} & & \\ & & \ddots & \\ & & & -\frac{R_c}{L_c} \\ & & & & -\frac{R_{dc}}{L_{dc}} \end{bmatrix}_{(n+2)\times(n+2)} \tag{C.2}$$

$$\dot{x} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} x + \begin{bmatrix} \underbrace{0 \quad \cdots \quad 0}_{n+1} & 0 \quad \cdots \quad \frac{1}{L_{dc}} \\ \underbrace{0 \quad \cdots \quad 0}_{n+1} & \underbrace{-\frac{1}{L_{dc}} \quad \cdots \quad 0}_{n+2} \end{bmatrix}^T \begin{bmatrix} v_{in} \\ v_o \end{bmatrix}$$
$$y = \begin{bmatrix} \underbrace{0 \quad \cdots \quad 0}_{n+1} & \underbrace{1 \quad \cdots \quad 0}_{n+2} \\ \underbrace{0 \quad \cdots \quad 0}_{n+1} & \underbrace{0 \quad \cdots \quad -1}_{n+2} \end{bmatrix} x \tag{C.3}$$

$$x = \begin{bmatrix} \underbrace{v_{c0} \quad v_{c1} \quad v_{c2} \quad \cdots \quad v_{c(n-1)} \quad v_{cn}}_{n+1} & \underbrace{i_{in} \quad i_{L1} \quad i_{L2} \quad \cdots \quad i_{L(n)} \quad i_o}_{n+2} \end{bmatrix}^T$$
$$y = \begin{bmatrix} i_{in} & -i_o \end{bmatrix}, \; u = \begin{bmatrix} v_{in} & v_o \end{bmatrix} \tag{C.4}$$

C.2 State-Space Representation of GSC Terminal

With the PLL and AC system model excluded, the state-space model of a GSC terminal in V_{dc}-P droop and V_{ac}-Q droop control mode (Model 1) is described as:

$$\begin{aligned}
\Delta x &= \begin{bmatrix} \Delta e_d & \Delta e_q & \Delta i_d & \Delta i_q & \Delta x_{id} & \Delta x_{iq} & \Delta v_{dc} & \Delta x_P & \Delta x_Q \end{bmatrix}^T \\
\Delta u &= \begin{bmatrix} \Delta i_{dc} & \Delta v_{dc}^* & \Delta P^* & \Delta Q^* & \Delta v_{ac}^* & \Delta v_d & \Delta v_q \end{bmatrix}^T \\
\Delta y &= \begin{bmatrix} \Delta v_{dc} & \Delta P_{ac} & \Delta Q & \Delta v_{ac} & \Delta i_d & \Delta i_q \end{bmatrix}^T
\end{aligned} \tag{C.5}$$

$$A1 = \begin{bmatrix}
-\frac{1}{\tau_v} & 0 & -\frac{K_p^P K_p^{id} v_{do} + K_p^{id}}{\tau_v} & -\frac{K_p^P K_p^{id} v_{qo} + L\omega}{\tau_v} & \frac{1}{\tau_v} & 0 & \frac{K_{droop} K_p^P K_p^{id}}{\tau_v} & \frac{K_p^{id}}{\tau_v} & 0 \\
0 & -\frac{1}{\tau_v} & \frac{K_p^Q K_p^{iq} v_{aco} v_{qo} + L\omega v_{aco}}{v_{aco}\tau_v} & -\frac{K_p^Q K_p^{iq} v_{aco} v_{do} + K_p^{iq} v_{aco}}{v_{aco}\tau_v} & 0 & \frac{1}{\tau_v} & 0 & 0 & \frac{K_p^{iq}}{\tau_v} \\
\frac{1}{L} & 0 & -\frac{R}{L} & \omega & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{L} & -\omega & -\frac{R}{L} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\left(K_p^P v_{do} + 1\right) K_i^{id} & -K_p^P v_{qo} K_i^{id} & 0 & 0 & K_{droop} K_p^P K_i^{id} & K_i^{id} & 0 \\
0 & 0 & K_i^{iq} K_p^Q v_{qo} & -\frac{K_i^{iq}\left(K_p^Q v_{aco} v_{do} + v_{aco}\right)}{v_{aco}} & 0 & 0 & 0 & 0 & K_i^{iq} \\
-\frac{i_{do}}{v_{dco} C_{dc}} & -\frac{i_{qo}}{v_{dco} C_{dc}} & -\frac{e_{do}}{v_{dco} C_{dc}} & -\frac{e_{qo}}{v_{dco} C_{dc}} & 0 & 0 & \frac{P_{dco}}{C_{dc} v_{dco}^2} & 0 & 0 \\
0 & 0 & -K_i^P v_{do} & -K_i^P v_{qo} & 0 & 0 & K_i^P K_{droop} & 0 & 0 \\
0 & 0 & K_i^Q v_{qo} & -K_i^Q v_{do} & 0 & 0 & 0 & 0 & 0
\end{bmatrix} \tag{C.6}$$

$$B1 = \begin{bmatrix}
0 & -\frac{K_p^P K_p^{id} K_{droop}}{\tau_v} & -\frac{K_p^P K_p^{id}}{\tau_v} & 0 & 0 & \frac{1 - K_p^P K_p^{id} i_{do}}{\tau_v} & -\frac{K_p^P K_p^{id} i_{qo}}{\tau_v} \\
0 & 0 & 0 & -\frac{K_p^Q K_p^{iq}}{\tau_v} & -\frac{K_p^Q K_p^{iq} K_{vQ}}{\tau_v} & \frac{K_p^Q K_p^{iq} K_{vQ} v_{do} - K_p^Q K_p^{iq} i_{qo} v_{aco}}{v_{aco}\tau_v} & \frac{K_p^Q K_p^{iq} K_{vQ} v_{qo} + K_p^Q K_p^{iq} i_{do} v_{aco} + v_{aco}}{v_{aco}\tau_v} \\
0 & 0 & 0 & 0 & 0 & -\frac{1}{L} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L} \\
0 & -K_p^P K_i^{id} K & K_p^P K_i^{id} & 0 & 0 & -K_p^P i_{do} K_i^{id} & -K_p^P i_{qo} K_i^{id} \\
0 & 0 & 0 & -K_i^{iq} K_p^Q & -K_i^{iq} K_p^Q K_{vQ} & \frac{K_i^{iq}\left(K_p^Q K_{vQ} v_{do} - K_p^Q i_{qo} v_{aco}\right)}{v_{aco}} & \frac{K_i^{iq}\left(K_p^Q K_{vQ} v_{qo} + K_p^Q i_{do} v_{aco}\right)}{v_{aco}} \\
\frac{1}{C_{dc}} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -K_i^P K & K_i^P & 0 & 0 & K_i^P i_{do} & -K_i^P i_{qo} \\
0 & 0 & 0 & -K_i^Q & -K_i^Q K_{vQ} & \frac{K_i^Q\left(K_{vQ} v_{do} - i_{qo} v_{aco}\right)}{v_{aco}} & \frac{K_i^Q\left(K_{vQ} v_{qo} + i_{do} v_{aco}\right)}{v_{aco}}
\end{bmatrix} \tag{C.7}$$

$$C1=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & v_{do} & v_{qo} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & v_{qo} & -v_{do} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad D1=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & i_{do} & i_{qo} \\ 0 & 0 & 0 & 0 & 0 & -i_{qo} & i_{do} \\ 0 & 0 & 0 & 0 & 0 & \frac{v_{do}}{v_{aco}} & \frac{v_{qo}}{v_{aco}} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}. \tag{C.8}$$

Please note that the converter terminal in constant active or reactor power mode, instead of in the droop AC or DC voltage control mode, can also be represented using this state-space model by setting the corresponding droop gain to zero.

With the PLL and AC system model excluded, the state-space model of a GSC terminal in constant DC voltage control and V_{ac}-Q droop control mode (Model 2) is described as:

$$\begin{aligned} \Delta x &= \begin{bmatrix} \Delta e_d & \Delta e_q & \Delta i_d & \Delta i_q & \Delta x_{id} & \Delta x_{iq} & \Delta v_{dc} & \Delta x_P & \Delta x_Q \end{bmatrix}^T \\ \Delta u &= \begin{bmatrix} \Delta i_{dc} & \Delta v_{dc}^* & \Delta Q^* & \Delta v_{ac}^* & \Delta v_d & \Delta v_q \end{bmatrix}^T \\ \Delta y &= \begin{bmatrix} \Delta v_{dc} & \Delta P_{ac} & \Delta Q & \Delta v_{ac} & \Delta i_d & \Delta i_q \end{bmatrix}^T \end{aligned} \tag{C.9}$$

$$A2=\begin{bmatrix} -\frac{1}{\tau_v} & 0 & -\frac{K_p^{id}}{\tau_v} & -\frac{L\omega}{\tau_v} & \frac{1}{\tau_v} & 0 & \frac{K_p^{vdc}K_p^{id}}{\tau_v} & \frac{K_p^{id}}{\tau_v} & 0 \\ 0 & -\frac{1}{\tau_v} & \frac{K_p^Q K_p^{iq} v_{aco} v_{qo} + L\omega v_{aco}}{v_{aco}\tau_v} & -\frac{K_p^Q K_p^{iq} v_{aco} v_{do} + K_p^{iq} v_{aco}}{v_{aco}\tau_v} & 0 & \frac{1}{\tau_v} & 0 & 0 & \frac{K_p^{iq}}{\tau_v} \\ \frac{1}{L} & 0 & -\frac{R}{L} & \omega & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L} & -\omega & -\frac{R}{L} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -K_i^{id} & 0 & 0 & 0 & K_p^{vdc}K_i^{id} & K_i^{id} & 0 \\ 0 & 0 & K_i^{iq}K_p^Q v_{qo} & -\frac{K_i^{iq}\left(K_p^Q v_{aco} v_{do} + v_{aco}\right)}{v_{aco}} & 0 & 0 & 0 & 0 & K_i^{iq} \\ -\frac{i_{do}}{v_{dco}C_{dc}} & -\frac{i_{qo}}{v_{dco}C_{dc}} & -\frac{e_{do}}{v_{dco}C_{dc}} & -\frac{e_{qo}}{v_{dco}C_{dc}} & 0 & 0 & \frac{P_{dco}}{C_{dc}v_{dco}^2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & K_i^{vdc} & 0 & 0 \\ 0 & 0 & K_i^Q v_{qo} & -K_i^Q v_{do} & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.10}$$

$$B2=\begin{bmatrix}
0 & -\frac{K_p^{vdc}K_p^{id}}{\tau_v} & 0 & 0 & \frac{1}{\tau_v} & 0 \\
0\ \ 0 & -\frac{K_p^{Q}K_p^{iq}}{\tau_v} & -\frac{K_p^{Q}K_p^{iq}K_{vQ}}{\tau_v} & \frac{K_p^{Q}K_p^{iq}K_{vQ}v_{do}-K_p^{Q}K_p^{iq}i_{qo}v_{aco}}{v_{aco}\tau_v} & \frac{K_p^{Q}K_p^{iq}K_{vQ}v_{qo}+K_p^{Q}K_p^{iq}i_{do}v_{aco}+v_{aco}}{v_{aco}\tau_v} & \\
0\ \ 0 & 0\ \ 0 & 0 & 0 & -\frac{1}{L} & 0 \\
0\ \ 0 & 0\ \ 0 & 0 & 0 & 0 & -\frac{1}{L} \\
0 & -K_p^{vdc}K_i^{id} & 0 & 0 & 0 & 0 \\
0\ \ 0 & -K_i^{iq}K_p^{Q} & -K_i^{iq}K_p^{Q}K_{vQ} & \frac{K_i^{iq}\left(K_p^{Q}K_{vQ}v_{do}-K_p^{Q}i_{qo}v_{aco}\right)}{v_{aco}} & \frac{K_i^{iq}\left(K_p^{Q}K_{vQ}v_{qo}+K_p^{Q}i_{do}v_{aco}\right)}{v_{aco}} & \\
\frac{1}{C_{dc}} & 0 & 0 & 0 & 0 & 0 \\
0 & -K_i^{vdc} & 0 & 0 & 0 & 0 \\
0\ \ 0 & -K_i^{Q} & -K_i^{Q}K_{vQ} & \frac{K_i^{Q}\left(K_{vQ}v_{do}-i_{qo}v_{aco}\right)}{v_{aco}} & \frac{K_i^{Q}\left(K_{vQ}v_{qo}+i_{do}v_{aco}\right)}{v_{aco}} &
\end{bmatrix} \tag{C.11}$$

$$C2=C1,\quad D2=D1(:,2:7). \tag{C.12}$$

With the PLL and AC system model excluded, the state-space model of a GSC terminal in V_{dc}-P droop and constant AC voltage control mode (Model 3) is described as:

$$\begin{aligned}
\Delta x &= \begin{bmatrix}\Delta e_d & \Delta e_q & \Delta i_d & \Delta i_q & \Delta x_{id} & \Delta x_{iq} & \Delta v_{dc} & \Delta x_P & \Delta x_Q\end{bmatrix}^T \\
\Delta u &= \begin{bmatrix}\Delta i_{dc} & \Delta v_{dc}^{*} & \Delta P^{*} & \Delta v_{ac}^{*} & \Delta v_d & \Delta v_q\end{bmatrix}^T \\
\Delta y &= \begin{bmatrix}\Delta v_{dc} & \Delta P_{ac} & \Delta Q & \Delta v_{ac} & \Delta i_d & \Delta i_q\end{bmatrix}^T
\end{aligned} \tag{C.13}$$

$$A3=\begin{bmatrix}
-\frac{1}{\tau_v} & 0 & -\frac{K_p^{P}K_p^{id}v_{do}+K_p^{id}}{\tau_v} & -\frac{K_p^{P}K_p^{id}v_{qo}+L\omega}{\tau_v} & \frac{1}{\tau_v} & 0 & \frac{K_{droop}K_p^{P}K_p^{id}}{\tau_v} & \frac{K_p^{id}}{\tau_v} & 0 \\
0 & -\frac{1}{\tau_v} & \frac{L\omega}{\tau_v} & -\frac{K_p^{iq}}{\tau_v} & 0 & \frac{1}{\tau_v} & 0\ \ 0 & \frac{K_p^{iq}}{\tau_v} & \\
\frac{1}{L} & 0 & -\frac{R}{L} & \omega & 0\ \ 0 & 0\ \ 0 & 0 & & \\
0 & \frac{1}{L} & -\omega & -\frac{R}{L} & 0\ \ 0 & 0\ \ 0 & 0 & & \\
0\ \ 0 & -\left(K_p^{P}v_{do}+1\right)K_i^{id} & -K_p^{P}v_{qo}K_i^{id} & 0\ \ 0 & K_{droop}K_p^{P}K_i^{id} & K_i^{id} & 0 & & \\
0\ \ 0\ \ 0 & -K_i^{iq} & 0\ \ 0\ \ 0 & 0 & K_i^{iq} & & & & \\
-\frac{i_{do}}{v_{dco}C_{dc}} & -\frac{i_{qo}}{v_{dco}C_{dc}} & -\frac{e_{do}}{v_{dco}C_{dc}} & -\frac{e_{qo}}{v_{dco}C_{dc}} & 0\ \ 0 & \frac{P_{dco}}{C_{dc}v_{dco}^2} & 0\ \ 0 & & \\
0\ \ 0 & -K_i^{P}v_{do} & -K_i^{P}v_{qo} & 0\ \ 0 & K_i^{P}K_{droop} & 0\ \ 0 & & & \\
0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0 & & & & & & & &
\end{bmatrix} \tag{C.14}$$

$$B3=\begin{bmatrix}
0 & -\frac{K_p^P K_p^{id} K}{\tau_v} & -\frac{K_p^P K_p^{id}}{\tau_v} & 0 & \frac{1-K_p^P K_p^{id} i_{do}}{\tau_v} & -\frac{K_p^P K_p^{id} i_{qo}}{\tau_v} \\
0\ 0\ 0 & -\frac{K_p^{vac} K_p^{iq}}{\tau_v} & \frac{K_p^{vac} K_p^{iq} v_{do}}{v_{aco}\tau_v} & \frac{K_p^{vac} K_p^{iq} v_{qo}+v_{aco}}{v_{aco}\tau_v} & & \\
0\ 0\ 0 & 0 & -\frac{1}{L} & 0 & & \\
0\ 0\ 0 & 0 & 0 & -\frac{1}{L} & & \\
0 & -K_p^P K_i^{id} K & K_p^P K_i^{id} & 0 & -K_p^P i_{do} K_i^{id} & -K_p^P i_{qo} K_i^{id} \\
0\ 0\ 0 & -K_i^{iq} K_p^{vac} & \frac{K_i^{iq} K_p^{vac} v_{do}}{v_{aco}} & \frac{K_i^{iq} K_p^{vac} v_{qo}}{v_{aco}} & & \\
\frac{1}{C_{dc}} & 0\ 0 & 0\ 0\ 0 & & & \\
0 & -K_i^P K & K_i^P & 0 & K_i^P i_{do} & -K_i^P i_{qo} \\
0\ 0\ 0 & -K_i^{vac} & \frac{K_i^{vac} v_{do}}{v_{aco}} & \frac{K_i^{vac} v_{qo}}{v_{aco}} & &
\end{bmatrix} \tag{C.15}$$

$$C3=C1,\quad D3=D1(:,2:7). \tag{C.16}$$

With the PLL and AC system model excluded, the state-space model of a GSC terminal in constant DC voltage control and constant AC voltage control mode (Model 4) is described as:

$$\begin{aligned}
\Delta x &= \begin{bmatrix}\Delta e_d & \Delta e_q & \Delta i_d & \Delta i_q & \Delta x_{id} & \Delta x_{iq} & \Delta v_{dc} & \Delta x_P & \Delta x_Q\end{bmatrix}^T \\
\Delta u &= \begin{bmatrix}\Delta i_{dc} & \Delta v_{dc}^* & \Delta v_{ac}^* & \Delta v_d & \Delta v_q\end{bmatrix}^T \\
\Delta y &= \begin{bmatrix}\Delta v_{dc} & \Delta P_{ac} & \Delta Q & \Delta v_{ac} & \Delta i_d & \Delta i_q\end{bmatrix}^T
\end{aligned} \tag{C.17}$$

$$A4=\begin{bmatrix}
-\frac{1}{\tau_v} & 0 & -\frac{K_p^{id}}{\tau_v} & -\frac{L\omega}{\tau_v} & \frac{1}{\tau_v} & 0 & \frac{K_p^{vdc} K_p^{id}}{\tau_v} & \frac{K_p^{id}}{\tau_v} & 0 \\
0 & -\frac{1}{\tau_v} & \frac{L\omega}{\tau_v} & -\frac{K_p^{iq}}{\tau_v} & 0 & \frac{1}{\tau_v} & 0\ 0 & \frac{K_p^{iq}}{\tau_v} & \\
\frac{1}{L} & 0 & -\frac{R}{L} & \omega & 0\ 0\ 0\ 0\ 0 & & & & \\
0 & \frac{1}{L} & -\omega & -\frac{R}{L} & 0\ 0\ 0\ 0\ 0 & & & & \\
0\ 0 & -K_i^{id} & 0\ 0\ 0 & K_p^{vdc} K_i^{id} & K_i^{id} & 0 & & & \\
0\ 0\ 0 & -K_i^{iq} & 0\ 0\ 0\ 0 & K_i^{iq} & & & & & \\
-\frac{i_{do}}{v_{dco} C_{dc}} & -\frac{i_{qo}}{v_{dco} C_{dc}} & -\frac{e_{do}}{v_{dco} C_{dc}} & -\frac{e_{qo}}{v_{dco} C_{dc}} & 0\ 0 & \frac{P_{dco}}{C_{dc} v_{dco}^2} & 0\ 0 & & \\
0\ 0\ 0\ 0\ 0\ 0 & K_i^{vdc} & 0\ 0 & & & & & & \\
0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0 & & & & & & & &
\end{bmatrix} \tag{C.18}$$

$$B4=\begin{bmatrix} 0 & 0 & 0 & -\frac{K_p^{vdc}K_p^{id}}{\tau_v} & 0 & \frac{1}{\tau_v} & 0 \\ 0 & 0 & -\frac{K_p^{vac}K_p^{iq}}{\tau_v} & \frac{K_p^{vac}K_p^{iq}v_{do}}{v_{aco}\tau_v} & \frac{K_p^{vac}K_p^{iq}v_{qo}+v_{aco}}{v_{aco}\tau_v} & & \\ & & 0 & 0 & 0 & -\frac{1}{L} & 0 \\ & & 0 & 0 & 0 & 0 & -\frac{1}{L} \\ & & 0 & -K_p^{vdc}K_i^{id} & 0 & 0 & 0 \\ 0 & 0 & -K_i^{iq}K_p^{vac} & \frac{K_i^{iq}K_p^{vac}v_{do}}{v_{aco}} & \frac{K_i^{iq}K_p^{vac}v_{qo}}{v_{aco}} & & \\ & & \frac{1}{C_{dc}} & 0 & 0 & 0 & 0 \\ & & 0 & -K_i^{vdc} & 0 & K_i^{P}i_{do} & -K_i^{P}i_{qo} \\ & & 0 & 0 & -K_i^{vac} & \frac{K_i^{vac}v_{do}}{v_{aco}} & \frac{K_i^{vac}v_{qo}}{v_{aco}} \end{bmatrix} \tag{C.19}$$

$$C4=C1,\quad D4=D1(:,3:7)\,. \tag{C.20}$$

The state-space representation of the PLL and lumped AC system model is detailed as:

$$\begin{aligned} &\Delta x=\begin{bmatrix}\Delta x_{pll} & \Delta\theta_m & \Delta v_d & \Delta v_q & \Delta i_{sd} & \Delta i_{sq}\end{bmatrix}^T \\ &\Delta u=\begin{bmatrix}\Delta i_d & \Delta i_q & \Delta\theta_s & \Delta v_s\end{bmatrix}^T,\quad \Delta y=\begin{bmatrix}\Delta v_d & \Delta v_q\end{bmatrix}^T \end{aligned} \tag{C.21}$$

$$A=\begin{bmatrix} 0 & 0 & 0 & K_i^{pll} & 0 & 0 \\ 1 & 0 & 0 & K_p^{pll} & 0 & 0 \\ 0 & 0 & 0 & \omega & \frac{1}{C_f} & 0 \\ 0 & 0 & -\omega & 0 & 0 & -\frac{1}{C_f} \\ 0 & -\frac{v_{sqo}}{L} & \frac{1}{L} & 0 & -\frac{R}{L} & \omega \\ 0 & \frac{v_{sdo}}{L} & 0 & \frac{1}{L} & -\omega & -\frac{R}{L} \end{bmatrix},\quad B=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{C_f} & 0 & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 & 0 \\ 0 & 0 & \frac{v_{sqo}}{L} & -\frac{v_{sdo}}{L} \\ 0 & 0 & -\frac{v_{sdo}}{L} & -\frac{v_{sqo}}{L} \end{bmatrix} \tag{C.22}$$

$$C=\begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix},\quad D=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.23}$$

C.3 Connections of the Models of VSC, PLL and Lumped AC System

The converter state-space model shown in C.2.2 can be written in the following form:

$$\begin{aligned}\dot{x}_1 &= A_1 x_1 + B_{12} u_{21} + B_1 u_1 \\ y_1 &= C_1 x_1 + D_{12} u_{12} + D_1 u_1 \\ y_{12} &= C_{1\_} x_1\end{aligned} \tag{C.24}$$

where

$$\begin{aligned}u_{12} &= \begin{bmatrix} v_d & v_q \end{bmatrix}^T,\ u_1 = \begin{bmatrix} i_{dc} & v_{dcr} & P_{ref} & Q_{ref} & v_{acr} \end{bmatrix}^T \\ y_1 &= \begin{bmatrix} \Delta v_{dc} & \Delta P_{ac} & \Delta Q & \Delta v_{ac} \end{bmatrix}^T,\ y_{12} = \begin{bmatrix} i_d & i_q \end{bmatrix}^T\end{aligned}. \tag{C.25}$$

The state-space model of the PLL and lumped AC system can be written as:

$$\begin{aligned}\dot{x}_2 &= A_2 x_2 + B_{21} u_{21} + B_2 u_2 \\ y_{21} &= C_{2\_} x_2 + D_{21\_} u_{21} + D_{2\_} u_2 \\ y_2 &= C_2 x_2 + D_{21} u_{21} + D_2 u_2\end{aligned} \tag{C.26}$$

where

$$\begin{aligned}u_{21} &= \begin{bmatrix} i_d & i_q \end{bmatrix}^T, u_2 = \begin{bmatrix} \theta_s & v_s \end{bmatrix} \\ y_{21} &= \begin{bmatrix} v_d & v_q \end{bmatrix}^T,\ y_2 = \begin{bmatrix} v_q & \theta_m \end{bmatrix}^T\end{aligned} \tag{C.27}$$

$$u_{12} = y_{21}, u_{21} = y_{12}. \tag{C.28}$$

According to the intermediate input/output relations shown in (C.28), the state-space models (C.26) and (C.24) can be re-written as:

$$\begin{aligned}\dot{x}_2 &= A_2 x_2 + B_{21} C_{1\_} x_1 + B_2 u_2 \\ y_{21} &= C_{2\_} x_2 + D_{21\_} C_{1\_} x_1 + D_{2\_} u_2 \\ y_2 &= C_2 x_2 + D_{21} C_{1\_} x_1 + D_2 u_2\end{aligned} \tag{C.29}$$

$$\begin{aligned}\dot{x}_1 &= A_1 x_1 + B_{12} C_{2\_} x_2 + B_{12} D_{21\_} C_{1\_} x_1 + B_{12} D_{2\_} u_2 + B_1 u_1 \\ y_1 &= C_1 x_1 + D_{12} C_{2\_} x_2 + D_{12} D_{21\_} C_{1\_} x_1 + D_{12} D_{2\_} u_2 + D_1 u_1\end{aligned} \tag{C.30}$$

The combined state-space model for the GSC terminal can then be represented as:

$$\begin{pmatrix}\dot{x}_1 \\ \dot{x}_2\end{pmatrix} = \underbrace{\begin{pmatrix} A_1 + B_{12} D_{21\_} C_{1\_} & B_{12} C_{2\_} \\ B_{21} C_{1\_} & A_2 \end{pmatrix}}_{A_{GSC}} \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \underbrace{\begin{pmatrix} B_1 & B_{12} D_{2\_} \\ 0 & B_2 \end{pmatrix}}_{B_{GSC}} \begin{pmatrix} u_1 \\ u_2 \end{pmatrix} \tag{C.31}$$

$$\begin{pmatrix} y_1 \\ y_2 \end{pmatrix} = \underbrace{\begin{pmatrix} C_1 + D_{12} D_{21\_} C_{1\_} & D_{12} C_{2\_} \\ D_{21} C_{1\_} & C_2 \end{pmatrix}}_{C_{GSC}} \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \underbrace{\begin{pmatrix} D_1 & D_{12} D_{2\_} \\ 0 & D_2 \end{pmatrix}}_{D_{GSC}} \begin{pmatrix} u_1 \\ u_2 \end{pmatrix}. \tag{C.32}$$

C.4 State-Space Modelling of WFC Terminal

The state-space representation for the simplified wind farm model shown in Figure 5.4:

$$\begin{aligned}\Delta x &= \begin{bmatrix}\Delta e_{d2} & \Delta e_{q2} & \Delta i_d & \Delta i_q & \Delta x_{id} & \Delta x_{iq} & \Delta x_P & \Delta x_Q\end{bmatrix}^T \\ \Delta u &= \begin{bmatrix}\Delta P^* & \Delta Q^* & \Delta v_{d2} & \Delta v_{q2}\end{bmatrix}^T,\ \Delta y = \begin{bmatrix}\Delta P & \Delta Q & \Delta e_{d2} & \Delta e_{q2} & \Delta i_q & \Delta i_q\end{bmatrix}^T\end{aligned} \tag{C.33}$$

$$A = \begin{bmatrix}
-\frac{1}{\tau_v} & 0 & -\frac{K_p^P K_p^{id} v_{d2o} + K_p^{id}}{\tau_v} & -\frac{K_p^P K_p^{id} v_{q2o} + \omega L_2}{\tau_v} & \frac{1}{\tau_v} & 0 & \frac{K_p^{id}}{\tau_v} & 0 \\
0 & -\frac{1}{\tau_v} & \frac{K_p^Q K_p^{iq} v_{q2o} + \omega L_2}{\tau_v} & \frac{K_p^Q K_p^{iq} v_{d2o} - K_p^{iq}}{\tau_v} & 0 & \frac{1}{\tau_v} & 0 & \frac{K_p^{iq}}{\tau_v} \\
\frac{1}{L_2} & 0 & -\frac{R_2}{L_2} & \omega & 0 & 0 & 0 & 0 \\
0 & \frac{1}{L_2} & -\omega & -\frac{R_2}{L_2} & 0 & 0 & 0 & 0 \\
0 & 0 & -\left(K_p^P v_{d2o} _ + 1\right) K_i^{id} & -K_p^P v_{q2o} K_i^{id} & 0 & 0 & K_i^{id} & 0 \\
0 & 0 & K_i^{iq} K_p^Q v_{q2o} & -K_i^{iq}\left(K_p^Q v_{d2o} + 1\right) & 0 & 0 & 0 & K_i^{iq} \\
0 & 0 & -K_i^P v_{d2o} & -K_i^P v_{q2o} & 0 & 0 & 0 & 0 \\
0 & 0 & K_i^Q v_{q2o} & -K_i^Q v_{d2o} & 0 & 0 & 0 & 0
\end{bmatrix} \tag{C.34}$$

$$B = \begin{bmatrix}
\frac{K_p^P K_p^{id}}{\tau_v} & 0 & \frac{1 - K_p^P K_p^{id} i_{do}}{\tau_v} & -\frac{K_p^P K_p^{id} i_{qo}}{\tau_v} \\
0 & -\frac{K_p^Q K_p^{iq}}{\tau_v} & -\frac{K_p^Q K_p^{iq} i_{qo}}{\tau_v} & \frac{K_p^Q K_p^{iq} i_{do} + 1}{\tau_v} \\
0 & 0 & -\frac{1}{L_2} & 0 \\
0 & 0 & 0 & -\frac{1}{L_2} \\
K_p^P K_i^{id} & 0 & -K_p^P i_{do} K_i^{id} & -K_p^P i_{qo} K_i^{id} \\
0 & -K_i^{iq} K_p^Q & -K_i^{iq} K_p^Q i_{qo} & K_i^{iq} K_p^Q i_{do} \\
K_i^P & 0 & -K_i^P i_{do} & -K_i^P i_{qo} \\
0 & -K_i^Q & -K_i^Q i_{qo} & K_i^Q i_{do}
\end{bmatrix} \tag{C.35}$$

$$C = \begin{bmatrix}
0 & 0 & v_{d2o} & v_{q2o} & 0 & 0 & 0 & 0 \\
0 & 0 & v_{q2o} & -v_{d2o} & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0
\end{bmatrix},\quad D = \begin{bmatrix}
0 & 0 & i_{do} & i_{qo} \\
0 & 0 & -i_{qo} & i_{do} \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0
\end{bmatrix}. \tag{C.36}$$

The state-space representation of the WFC model shown in Figure 5.4:

$$\Delta x=\begin{bmatrix}\Delta e_{d1} & \Delta e_{q1} & \Delta v_{dc} & \Delta x_{vac}\end{bmatrix}^T$$
$$\Delta u=\begin{bmatrix}\Delta i_{dc} & \Delta v_{ac}^{*} & \Delta e_{d2} & \Delta e_{q2} & \Delta i_d & \Delta i_q & \Delta\theta_m\end{bmatrix}^T,\ \Delta y=\begin{bmatrix}\Delta v_{dc} & \Delta i_{dc} & \Delta v_{ac1} & \Delta v_{d2} & \Delta v_{q2}\end{bmatrix}^T \quad \text{(C.37)}$$

$A=$

$$\begin{bmatrix}\begin{bmatrix}-\frac{L_2 e_{d1o} k_o v_{d1o} v_{dco} K_{p\_vac}+L_m e_{d1o} k_o v_{d1o} v_{dco} K_{p\_vac}+L_t v_{ac1o}}{L_t v_{ac1o}\tau}, \\ -\frac{L_2 e_{d1o} k_o v_{dco} v_{q1o} K_{p\_vac}+L_m e_{d1o} k_o v_{dco} v_{q1o} K_{p\_vac}}{L_t v_{ac1o}\tau}, \frac{e_{d1o} k_o P_{mo}}{\tau}, \frac{e_{d1o} k_o v_{dco}}{\tau}\end{bmatrix}, \\ \begin{bmatrix}-\frac{L_2 e_{q1o} k_o v_{d1o} v_{dco} K_{p\_vac}+L_m e_{q1o} k_o v_{d1o} v_{dco} K_{p\_vac}}{L_t v_{ac1o}\tau}, \\ -\frac{L_2 e_{q1o} k_o v_{dco} v_{q1o} K_{p\_vac}+L_m e_{q1o} k_o v_{dco} v_{q1o} K_{p\_vac}+L_t v_{ac1o}}{L_t v_{ac1o}\tau}, \frac{e_{q1o} k_o P_{mo}}{\tau}, \\ \frac{e_{q1o} k_o v_{dco}}{\tau}\end{bmatrix}, \\ \begin{bmatrix}-\frac{i_{do}}{v_{dco} C}, -\frac{i_{qo}}{v_{dco} C}, \frac{P_{dco}}{C v_{dco}^{\ 2}}, 0\end{bmatrix}, \\ \begin{bmatrix}-\frac{K_{i\_vac}\left(L_2 v_{d1o}+L_m v_{d1o}\right)}{L_t v_{ac1o}}, -\frac{K_{i\_vac}\left(L_2 v_{q1o}+L_m v_{q1o}\right)}{L_t v_{ac1o}}, 0, 0\end{bmatrix}\end{bmatrix}$$

$B=$

$$\begin{bmatrix}\begin{bmatrix}0, \frac{e_{d1o} k_o v_{dco} K_{p\_vac}}{\tau}, -\frac{e_{d1o} k_o L_1 v_{d1o} v_{dco} K_{p\_vac}}{L_t v_{ac1o}\tau}, -\frac{e_{d1o} k_o L_1 v_{dco} v_{q1o} K_{p\_vac}}{L_t v_{ac1o}\tau}, -\frac{1}{L_t v_{ac1o}\tau}(\\ -L_1 R_2 e_{d1o} k_o v_{d1o} v_{dco} K_{p\_vac}-L_1 R_m e_{d1o} k_o v_{d1o} v_{dco} K_{p\_vac}+L_2 R_1 e_{d1o} k_o v_{d1o} v_{dco} K_{p\_vac} \\ +L_m R_1 e_{d1o} k_o v_{d1o} v_{dco} K_{p\_vac}), -\frac{1}{L_t v_{ac1o}\tau}(-L_1 R_2 e_{d1o} k_o v_{dco} v_{q1o} K_{p\_vac} \\ -L_1 R_m e_{d1o} k_o v_{dco} v_{q1o} K_{p\_vac}+L_2 R_1 e_{d1o} k_o v_{dco} v_{q1o} K_{p\_vac} \\ +L_m R_1 e_{d1o} k_o v_{dco} v_{q1o} K_{p\_vac}), \frac{e_{q1o}}{\tau}\end{bmatrix}, \\ \begin{bmatrix}0, \frac{e_{q1o} k_o v_{dco} K_{p\_vac}}{\tau}, -\frac{e_{q1o} k_o L_1 v_{d1o} v_{dco} K_{p\_vac}}{L_t v_{ac1o}\tau}, -\frac{e_{q1o} k_o L_1 v_{dco} v_{q1o} K_{p\_vac}}{L_t v_{ac1o}\tau}, \\ -\frac{1}{L_t v_{ac1o}\tau}(-L_1 R_2 e_{q1o} k_o v_{d1o} v_{dco} K_{p\_vac}-L_1 R_m e_{q1o} k_o v_{d1o} v_{dco} K_{p\_vac} \\ +L_2 R_1 e_{q1o} k_o v_{d1o} v_{dco} K_{p\_vac}+L_m R_1 e_{q1o} k_o v_{d1o} v_{dco} K_{p\_vac}), -\frac{1}{L_t v_{ac1o}\tau}(\\ -L_1 R_2 e_{q1o} k_o v_{dco} v_{q1o} K_{p\_vac}-L_1 R_m e_{q1o} k_o v_{dco} v_{q1o} K_{p\_vac}+L_2 R_1 e_{q1o} k_o v_{dco} v_{q1o} K_{p\_vac} \\ +L_m R_1 e_{q1o} k_o v_{dco} v_{q1o} K_{p\_vac}), -\frac{e_{d1o}}{\tau}\end{bmatrix}, \\ \begin{bmatrix}\frac{1}{C}, 0, 0, 0, -\frac{e_{d1o}}{v_{dco} C}, -\frac{e_{q1o}}{v_{dco} C}, 0\end{bmatrix}, \\ \begin{bmatrix}0, K_{i\_vac}, -\frac{K_{i\_vac} L_1 v_{d1o}}{L_t v_{ac1o}}, -\frac{K_{i\_vac} L_1 v_{q1o}}{L_t v_{ac1o}}, \\ -\frac{K_{i\_vac}\left(-L_1 R_2 v_{d1o}-L_1 R_m v_{d1o}+L_2 R_1 v_{d1o}+L_m R_1 v_{d1o}\right)}{L_t v_{ac1o}}, \\ -\frac{K_{i\_vac}\left(-L_1 R_2 v_{q1o}-L_1 R_m v_{q1o}+L_2 R_1 v_{q1o}+L_m R_1 v_{q1o}\right)}{L_t v_{ac1o}}, 0\end{bmatrix}\end{bmatrix}$$

$$C=\begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ \dfrac{L_2 v_{d1o}+L_m v_{d1o}}{L_t v_{ac10}} & \dfrac{L_2 v_{q1o}+L_m v_{q1o}}{L_t v_{ac1o}} & 0 & 0 \\ \dfrac{L_2}{L_t} & 0 & 0 & 0 \\ 0 & \dfrac{L_2}{L_t} & 0 & 0 \end{bmatrix} \tag{C.38}$$

$$D=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{L_1 v_{d1o}}{L_t v_{ac1o}} & \dfrac{L_1 v_{q1o}}{L_t v_{ac1o}} & \dfrac{L_2 R_1 v_{d1o}+L_m R_1 v_{d1o}-L_1 R_2 v_{d1o}-L_1 R_m v_{d1o}}{L_t v_{ac1o}} & \dfrac{L_2 R_1 v_{q1o}+L_m R_1 v_{q1o}-L_1 R_2 v_{d1o}-L_1 R_m v_{d1o}}{L_t v_{ac1o}} & 0 \\ 0 & 0 & \dfrac{L_1+L_m}{L_t} & 0 & \dfrac{L_2(R_1+R_m)-(L_1+L_m)R_2}{L_t} & 0 & 0 \\ 0 & 0 & 0 & \dfrac{L_1+L_m}{L_m} & 0 & \dfrac{L_2(R_1+R_m)-(L_1+L_m)R_2}{L_t} & 0 \end{bmatrix} \tag{C.39}$$

In order to interconnect the WFC model, the SWF model and the PLL, the state-space model for the WFC is written in the following form:

$$\begin{aligned} \dot{x}_1 &= A_1 x_1 + B_1 u_1 + B_{12} u_{12} + B_{13} u_{13} \\ y_{12} &= C_{12} x_1 + D_{1\_} u_1 + D_{12\_} u_{12} + D_{13\_} u_{13} \\ y_1 &= C_1 x_1 + D_1 u_1 + D_{12} u_{12} + D_{13} u_{13} \end{aligned} \tag{C.40}$$

where

$$\begin{aligned} x_1 &= \begin{bmatrix} e_{d1} & e_{q1} & v_{dc} & x_{vac} \end{bmatrix}^T, \\ y_1 &= \begin{bmatrix} v_{dc} & i_{dc} & v_{ac} \end{bmatrix}^T,\ y_{12} = \begin{bmatrix} v_{d2} & v_{q2} \end{bmatrix}^T \quad . \\ u_1 &= \begin{bmatrix} i_{dc} & v_{acr} \end{bmatrix}^T,\ u_{12} = \begin{bmatrix} e_{d2} & e_{q2} & i_d & i_q \end{bmatrix}^T,\ u_{13} = \theta_m \end{aligned} \tag{C.41}$$

The state-space model for the SWF is represented as:

$$\begin{aligned} \dot{x}_2 &= A_2 x_2 + B_2 u_2 + B_{21} u_{21} \\ y_2 &= C_2 x_2 + D_2 u_2 + D_{21} u_{21} \\ y_{21} &= C_{2\_} x_2 \end{aligned} \tag{C.42}$$

$$\begin{aligned} x_2 &= \begin{bmatrix} e_{d2} & e_{q2} & i_d & i_q & x_{id} & x_{iq} & x_P & x_Q \end{bmatrix}^T \\ u_2 &= \begin{bmatrix} P_{ref} & Q_{ref} \end{bmatrix}^T,\ u_{21} = \begin{bmatrix} v_{d2} & v_{q2} \end{bmatrix}^T \quad . \\ y_2 &= \begin{bmatrix} P_{ac} & Q \end{bmatrix}^T,\ y_{21} = \begin{bmatrix} e_{d2} & e_{q2} & i_d & i_q \end{bmatrix}^T \end{aligned} \tag{C.43}$$

The state-space model for the PLL of the SWF is represented as:

$$\begin{aligned} \dot{x}_3 &= A_3 x_3 + B_{31} u_{31} \\ y_{31} &= C_{31} x_3 \end{aligned} \tag{C.44}$$

where $x_3 = \begin{bmatrix} \Delta x_{pll} & \Delta\theta_m \end{bmatrix}^T$, $u_3 = \begin{bmatrix} \Delta v_{d2} & \Delta v_{q2} \end{bmatrix}$, $y_3 = \Delta\theta_m$.

$$u_{21} = u_3 = y_{12}, \quad u_{12} = y_{21}. \tag{C.45}$$

By eliminating the intermediate variables shown in (C.45), the state-space models shown in (C.40), (C.42) and (C.44) can then be represented as:

$$\begin{aligned} \dot{x}_1 &= A_1 x_1 + B_1 u_1 + B_{12} C_{21} x_2 + B_{13} C_{31} x_3 \\ y_{12} &= C_{12} x_1 + D_{1\_} u_1 + D_{12\_} C_{21} x_2 + D_{13\_} C_{31} x_3 \\ y_1 &= C_1 x_1 + D_1 u_1 + D_{12} C_{21} x_2 + D_{13} C_{31} x_3 \end{aligned} \tag{C.46}$$

$$\begin{aligned} \dot{x}_2 &= B_{21} C_{1\_} x_1 + + \left(A_2 + B_{21} D_{12\_} C_{21} \right) x_2 + B_{21} D_{13\_} C_{31} x_3 + B_{21} D_{1\_} u_1 + B_2 u_2 \\ y_2 &= D_{21} C_{1\_} x_1 + \left(C_2 + D_{21} D_{12\_} C_{21} \right) x_2 + D_{21} D_{13\_} C_{31} x_3 + D_{21} D_{1\_} u_1 + D_2 u_2 \end{aligned} \tag{C.47}$$

$$\begin{aligned} \dot{x}_3 &= A_3 x_3 + B_{31} \left(C_{1\_} x_1 + D_{1\_} u_1 + D_{12\_} C_{21} x_2 + D_{13\_} C_{31} x_3 \right) \\ &= B_{31} C_{1\_} x_1 + B_{31} D_{12\_} C_{21} x_2 + \left(A_3 + B_{31} D_{13\_} C_{31} \right) x_3 + B_{31} D_{1\_} u_1 \end{aligned}. \tag{C.48}$$

The overall state-space model for the WFC terminal is subsequently obtained as:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} A_1 & B_{12} C_{21} & B_{13} C_{31} \\ B_{21} C_{12} & A_2 + B_{21} D_{12\_} C_{21} & B_{21} D_{13\_} C_{31} \\ B_{31} C_{12} & B_{31} D_{12\_} C_{21} & A_3 + B_{31} D_{13\_} C_{31} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} B_1 & 0 \\ B_{21} D_{1\_} & B_2 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} \tag{C.49}$$

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} C_1 & D_{12} C_{21} & D_{13} C_{31} \\ D_{21} C_{12} & C_2 + D_{21} D_{12\_} C_{21} & D_{21} D_{13\_} C_{31} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} D_1 & 0 \\ D_{21} D_{1\_} & D_2 \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} \tag{C.50}$$

C.5 Initial Condition Calculation

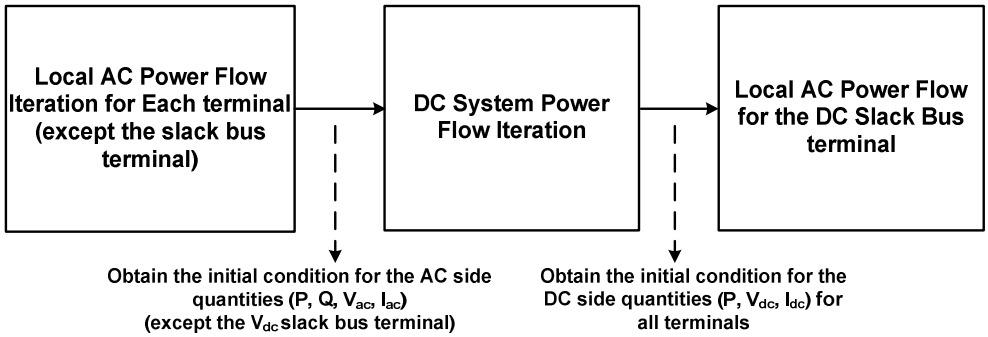

Figure C.1: Power flow calculation procedure for the initial condition computation.

The power flow operating point of the MTDC system needs to be solved in order to perform the initial condition calculation required for the parameterisation of the dynamic mathematical model. The AC/DC power flow procedure shown in Figure C.1 is employed for this purpose. Firstly, the AC system power flow using the Newton-Raphson iteration is performed to solve the AC side quantities of the all the converter terminals except the DC slack bus terminal. Secondly, the DC power flow is performed based on the slack bus voltage and the solved power of the other terminals. Finally, the local AC power flow iteration is used to solve the AC side quantities of the DC slack bus terminal.

Please note that this procedure is designed for a system with lumped AC system representation, while a more complex power flow calculation may be required for a meshed AC system. However, it should be noted that the accuracy of the power flow results is not very strictly demanded by the initial condition calculation.

Based on the power flow results of the MTDC system, the initial condition of the variables required for the construction of the GSC state-space model can be calculated using the following steady-state equations:

$$v_{do} = v_{aco}, \quad v_{qo} = 0 \tag{C.51}$$

$$i_{do} = \frac{v_{do}P_o + v_{qo}Q_o}{v_{do}^2 + v_{qo}^2} = \frac{P_o}{v_{do}}, \quad i_{qo} = \frac{v_{qo}P_o - v_{do}Q_o}{v_{do}^2 + v_{qo}^2} = -\frac{Q_o}{v_{do}} \tag{C.52}$$

$$e_{do} = v_{do} + Ri_{do} - \omega Li_{qo}, \quad e_{qo} = v_{qo} + Ri_{qo} + \omega Li_{qo} \tag{C.53}$$

$$i_{sdo} = i_{do} + \omega C_f v_{qo}, \quad i_{sqo} = i_{qo} - \omega C_f v_{do} \tag{C.54}$$

$$v_{sdo} = v_{do} - R_s i_{sdo} + \omega L_s i_{sqo},\ v_{sqo} = v_{qo} - R_s i_{sqo} - \omega L_s i_{sqo} \tag{C.55}$$

$$x_{Po} = x_{vdco} = i_{do},\ \ x_{Qo} = x_{vaco} = i_{qo} \tag{C.56}$$

$$x_{ido} = e_{do} - v_{do} + \omega L i_{qo},\ \ x_{iqo} = e_{qo} - v_{qo} - \omega L i_{do} \tag{C.57}$$

The initial condition of the variables required for the construction of the WFC state-space model can be calculated using the following steady-state equations:

$$v_{d2o} = v_{ac2o},\ v_{q2o} = 0,\ i_{do} = \frac{P_{wf}^*}{v_{d2o}},\ i_{qo} = \frac{Q_{wf}^*}{v_{d2o}} \tag{C.58}$$

$$e_{d2o} = v_{d2o} + R_2 i_{do} - \omega L_2 i_{qo},\ e_{q2o} = v_{q2o} + R_2 i_{qo} + \omega L_2 i_{do} \tag{C.59}$$

$$e_{d1o} = v_{d2o} - \left(R_1 + R_m\right) i_{do} + \omega\left(L_1 + L_m\right) i_{qo},\quad e_{q1o} = v_{q2o} - \left(R_1 + R_m\right) i_{qo} - \omega\left(L_1 + L_m\right) i_{do} \tag{C.60}$$

$$v_{d1o} = v_{d2o} - R_m i_{do} + \omega L_m i_{qo},\ \ v_{q1o} = v_{q2o} - R_m i_{qo} - \omega L_m i_{do} \tag{C.61}$$

$$v_{ac1o} = \sqrt{e_{d1o}^2 + e_{q1o}^2},\quad P_{mo} = v_{ac1o} / \left(v_{dco} k_o\right) \tag{C.62}$$

C.6 Verification of the Analytical Model of the Four-terminal System

The validity of the state-space (SS) model of the four-terminal MTDC system is evaluated by comparing the step response results generated by this analytical model and the dynamic simulations performed in DIgSILENT PowerFactory. Some results of the comparative study are shown in Figure C.2 to Figure C.7, where the step responses of various quantities to the step change of the power reference of GSC1 are illustrated. It should be noted that a small step (0.01 pu) of P_{ref1} is performed in the simulations, and the results are scaled appropriately to compare with the step responses generated by the state-space model.

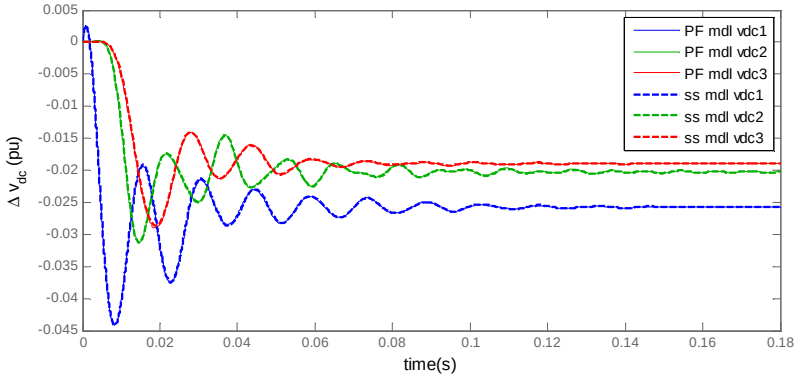

Figure C.2: Δv_{dc} responses to the step of ΔP_{ref1} (all GSCs in droop V_{dc}-P and constant Q control).

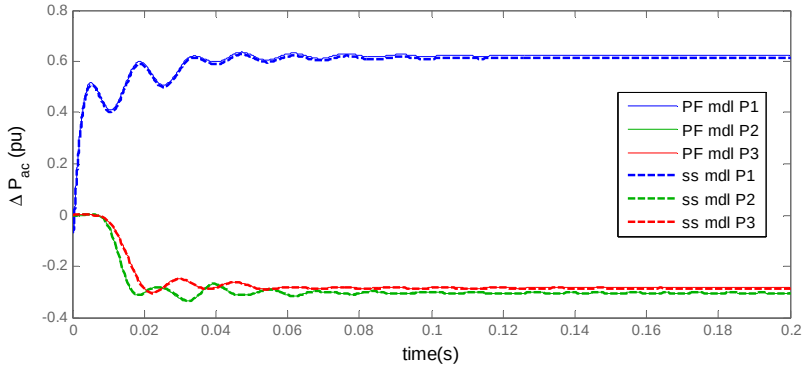

Figure C.3: ΔP_{ac} responses to the step of ΔP_{ref1} (all GSCs in V_{dc}-P droop and constant Q control).

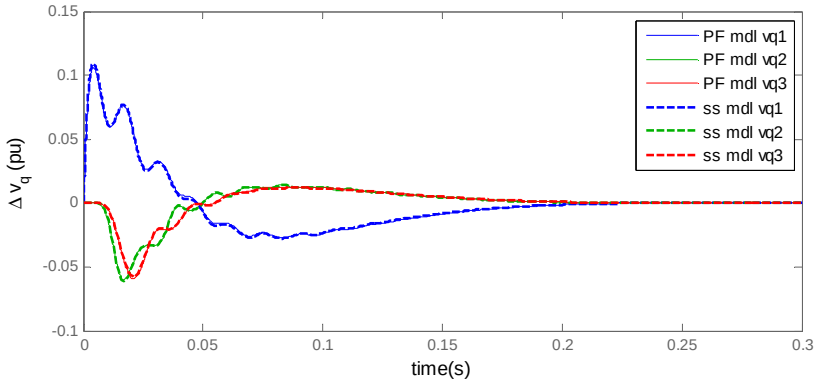

Figure C.4: Δv_q responses to the step of ΔP_{ref1} (all GSCs in V_{dc}-P droop and constant Q control).

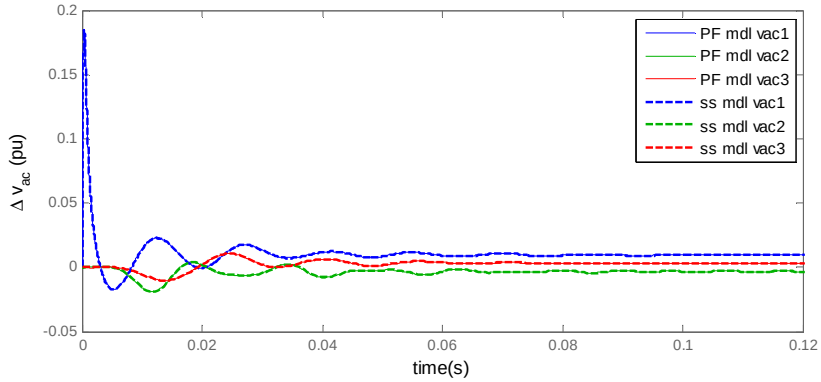

Figure C.5: Δv_{ac} responses to the step of ΔP_{ref1} (all GSCs in V_{dc}-P droop and V_{ac}-Q droop control).

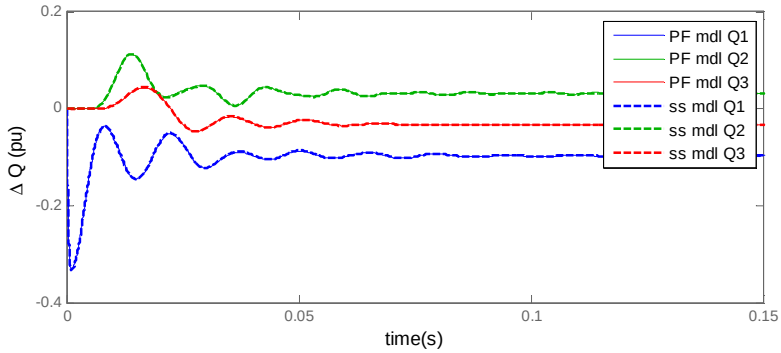

Figure C.6: ΔQ responses to the step of ΔP_{ref1} (all GSCs in V_{dc}-P droop and V_{ac}-Q droop control).

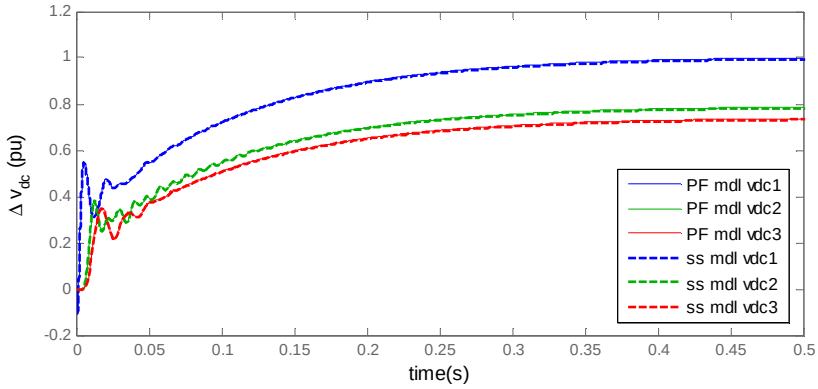

Figure C.7: Δv_{dc} responses to the step of Δv_{dcref1} (GSC1: constant V_{dc} control, V_{ac}-Q droop control; GSC2 and GSC3: V_{dc}-P droop control, V_{ac}-Q droop control).

C.7 Selected Participation Factors

Table C.1: The participation variables and participation factors for the base-case four-terminal model shown in Figure 5.9.

Eigenvalues	Top four participation variables				Participation factors			
-1.9919+1299.8i	'vC2 Line2'	'i(out) Line2'	'i(in) Line2'	'vC1 Line2'	1.0000	0.8289	0.8244	0.3539
-1.9919-1299.8i	'vC2 Line2'	'i(out) Line2'	'i(in) Line2'	'vC1 Line2'	1.0000	0.8289	0.8244	0.3539
-3.9224+762.36i	'i(in) Line3'	'i(out) Line3'	'vC4 Line3'	'vC3 Line3'	1.0000	0.8873	0.5622	0.5490
-3.9224-762.36i	'i(in) Line3'	'i(out) Line3'	'vC4 Line3'	'vC3 Line3'	1.0000	0.8873	0.5622	0.5490
-5.0483+817.38i	'i(out) Line1'	'i(in) Line1'	'vC3 Line1'	'vC4 Line1'	1.0000	0.8963	0.5233	0.5117
-5.0483-817.38i	'i(out) Line1'	'i(in) Line1'	'vC3 Line1'	'vC4 Line1'	1.0000	0.8963	0.5233	0.5117
-8.379+1760i	'iL3 Line3'	'vC2 Line3'	'vC5 Line3'	'iL4 Line3'	1.0000	0.8762	0.8762	0.4780
-8.379-1760i	'iL3 Line3'	'vC2 Line3'	'vC5 Line3'	'iL4 Line3'	1.0000	0.8762	0.8762	0.4780
-8.5228+1846.2i	'iL3 Line1'	'vC5 Line1'	'vC2 Line1'	'iL2 Line1'	1.0000	0.8688	0.8678	0.4865
-8.5228-1846.2i	'iL3 Line1'	'vC5 Line1'	'vC2 Line1'	'iL2 Line1'	1.0000	0.8688	0.8678	0.4865
-9.2369+3755.7i	'vC3 Line2'	'vC1 Line2'	'iL2 Line2'	'iL1 Line2'	1.0000	1.0000	0.7527	0.7527
-9.2369-3755.7i	'vC3 Line2'	'vC1 Line2'	'iL2 Line2'	'iL1 Line2'	1.0000	1.0000	0.7527	0.7527
-10.425+2868.3i	'iL4 Line3'	'iL2 Line3'	'vC3 Line3'	'vC4 Line3'	1.0000	1.0000	0.6099	0.6098
-10.425-2868.3i	'iL4 Line3'	'iL2 Line3'	'vC3 Line3'	'vC4 Line3'	1.0000	1.0000	0.6099	0.6098
-10.504+3024.5i	'iL4 Line1'	'iL2 Line1'	'vC3 Line1'	'vC4 Line1'	1.0000	1.0000	0.6150	0.6149
-10.504-3024.5i	'iL4 Line1'	'iL2 Line1'	'vC3 Line1'	'vC4 Line1'	1.0000	1.0000	0.6150	0.6149
-11.06+4441.6i	'iL1 Line3'	'iL5 Line3'	'vC1 Line3'	'vC6 Line3'	1.0000	0.9999	0.7412	0.7411
-11.06-4441.6i	'iL1 Line3'	'iL5 Line3'	'vC1 Line3'	'vC6 Line3'	1.0000	0.9999	0.7412	0.7411
-11.097+3804.6i	'iL3 Line3'	'vC4 Line3'	'vC3 Line3'	'vC1 Line3'	1.0000	0.7213	0.7212	0.4378
-11.097-3804.6i	'iL3 Line3'	'vC4 Line3'	'vC3 Line3'	'vC1 Line3'	1.0000	0.7213	0.7212	0.4378
-11.105+4807.7i	'iL2 Line2'	'iL1 Line2'	'vC2 Line2'	'vC3 Line2'	1.0000	1.0000	0.9186	0.6365
-11.105-4807.7i	'iL2 Line2'	'iL1 Line2'	'vC2 Line2'	'vC3 Line2'	1.0000	1.0000	0.9186	0.6365
-11.133+4691i	'iL1 Line1'	'iL5 Line1'	'vC1 Line1'	'vC6 Line1'	1.0000	0.9999	0.7294	0.7293
-11.133-4691i	'iL1 Line1'	'iL5 Line1'	'vC1 Line1'	'vC6 Line1'	1.0000	0.9999	0.7294	0.7293
-11.146+4018.4i	'iL3 Line1'	'vC4 Line1'	'vC3 Line1'	'vC1 Line1'	1.0000	0.7177	0.7176	0.4443
-11.146-4018.4i	'iL3 Line1'	'vC4 Line1'	'vC3 Line1'	'vC1 Line1'	1.0000	0.7177	0.7176	0.4443
-11.485+4578.8i	'iL5 Line3'	'iL1 Line3'	'vC5 Line3'	'vC2 Line3'	1.0000	1.0000	0.7698	0.7698
-11.485-4578.8i	'iL5 Line3'	'iL1 Line3'	'vC5 Line3'	'vC2 Line3'	1.0000	1.0000	0.7698	0.7698
-11.538+4840.8i	'iL5 Line1'	'iL1 Line1'	'vC5 Line1'	'vC2 Line1'	1.0000	0.9997	0.7821	0.7819
-11.538-4840.8i	'iL5 Line1'	'iL1 Line1'	'vC5 Line1'	'vC2 Line1'	1.0000	0.9997	0.7821	0.7819
-15.972+353.05i	'vdc T4'	'vdc T2'	'i(in) Line2'	'i(out) Line2'	1.0000	0.4660	0.3403	0.3146
-15.972-353.05i	'vdc T4'	'vdc T2'	'i(in) Line2'	'i(out) Line2'	1.0000	0.4660	0.3403	0.3146
-23.683+0i	'xpll T1'	'theta_m T1'	'xvac T1'	'iq T1'	1.0000	0.5305	0.0468	0.0179
-28.55+186.77i	'vdc T1'	'vdc T3'	'xP T3'	'i(out) Line1'	1.0000	0.8280	0.5191	0.4231
-28.55-186.77i	'vdc T1'	'vdc T3'	'xP T3'	'i(out) Line1'	1.0000	0.8280	0.5191	0.4231
-29.885+4.2571i	'x_pll T4'	'theta_m T4'	'iq T4'	'xQ T4'	1.0000	0.9710	0.0218	0.0077
-29.885-4.2571i	'x_pll T4'	'theta_m T4'	'iq T4'	'xQ T4'	1.0000	0.9710	0.0218	0.0077
-30.178+3.8234i	'xpll T2'	'theta_m T2'	'xpll T3'	'theta_m T3'	1.0000	0.9818	0.1343	0.1318
-30.178-3.8234i	'xpll T2'	'theta_m T2'	'xpll T3'	'theta_m T3'	1.0000	0.9818	0.1343	0.1318
-30.812+2.1675i	'theta_m T3'	'xpll T3'	'theta_m T2'	'xpll T2'	1.0000	0.9990	0.1384	0.1382
-30.812-2.1675i	'theta_m T3'	'xpll T3'	'theta_m T2'	'xpll T2'	1.0000	0.9990	0.1384	0.1382
-33.599+231.1i	'vdc T2'	'vdc T3'	'xP T2'	'xP T3'	1.0000	0.7362	0.5013	0.3392
-33.599-231.1i	'vdc T2'	'vdc T3'	'xP T2'	'xP T3'	1.0000	0.7362	0.5013	0.3392

-44.008+22.474i	'theta_m T1'	'xvac T1'	'xpll T1'	'xP T1'	1.0000	0.4395	0.4261	0.1380
-44.008-22.474i	'theta_m T1'	'xvac T1'	'xpll T1'	'xP T1'	1.0000	0.4395	0.4261	0.1380
-47.159+82.173i	'xP T2'	'vdc T1'	'xP T3'	'vdc T4'	1.0000	0.8696	0.8495	0.5596
-47.159-82.173i	'xP T2'	'vdc T1'	'xP T3'	'vdc T4'	1.0000	0.8696	0.8495	0.5596
-67.266+0i	'xP T2'	'xP T3'	'theta_m T3'	'xQ T3'	1.0000	0.9980	0.3120	0.2717
-126.5+22.721i	'xP T4'	'xvac T4'	'xQ T4'	'theta_m T4'	1.0000	0.8590	0.7454	0.0955
-126.5-22.721i	'xP T4'	'xvac T4'	'xQ T4'	'theta_m T4'	1.0000	0.8590	0.7454	0.0955
-137.76+0i	'xQ T3'	'iq T3'	'theta_m T3'	'xiq T3'	1.0000	0.0823	0.0799	0.0570
-144.03+0i	'xP T1'	'xvac T1'	'id T1'	'theta_m T1'	1.0000	0.2053	0.1502	0.0644
-180.31+0i	'xvac T4'	'xQ T4'	'xP T4'	'id T4'	1.0000	0.2283	0.2228	0.1194
-326.76+0i	'xiq T2'	'xQ T2'	'iq T2'	'xid T2'	1.0000	0.4658	0.1677	0.0281
-527.75+0i	'xid T4'	'id T4'	'xP T4'	'ed2 T4'	1.0000	0.2706	0.0578	0.0307
-575.03+0i	'xiq T4'	'iq T4'	'xQ T4'	'eq2 T4'	1.0000	0.4883	0.1996	0.0719
-637.97+0i	'xiq T1'	'iq T1'	'xid T1'	'eq T1'	1.0000	0.5716	0.0824	0.0626
-751.35+0i	'xid T3'	'id T3'	'ed T3'	'xP T3'	1.0000	0.8249	0.0763	0.0748
-754.99+260.43i	'id T2'	'xid T2'	'iq T2'	'xiq T2'	1.0000	0.9202	0.2174	0.1768
-754.99-260.43i	'id T2'	'xid T2'	'iq T2'	'xiq T2'	1.0000	0.9202	0.2174	0.1768
-776.45+1128i	'iq T2'	'xQ T2'	'xiq T2'	'id T2'	1.0000	0.5582	0.3195	0.2440
-776.45-1128i	'iq T2'	'xQ T2'	'xiq T2'	'id T2'	1.0000	0.5582	0.3195	0.2440
-825.77+429.21i	'id T1'	'xid T1'	'xP T1'	'ed T1'	1.0000	0.5811	0.2920	0.1375
-825.77-429.21i	'id T1'	'xid T1'	'xP T1'	'ed T1'	1.0000	0.5811	0.2920	0.1375
-825.82+384.3i	'iq T3'	'xiq T3'	'xQ T3'	'eq T3'	1.0000	0.6378	0.2519	0.1197
-825.82-384.3i	'iq T3'	'xiq T3'	'xQ T3'	'eq T3'	1.0000	0.6378	0.2519	0.1197
-1156.1+0i	'id T3'	'xid T3'	'ed T3'	'iq T3'	1.0000	0.5692	0.1481	0.0887
-1644.1+0i	'iq T1'	'xiq T1'	'eq T1'	'xvac T1'	1.0000	0.3246	0.2947	0.0566
-2307+1814.1i	'iq T4'	'eq2 T4'	'id T4'	'ed2 T4'	1.0000	0.7563	0.1817	0.1527
-2307-1814.1i	'iq T4'	'eq2 T4'	'id T4'	'ed2 T4'	1.0000	0.7563	0.1817	0.1527
-2962.4+2266i	'id T4'	'ed2 T4'	'iq T4'	'eq2 T4'	1.0000	0.9875	0.2370	0.2196
-2962.4-2266i	'id T4'	'ed2 T4'	'iq T4'	'eq2 T4'	1.0000	0.9875	0.2370	0.2196
-3985.7+0i	'eq T1'	'iq T1'	'ed T1'	'id T1'	1.0000	0.8374	0.6240	0.2913
-6170.8+0i	'ed T1'	'eq T1'	'id T1'	'iq T1'	1.0000	0.7800	0.3328	0.1081
-6287.7+989.33i	'ed T2'	'eq T2'	'iq T2'	'id T2'	1.0000	0.9778	0.3160	0.3120
-6287.7-989.33i	'ed T2'	'eq T2'	'iq T2'	'id T2'	1.0000	0.9778	0.3160	0.3120
-6881.1+420.89i	'ed T3'	'eq T3'	'iq T3'	'id T3'	1.0000	0.9673	0.2801	0.2790
-6881.1-420.89i	'ed T3'	'eq T3'	'iq T3'	'id T3'	1.0000	0.9673	0.2801	0.2790
-19997+0i	'eq1 T4'	'ed1 T4'	'eq2 T4'	'theta_m T4'	1.0000	0.0129	0.0010	0.0001
-21853+0i	'ed1 T4'	'ed2 T4'	'eq1 T4'	'xvac T4'	1.0000	0.0330	0.0132	0.0041

C.8 State-Space Type1 GSC Model Used in Chapter 6

$$
\begin{aligned}
u &= \begin{bmatrix} \Delta i_d^* & \Delta i_q^* & \Delta v_s & \Delta \theta_s & \Delta i_{dc} \end{bmatrix}^T \\
y &= \begin{bmatrix} \Delta v_{dc} & \Delta P_{pcc} & \Delta P_{vsc} & \Delta Q & \Delta v_{ac} & \Delta i_d & \Delta i_q \end{bmatrix}^T \\
x &= \begin{bmatrix} \Delta i_d & \Delta i_q & \Delta i_{sd} & \Delta i_{sq} & \Delta x_{id} & \Delta x_{iq} & \Delta v_d & \Delta v_q & \Delta e_d & \Delta e_q & \Delta x_{pll} & \Delta \theta_m & \Delta v_{dc} \end{bmatrix}^T
\end{aligned}
\tag{C.63}
$$

$$
A = \begin{bmatrix}
-\frac{R}{L} & \omega & 0 & 0 & 0 & 0 & -\frac{1}{L} & 0 & \frac{1}{L} & 0 & 0 & 0 & 0 \\
-\omega & -\frac{R}{L} & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L} & 0 & \frac{1}{L} & 0 & 0 & 0 \\
0 & 0 & -\frac{R_s}{L_s} & \omega & 0 & 0 & \frac{1}{L_s} & 0 & 0 & 0 & 0 & -\frac{v_{sqo}}{L_s} & 0 \\
0 & 0 & -\omega & -\frac{R_s}{L_s} & 0 & 0 & 0 & \frac{1}{L_s} & 0 & 0 & 0 & \frac{v_{sdo}}{L_s} & 0 \\
-K_i^{id} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -K_i^{iq} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 & 0 & 0 & 0 & \omega & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 & 0 & -\omega & 0 & 0 & 0 & 0 & 0 & 0 \\
-\frac{K_p^{id}}{\tau_v} & -\frac{\omega L}{\tau_v} & 0 & 0 & \frac{1}{\tau_v} & 0 & \frac{1}{\tau_v} & 0 & -\frac{1}{\tau_v} & 0 & 0 & 0 & 0 \\
\frac{\omega L}{\tau_v} & -\frac{K_p^{iq}}{\tau_v} & 0 & 0 & 0 & \frac{1}{\tau_v} & 0 & \frac{1}{\tau_v} & 0 & -\frac{1}{\tau_v} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & K_i^{pll} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & K_p^{pll} & 0 & 0 & 1 & 0 & 0 \\
-\frac{e_{do}}{v_{dco}C_{dc}} & -\frac{e_{qo}}{v_{dco}C_{dc}} & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{i_{do}}{v_{dco}C_{dc}} & -\frac{i_{qo}}{v_{dco}C_{dc}} & 0 & 0 & \frac{P_o}{C_{dc}v_{dco}^2}
\end{bmatrix}
\tag{C.64}
$$

$$
B = \begin{bmatrix}
0 & 0 & 0 & 0 & K_i^{id} & 0 & 0 & 0 & \frac{K_p^{id}}{\tau_v} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & K_i^{iq} & 0 & 0 & 0 & \frac{K_p^{iq}}{\tau_v} & 0 & 0 & 0 \\
0 & 0 & -\frac{v_{sdo}}{L_s} & -\frac{v_{sqo}}{L_s} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\frac{v_{sqo}}{L_s} & -\frac{v_{sdo}}{L_s} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{dc}}
\end{bmatrix}^T
\tag{C.65}
$$

$$C=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ v_{do} & v_{qo} & 0 & 0 & 0 & 0 & i_{do} & i_{qo} & 0 & 0 & 0 & 0 & 0 \\ e_{do} & e_{qo} & 0 & 0 & 0 & 0 & 0 & 0 & i_{do} & i_{qo} & 0 & 0 & 0 \\ v_{qo} & -v_{do} & 0 & 0 & 0 & 0 & -i_{qo} & i_{do} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{v_{do}}{v_{aco}} & \frac{v_{qo}}{v_{aco}} & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.66}$$

$$D=zeros(7,5) \tag{C.67}$$

C.9 Open-Loop State-Space GSC Model Used in Chapter 7

$$A_j=\begin{bmatrix} -\frac{1}{\tau_v} & \frac{1-K_p^P K_p^{id} i_{do}}{\tau_v} & \frac{-K_p^P K_p^{id} v_{do}-K_p^{id}}{\tau_v} & 0 & \frac{1}{\tau_v} & \frac{K_p^{id}}{\tau_v} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & 0 \\ \frac{1}{L} & -\frac{1}{L} & -\frac{R}{L} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L_s} & 0 & -\frac{R_s}{L_s} & 0 & 0 & 0 & 0 & 0 \\ 0 & -K_i^P i_{do} K_i^{id} & -\left(K_p^P v_{do}+1\right)K_i^{id} & 0 & 0 & K_i^{id} & 0 & 0 & 0 \\ 0 & -K_i^P i_{do} & -K_i^P v_{do} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{i_{do}}{v_{dco}C} & -\frac{v_{do}}{v_{dco}C} & 0 & 0 & 0 & \frac{P_o}{Cv_{dco}^2} & 0 & \frac{1}{C} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_o} \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_a} & \frac{1}{L_a} & -\frac{R_a}{L_a} \end{bmatrix} \tag{C.68}$$

$$B_{jG}=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_o} & 0 \end{bmatrix}^T \tag{C.69}$$

$$B_j=\begin{bmatrix} \frac{K_p^P K_p^{id}}{\tau_v} & 0 & 0 & 0 & K_p^P K_i^{id} & K_i^P & 0 & 0 & 0 \end{bmatrix}^T \tag{C.70}$$

Appendix D AC Fault Studies of MTDC

The AC fault studies presented in this section were performed using the four-terminal test system shown in Figure 2.32. The nominal droop and other control settings of the test system are illustrated in Figure D.1 and Table D.1. This work formed part of [60].

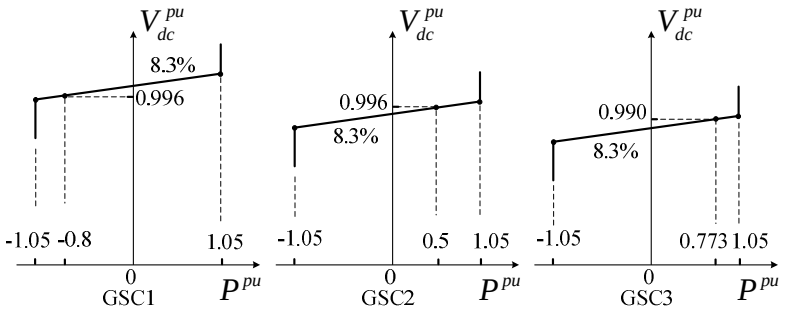

Figure D.1: Droop characteristics for the three GSCs of the test system.

Table D.1: Default settings for the controllers to be studied

Control mode	V_{dc}	PLL	V_{ac}/Q	i_d/i_q	P/Q
Setting	V-P Droop	10 Hz SRF	droop V_{ac}-Q	250 Hz (PI)	25 Hz (PI)

D.1 Impact of Inverter Operation

The pre-fault power level of the faulted terminal could strongly affect how severely the AC fault perturbs the system. If an AC fault with a low fault impedance occurs in a heavily loaded MTDC system, the faulted terminal is likely to operate in its current limit mode during the fault. In terms of transient performance, the clearance of an AC fault could be a much worse scenario than the occurrence of the fault.

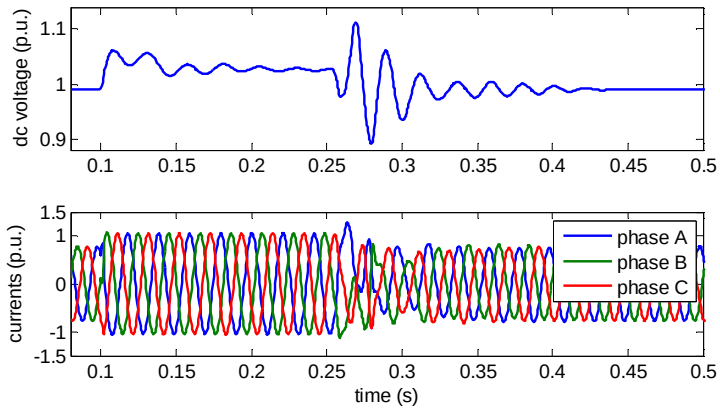

Figure D.2: Responses of DC voltage and phase currents of GSC3 to a fault at PCC3 (fault impedance: 4 Ω).

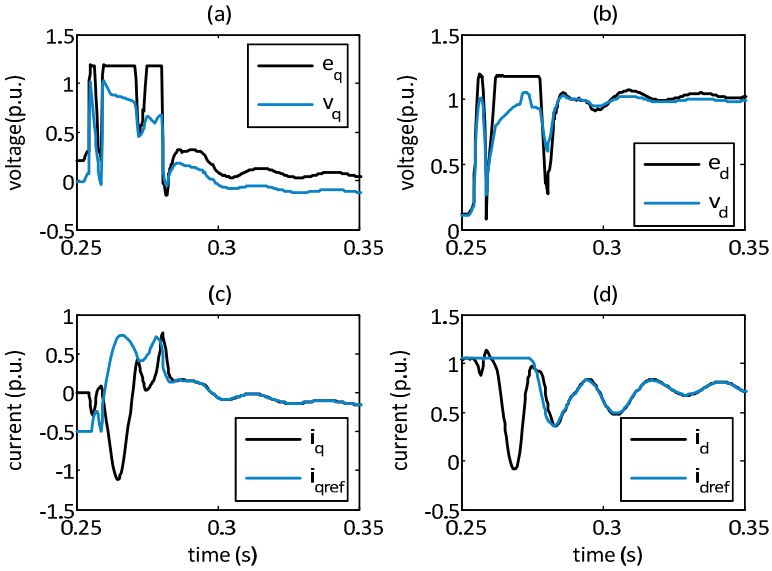

Figure D.3: Responses of the d-axis and q-axis voltages and currents of GSC3 to the clearance of the fault at PCC3 (fault impedance: 4 Ω).

The dynamic behaviours of terminal 3, which is the inverter with the largest power transfer in the system, in response to an AC fault at PCC3 are shown in Figure D.2 and Figure D.3. Overcurrent and DC overvoltage protections have been turned off to obtain the natural responses. As shown in Figure D.2, when the fault is cleared, the currents and the DC voltage rise fiercely and would have triggered the converter protection. The FRT requirement of this system is not satisfied in this case.

This severe transient problem is mainly due to the saturations of the converter voltage and the reliance of the current control on the PLL, as shown in Figure D.3. In the first a few cycles since the fault clearance starts, the voltage at the PCC is unbalanced and this acts as a disturbance to the PLL and induces large value of v_q. Together with the d-axis current of the faulted inverter reaching its maximum value, the q-axis converter voltage cannot overtake the term (v_q+$\omega L i_d$), and this causes i_q to decrease rapidly, as shown in (D.1). As i_q becomes negative and causes AC overvoltage, the d-axis voltage e_d reaches its maximum limit, shown in (D.2), and the current of both axes are no longer controlled until the i_d decreases to a sufficiently small value and the PLL recovers.

According to (D.3), the large negative values of i_d and i_q cause sudden rise of rectifying power and induce DC overvoltage.

$$e_q - \omega L i_d - v_q = L\frac{di_q}{dt} + Ri_q \tag{D.1}$$

$$e_d + \omega L i_q - v_d = L\frac{di_d}{dt} + Ri_d \tag{D.2}$$

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} v_d & v_q \\ v_q & -v_d \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{D.3}$$

For rectifier operations, the large v_q created due to the fault clearance is not such a severe issue, as the voltage e_q is much less likely to be saturated due to the negative $\omega L i_d$. A series tests have been performed for rectifier operations and robust performances to the PLL malfunction have been obtained.

D.2 Impact of PLL and Reactive Power Control

For the PLL control with three different bandwidths, the responses to a low-impedance AC fault at PCC1 and a high-impedance fault at PCC2 are shown in Figure D.4 and Figure D.5 respectively. A PLL of higher bandwidth is supposed to provide better disturbance rejection and faster reference tracking. However, the worst performance for the clearance of the fault at the PCC1 is given by the 30-Hz-bandwidth PLL, which produces large and slow oscillations of active and reactive powers, shown in Figure D.4. This is mainly due to the fact that the increased bandwidth deteriorates the PLL's robustness to the voltage distortions. For the high-impedance fault at the inverter side PCC2, as anticipated the slowest and the most oscillatory performance is provided by the PLL with the lowest bandwidth, as shown in Figure D.5. A comparison of the two responses with the 3.5Hz-bandwidth PLL also shows that a fault with lower fault impedance does not necessarily represent a worse case. Actually, the behaviours of the PLL under AC fault conditions are not only determined by the controller design itself but also severely affected by the combined effect of the fault impedance, the AC system strength, the converter operating point, etc. Therefore more advanced PLL designs with improved robustness and performance may be required for practical VSC installations.

With the four types of V_{ac}/Q controllers implemented, the performances of GSC3 in response to a three-phase fault at PCC3 are compared in Figure D.6. The reactive power reference of 0 is employed by the two reactive power control methods. The d-axis and q-axis currents are limited independently in this case in order to observe the natural response of these reactive power controllers. During the fault, the q-axis current for all the three PI/P-based V_{ac}/Q controllers operates in its lower limit as the converter tries to maintain the PCC voltage. However, for this low-impedance fault, very limited amount of reactive power is injected by the VSC with maximum reactive current. Within a short period since the fault is cleared, the AC voltage controls are likely not to be sufficiently

fast to reduce the reactive current, and this may cause converter voltage saturations and uncontrolled large transients. Fast recovery of the converter control system can be provided by the feedforward Q control as the reactive current i_q is kept around 0 during the fault. However, this feedforward control is not recommended due to its relatively poor robustness. In addition, similar fault behaviours will be obtained if the active current control is prioritised over the reactive current.

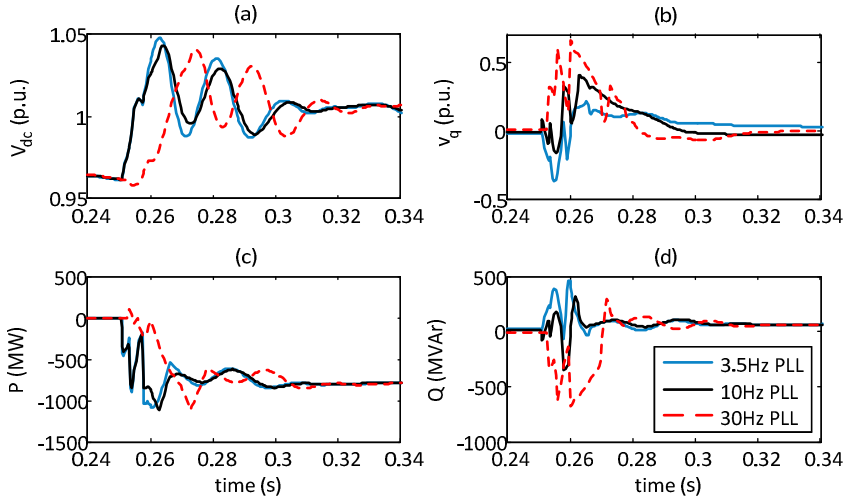

Figure D.4: Impact of the PLL bandwidth on the responses to the fault clearance (fault location: PCC1, fault impedance: 1 Ω).

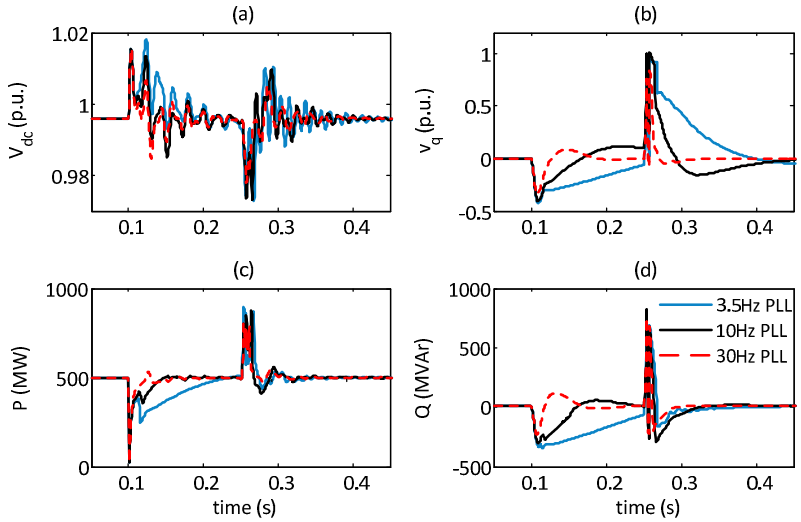

Figure D.5: Impact of the PLL bandwidth on the responses to the fault clearance (fault location: PCC2, fault impedance: 20 Ω).

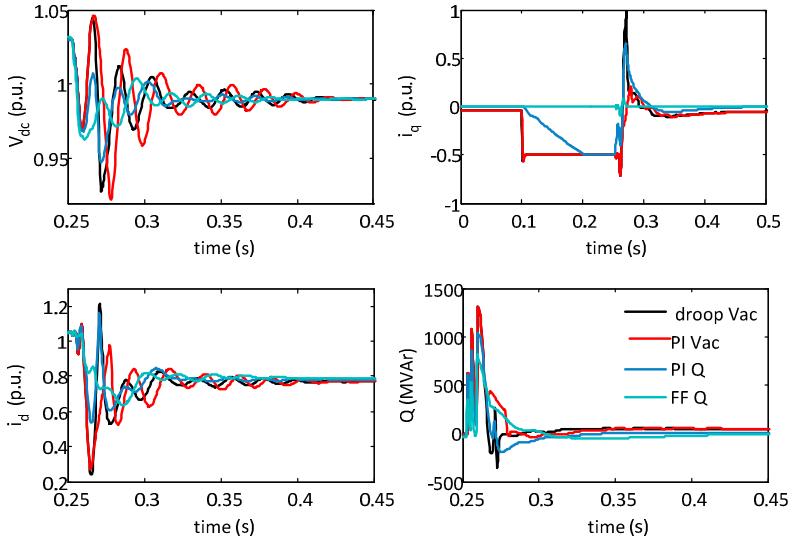

Figure D.6: Impact of reactive power controllers on the AC grid fault responses of GSC3 (fault location: PCC3, fault impedance: 2 Ω)

D.3 Performance of the Adaptive Current Limit

Comparisons of the responses of GSC3 with and without the adaptive current limit are presented in Figure D.7 and Figure D.8. The identical AC fault event for the simulation shown in section 4.2 is performed here. When the fault is cleared at 0.25s, due to the PLL struggling to track and the sudden rise of v_q, the adaptive current is activated and the d-axis current is controlled very tightly to a small value by the fast current controller. Shown in Figure D.8, unlike the fixed current limit scenario where severe transients occur due to the saturation of both d-axis and q-axis current control, much more damped and stable performances are obtained through the adaptive current control and a rate limiter. Furthermore, all the voltage and current quantities are maintained well below their protection limits. During the period when the adaptive limit is in operation, the MTDC system relies on other GSCs to maintain the DC voltage. It should be noted that, under unbalanced fault conditions, the phase currents may violate their thresholds, even if the currents in dq frames are well limited.

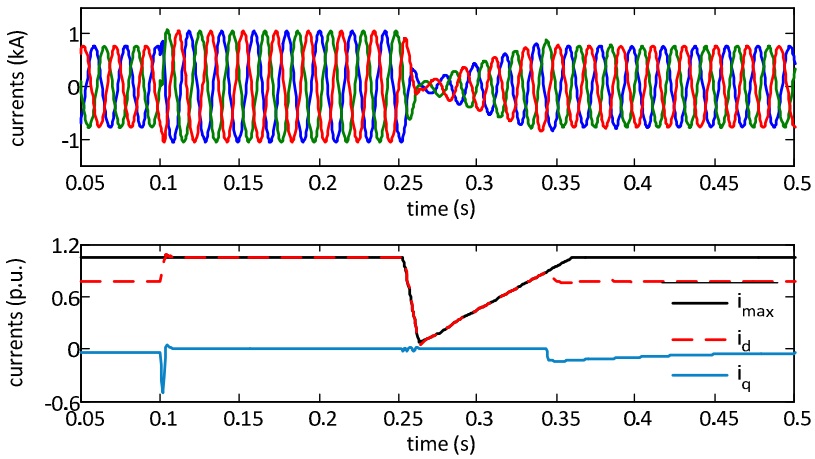

Figure D.7: Response of the GSC3 currents to the fault at the bus PCC3, with the adaptive current limit applied (fault impedance: 4 Ω).

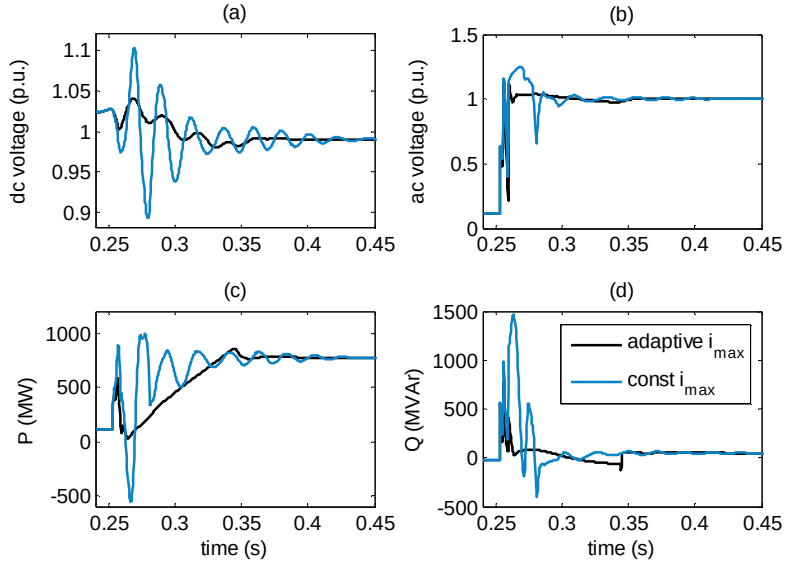

Figure D.8: Response of voltages and powers of GSC3 with the adaptive current limit applied (fault location: PCC3, fault impedance: 4 Ω).