FABRICATION AND CHARACTERISATION OF 3D MULTILAYER CIRCUITS FOR COMPACT MMIC APPLICATIONS

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Abstract

The expansion of the market for wireless communications and sensors has led to the recent increase in demand for highly integrated MMICs for millimetre-wave wireless applications. These applications require MMICs that offer low cost, high integration, high functionality and high performance as well as simpler, more rapid development. An effective way of meeting these requirements and realising highly integrated MMICs is by employing multilayer three-dimensional (3-D) MMIC technology. The research work described in this thesis presents the modelling and characterisation of newly developed passive components such as coplanar waveguides (CPWs), thin-film microstrips (TFMSs) and transition transmission line structures using 3-D multilayer technology. These structures have been developed with low losses in mind, along with variable characteristic impedances and miniaturised size. With the knowledge obtained from the design and optimisation of CPW and TFMS transmission lines, new and improved compact CPW-to-TFMS transitions have been successfully achieved. Accurate electromagnetic modelling was carried out using the 2.5-dimensional ADS Momentum simulator. Newly improved fabrication techniques were employed to produce reported compact microwave components and circuits, in order to lower cost and simplify the process. Compact MMIC components were fabricated using a seven-layer fabrication procedure on semi-insulating GaAs substrate where pseudomorphic high electron mobility transistors (pHEMTs) pre-fabricated by the manufacturer. High frequency on-wafer RF measurements were carried out using Agilent 8510 series vector network analysers (VNAs). In-depth analysis and comparisons between the simulated and measured results are provided. Analysis of active MMIC components was achieved by developing small-signal equivalent circuits of the GaAs pHEMTs, and knowledge extracted from this analysis was employed in the development of large signal models of the pHEMT devices. Furthermore, the design and characterisation of a few MMIC circuits, such as limiters and amplifiers, demonstrates the integration of multilayer CPW passive components with prefabricated pHEMTs. These components are compatible with RF systems-on-chip sub-systems providing low cost, low loss performance with their ease of fabrication.

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List of Publications

[1] **P. B. K. Kyabaggu**, A. A. Rezazadeh, "3D Multilayer Heterogeneously Integrated Systems-On-Chip," *EEE Postgraduate Poster Conference, The University of Manchester*, November 2010.

[2] **P. B. K. Kyabaggu**, E. Sinulingga, M. M. Ali, Q. Sun and A. A. Rezazadeh, "Wideband 3D Coplanar Waveguide to Thin-Film Microstrip Transition in Multilayer Technology," *European Microwave Integrated Circuits Conference*, Manchester, October 2011, pp. 604-607.

[3] E. P. Sinulingga, **P. B. K. Kyabaggu** and A. A. Rezazadeh, "Dispersion Characteristics and Loss Analysis of Low-Impedance 3D Interconnects for Compact MMIC," *UK Semiconductor Conference*, Sheffield, July 2011.

[4] M. Mohammed-Ali, **P. B. K. Kyabaggu**, E. Sinulingga and A. A. Rezazadeh, "Nonlinearity Study of Double and Single Channel GaAs HEMTs*," European Microwave Integrated Circuits Conference, 2011 IEEE 6th,*, Manchester, October 2011, pp. 362 – 365.

[5] **P. B. K. Kyabaggu**, E. Sinulingga and A. A. Rezazadeh, "Design and Realisation of 3D Multilayer Components for Compact MMIC Applications," *EEE Postgraduate Poster Conference, The University of Manchester*, November 2012.

[6] E. P. Sinulingga, **P. B. K. Kyabaggu** and A. A. Rezazadeh, "A Sub-THz Parameter Extraction of Low Loss 3D Compact Multilayer MMIC Coplanar Waveguides," *UK Semiconductor Conference*, Sheffield, July 2014.

[7] M. A. Alim, A. A. Rezazadeh, M. M. Ali, E. P. Sinulingga, **P. B. K. Kyabaggu**, Y. Zhang and C. Gaquiere, " Thermal Characterisation of AlGaN/GaN HEMTs on Silicon Carbide Substrate for High Frequency Application," *Proceedings of European Microwave Week Conference*, Rome, October 2014, pp. 210-213.

[8] Y. Zhang, A. A. Rezazadeh, H. A. Khan, E. P. Sinulingga, **P. B. K. Kyabaggu** and M. A. Alim, "Simulation and Analysis of InGaP/GaAs DHPTs using Eye Diagrams for Short Wavelength Optical Detection," *Proceedings of European Microwave Week Conference*, Rome, October 2014, pp. 524-527.

[9] **P. B. K. Kyabaggu**, E. P. Sinulingga, N. Haris and A. A. Rezazadeh, "Design and Realisation of 3D Multilayer Components for Compact MMIC Applications," *The University of Manchester Postgraduate Summer Research Showcase*, June 2014.

[11] **P. B. K. Kyabaggu,** N. Haris, A. A. Rezazadeh and E. P. Sinulingga, "Design and Realisation of a MMIC Power Limiter using 3D GaAs Multilayer CPW Technology," *European Microwave Week Conference*, Paris, September 2015– (accepted).

[12] M. A. Alim, A. A. Rezazadeh, M. M. Ali, **P. B. Kyabaggu**, N. Haris and C. Gaquiere, "0.25 Î¼m AlGaN/GaN HEMT Nonlinearity Modelling and Characterization Over a WideTemperature Range," *European Microwave Week Conference*, Paris, September 2015– (accepted).

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[15] **P. B. K. Kyabaggu,** N. Haris, A. A. Rezazadeh and E. P. Sinulingga, "Design and Realisation of Compact MMIC Limiters using 3D Multilayer Technology," to be submitted for journal publication.

Chapter 1 Introduction

In the Monolithic Microwave Integrated Circuit (MMIC), the monolithic describes the fundamental nature of MMICs, namely that they are fabricated on one single piece of semiconductor, while 'microwave' refers to an electromagnetic wave with a free-space wavelength and a frequency ranging from 300 MHz up to 300 GHz. Finally, 'integrated circuit' refers to the act of integration between the passive and active components and with interconnects fabricated on the same semiconductor substrate. The expansion of the market for wireless communications and sensors has led to the recent interest in highly integrated MMICs for millimetre-wave wireless applications. These applications require MMICs that are low cost, high integration levels and high performance, as well as simpler, more rapid development [1]. An effective way of meeting these requirements and producing highly integrated MMICs is by employing three-dimensional (3-D) MMIC technology [1]. A key part of this 3-D MMIC technology is the thin-film microstrip (TFMS) transmission line, which is formed on a 3-D structure – as shown in Figure 1. The TFMS line offers a narrow line width and spacing because of its thin substrate, with thicknesses ranging from 1 to 20 μm. A 3-D structure offers several other benefits, including compactness and the isolation of passive components from substrate properties using the ground plane.

In addition, recently there has been an increasing demand in the field of microwave integrated-circuit technologies to lower the dissipation loss of transmission lines, in order to improve noise output and efficiency performance of circuits such as low-noise and power amplifiers [2]. Low-loss transmission lines are also desirable when creating low-loss passive components such as filters, baluns, transitions and couplers. In a CPW design, via holes are not necessary and fragile semiconductors do not need to be excessively thin. In addition, individual component sizes are unlimited [2]; these factors can greatly reduce processing costs. For applications such as reduced-size couplers and non-linear transmission lines, it is desirable to use high impedance transmission lines. On the other hand, ultra-low transmission lines are required in matching networks where low impedance devices, such as power field-effect transistors (FETs) or photodiodes, are used. The range of maximum impedance is limited by the practical size of the slot and the width of the centre line, while a practical low limit is imposed by fabricating the very narrow slot, and high losses result from current crowding on the edges [2].

One problem associated with the CPW is that the ground must be on either side of the signal lines, which increases the complexity of the circuit designs. A potential solution to this problem is to utilise a multilayer technique in which several metal layers are sandwiched by insulators. This technique gives microwave engineers flexibility in designing multilayer structures with improved circuit performance [2].

Increasing demand for high-density and high-functionality microwave and millimetre-wave circuits has led to innovative circuit architectures such as three-dimensional (3D) multilayer MMICs. The major advantage of the multilayer techniques is not only that one can design miniature microstrip lines, but they also allow for employing other 3D passive components [3]–[10]. However, these complex architectures require interconnect transitions with low insertion and return losses, in order to yield low-loss, compact multilayer MMIC circuits.

Various types of transitions have already been developed and reported, including transitions by electrical contact [4] and those that use electromagnetic coupling [5]. Electrical contact transitions usually call for via holes, bonding wires or abrupt steps in the conductor [6], and they are compact in size and have a relatively wide bandwidth despite involving some degree of mechanical complexity [6]-[8]. Electromagnetic coupling transitions, on the other hand, require no via holes or wire bonds, though most of them suffer from narrow bandwidth and are larger in size. Several reports [3]–[5], [9]–[12] have discussed transitions based on electromagnetic coupling, which occurs in the overlap region between the coplanar waveguide (CPW) and the microstrip (MS). However, existing published transitions have poor robustness due to their simple structures and the lack of availability of multilayer technology for flexible compact designs. In addition, to the best of our knowledge, there is no information available on thin film microstrips (TFMSs) in the construction of transitions. This work discusses and provides for the first time full analyses of transitions operating at high frequencies between CPWs and thin film microstrips, by using multilayer technology. Most characterisations of MMIC interconnects reported so far have been carried out using analytical approaches such as quasi-static analysis [13], developed further by Bedair et al. [14]. However the accuracy of these analytical techniques is limited at higher frequencies (above 40GHz) due to some higher order modes occurring in the CPW transmission lines. Since wideband CPW transition structures in this work are designed and modelled up to a frequency of 50 GHz, quasi-static approximation is not suitable to be applied as a primary modelling technique. Eisenstadt et al. [15] reported another characterisation technique based on S-parameters for

the non-multilayer structure. Since this technique enables wideband characterisation, regardless of how the modes occur in the structure, we have therefore chosen this method as the main modelling tool in our work.

The major advantage of multilayer techniques is that with either a conventional or a multilevel technique, one can not only design miniature microstrip lines, but can also employ 3D passive components [16]. At millimetre frequencies, CPWs provide many solutions to the design of low-loss, uniplanar, low-cost and compact integrated circuits. However, many applications, such as on-wafer measurements of microstrip circuits or vertically integrated circuits, require the flexibility to use a combination of planar technologies. Consequently, this leads to the development of transition structures such as CPW to thin-film microstrip transition.

In this work, the design and characterisation of compact multilayer CPW components and circuits fabricated on semi-insulating GaAs substrates has been carried out successfully. Three-dimensional MMICs are realised on a semi-insulating GaAs substrate by stacking two dielectric layers separated by three metal conductor layers. A number of passive components, such as thin film resistors, inductors, capacitors and CPW-to-TFMS transitions, were designed and realised. Furthermore, active circuit components such as pHEMT diodes, limiters and LNAs were realised at the University of Manchester with prefabricated pHEMT devices from Filtronic on a S.I. GaAs substrate. An improved 7-layer multilayer fabrication procedure is also demonstrated in this work.

In order to analyse and predict the properties of these multilayer active and passive CPW components and circuits, electromagnetic simulations were carried out using a 2.5-dimensional ADS Momentum simulator as well as Agilent IC-CAP. RF on-wafer measurements were performed using the Cascade wafer probe station and HP8510 Vector Network Analyser (VNA) aligned with the LRRM calibration technique. Good agreements between the measured and simulated results are reported from the comparative analyses performed in this work.

This research presents design guidelines for the development of compact, wideband multilayer coplanar waveguide to thin-film microstrip transitions, which does not require any via holes between the CPW ground strips and the TFMS backside ground plane. Two transition designs are studied: a design with a footprint on the CPW end (design A) and a design without a footprint (design B) [17]. The work presented in this thesis shows the

performance of a compact transition design using multilayer technology, along with their design characteristics and optimisations. The results provide RF engineers a better understanding of the electromagnetic behaviour of the transition and hence reduce the design time required to develop broadband transitions.

The integration between passive components with commercially available active components such as pHEMTs is also demonstrated in this work. This shows the advantage of using 3D multilayer CPW technology in regards to making circuits compact and reducing overall fabrication costs. Circuit compactness in this work is demonstrated in the spiral limiters and a 10 GHz low-noise amplifier. Therefore, the knowledge acquired from the design and characterisation of multifunctional passive and active multilayer CPW components and circuits in this research work can be adopted by RF circuit designers for various compact MMIC applications.

1.1 Key aims and objectives of this research

The aims of this research is to design and produce an array of multifunctional passive and active CPW components and circuits that can be employed for compact MMIC applications. To achieve compactness while maintaining better performance at a wide band, 3D multilayer technology is employed.

The main objectives of this research include:

- Analysing published theoretical and experimental literature on the transmission line theorem, in order to establish a solid foundation for the modelling of 3D MMICs.
- Developing novel simulation techniques to improve the accuracy of the results obtained and comparing these results with data already published, thus demonstrating the merits of 3D multilayer MMICs;
- Improving multilayer fabrication techniques for creating multilayer passive and active circuits.
- Analysing and establishing optimisation techniques for multilayer components and exploiting available flexibility in multilayer technology in producing low-loss performance chips at low cost, reduced sizes and which are easy to fabricate.

- Attaining in-depth knowledge on different loss parameters involved in multilayer CPW components, such as transitions. Identifying solutions to minimise these losses and optimising their performance to make them suitable for RF applications.

- Carrying out parameter extractions to develop both small- and large-signal GaAs pHEMTs models to facilitate the integration of passive and active components. Hence, this helps yield compact circuits such as limiters and amplifiers.

1.2 Key Research Contributions

The key research contributions of this work that highlight the mentioned objectives in sub-chapter 1.1 are summarised as:

- The development of an improved step by step guide for multilayer fabrication of MMICs.
- Design guidelines for a noval CPW-to-TFMS transition have been developed based on 3D multilayer technology and employs electromagnetic coupling.
- New Schottky diodes using pHEMT configurations have been designed and fabricated.
- New MMIC power limiters using pHEMT diodes have been designed and fabricated.
- A low noise amplifier is used to demonstrate the integration between active devices with passive components using 3D multilayer technology. Hence this leads to the reduction of the overall chip size.

1.3 Thesis overview

Chapter 1

This chapter gives a general overview of the key research contributions along with the realised aims and objectives.

Chapter 2

Any research work being undertaken requires a strong foundation or background in-depth study. This chapter provides background reviews on MMIC technology and also discusses its applications. A background study of different types of transmission lines, including CPW-to-TFMS transition, is undertaken. An insight into unipolar and bipolar transistors is

also given as well as HEMT transistors, in particular for the pHEMT transistor. An in-depth review of the microwave diodes and limiter circuits is also presented herein.

Chapter 3 and Chapter 4

Experimental techniques and methodologies, which include electromagnetic simulator momentum in ADS and the detailed fabrication procedure involved in 3D multilayer passive and active components, are presented in Chapter 3. Calculation methodologies for parameter extraction using the S-parameters are also detailed in this chapter, and different types of on-wafer calibration techniques are presented. Any fabrication problems encountered, and their solutions, are discussed along with the fabrication calibration results in chapter 4.

Chapter 5 and Chapter 6

Multilayer transmission lines, such as CPW and thin-film microstrips (TFMSs), are designed and modelled in chapter 5, and their design parameters are used later to design CPW-to-TFMS transitions. This chapter also discusses why different parameters were chosen for the transition transmission line design. CPW, TFMS and transition regions are analysed and discussed in relation to why a tapered design was used for the transition and why a footprint on the CPW region was considered a good design aspect. Improved compact and low-loss transitions are also provided. Chapter 5 further includes fabricated GaAs pHEMTs characterised over fixed bias points and frequencies. The small-signal analysis of these GaAs pHEMTs, and their integration with MMIC passive components to form integrated circuits such as a low noise amplifier and microwave limiters, are discussed in chapter 6. Comparisons of the measured results with the small-signal and large-signal TOM3 models are also presented in chapter 6.

Chapter 7

This chapter details the key objectives achieved in this work, and then it identifies and discusses some aspects of future work for compact MMIC applications.

Chapter 2 Literature Review

2.1 MMIC TECHNOLOGY

In 1959, the first concept relating to integrated circuits (ICs) was put forward by Kilby of Texas Instruments [18]. Rapid development was started in early 1960s by Moll, following several publications on integrated circuit applications [19-22, 23]. In 1964, the first silicon-based monolithic microwave integrated circuit (MMIC) was invented by Ruegg [24] as an analogue FET switch. However, as with all pioneering inventions, it suffered from poor switching speed due to the low mobility of silicon. MMICs proceeded to improve further, and in the 1960s, in line with maturing development of microstrip lines, as reported by Wheeler [25-27], two researches were published [28, 29] and widely recognised as the first original production of gallium arsenide based on MMIC technology.

Advantages and Disadvantages of MMICs

- A traditional microwave hybrid integrated circuit (MIC) consists of wire bonding and other surface-mounted discrete components. Soldering and conductive epoxy can also be found to bond on-chip and off-chip components to a single substrate. In contrast, a monolithic microwave integrated circuit (MMIC) is a microwave circuit where all active and passive components are fabricated together on a single semiconductor substrate [30].
- Many unwanted losses are introduced in MIC, such as the parasitic losses associated with the wiring and solders. During assembly, the use of various interconnects results in a good deal of undesirable coupling or interference that can seriously affect the target performance of the circuit.
- With MMIC technology, there is no need for any kind of bonding wires, solders or glue. Hence, parasitic losses are kept at a minimum, while unwanted losses are also minimised; thus, at high frequency, better performance is achieved.

Table 2.1: Advantages and disadvantages of MMIC and Hybrid MIC [30]

	MMIC	Hybrid MIC
Cost	• Cheap in large quantities • Cheap for complicated circuits with large number of components	• Cheap for simple circuits and with automated assembly
Parasitic	• Less unwanted parasitics • Can be controlled	• More unwanted parasitic from bond pads/bond wires • Cannot be controlled
Choice of components	• Limited choice of components	• Vast selection of components
Performance	• Good broadband performance	• Limited bandwidth performance
Frequency of operation	• Good performances to well over 100GHz	• Very hard to realise above 30GHz
Assembly work	• Its minimal	• Can be difficult and time-consuming to assemble
Reproducibility	• Very good	• Poor
Reliability	• Very good	• Adequate
Turnaround and post-fabrication modifications	• Typically 3-6 months • Cannot make any changes to the design after fabrication	• Typically a few days • Possible to tune after fabrication
Size, weight and layout area	• Very small and light in general • Must miniaturise area as much as possible to stay commercially competitive	• Larger and heavier than MMICs • Less pressure to miniaturise layout as substrate is low cost
Investment required	• Very expensive to start up	• Little investment required to start up

The main attractiveness of MMICs lies in the fact that they can be produced in large quantities and at relatively cheap cost. As seen in Table 2.1, the smaller chip size is attractive due to a more compact structure and at the same time lower production costs. Figure 2.1 shows an example of a cross-sectional view of a 3-D MMIC incorporating passive CPW multilayer and GaAs pHEMT technologies.

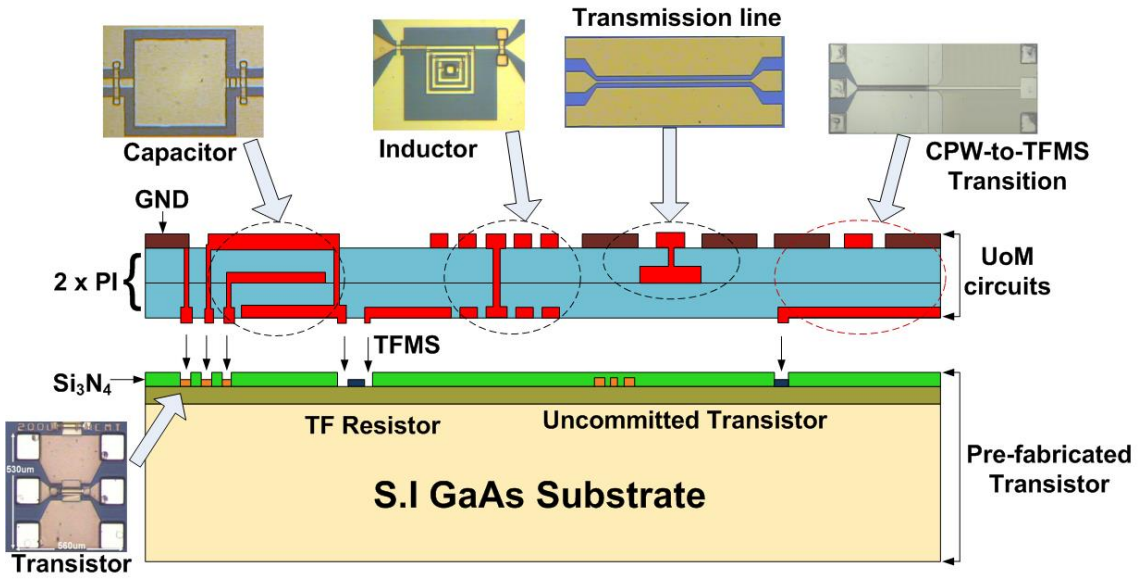


Figure 2.1: Cross-sectional view of a 3-D MMIC incorporating passive CPW multilayer and GaAs pHEMT technologies [2, 31].

2.2 Transmission Line Theory

The transmission line theory bridges the gap between circuit theory and a complete field analysis. Transmission lines can be approximated by a distributed parameter network with parameters distributed throughout the entire line. Furthermore, in line with more conventional circuits [32], they have the properties of inductance, capacitance and resistance. Circuit analysis assumes that the physical dimensions of a network are much smaller than the electrical wavelength, while transmission lines may be a considerable fraction of a wavelength or many wavelengths in size, hence making electrical size the key difference between circuit theory and transmission line theory [32]. Thus, a transmission line is defined as a material medium or structure that forms all or part of a path from one place to another for directing the transmission of energy [33]. It is often represented as a two-port network, since they always have at least two conductors, as shown in Figure 2.2.

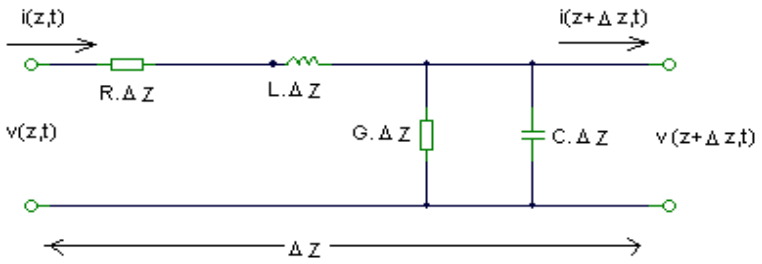


Figure 2.2: Equivalent circuit of a transmission line [33].

The parameters in Figure 2.2 are defined as follows:

- R is the resistance of the conductors per unit length in Ω/m
- L is the inductance of the conductors per unit length in H/m
- C is the capacitance between the conductors per unit length in F/m
- G is the conductance of the dielectric media per unit length in S/m

From Figure 2.2, Kirchhoff's voltage law, when applied, gives [23, 32, 34]:

$$v(z,t) - R \cdot \Delta z \cdot i(z,t) - L \cdot \Delta z \frac{\partial i(z,t)}{\partial t} - v(z + \Delta z, t) = 0 \tag{2.1}$$

By dividing (2.1) by Δz and taking the limit as $\Delta z \to 0$, the following simplified transmission line equation is derived:

$$\frac{\partial v(z,t)}{\partial z} = -R \cdot i(z,t) - L \frac{\partial i(z,t)}{\partial t} \tag{2.2}$$

Kirchhoff's current law, when applied, gives:

$$i(z,t) - G \cdot \Delta z \cdot v(z + \Delta z, t) - C \cdot \Delta z \frac{\partial (z + \Delta z, t)}{\partial t} - i(z + \Delta z, t) = 0 \tag{2.3}$$

By dividing (2.2) by Δz and taking the limit as $\Delta z \to 0$, the following simplified transmission line equation is then derived:

$$\frac{\partial i(z,t)}{\partial z} = -G \cdot i(z,t) - C \frac{\partial v(z,t)}{\partial t} \tag{2.4}$$

The above equations (2.1 and 2.3) can be simplified if voltage $v(t,z)$ and current $i(z,t)$ are time-harmonic cosine functions:

$$v(t,z) = \mathrm{Re}(V(z)e^{jwt}) \tag{2.5a}$$

$$i(z,t) = \mathrm{Re}(I(z)e^{jwt}) \tag{2.5b}$$

In [34], equations (2.5a) and (2.5b), the general transmission line equations (2.1) and (2.3) are written as:

$$-\frac{dV(z)}{dz} = (R + j\omega L)I(z) \tag{2.6a}$$

$$-\frac{dI(z)}{dz} = (G + j\omega C)V(z) \tag{2.6b}$$

The derivatives for the above equations (2.6a) and (2.6b) are [34]:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{2.7a}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0 \tag{2.7b}$$

where γ is defined as:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.8}$$

γ is the propagation constant, α, the real part of propagation constant is called the attenuation constant in Np/m and β, the imaginary part of the propagation constant is called the phase constant of the line in rad/m.

$V(z)$ and $I(z)$ are found to be [34]:

$$V(z) = V^+(z) + V^-(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{2.9a}$$

$$I(z) = I^+(z) + I^-(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z} \tag{2.9b}$$

The two terms in each equation represent the travelling waves in positive and negative directions along the z path, respectively. This transmission line theory will be used when characterising the multilayer transmission lines.

2.3 Thin-Film Microstrip (TFMS) Transmission Line

The microstrip is the most common type of transmission line used in MMICs. A thin-film microstrip appears to be similar to a conventional microstrip, albeit with very different electrical characteristics. A conventional microstrip consists of a metal track on a dielectric substrate with an infinite ground plane on the back surface, whereas a TFMS uses a thin dielectric layer deposited on top of a ground plane which has been deposited onto a carrier substrate such as GaAs or Si. TFMS dielectric layers are normally thin, with a substrate height varying between 1 and 25 µm compared to that of a conventional microstrip, which varies between 100 and 600 µm [35]. In this work, polyimide is the preferred dielectric layer because of its compatibility with monolithic microwave integrated circuit (MMIC) processing steps, ease of use and low cost. Figure 2.3 shows the cross-sectional view of a thin-film microstrip transmission line.

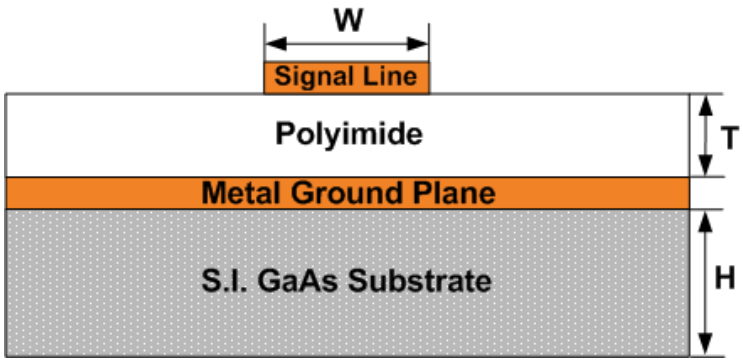


Figure 2.3: Cross-sectional sketch of a thin-film microstrip.

In figure 2.3, H is the height of the substrate layer, W is the width of the conductive signal line and T is the height of the dielectric.

The conductive signal line width and substrate height are of finite dimensions, and the substrate width and length are assumed to be infinite. The small dimensions which describe TFMSs offer several advantages to the microwave circuit designer, in that the thin substrate is easily etched to form very small via holes, the small line widths lead to denser circuits and the use of ground planes between dielectric layers permits novel circuit layouts that minimise circuit size. The low relative dielectric constant results in a higher propagation velocity, which is necessary for high-speed digital circuits [35].

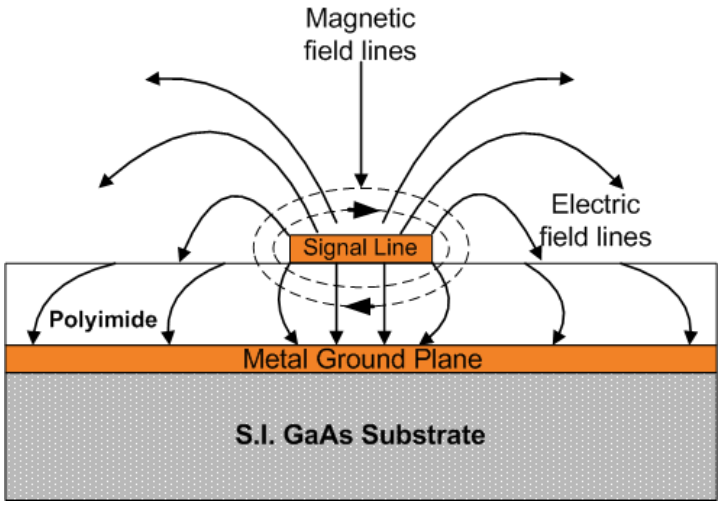


Figure 2.4: Cross-sectional view of a thin-film microstrip transmission line showing electric and magnetic field patterns.

The electric fields are confined mainly underneath the track but extend a significant distance away from the edges of the track. A track with a width similar to the substrate height has more parallel electrical field underneath the track, similar to a parallel plate capacitor and hence making it more capacitive [36]. A track with a width much narrower than the substrate height has tightly packed magnetic field lines that look more similar to a simple wire, and hence they behave more inductively [36].

2.4 Coplanar waveguide Transmission Line

A coplanar waveguide is the second most common type of planar transmission line and is a good alternative to microstrip. It consists of a metal track and ground planes on the same surface of a dielectric substrate, with a fixed gap between the metal track and the ground planes [36]. CPWs offer low-dispersive microwave propagation properties, and backside processing is not required.

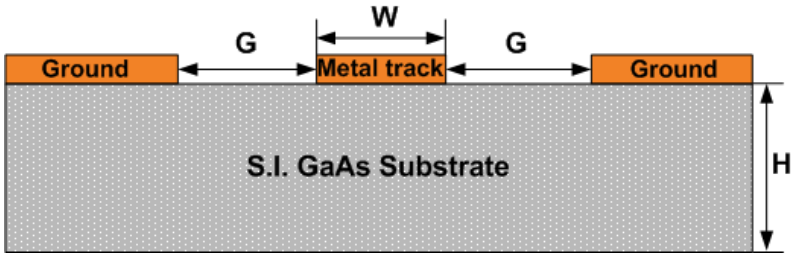


Figure 2.5: Cross-sectional view of a conventional CPW transmission line.

In figure 2.5, H is the height of the substrate layer, W is the width of the metal track and G is the gap width between the metal track and ground plane.

The metal track width and gap are of finite dimensions, and the ground plane and substrate's height, width and length are assumed to be infinite.

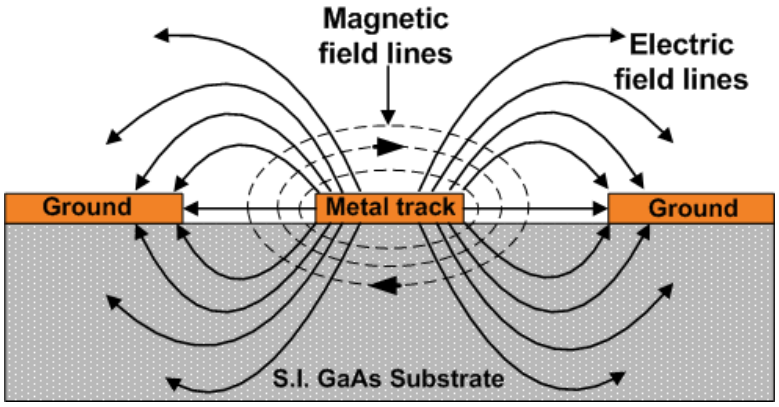


Figure 2.6: Cross-sectional view of a conventional CPW transmission line showing electric and magnetic field patterns.

The electric and magnetic fields are in both the dielectric and the air above, so the mode of propagation in CPW is also quasi-TEM [36]. The structure of the electrical field lines allows both series and shunt elements to be integrated into the transmission line, without the need to drill holes into the substrate [37]. To increase the characteristic impedance of CPWs, the gap must be widened and the centre metal track reduced, which has the effect of increasing conductivity loss. Elevation of the centre metal track, however, can increase impedance, albeit without reducing centre metal track width [36].

2.5 CPW to Thin-Film Microstrip Transition

As demand for high-density and high-performance microwave and millimetre wave circuits increases, RF devices become smaller and more highly integrated. The microstrip is one of the most commonly used transmission lines in RF circuit design due to its compact size, ease of fabrication and low cost [38]. Currently, the low-cost and rapid characterisation of microwave integrated circuits requires coplanar waveguide probe pads. Thus, a transition from CPW probe pads to microstrip lines is required, in order to achieve the highest possible integration while maintaining each circuit's effective performance. The transition is also needed in order to reduce mis-matches and coupling between circuit elements [38].

In the past, different types of transitions were developed, including transitions by electrical contact in [39] and ones that use electromagnetic coupling, as in [16]. Electrical contact transitions usually call for via holes, bonding wires or abrupt steps in the conductor, and

they are compact in size but wide in bandwidth despite the majority of them involving some degree of mechanical complexity [16]. Electromagnetic coupling transitions require no via holes or wire bonds, though most of them suffer from narrow bandwidth and larger size. Electromagnetic coupling occurs in the overlap region between the coplanar waveguide and the microstrip. Recently, some wider bandwidth transitions have been studied for microwave circuit applications, as in [32, 33].

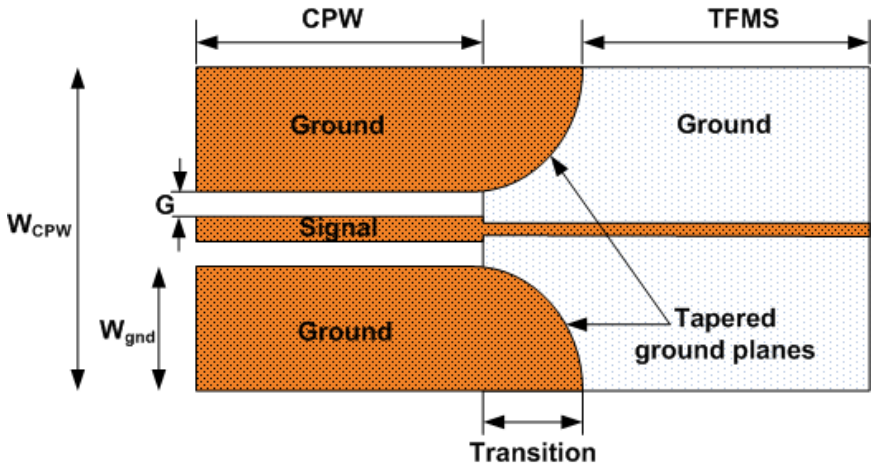


Figure 2.7: Top view of a CPW to thin-film microstrip transition.

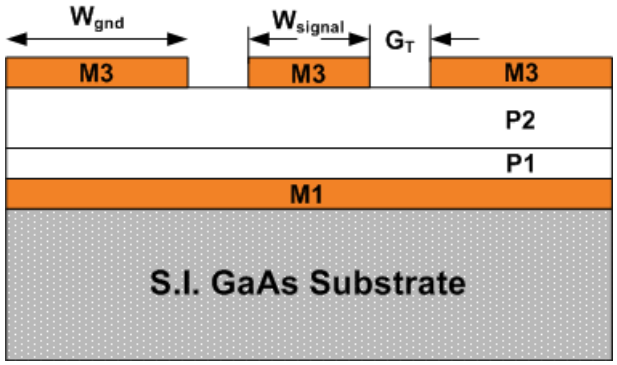


Figure 2.8: Cross-sectional view of CPW to thin-film microstrip transition for figure 2.7.

Figure 2.7 shows a sketch of the aerial view of the CPW to thin-film microstrip transition transmission line, while Figure 2.8 shows the cross-sectional view of CPW to thin-film microstrip transition transmission line. This work presents the simulated and experimental results of a transition interconnection between a multilayer CPW and a thin-film microstrip based on electromagnetic coupling. The design is uniplanar, i.e. it uses the coupling between the ground plane of the thin-film microstrip and the ground planes of the coplanar line. It is also simple to fabricate, as it does not rely on via holes or other micromachining techniques.

2.6 Scattering Parameters

Scattering parameters refer to a scattering matrix – a mathematical construct that quantifies how RF energy propagates through a multi-port network [40]. S-parameters are all about power, both reflected and incidental in a linear two-port system. S-parameters are important in microwave design because they are easier to measure and to work with at high frequencies than other kinds of two-port parameters [29].

That said, S-parameters are complex because both the magnitude and phase of the input signal are changed by the network. They come in a matrix, with the number of rows and columns equal to the number of ports.

The S-matrices for one-, two- and three-port networks can be represented as follows:

$(S_{11}) \rightarrow$ One-port

$\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \rightarrow$ Two-port

$\begin{pmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{pmatrix} \rightarrow$ Three-port

The first number in the subscript refers to the responding port, while the second number refers to the incident port. Thus, S_{12} means the response at port 1 due to a signal at port 2 [40]. Therefore, the "N-port" used for this project is the two-port network S-parameter, because they are easy to model with ADS Momentum simulation software [40].

A two-port examination shows that s-parameters relate travelling waves (power) to a two-port's reflection and transmission behaviour. Therefore, since the two-port network is embedded in characteristic impedance, Z_0, these waves can be interpreted in terms of normalised voltage or current amplitudes [36]. This is shown in Figure 2.9:

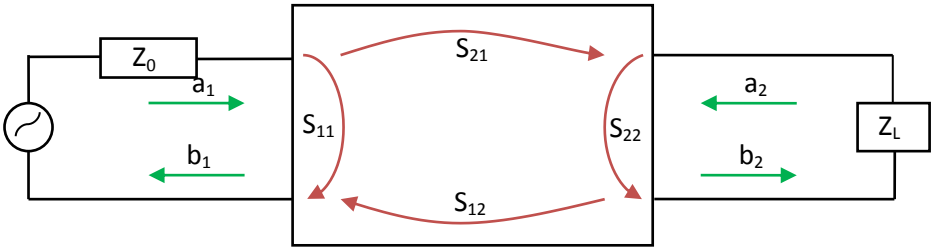


Figure 2.9: Two-port network model.

The S-parameter definition is as follows [36, 42]:

$$b_1 = S_{11}a_1 + S_{12}a_2 \qquad b_2 = S_{21}a_1 + S_{22}a_2$$

a and b are independent and dependent variables.

S_{11} = input reflection coefficient with the output port terminated by a matched load ($Z_L = Z_0$ sets $a_2 = 0$)

S_{22} = output reflection coefficient with the input port terminated by a matched load ($Z_S = Z_0$ sets $a_1 = 0$)

S_{21} = forward transmission (insertion) gain with the output port terminated by a matched load ($Z_L = Z_0$ sets $a_2 = 0$)

S_{12} = reverse transmission (insertion) gain with the input port terminated by a matched load ($Z_S = Z_0$ sets $a_1 = 0$)

2.7 Transmission Line Extracted Parameters

The main transmission line's extracted parameters include characteristic impedance, phase velocity, the effective dielectric constant and dissipation loss.

2.7.1 Characteristic Impedance

The characteristic impedance of a transmission line, Z_0 is the ratio between the voltage and current for an infinitely long line. It's the most important parameter in circuit design and its derivation from first principles, using the classical Telegrapher's transmission line equation, is as follows [39, 42].

Applying equation (2.6a) to (2.9a) gives [39, 42]:

$$I(z) = \frac{\gamma}{R + j\omega L}(V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}) \tag{2.10}$$

Therefore, characteristic impedance is defined as:

$$Z_0 = \frac{V_0^+}{I_0^+} = -\frac{V_0^-}{I_0^-} \tag{2.11}$$

Comparing equations (2.9b) and (2.10) gives:

$$Z_0 = \frac{R + j\omega L}{\gamma} \tag{2.12}$$

By substituting equation (2.8) into (2.12), we get:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.13}$$

Equation (2.13) represents Z_0 by R, L, G, C and frequency.

2.7.2 Phase Velocity

Phase velocity, V_p is the speed at which a point of fixed phase propagates, though it is not always the speed at which electromagnetic information travels [43]. The phase velocity in a transmission line is defined as [32, 43]:

$$V_P = \frac{dz}{dt} = \frac{d}{dt}(\frac{\omega t - cons}{\beta}) = \frac{\omega}{\beta} \tag{2.14a}$$

where $z = \frac{\omega t - cons}{\beta}$, $cons$ is a constant.

Wavelength λ is defined as the distance between two successive wave peaks [41].

$$\lambda = \frac{2\pi}{\beta} \tag{2.14b}$$

Therefore, substituting equation (2.14b) into (2.14a), the phase velocity V_p is expressed as:

$$V_p = \lambda \times f \tag{2.14c}$$

where f is the signal frequency of the transmission line.

The phase velocity in a medium is $V_p = \frac{1}{\sqrt{\mu\varepsilon}}$ and the speed of light, $c = \frac{1}{\sqrt{\mu_0\varepsilon_0}}$ [41].

Therefore, phase velocity in a transmission line, according to dielectric constant $\varepsilon_r \equiv \frac{\varepsilon}{\varepsilon_0}$, is expressed as [40]:

$$V_p = \frac{1}{\sqrt{\mu_0\varepsilon_0\varepsilon_{r,eff}}} = \frac{c}{\sqrt{\varepsilon_{r,eff}}} \tag{2.14d}$$

where ε is the permittivity of the material, ε_0 is the permittivity of free space, c is the speed of light, $\varepsilon_{r,eff}$ is the effective dielectric constant and μ_0 is the permeability of the dielectric.

2.7.3 Effective dielectric constant

In quasi-static analysis, the wave propagation mode in a transmission line is assumed to be TEM, and the effective dielectric constant is expressed in terms of line capacitance [32, 44]. It is derived by forming the ratio of capacitance of the transmission line, with and without the dielectric filter.

$$\varepsilon_{r,eff} = \frac{C}{C_{air}} = \frac{\varepsilon}{\varepsilon_0} \quad [44]$$

where C is the total transmission line capacitance per unit length, in the presence of the dielectric substrate, and C_{air} is the line capacitance with air as the substrate.

2.7.4 Dissipation Loss

Dissipation loss, or attenuation, in a transmission line is equal to conductor losses, α_c, plus dielectric losses, α_d. $[\alpha = \alpha_c + \alpha_d]$. Dissipation loss is defined as the ratio of output power (P_{out}) and incident power (P_{in}) of a transmission line [41].

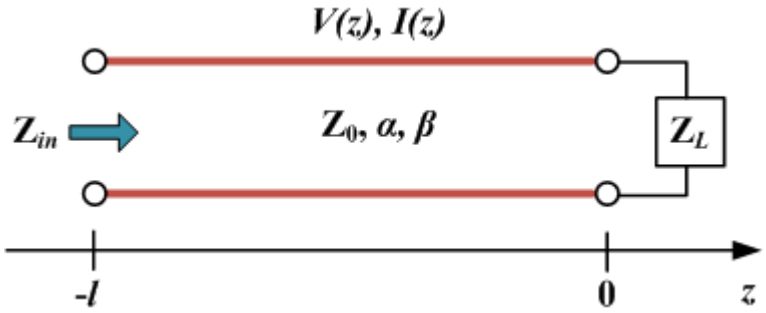


Figure 2.10: A lossy transmission line terminated in the impedance Z_L [30].

Dissipation loss of a lossy transmission line with a length *l*, propagation constant $\gamma = \alpha + j\beta$ and characteristic impedance Z_0 terminated in a load impedance Z_L as illustrated in Figure 2.10, can be derived as follows [32]:

The analogous expressions for the voltage and current wave on a lossy line are obtained as

$$V(z) = V_o^+[e^{-\gamma z} + \Gamma e^{\gamma z}] \tag{2.15a}$$

$$I(z) = \frac{V_o^+}{Z_0}[e^{-\gamma z} - \Gamma e^{\gamma z}] \tag{2.15b}$$

where V_o^+ is the incident voltage amplitude referenced at z = 0, Γ is the reflection coefficient of the load which is expressed as

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.15c}$$

The power delivered to the input of the terminated line at z = -*l* can be computed as

$$P_{in} = \frac{1}{2}\mathrm{Re}\{V(-l)I^*(-l)\} = \frac{|V_o^+|^2}{2Z_0}(e^{2\alpha l} - |\Gamma|^2 e^{-2\alpha l}) \tag{2.15d}$$

$$= \frac{|V_o^+|^2}{2Z_0}(1 - |\Gamma(l)|^2 e^{2\alpha l}),$$

where equations (2.15a) and (2.15b) have been used for $V(-l)$ and $I(-l)$.

The power delivered to the load is given as

$$P_L = \frac{1}{2}\mathrm{Re}\{V(0)I^*(0)\} = \frac{|V_0^+|^2}{2Z_0}(1 - |\Gamma|^2). \quad (2.15e)$$

Therefore using equations (2.15d) and (2.15e), the dissipation loss can be obtained in dB as

$$\text{Dissipation loss} = \frac{P_{out}}{P_{in}} = 10\log\frac{P_L}{P_{in}} = 20\log e^{-\alpha l} = -\frac{\alpha l}{In10}\ , \quad (2.15f)$$

where α is the attenuation factor which is the real part of the propagation constant γ.

2.8 Electrical Length

Electrical length or phase length refers to the length of an electrical conductor in terms of the phase shift introduced by transmission over the conductor at some frequency [45]. It also refers to a point to point measure of phase shift of a wave [46]. The electrical length can be expressed in wavelengths, radians or degrees.

The electrical length assumes a sine wave of some frequency. The sine wave will repeat with a period of $T=1/f$. The frequency f would correspond to a particular wavelength, λ along a particular conductor. For conductors that transmit signals at the speed of light c, the wavelength is given by $\lambda=c/f$, and a distance l along the conductor corresponds to N wavelengths where $N=l/\lambda$ [47].

When electrical length is expressed in angular units, it is the length in wavelengths multiplied by 2π to obtain radians, or by 360 to give degrees [46]. N wavelengths corresponds to the phase $\varphi = 360^o \cdot N$ in degrees or $\varphi = 2\pi \cdot N$ in radians [46, 47].

2.9 Transistors

A transistor is normally made of a solid piece of semiconductor material with three terminals. The voltage or current applied to one of the terminals controls the current flowing through the other two terminals, because the controlled power can be much greater than the controlling power, and so the transistor therefore provides amplification to the input signals [48].

As the transistor dimensions push into the sub-micron region, it becomes more and more challenging to produce CMOS transistors with good performance at microwave frequencies. As the gate length gets shorter, coupled with the scaled down oxide, off-state

leakage current becomes a prominent issue. Also, parasitic resistance and capacitance become comparable to channel resistance and capacitance.

As a result of its physical structure, the bipolar transistor is a current-controlled device, and its output current is linearly related to the input current. Its input resistance is low (dependent on signal amplitude) and its output resistance is high. In order to overcome these limitations with silicon material, a number of researchers have tried to find alternative semiconductor technologies, and group III and group V semiconductors were found. As these offer lighter effective masses, higher electron mobility and larger output currents are available. This makes them good candidates for microwave applications [48].

Defining a Semiconductor for Diodes and Transistor Applications

A transistor consists of a semiconducting material, e.g. silicon, and the behaviour of the transistor largely depends on the properties of this material. A semiconducting material is one with a conductivity lying between that of an insulator and that of a conductor; that is to say, one for which the resistivity lies between, say, 10^{12} Ω-cm (typical value of glass) and 10^{-6} Ω-cm (approximate value of copper). Hence, typical values for the resistivity of a semiconducting material lie between 1 and 100 Ω-cm [48].

A semiconductor's electrical resistance decreases in line with increases in temperature over a particular temperature range characteristic of the semiconductor. The resistance of a conductor increases linearly whereas that of the semiconductor decreases exponentially as temperature rises. The relationship between resistance and temperature for a semiconductor could be written as [48]:

$$R_t = ae^{b/T} \tag{2.16}$$

where R_t is the resistance at an absolute temperature T; a and b are constants and *e* is the base of the natural logarithms.

Intrinsic and Extrinsic Semiconductors

If a semiconductor crystal contains no impurities, the only charge carriers present are those produced by thermal breakdown of the covalent bonds. Conducting properties are thus characteristic of the pure semiconductor. Such a crystal is termed an 'intrinsic' semiconductor.

However, semiconductor crystals contain some Group III and some Group V impurities, i.e. some donors and some acceptors. Some free electrons fit into some holes and neutralise them, but there are some residual charge carriers left. If these charge carriers are mainly electrons, they are termed ‘majority carriers’ and then the holes become the minority carriers. The material is then n-type. If the residual charge carriers are mainly holes, then they are the majority carriers and the electrons become the minority carriers. The semiconductor is then termed ‘p-type’ [48]. In an n-type or a p-type crystal, impurities are mainly responsible for conduction, and the material is termed an ‘extrinsic semiconductor’.

2.9.1 PN Junctions

If a semiconductor crystal has n-type conductivity at one end and p-type at the other end, as shown in Figure 2.11, the crystal produced has asymmetrical conducting properties. Crystals with such conductive properties have obvious applications as detectors or rectifiers.

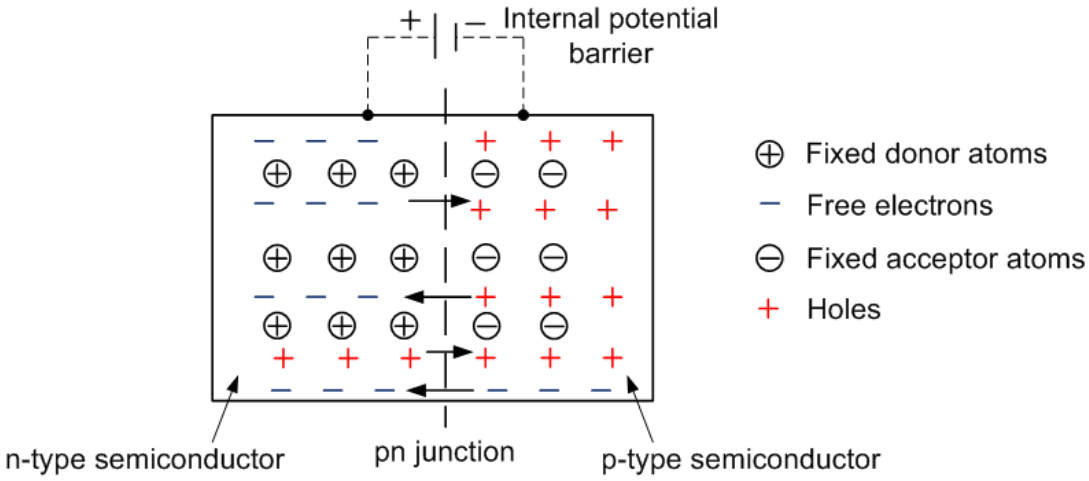


Figure 2.11: Pattern of fixed and mobile charges in the region of a pn junction [48].

The way of achieving a structure of this type is by treating one end of a single crystal of n-type semiconductor with a Group-III impurity so as to offset n-type conductivity at this point instead. The semiconducting device obtained from this configuration is termed a ‘junction diode’ [48, 49].

2.9.2 Basic Principles of Transistors

Solid state transistors are generally categorised into two families, namely unipolar and bipolar. Unipolar transistors (field-effect transistors) deploy only one type of carrier, either an electron or a hole, to perform transistor functions. Bipolar transistors, on the other hand, employ both the hole and electron carriers to perform the tasks. One of the main differences between a unipolar and bipolar transistor is that a unipolar transistor has higher input impedance than the bipolar transistor [49]. Examples of unipolar transistors include:

- Junction Field-Effect Transistor (JFET)
- Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET)
- Metal Semiconductor Field-Effect Transistor (MESFET)
- High Electron Mobility Transistor (HEMT)
- Pseudomorphic High Electron Mobility (pHEMT).

Examples of bipolar transistors include:

- Bipolar Junction Transistor (BJT)
- Hetero-junction Bipolar Transistor (HBT).

2.9.3 Field Effect Transistors (FET)

Field effect transistors (FETs) can be fabricated using silicon or gallium arsenide (GaAs). GaAs-based active devices generally perform much faster than silicon-based devices because of the material properties of GaAs [51]. HEMTs are a class of field effect devices which depend upon the presence of energy states at the hetero-interface of adjacent compound semiconductors for efficient carrier conditions. At the interface of the hetero layers, a quasi-two-dimensional electron gas (2-DEG), confined in a quantum well, exists. A hetero-junction is created when two materials having two different energy band gaps are joined together. Fundamental physics requires the Fermi levels of the two materials to be aligned with that at the interface, whereby a quantum well is created, with the bands bending in order to be joined together. The existence of the quantum well makes a good confinement area for the electrons to travel through in a certain path (the channel). The electrons are very well confined in this path, and hence it almost makes the electrons travel in two dimensions. Therefore, the electrons in this case are called ‘two-dimensional electron gas’. In 2-DEG the electrons move in an intrinsic environment (undoped GaAs), and hence their movement is limited by interactions with the lattice only [51, 52].

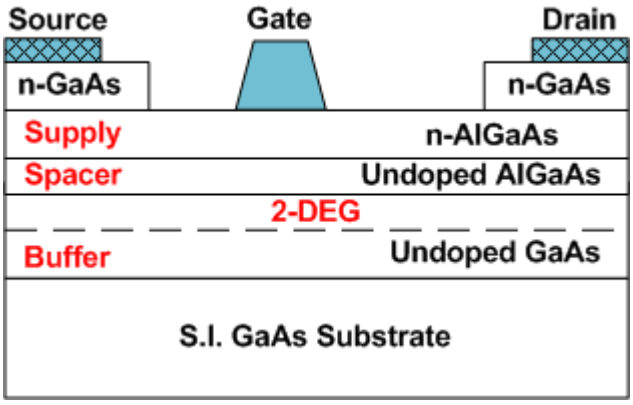


Figure 2.12: Basic HEMT epitaxial layer schematic structure [53].

The electrons from the supply layer are free to move throughout the entire crystal lattice and are controlled by their thermal energy until they are trapped in the quantum well. Undoped AlGaAs is grown on top of the buffer layer and is called the 'spacer layer'. It is lattice matched with the GaAs buffer layer, which in turn is grown on top of the bottom semi-insulating layer. Buffer layer thickness can be up to 5000 A˚, and the supply layer thickness is typically (300 – 2000 A˚) [54]. The undoped AlGaAs spacer layer thickness and doping profile are carefully designed so that they are fully depleted when the device is under normal biasing conditions. On top of the n-doped supply layer of about (10^{17} – 10^{18} cm^{-3}) [55], a highly doped GaAs layer of up to ($7x10^{18}$ cm^{-3}) is grown. This layer is referred to as the 'ohmic' (contact) layer, in order to facilitate the source and drain contacts. The layer is recessed so that the Schottky gate contact is deposited on top of the doped AlGaAs supply layer.

An active layer is formed in the quantum well (GaAs buffer layer) because two layers of different band gap energy and doping profile are grown on top of each other. The electrons transfer from the high conduction band to the lower conduction band, where a dip occurs at the boundary between these two layers as a result of the difference in their conduction band energy levels [54]. The active thin layer is formed at the interface between the undoped AlGaAs space layer and the GaAs buffer layer. The electrons in the quantum well create a very thin sheet, with a carrier density of about ($5x10^{11}$ cm^{-2} to 10^{12} cm^{-2}) for AlGaAs based HEMTs [55].

Growing interest in HEMTs has initiated a great deal of activity in the field of advanced heterostructure growth techniques, such as molecular beam epitaxy (MBE) and metal-organic chemical vapour deposition (MOCVD). With the improvement in MBE, new types of HEMT devices have been produced based on materials with different lattice constants.

Compound semiconductors with varying lattice constants are grown on GaAs – these types of HEMTs are called ‘pseudomorohic high electron mobility transistors’ (pHEMTs) [56], which have the advantages of the superior transport properties of InGaAs, and the saturation velocity of pHEMT is higher compared to a conventional HEMT and MESFET.

Principle of the GaAs Pseudomorphic HEMT

In 1986, the GaAs pseudomorphic HEMT was introduced as a high-performance alternative to the AlGaAs/GaAs HEMT. Substituting InGaAs for GaAs as the two-dimensional electron gas channel improves transport properties due to the higher mobility of InGaAs and stronger electron confinement associated with the quantum well at the hetero-junction. Thus, injecting electrons back into the AlGaAs from the InGaAs is reduced significantly and hence improves the transport properties. The larger conduction-band discontinuity at the AlGaAs/InGaAs hetero-junction allows for higher sheet charge density and hence higher current density and transconductance [57 - 59].

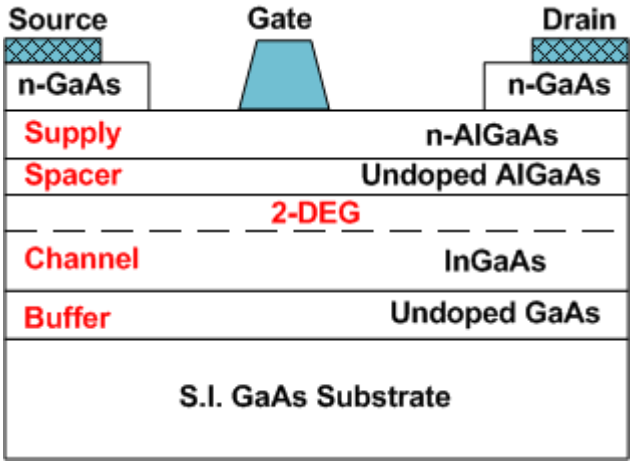


Figure 2.13: pHEMT epitaxial layer structure [53].

In the pHEMT, no two materials could be joined to create the hetero-junction. A lattice constant matched is a prerequisite for a hetero-junction to be formed. However, in the 1990s, it was found that a lattice constant mismatched pair of materials could still be joined together to form a hetero-junction [57-59], whereby a very thin layer of InGaAs is placed on top of the GaAs. InGaAs compared to GaAs can further improve the performance of the transistor because it can be made to have a very narrow band gap, and much better confinement is made possible due to the bigger band gap mismatch between AlGaAs and InGaAs. pHEMT gates are mushroom structures, thereby reducing gate metal resistance that would result from a narrower gate base area [60]. The Schottky contact with the

semiconductor is made through a standard Pt/Ti/Au layered structure. Drain and source contacts are alloyed AuGe/ NiAu, and this type of contact structure has been established as very stable and robust. All discrete pHEMTs are passivated with silicon nitride (Si_3N_4), which doubles as scratch protection [55].

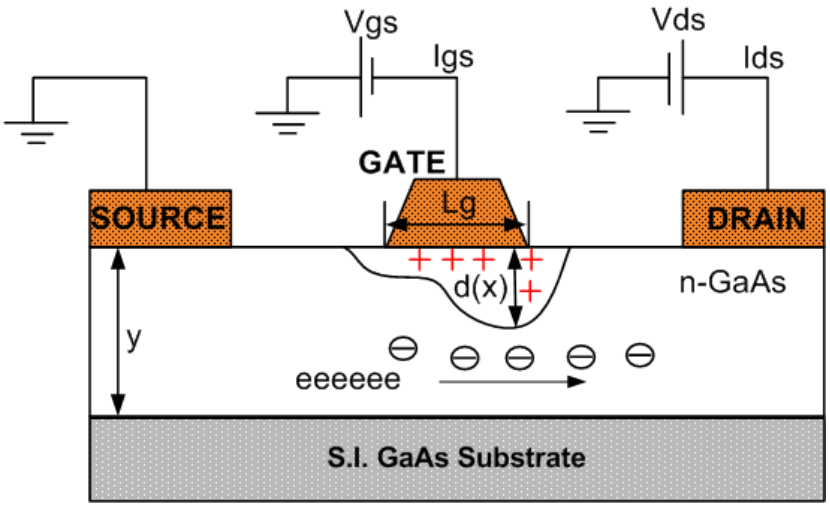


Figure 2.14: Cross-sectional view of a GaAs MESFET under common source configuration [61].

The operation of a pHEMT or HEMT is very similar to the MESFET operation. Figure 2.14 shows the operation of an n-type depletion-mode MESFET under common source configuration. The gate is used as the input and is reverse-biased, and the drain is used as the output and is forward-biased. A depletion region under the gate semiconductor Schottky barrier is formed, due to reverse biasing [61]. The depletion region will have a rectifying effect on electron transport along the channel, which flows from the source to the drain end. If the gate voltage is fixed as the drain voltage increases, more current will flow through, which is why, initially, for small drain voltages, the MESFET behaves like a resistor. However, as the potential at the drain end is increased, the depletion width closer to the drain end will become larger and a point will be reached when the channel can accommodate the maximum velocity of electrons. When this happens, the current starts to saturate. Most applications use the n-channel MESFET rather than the p-channel MESFET because of higher carrier mobility in n-channel devices [61]. Typical measured DC output characteristics of a ($0.5 \times 120\ \mu m^2$) pHEMT are illustrated in Figure 2.15.

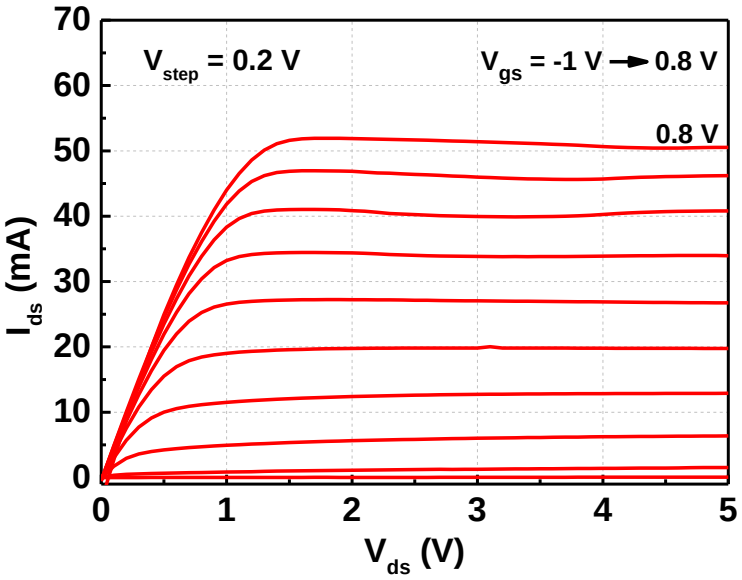


Figure 2.15: A typical measured DC output characteristics of a pHEMT.

A microwave or millimetre wave device typically has a gate length in the range 0.1 – 1 μm. The thickness y of the epitaxial layer is typically one-third to one-fifth of the gate length, while the spacing between the source and drain electrodes is one to four times that of the gate length Lg. The current handling capability of an MESFET is directly proportional to the gate width, because the cross-sectional area available for the channel current is proportional to the gate width [61].

For a long channel (gate length Lg >> y), based on constant low field mobility and gradual channel approximation, the current I_{ds} is given as [53]:

$$I_{ds} = Z[y - d(x)]qN_d\mu.\frac{dV}{dx} \tag{2.17}$$

where Z is the gate width, y is the channel depth, d(x) is the depletion width and N_d is the donor concentration.

d(x), the depletion width, is given by [53]:

$$d(x) = \left\{\frac{2\varepsilon[V(X)+V_{bi}-V_{gs}]}{qN_d}\right\}^{1/2} \tag{2.18}$$

where $\varepsilon_s = \varepsilon_0\varepsilon_r$ is the semiconductor dielectric constant and V_{bi} is the built- in potential.

Substituting equation 2.18 in 2.17:

$$I_{ds} = G_0 \left\{ V_{ds} - \frac{2[(V_{ds}+V_{bi}-V_{gs})^{3/2}-(V_{bi}-V_{gs})^{3/2}}{3V_p^{1/2}} \right\} \quad (2.19)$$

where G_0, the channel conductance and is given as [53]:

$$G_0 = \frac{q\mu N_d Z y}{L} \quad (2.20)$$

and V_p, the pinch-off voltage, when the depletion width d(x) equals the channel depth y, is:

$$V_p = \frac{qN_d y^2}{2\varepsilon_s} \quad (2.21)$$

For a short channel MESFET (small L_g/y ratio), the $I_{ds(sat)}$ can be approximated as:

$$I_{ds(sat)} = Z[y-d]qN_d v_{sat} \quad (2.22)$$

where v_{sat} is the saturation velocity, and intrinsic transconductance g_m can be given as:

$$g_m = \frac{\varepsilon_s Z v_{sat}}{d} \quad (2.23)$$

The expression shows clearly the dependence of g_m with v_{sat} and to the reciprocal of depletion width of the device.

2.9.4 Small-Signal Analysis

To design any analogue or digital circuitry, one needs to know device performance in relation to bias and frequency limits, which results into a volume of S-parameters. For this purpose, a small-signal model at a required bias point, valid over a wide range of frequencies, can be developed by understanding the underlying physics of the FET. Small-signal equivalent models help in analysing gain, noise, stability, signal delay, charging properties and energy losses of a pHEMT while designing any microwave circuits, and they also assist in understanding device process techniques. The direct parameter extraction technique is used in this work whereby device parameters are extracted from the measured device's scattering parameters at different biasing conditions over a frequency. The small-signal equivalent circuit of an FET is shown in Figure 2.16.

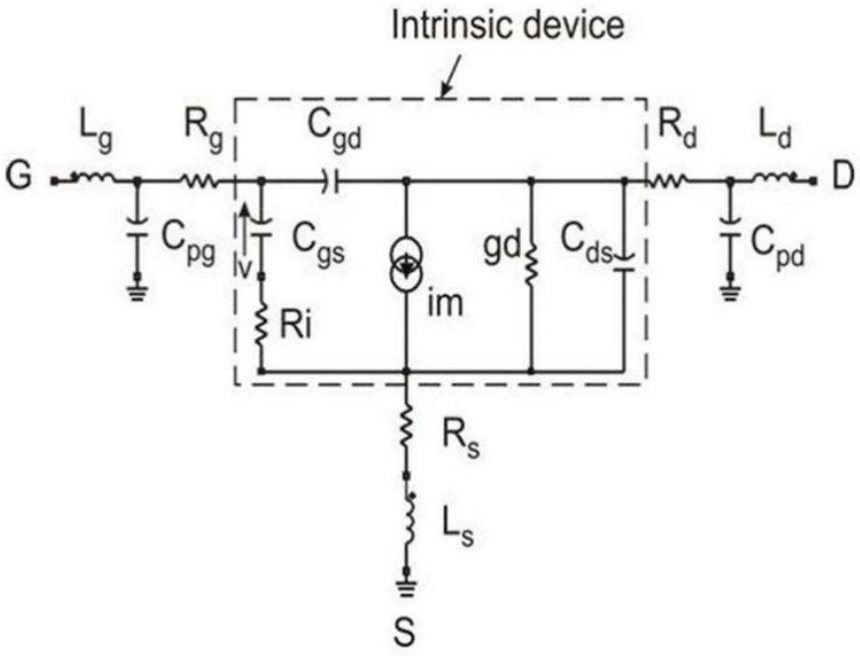


Figure 2.16: Small-Signal equivalent circuit of a FET in common source configuration [55, 62].

On-wafer S-parameter measurements were carried out on a 0.5 x 200μm^2 pHEMT and a 0.5 x 120μm^2 pHEMT from 45 MHz to 50 GHz, by using the HP8510C Network Analyzer controlled by IC-CAP at V_{gs} = -0.2V and V_{ds} = 3V. The device was biased via ground-signal-ground microwave probes, using an Agilent 4142B Modular DC source/monitor unit in conjunction with IC-CAP. All the measurement setups were configured on IC-CAP, which in turn administered the instruments connected via a standard GPIB interface. The collected data were stored in an industry-specific MDM format understandable through IC-CAP. Parameter extraction routines were implemented using parameter extraction language (PEL), which is similar to HP BASIC programming language. IC-CAP is the preferred tool for advanced device modelling because of its powerful data handling and analysis procedures [55].

A pi-model is conventionally adopted to represent a pHEMT. The equivalent circuit of a small-signal pHEMT pi-model can be divided into two parts, namely intrinsic and extrinsic.

- Intrinsic elements include C_{gs}, C_{gd}, C_{ds}, R_i, g_d, g_m and τ. They are bias-dependent and hence need to be extracted at hot biasing or on condition. C_{gs} and C_{gd} are capacitances associated with the depletion region underneath the gate. C_{ds} is attributed to the substrate current, which can be seen as a leakage current from the main channel current. The substrate material affects the value of the C_{ds}. R_i is

channel resistance, measuring how difficult it is for electrons to flow in the channel, while g_d, also referred to as R_{ds}, is the drain to source conductance/resistance. g_m is transconductance and can be used to represent the gain of the device, and τ represents the time delay for the output current [55].

- Extrinsic elements include C_{pg}, C_{pd}, L_g, L_d, L_s, R_g, R_d and R_s. They are bias-independent and are extracted using off and cold or strong pinch-off biasing conditions. C_{pg} and C_{pd} are parasitic capacitances and are mainly made up of the sum of capacitances formed between the gate and the drain contact pads to the ground. L_g, L_d and L_s are inductances of the three contacts. R_g, R_d and R_s are resistances associated with the three terminal contacts. It should be noted that only the metalisation contacts contribute to resistance; hence, the semiconductor contact and bulk resistances contribute overall R_s and R_d [55, 62, 63].

Table 2.2: Relationships of small-signal parameters to physical properties of FET [53, 62].

Element	Equation	Comment
$R_{contact}$	$\frac{1}{Z}\sqrt{\frac{\rho_c}{q\mu N_d Y}}$	Contact Resistance
R_{SG}	$\frac{L_{SG}}{qN_d\mu YZ}$	Bulk Resistance; $R_g = R_{contact}+R_{SG}$ L_{SG} is the distance between source and gate contact
R_{GD}	$\frac{L_{GD}}{qN_d\mu YZ}$	Bulk Resistance; $R_d = R_{contact}+R_{GD}$ L_{GD} is the distance between drain and gate contact
R_g	$\frac{\rho Z}{3m^2hL}$	Gate Series Resistance; M = number of gate strips
C_{gs}	$\frac{\varepsilon_s ZL}{d}\left(1+\frac{X}{2L}-\frac{2d}{L+2X}\right)$	Gate-Source Capacitance
C_{gd}	$\frac{2\varepsilon_s Z}{1+2X/L}$	Gate-Drain Capacitance
R_i	$\frac{v_{sat}L}{\mu I_{ds}}$	Input Resistance; μ is the low field mobility
g_{m0}	$\frac{\varepsilon_s v_{sat} Z}{d}$	Intrinsic Transconductance
τ	$\frac{1}{v_{sat}}\left(\frac{X}{2}-\frac{2d}{1+2X/L}\right)$	Signal Delay
d	$\left[\frac{2\varepsilon_s(V_{SG}+V_{bi})}{qN}\right]^{1/2}$	Depletion Width
X	$\left[\frac{2\varepsilon_s}{qN_d(V_{SG}+V_{bi})}\right]^{1/2}(V_{DG}+V_{bi})$	Depletion Extension toward the Drain End
I_{ds}	$qN_d v_{sat}(Y-d)Z$	Drain-Source Current

2.10 Microwave Diodes and Power Limiters

Recently, most commercial microwave RF power limiters have been based on PIN diodes due to their ease of manufacturing and low cost requirements. An RF power limiter should be able to provide low insertion loss for in-band signals, and high insertion loss for signals exceeding the receiver power threshold. It should also have very fast switching speed (within nanoseconds), in order to provide protection upon the arrival of a damaging signal [64], [65 - 68]. These RF power limiters are operated either in a passive or in an active configuration whereby each configuration has its own pros and cons. The passive circuit configuration depends solely on the incoming RF signal in generating a DC bias for the limiting operation, whereas the active circuit configuration employs an external DC supply to pre-bias the shunt-mounted limiting diodes [69]. In this subchapter, background literature on PIN diodes and Schottky diodes is provided. Furthermore, in order to help understand those limiters using Schottky diodes in this work, some background literature on PIN diode limiters is also provided.

2.10.1 Microwave PIN Diodes

A microwave PIN diode is a semiconductor device that operates as a variable resistor at RF and microwave frequencies, and it is classified as a current-controlled device. When the forward bias control current of the PIN diode is varied continuously, it can be used for attenuating, levelling and amplitude modulating an RF signal. When the control current is switched on and off, or in discrete steps, the device can be used for switching, pulse modulating and phase shifting an RF signal. PIN diodes have the ability to control large amounts of RF signal power while using much smaller levels of control power [70]. When the diode is forward-biased, holes and electrons are injected into the intrinsic layer, or I – region.

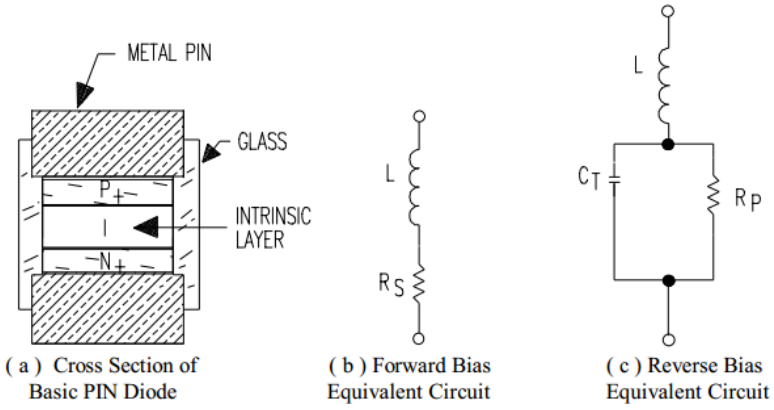


Figure 2.17: PIN diode and the corresponding equivalent circuits [70].

2.10.2 Schottky Diodes

The Schottky diode barrier diode is formed by a metal contact (anode) connecting to a semiconductor (cathode), instead of the more common junction between P- and N-type semiconductors. In Schottky diodes, conduction is not controlled by minority carrier recombination in the semiconductor but by the thermionic emission of majority carriers over the barrier created by unequal work functions [71]. The success of the Schottky barrier is that it can reach very high frequencies (up to 100 GHz) and it is relatively cheap.

Electrons in the conduction band of a crystal can be viewed as sitting in a potential energy box formed by crystal boundaries, as shown in Figure 2.18. This potential energy box for electrons is usually deeper in a metal than in a semiconductor. If a metal and a semiconductor are brought together, some electrons from the semiconductor will move into the metal and vice versa. However, since the barrier for electron escape from the metal is higher, more electrons will transfer from the semiconductor rather than travel in the opposite direction [71]. The metal charges negatively at thermal equilibrium, while the semiconductor will be charged positively, thereby forming a dipole layer that is very similar to that of the PN junction. The Schottky diode is therefore a majority carrier device whose switching speed is not limited by minority carrier effects. A number of metals can create a Schottky barrier on either silicon or GaAs semiconductors. For the case of GaAs the most common types are constructed from titanium, platinum or gold [71]. The favourable characteristics of gallium arsenide (GaAs) Schottky barrier diodes have led to an important development of millimetre-wave mixers, as GaAs has greater electron mobility and saturation velocity than silicon semiconductors [72].

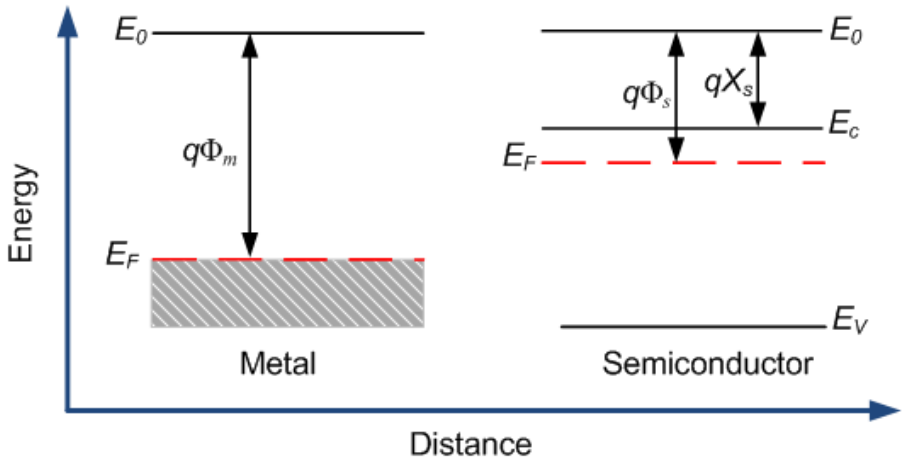


Figure 2.18: Schematic energy band diagram for electrons in conduction bands of a metal and of a semiconductor [61, 71].

Figure 2.19(a) shows the energy band diagrams of a metal and an N-type semiconductor. Energies Φ_m and Φ_s are referred to as the metal and semiconductor work functions. The work function is equal to the difference between the vacuum level and the Fermi level, and therefore it represents the average energy required to remove an electron from the material. The electron affinity of the semiconductor, X_s, corresponds to the energy separation between the vacuum level and the conduction band edge of the semiconductor [71]. When the metal makes intimate contact with the semiconductor, the Fermi levels in the two materials must be equal at thermal equilibrium. In addition, the vacuum level must be continuous. These requirements determine a unique energy band diagram for the ideal metal-semiconductor contact, as shown in Figure 2.19(a).

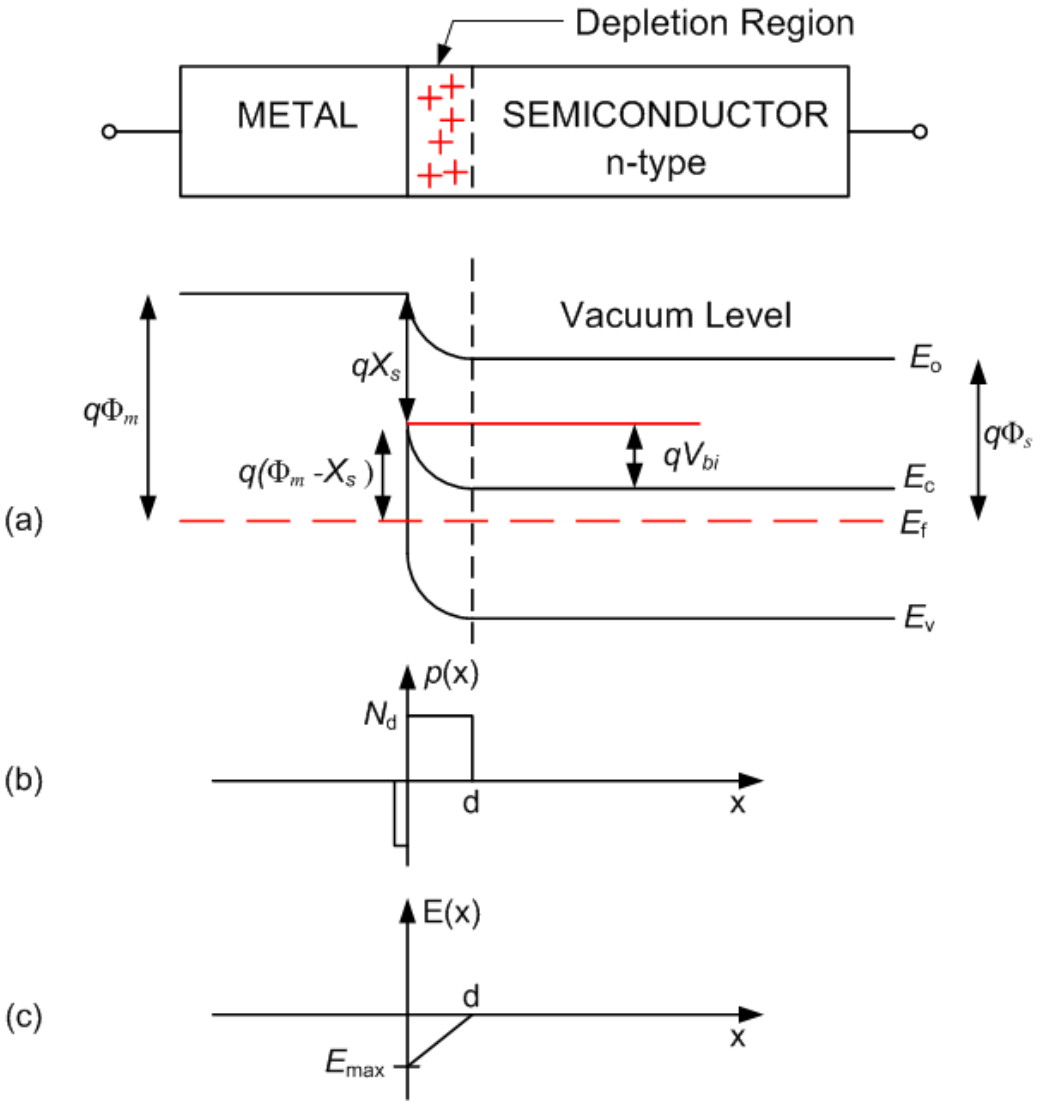


Figure 2.19: (a) Energy band structure of the Schottky junction in thermal equilibrium in n-type semiconductor; (b) charge densities at the junction (negative component is the surface electron concentration on the metal); (c) electric field in the depletion region.

A metal-semiconductor diode is referred to as a Schottky diode. In the idealised diagram of the Schottky junction shown in Figure 2.19(a), the energy barrier height $q\phi_b$ is the difference between the metal work function and the semiconductor electron affinity [61, 71]:

$$q\phi_b = q\Phi_m - qX_s \tag{2.24}$$

Since $\Phi_m > \Phi_s$ the metal is charged negatively. The positive net space charge in the semiconductor leads to a band bending:

$$qV_{bi} = q(\Phi_m - \Phi_s) \tag{2.25}$$

where V_{bi} is the built-in voltage, analogous with the corresponding quantity in a p-n junction. qV_{bi} is identical to the difference between the Fermi levels in the metal and the semiconductor when separated by a large distance [71]. Electron transportation from the semiconductor to the metal contact is blocked by an energy barrier known as the 'built-in potential', qV_{bi}. Both the depletion region and the energy barrier can be modulated by altering the biasing condition, as shown in Figures 2.20(a) and 2.20(b).

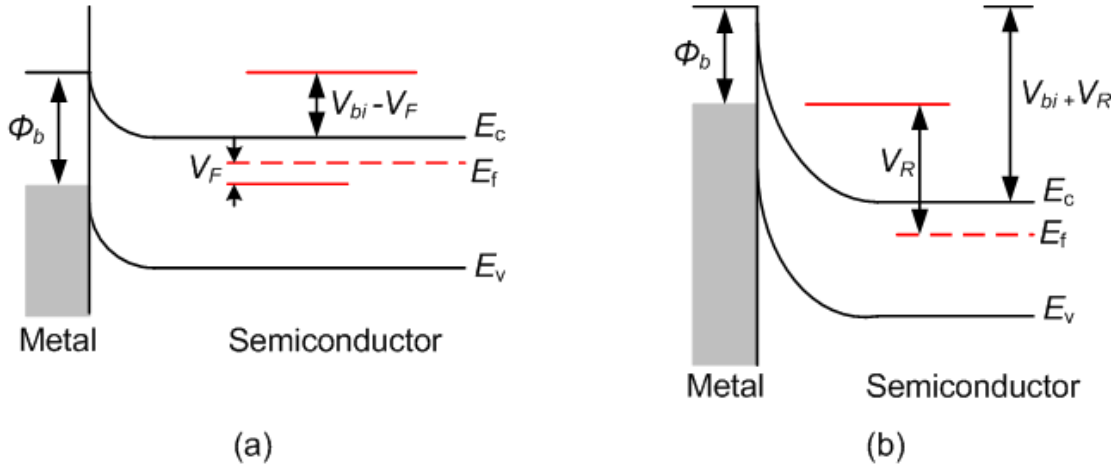


Figure 2.20: Energy-band diagram for a metal-semiconductor system under (a) forward-biased condition; (b) reverse-biased condition [73].

Under the forward-biased condition, the diode operates as a controlled resistor (i.e. a varistor or variable resistor) due to the built-in potential being lowered by a forward-biased voltage, V_F . On the other hand, the depletion region is modulated under a reverse-biased condition voltage, V_R. As a result, the diode operates as a voltage-controlled capacitor (i.e. a variable reactor or varactor) [73].

The shape of the energy diagram of the metal-semiconductor junction is governed by three rules:

- In equilibrium, the Fermi levels for the semiconductor and metal must be constant throughout the system
- Electron affinity must be constant
- The free-space energy level must be continuous

In order to satisfy all three rules simultaneously, the valence and conduction bands of the semiconductor are forced to bend at the junction, and the upward bend of the conduction band of the N-type semiconductor indicates the depletion region. The positively charged depletion region in the semiconductor can be considered an area of stored charge. Before it is possible to determine capacitance, it is necessary to find the quantity of charge that has been moved, which is equal to the depletion zone charge. The electrical field in the depletion zone is found by applying the Gauss law to the region. The electrical field is in the negative x direction, as shown in Figure 2.19(c), and it is at its maximum at the junction. It must also be zero at the edge of the depletion region, because E=-dΦ, dx=0, as shown by the flat band at this point. The voltage across the junction, found by integrating the electrical field, must be equal to Φ_{bi} [71].

Variations between the space charge density, ρ, the electrical field, F, and the potential, ΔV, in the semiconductor near the metal-semiconductor interface can be found using the depletion approximation. Applying the Gauss law in one dimension [61, 71]:

$$\frac{dE(x)}{dx} = \frac{\rho(x)}{\varepsilon_s} = \frac{qN_d}{\varepsilon_s} \quad \rightarrow \quad \rho = qN_d \tag{2.26}$$

$$E(x) = E_{max}\left(1 - \frac{x}{d}\right) \tag{2.27}$$

where

$$F = -\frac{qN_d d}{\varepsilon_s} \tag{2.28}$$

E_{max} is maximum electric field, d is depletion width, N_d is doping density (assumed uniform) and ε_s is dielectric permittivity of the semiconductor.

Since $E_{(x)}$ is a simple triangle function as shown in Figure 2.19c, it is easily integrated to give [61];

$$\Delta V = \frac{E_{max} d}{2} = \frac{q d^2 N_d}{2\varepsilon_s} = V_{bi} - V_{app}, \tag{2.29}$$

where V_{app} is the applied voltage. The resulting depletion-layer width d, is expressed as

$$d = \sqrt{\frac{2\varepsilon_s \Delta V}{q N_d}} = \sqrt{\frac{2\varepsilon_s (V_{bi} - V_{app})}{q N_d}} \tag{2.30}$$

The space-charge density, Q_{SC} in the semiconductor is given as

$$Q_{SC} = q N_d d = \sqrt{2 q \varepsilon_s N_d (V_{bi} - V_{app})} \text{ C/area,} \tag{2.31}$$

where the voltage V is equal to ($+V_F$) for forward bias and to ($-V_R$) for reverse bias. The depletion-layer capacitance C per unit area can then be calculated by using equation (2.31):

$$C = \left| \frac{\partial Q_{SC}}{\partial V} \right| = \sqrt{\frac{q \varepsilon_s N_d}{2(V_{bi} - V_{app})}} = \frac{\varepsilon_s}{W} \text{ F/area} \tag{2.32}$$

and

$$\frac{1}{C^2} = \frac{2(V_{bi} - V_{app})}{q \varepsilon_s N_d} = \frac{2}{q \varepsilon_s N_d} V_{bi} - \frac{2}{q \varepsilon_s N_d} V_{app} \text{ (F/area)}^{-2} \tag{2.33}$$

where $\frac{2}{q \varepsilon_s N_d}$ is the slope on the $1/C^2$ plot. $1/C^2$ is differentiated with respect V to obtain the donor concentration expression N_d as

$$N_d = \frac{2}{q \varepsilon_s} \left[\frac{-1}{d(1/C^2)/dV} \right] = \frac{2}{q \varepsilon_0 \varepsilon_r A^2} \times \left[\frac{-1}{d(1/C^2)/dV} \right] \tag{2.34}$$

The impurity distribution from equation (2.34) is provided by the measurements of the capacitance C per unit area as a function of voltage [61].

A typical Schottky diode circuit is modelled with a junction resistor, $R_j(V_j)$, a junction capacitor, $C_j(V_j)$, and a series resistor R_s, as shown in Figure 2.21. The series resistor represents total resistance from the undepleted semiconductor to the cathode ohmic-contact.

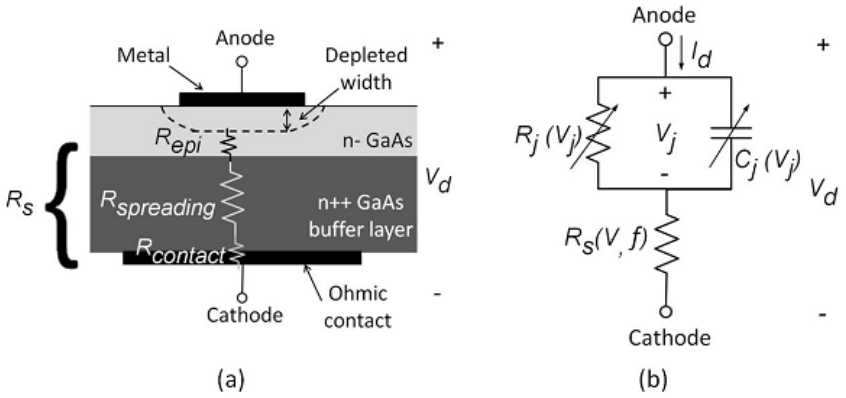


Figure 2.21: A typical Schottky diode: (a) cross-sectional view; (b) equivalent circuit model but with R_S is independent of voltage [73].

Current-Voltage Characteristics

In the forward-biased condition, electron transport mechanisms across the metal-GaAs interface include thermionic emission and recombination in the neutral region. An electron transport mechanism in the opposite direction of the rectification process is known as 'quantum-mechanical tunnelling'. For a good metal-GaAs contact, the overall transport mechanism is dominated by thermionic emission. The current (I-V) relationship of a Schottky diode can be written as [72, 73]:

$$I_d(V_j) = I_S\left(e^{\frac{qV_j}{\eta k_B T}} - 1\right) \tag{2.35}$$

$$I_S = AA^{**}T^2\left(e^{\frac{-q\phi_b}{k_B T}}\right) \tag{2.36}$$

where I_d is total diode current; I_S is reverse saturation current; V_j is junction voltage; q is elementary charge; η is ideality factor; A is junction area; A^{**} is effective Richardson constant (for GaAs: 16 $Acm^{-2}k^{-2}$); T is absolute temperature; ϕ_b is barrier height and k_B is Boltzmann's constant. For a thermionic emission-dominated electron transport mechanism, the ideality factor in the current-voltage relation is closed to unity. However, due to the onset of the tunnelling current, the ideality factor departs from unity. The electron transport mechanism based on tunnelling is more pronounced at a lower temperature and higher doping concentration, N_d. The ideality factor is expressed as:

$$\eta = \frac{q}{k_B \cdot T} \cdot \frac{\Delta V}{\Delta \mathrm{In} I} \tag{2.37}$$

where ΔV is the change in voltage across the junction per decade of current applied and ΔI is the change in current.

2.10.3 Microwave Power Limiters

A device that allows low power signals to pass, and at the same time blocks high power level signals, is a microwave power limiter, which is dependent on incoming signal power levels and is usually characterised by its output power profile. The three important parameters in a microwave power limiter are insertion loss, limiting threshold and flat leakage, where [69]:

- Insertion loss is a common rating associated with all high-frequency circuits and is the undesirable signal power loss introduced to incoming signals by a device.
- The limiting threshold is the input power level where the limiter starts to attenuate the incoming signal.
- Flat leakage is the amount of microwave energy allowed to leak through the device when the limiter is actively limiting the incoming signal [74].

Limiters have traditionally been designed by employing PIN diodes. In order to govern the limiting action in conventional PIN diode limiters, the RF resistance of the diode has to be varied. The addition of an intrinsic layer made of an almost lossless dielectric between doped layers in the PIN diodes is the fundamental difference between a PIN diode and a classic diode. Conventionally the diode is mounted in a shunt across the transmission line at the receiver's front end and is provided with a DC bias return. For incoming signals below the damage threshold, the diode appears to be a capacitor of small value. When incoming signals exceed the threshold level, the diode's intrinsic layer is flooded with carriers during the positive half-cycle and persists through the negative half-cycle [75].

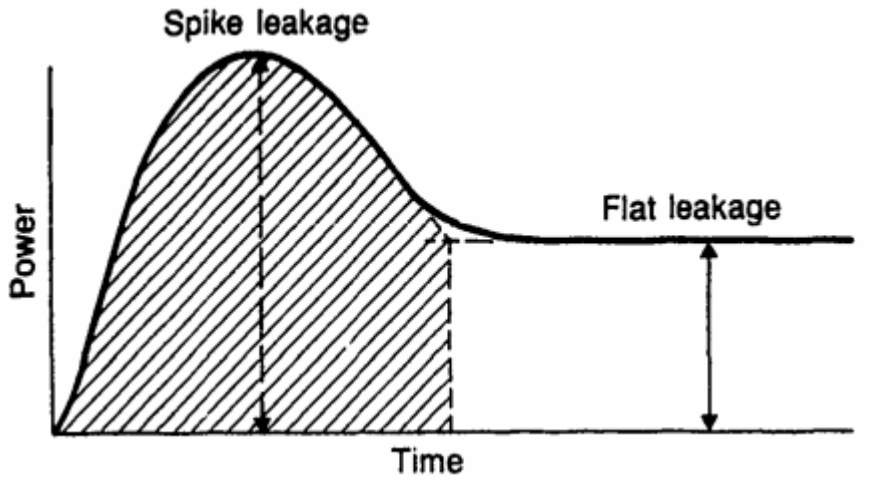


Figure 2.22: Illustration of the Spike leakage [56].

2.10.3.1 Spike Leakage

In the above Figure 2.22, spike leakage is the initial transient power moving past the limiter before it is turned on. The shaded area indicates energy in the spike. The first limitation of PIN diode limiters is the presence of spike leakage, as it takes a finite amount of time for any RF limiter, exposed to a fast-rising pulse, to produce its limiting action. Spike leakage in a limiter is particularly important since, if the energy in the spike is too great, sensitive electronics being protected can be damaged, even though the flat leakage level does not impose any danger. Generally, spike leakage energy increases in line with the width (thickness) of the intrinsic region of the PIN diode [70]. The danger of damage to the PIN diode limiter as a result of excess absorbed power increases as the width of the intrinsic region decreases. This indicates that there is a trade-off between spike leakage and damage thresholds in selecting the width of the intrinsic region of PIN diode limiters. Spike leakage may also be reduced by using dual diode limiters, where the second diode reduces spike leakage from the first [70].

When a PIN diode changes the impedance state, RF energy is not blocked entirely, and this is the period when the limiter is prone to permanent damage. During this period, the limiter generates the highest degree of distortion and exhibits the greatest insertion loss, which is caused by the intermediate impedance level of the PIN diodes. Research findings from Ward [76] suggest that 1) when the input power level decreases, spike leakage duration decreases, 2) spike energy tends to increase slightly with input power, 3) spike leakage increases as the intrinsic layer is widened for a fixed amount of input power and 4) spike leakage increases in line with frequency [69].

2.10.3.2 Flat leakage

Flat leakage power is the constant power level which follows spike leakage and which is transmitted past the limiter to the load or device that needs to be protected. As the input power to the limiter increases, flat leakage remains constant up to maximum isolation. Isolation in decibels is the ratio of output power to input power [70].

2.10.3.3 Recovery time

When the incident RF power level falls below the limiting threshold, the limiter will return to its low insertion loss state. Ideally, this process should be instantaneous; however, a finite measurable amount of time will elapse for the injected free carriers in the intrinsic

region to recombine. The recombination rate is reciprocal to the minority carrier's lifetime, while the carrier lifetime of the PIN diode is directly proportional to the intrinsic layer thickness. Hence, a thin diode will recover faster than a bulk PIN diode. Under high power conditions, the free charge requires about 4.5 lifetimes to decay to 1% of the charge present at the limiting operation. This could result in excessive insertion circuit loss [70].

If the limiter is implemented with the inclusion of a Schottky diode as a detector, recovery time is shorter, as the Schottky diode exhibits a high recombination rate. The resistor value should be chosen carefully, to avoid high insertion loss. The fast recombination rate offered by the Schottky diode suggests the diode is being used in limiter circuits [70].

2.10.4 Comparisons between the PIN diode and Schottky diode limiters

Although PIN diodes are superior in performance compared to the Schottky diode used as a limiter, Schottky diode limiters are a better choice because of their suitability in MMIC technology [77].

Schottky diode limiters are more suitable at higher frequencies because they rectify higher microwave and millimetre wave signals more efficiently than PIN diodes due to the absence of the minority carrier storage effect in the PIN diodes [77].

Chapter 3 Experimental and Fabrication Techniques

3.1 Electromagnetic Modelling

Momentum is a 2.5-D electromagnetic simulator used in the ADS software package, and it is employed in this work to calculate the S-parameters used to obtain results for characteristic impedance, dissipation loss and the effective dielectric constant for MMIC components.

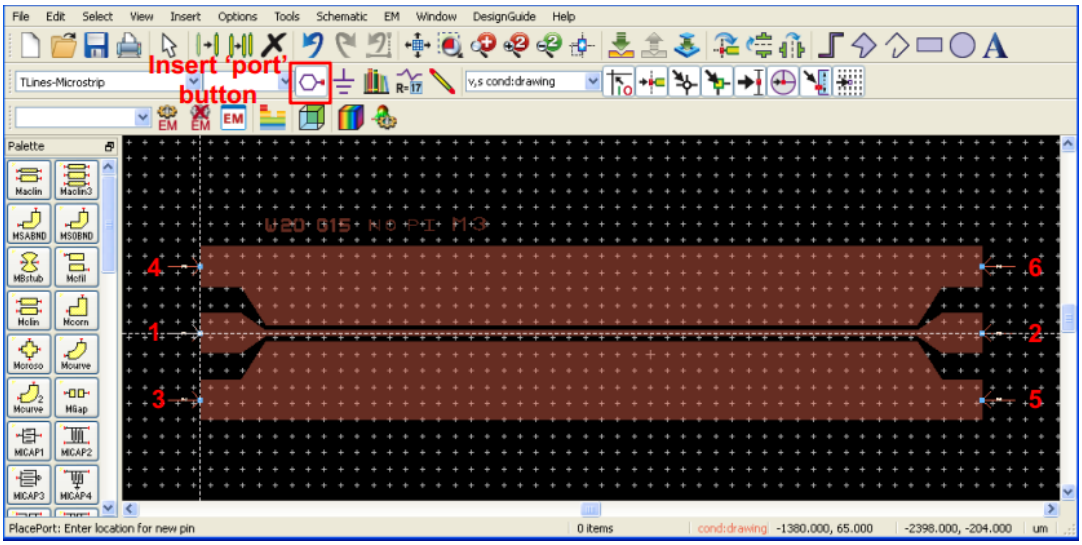


Figure 3.1: Inserting the ports onto the device.

The layout of the device is modelled in the layout window shown in Figure 3.1. The figure also shows how the ports are inserted and snapped to the edges of the transmission line probing pads.

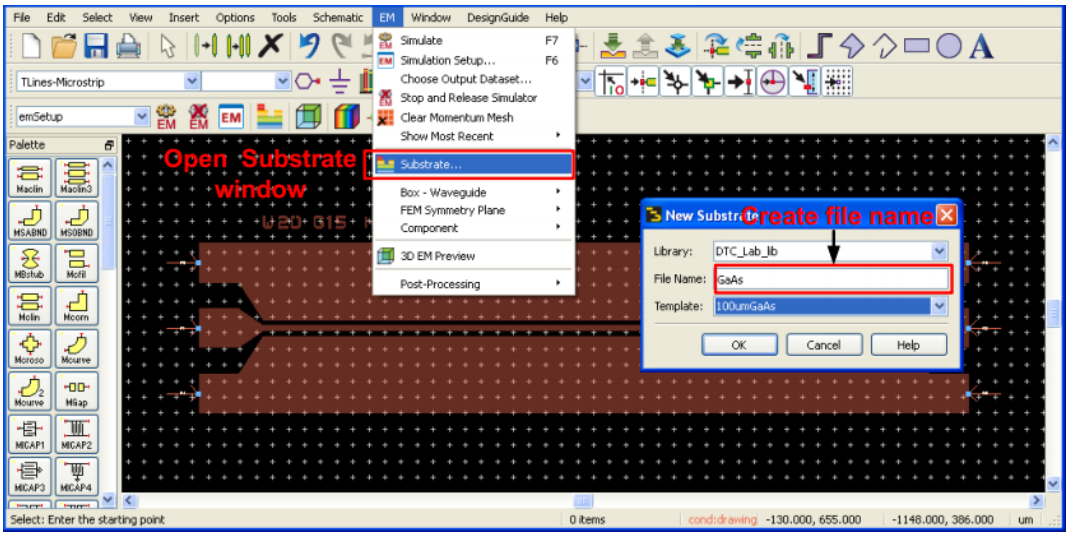


Figure 3.2: Menu of substrate configuration in Momentum.

A new substrate window is opened and a file name for the substrate is created as shown in figure 3.2.

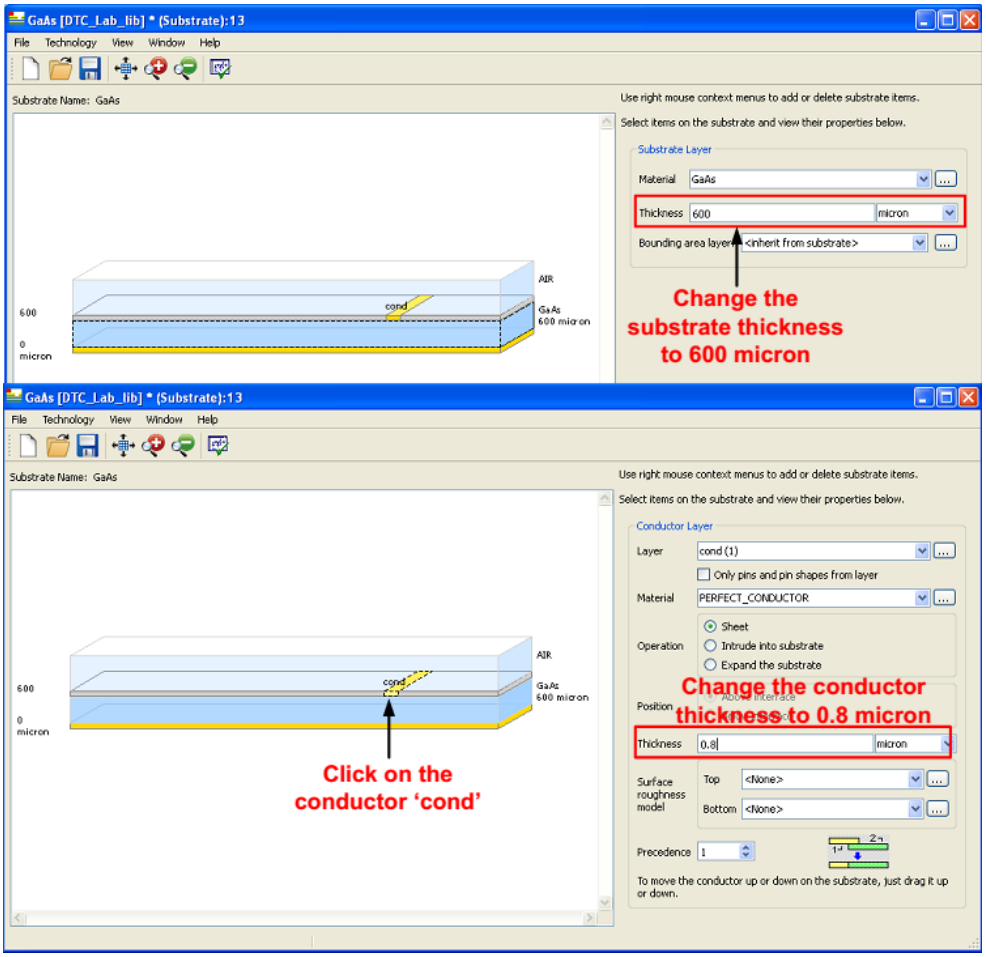


Figure 3.3: Setting-up the substrate and conductor layers.

By clicking on the conductor "cond" in Figure 3.3, one can set the conductor properties, for example setting "cond" as metal 1 (top metal layer that is below free space). The material is also set as well as the thickness of the metal conductor. In reality the metal conductor protrudes out of the substrate; therefore, the operation of the conductor should be set to 'Intrude into substrate'.

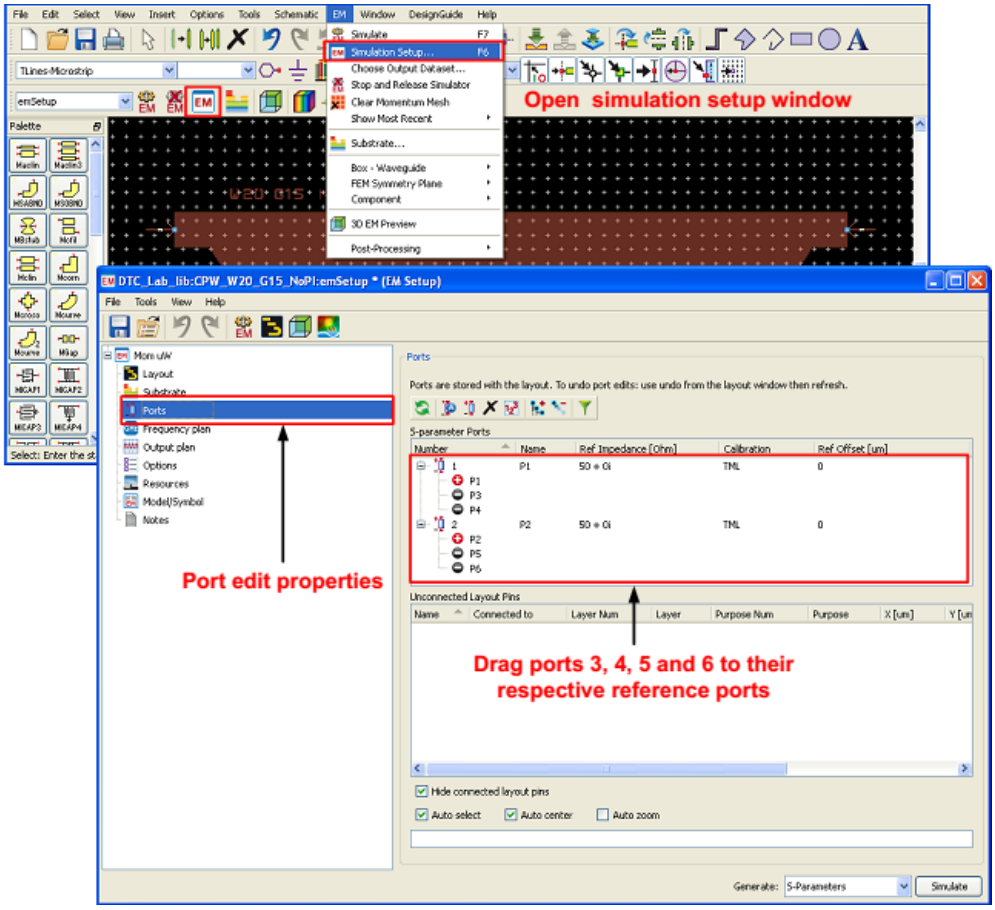


Figure 3.4: Setting-up the Ports Editor.

To define and edit ports, one has to use the ‘EM’ window, then ‘Simulation Setup’ and click ‘Ports’ in the EM setup window. In this tab window, ground ports like 3, 4, 5 and 6 can be dragged to their respective reference ports, as shown in Figure 3.4. A reference offset can also be set to a desired length, to match the probing pads offset during measurement.

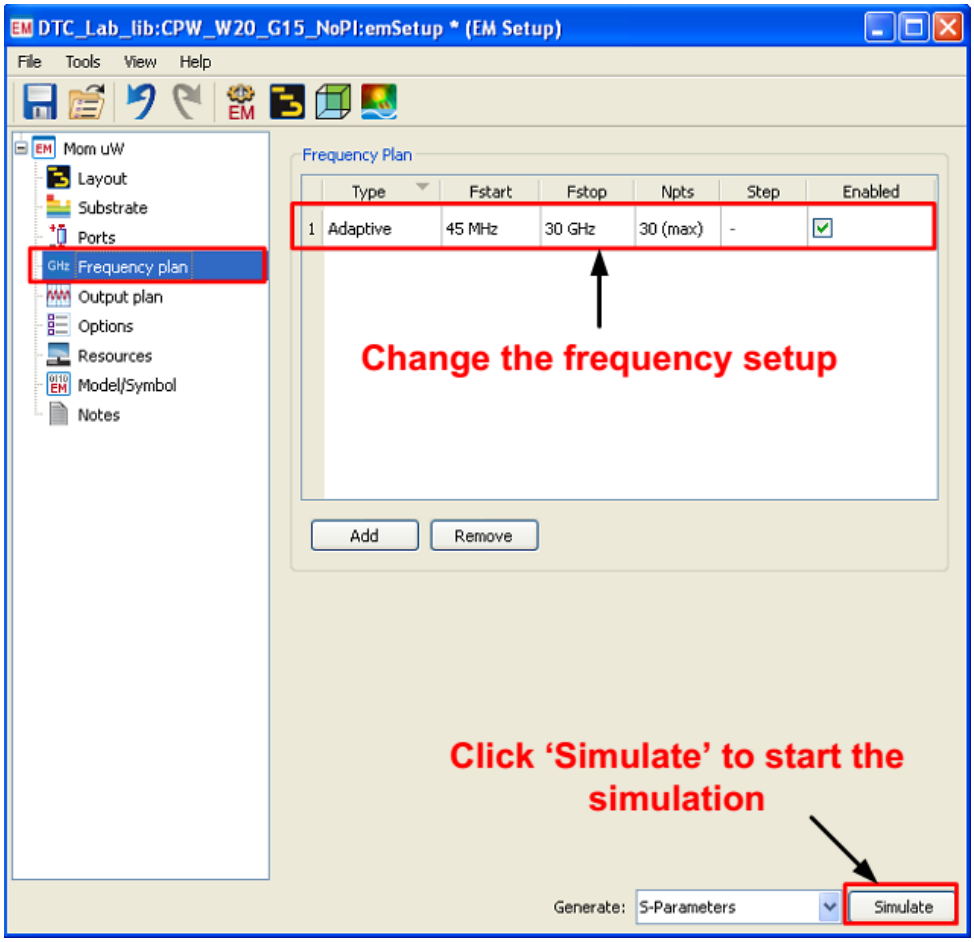


Figure 3.5: Setting-up the S-parameters simulation menu.

To run the simulation, one has to go to the 'Frequency Plan' tab. In this tab, a choice of simulation type can be made with the Adaptive or Linear options, and these can change the frequency setup to a desired range before proceeding to run the simulation, as shown in Figure 3.5.

In order to analyse the simulated structure, parameter extraction is carried out and the expressions for these parameters are derived from S-parameters, as shown in subchapter 3.2.

3.2 Extraction of Transmission Line Parameters using S-parameters

In this subchapter, the calculation methodologies used in ADS Momentum are generated from S-parameters. The transmission line parameters extracted using S-parameters are dependent on the length of the transmission line. These transmission line parameters are characteristic impedance, the effective dielectric constant and dissipation loss.

3.2.1 Calculation methodology for the Characteristic Impedance, Z_0

$$Z_0 = Z_{sys}\sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}} \tag{3.1}$$

Where $Z_{sys} = 50\,\Omega$ [55].

Equation (3.1) is inputted in the ADS Momentum to gain the characteristic impedance waveform.

3.2.2 Calculation methodology for effective dielectric constant $\varepsilon_{effective}$

The S-parameter responses measured from a lossy-matched transmission line with parameters γ and Z in a Z_0 impedance system are [77]:

$$[S] = \frac{1}{D_s}\begin{bmatrix} (Z^2 - Z_0^2)\sinh\gamma l & 2ZZ_0 \\ 2ZZ_0 & (Z^2 - Z_0^2)\sinh\gamma l \end{bmatrix} \tag{3.2a}$$

Where [27];

$D_s = 2ZZ_0\cosh\gamma l + (Z^2 + Z_0^2)\sinh\gamma l$

Since matrix (3.2a) is symmetrical it contains two independent linear equations. This S-parameter matrix is converted to ABCD parameters which incorporate the interconnect propagation constant $\gamma(\omega)$ and the impedance $Z(\omega)$ more explicitly.

The equivalent ABCD matrix (3.2b) is [47]: $$[ABCD] = \begin{bmatrix} \cosh\gamma l & Z\sinh\gamma l \\ \dfrac{\sinh\gamma l}{Z} & c\cosh\gamma l \end{bmatrix} \tag{3.2b}$$

In [30] the relationship between the S-parameters and the ABCD matrix is given as:

$$\begin{aligned} A &= (1 + S_{11} - S_{22} - \Delta S)/(2S_{21}) \\ B &= (1 + S_{11} + S_{22} + \Delta S)Z_0/(2S_{21}) \\ C &= (1 - S_{11} - S_{22} + \Delta S)/(2S_{21}Z_0) \\ D &= (1 - S_{11} + S_{22} - \Delta S)/(2S_{21}) \end{aligned} \tag{3.2c}$$

Where; $\Delta S = S_{11}S_{22} - S_{21}S_{12}$ [30]

$$\sinh(\gamma l) = \left\{ \frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11}^2)^2}{(2S_{21}^2)^2} \right\}^{1/2} \tag{3.2d}$$

$$\cosh(\gamma l) = \frac{\left(1 - S_{11}^2 + S_{21}^2\right)}{2S_{21}} \tag{3.2e}$$

Combining equations (3.2d) and (3.2e) yields:

$$\cosh(\gamma l) \pm \sinh(\gamma l) = e^{\pm \gamma l} = \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm \sqrt{\frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2}} \tag{3.2f}$$

where S_{11} is the power reflected from port 1, S_{21} is the power transmitted from port 2 to port 1 and l is the physical length of the transmission line in millimetres.

γ is made the subject in equation (3.2f).

$$\gamma = -l^{-1} \times In\left[\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} + \sqrt{\frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2}} \right] \tag{3.2g}$$

Therefore, from equation (2.8),

$$\beta = \mathrm{Im}\, ag(\gamma) = \mathrm{Im}\, ag\left[-l^{-1} \times In\left(\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} + \sqrt{\frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2}} \right) \right] \tag{3.2h}$$

Equation (3.2h) is inputted in the ADS Momentum to generate the effective dielectric constant waveform.

3.2.3 Dissipation Loss

The dissipation loss is obtained using S-parameters as follows:

$\alpha = (\mathrm{Re}\, al(\gamma))$ from equation (2.8)

$$= 10\log[\mathrm{Re}\, al(\gamma)]$$

$$\text{Dissipation loss} = 10\log\left\{\mathrm{Re}\, al\left[-l^{-1}\times In\left(\frac{1-S_{11}^2+S_{21}^2}{2S_{21}}+\sqrt{\frac{(S_{11}^2-S_{21}^2+1)^2-(2S_{11})^2}{(2S_{21})^2}}\right)\right]\right\}$$

(3.3c)

Second formula for dissipation loss

$$\text{Dissipation Loss} = 10*\log\left(\frac{1-|S_{11}|^2}{|S_{21}|^2}\right) \tag{3.3d}$$

where Pout = $|S_{21}|^2$ and transmitted power to the device = $\left(1-|S_{11}|^2\right)$

Either equation (3.3c) or (3.3d) is inputted in the ADS Momentum to generate the dissipation loss waveform.

3.3 On-wafer Measurements

Accurate device characterisation is essential for obtaining an overall precise performance of fabricated MMIC components. S-parameters can only be determined at microwave frequencies because they require matching load terminations [79]. Characterisation is carried out in two forms, i.e. the DC and the RF, as discussed in the proceeding subchapters.

3.3.1 DC Characterization

In this work the Keithley Semiconductor Parameter Analyser (SPA) is used to carry out DC characterisation. It is a modular, fully integrated parameter analyser that performs the electrical characterisation of materials, semiconductor devices such as diodes, field effect and bipolar transistors and processes with high precession [79]. The Keithley is used as a standalone system to check the initial functionality of Filtronic pHEMTs, and it can also be used with the general purpose interface bus (GPIB) interface to control the instrument from a PC. The GPIB is an IEEE 488 standard which supports a 1MBPS data transfer rate with 8-bit bi-directional data transfer. The Keithley is controlled by IC-CAP software installed on a PC through the GPIB interface between the PC and the Keithley. When IC-CAP is configured to perform measurements, it sends out commands to the Keithley which in turn sources the specified voltage or current. IC-CAP then collects and stores the measured data

in a specific format (*.mdm). During RF measurements or characterisation, the Keithley is used to supply the required DC bias to the device [55].

3.3.1.1 DC Measurements using IC-CAP

Agilent's IC-CAP is powerful commercial software specialising in DC and RF semiconductor device modelling. It extracts accurate compact model parameters for various applications, such as high speed digital, analogue and power RF applications. Technologies such as silicon CMOS, gallium nitride (GaN), III-V compound gallium arsenide (GaAs) and many more use IC-CAP to perform the tasks of measurement, simulation, optimisation and statistical analysis. IC-CAP not only provides a very reliable toolkit for the required tasks, but it also manages to perform all of these functions on a single platform.

The several industry-standard CMOS and FET models built-in to IC-CAP help in data acquisition and handling capabilities, which allows the user to perform a huge amount of measurements, extractions and optimisations with ease. Interactions with other instrumentation, such as DC sources, vector network analysers (VNAs) and other time/frequency domain instruments are carried out using the GPIB interface.

IC-CAP has an inherently built scripting language PEL (parameter extraction language) which automates a huge amount of tasks, hence minimising human interference. In this work, IC-CAP is used to perform DC and RF measurements as well as model parameter extractions. A typical view of the IC-CAP working environment is shown in Figure 3.6 [53].

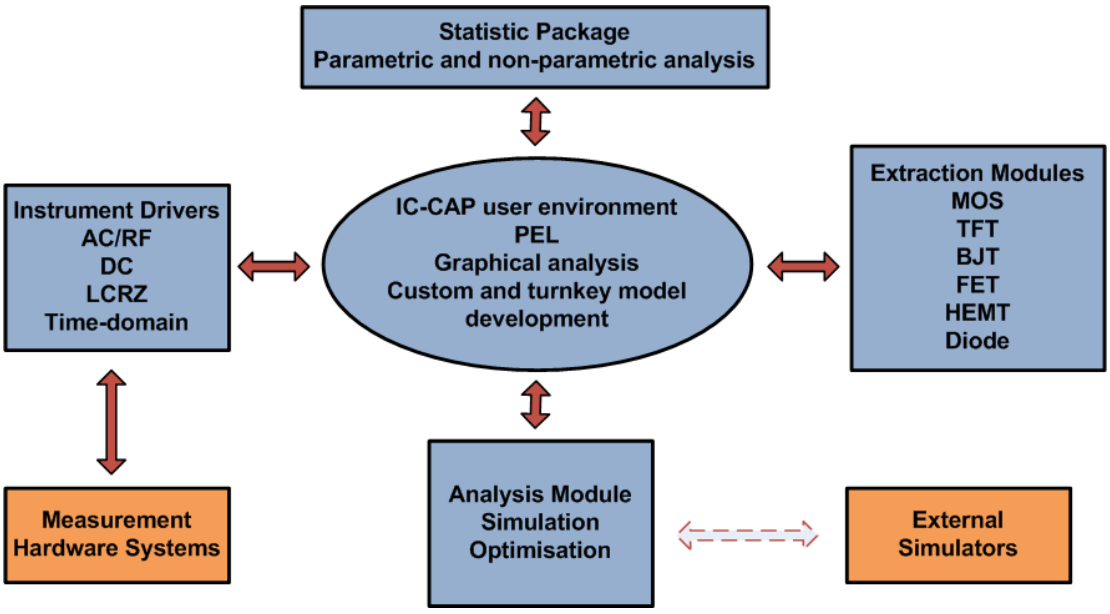


Figure 3.6: Pictorial view of IC-CAP environment.

3.3.2 Parameter Extraction in IC-CAP

The required bias conditions and measurement input parameters should be configured in such a way that IC-CAP can understand them and no errors can be found. Multiple measurements are taken and the results plotted on representative graphs. Figure 3.7 shows a typical IC-CAP measurement setup for measuring the input and output characteristics of a pHEMT. The Measure/Simulate tab in the window consists of forms for input and output, which correspond to source and monitor in the modular DC biasing units.

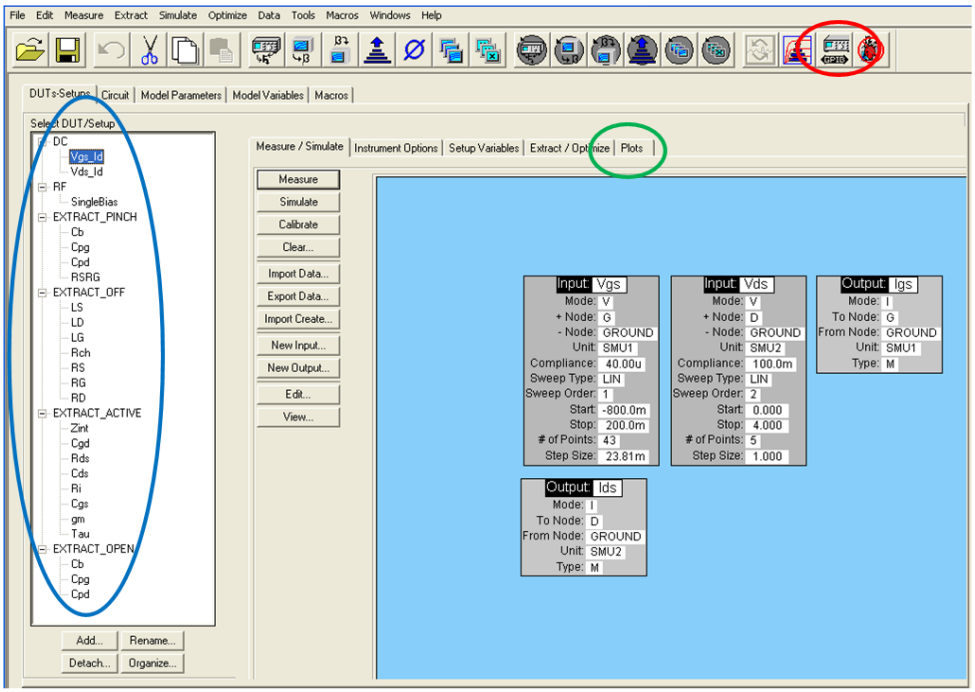


Figure 3.7: Typical IC-CAP window showing the DUT and setups (blue oval) and the instrument server option (red oval).

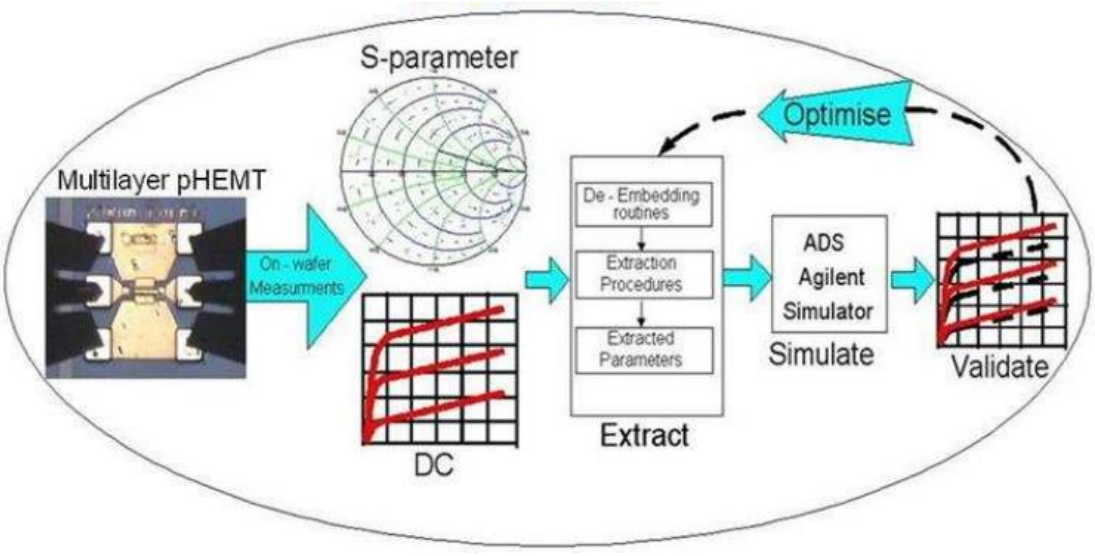


Figure 3.8: Flow diagram of parameter extraction using IC-CAP [53].

The instrument server options tab (red circle) is activated only when the measuring instruments are recognised by the setup. The procedure used to recognise the measuring instruments involves clicking the ‘GPIB’ icon, marked by the red circle in Figure 3.7. The GPIB icon sends signals on the GPIB bus which is connected to the DC source which should be switched ON. Upon sensing the instrument on the ‘Bus’, the instrument options tab is filled up with parameters related to the unit setting. The term ‘Bus’ corresponds to the connection between the SPA and the PC installed with IC-CAP. Each Bus connection between the PC and the instrument has a unique ID; hence, there will be no conflicts when the instruments operate simultaneously.

Under the ‘Setup Variables’ tab there are in-built variables available which control various operations for declaring arrays, plot options under the setup and file access variables. The DUT is always at the top level and under which we can have a number of setups; likewise, we can have a number of DUTs under one model file. The setup variables are local to the particular DUT. The option of defining a measurement or a simulation allows one to create model files which can measure and extract parameters and simulation models, allowing for comparison with measured results.

A DUT has three tabs, in which the simulation setup is specified under the ‘Test Circuit’ tab. The simulation can be defined in a standard SPICE format or more complicated Verilog/VHDL code. The ‘Extract/Optimise’ tab, which is used the most often, contains user-specific PEL routines which can be configured to operate on the measured data for parameter extraction purposes. ‘Optimise’ allows optimisation options that are used to optimise the extracted parameters so that the model correlates well to the measured data. However, in this work, optimisation is not used, as all the model parameters are directly extracted from measured S-parameters using well-established techniques.

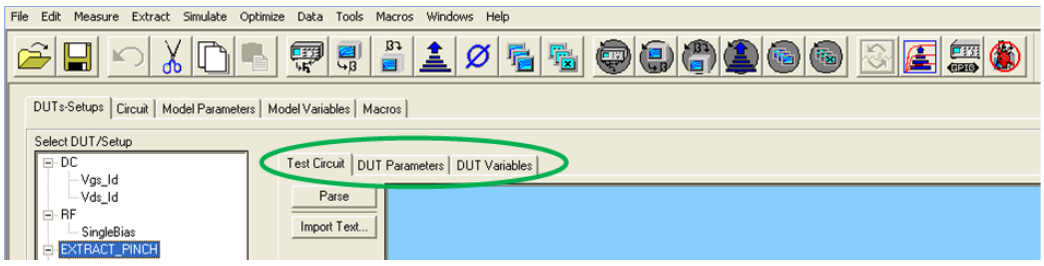


Figure 3.9: DUT tabs that allow options to define test circuits and corresponding parameters and local variables.

The IC-CAP also has available a ‘Macros’ feature. Macros are sets of programs which control the execution of other programs or operations. By using macros, the user can define the sequence of modelling activities, such as when the measurements should run.

3.3.3 Device Modelling Tool

Agilent's Advanced Design System (ADS) CAD software, used in this work, is a suitable electric circuit simulator that allows circuit design engineers to run circuit simulations in various settings, such as time or frequency domains. Its comprehensive library of electronic components and a user-friendly environment make it a vital tool for tasks such as modelling, designing and optimising electronic devices or circuits [53]. ADS provides several circuit configurations that reduce circuit complexity. Table 3.1 lists brief descriptions of the simulation types used in this work.

Table 3.1: Descriptions of ADS simulation types [53].

Simulator	Description
DC	Fundamental to all simulations; it performs a topology check and an analysis of the DC operating point of a circuit.
AC	Obtains small-signal parameters; such as voltage gain, current gain, and linear noise voltage and currents. This simulator is useful in designing passive circuits and small-signal active circuits such as low-noise amplifiers (LNAs).
S-parameters	Provides S-parameters, linear noise parameters, trans-impedance and trans-admittance. A linear small-signal analysis is performed that treats the circuit as a multiport. Each port is turned on sequentially and S-parameters can be converted to Y and Z-parameters.

DC simulation provides the DC operating characteristics of a circuit design. The simulator calculates the response of a circuit to a particular stimulus by solving it numerically with a formulated circuit equation system. Small-signal linear AC analysis and two-port scattering parameter simulations can also be carried out in ADS, while conversion to other parameters, such as Z, Y and ABCD, can also be performed.

The basic simulation procedure in ADS goes through the first step of creating the schematic, adding stimuli such as probes, labelling wires and pins. A simulation method is then selected with the required parameters specified. After the simulation is carried out, the acquired results can be viewed as specified. The data display window shows results plotted in various meaningful plots, such as logarithmic S-parameters (dB/frequency) or as a Smith chart. With the generated data plots, the circuit schematic can be retuned and

optimised to the desired targets. An example of a circuit schematic created in ADS is shown in Figure 3.10.

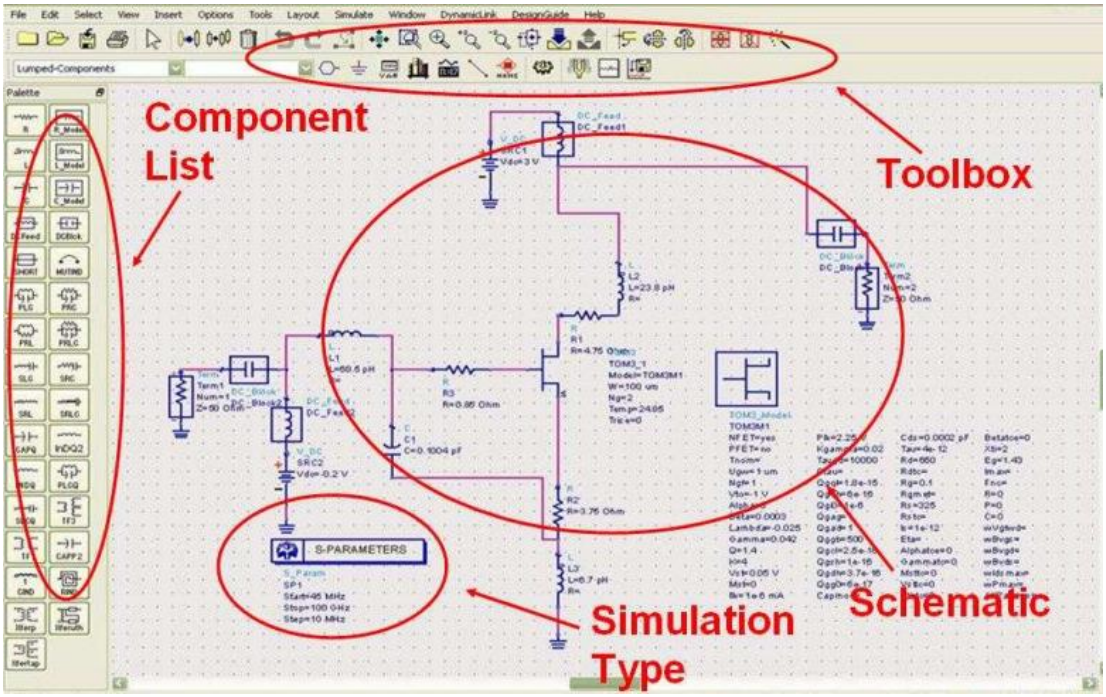
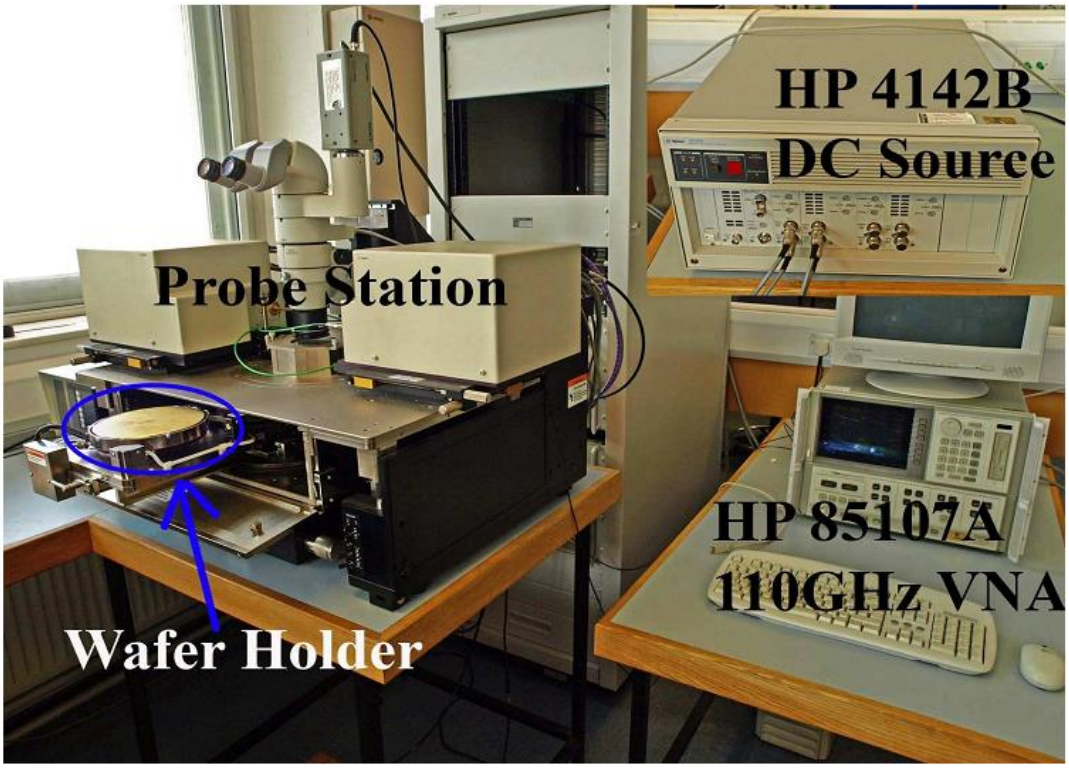


Figure 3.10: ADS Schematic simulator user interface.

3.3.4 On-wafer RF measurements

In this work, on-wafer RF measurements are carried out on all CPW-based multilayer passive components such as transmission lines, diodes, passive limiters and amplifiers. The proposed multilayer CPW components and circuits are measured with the HP85107A vector network analyser (VNA). Active components, such as the prefabricated pHEMTs from Filtronic and amplifiers, are also measured using the HP85107A VNA and DC source HP4142B controlled by the IC-CAP. The HP85107A VNA is able to provide S-parameter measurements from 45 MHz to 110 GHz. Ground-signal-ground (GSG) types of microwave probe with a pitch size of 200µm are used to probe the components, and a Keithley 4200 SPA DC biasing unit in conjunction with IC-CAP is used to bias the components with active pHEMTs. Figure 3.11 shows the equipment setup.



(a)

(b)

Figure 3.11: Probe stations and VNA systems used in this work; (a) for frequencies up to 110 GHz and (b) for frequencies up to 50 GHz.

3.4 Network Analyser Calibration

Calibration is performed using the impedance standard substrate (ISS), which contains impedance standards with known microwave characteristics. The commonly used impedance standards are: open, short, load and thru (shown in Figure 3.12). The probes used for this work are 200µm pitch-sized from 45 MHz to 50 GHz.

Network analyser calibration involves characterising the entire test fixture so that subsequent measurements will pertain only to the device under test (DUT). When performing a calibration, there are trade-offs between the type of standards measured and the mathematical algorithms used to compute the error model [81]. For a particular technique, certain standards play a particular role in the overall characterisation. For some calibration methods, such as SOLR, the characteristics of other standards, such as the thru path, are of little or no significance [81].

The three most common calibration techniques are as follows:

- SOLT (Short, Open, Load, Thru)
- SOLR (Short, Open, Load, Reciprocal)
- LRRM (Line, Reflect, Reflect, Match)

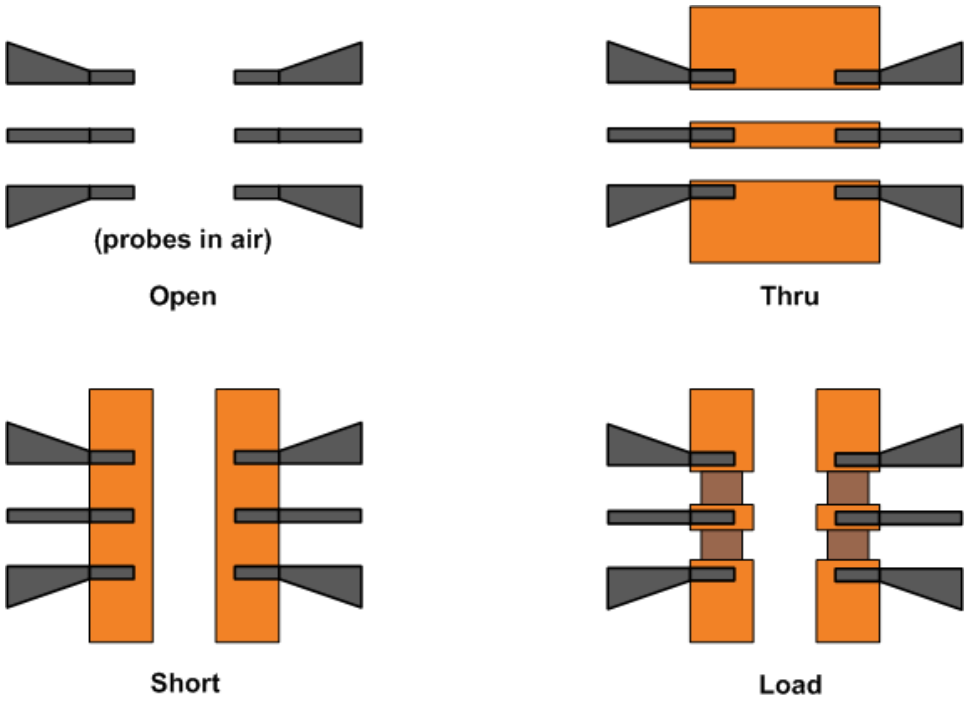


Figure 3.12: Sketch of the GSG probes on Impedance Standard Substrate (ISS) standard.

3.4.1 SOLT Calibration

SOLT calibration is defined as Short-Open-Load-Thru calibration, and it is currently the most commonly used calculation kit and is readily available. The open standard has an open capacitance which is often negative and is measured when the probes are in air. Short and load standards have inductance and are measured as shown in Figure 3.12. The SOLT calibration technique performs reasonably well, if accurate models of calibration standards can be determined, and it is very sensitive to probe placement.

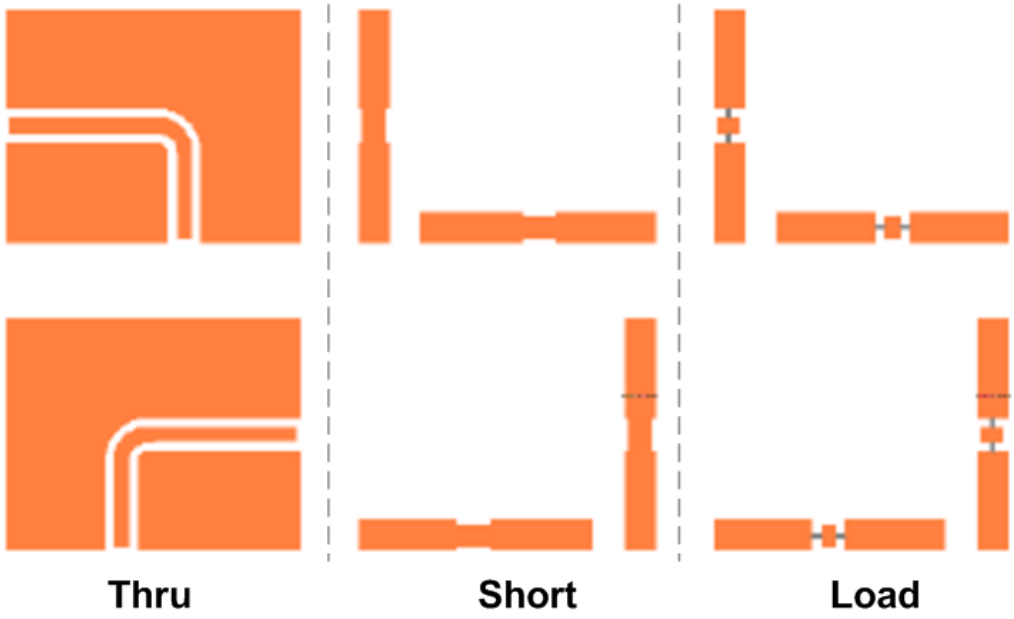


Figure 3.13: Schematic diagram of a calibration standard used in SOLT calibration [81].

3.4.2 SOLR Calibration

SOLR calibration is defined as Short-Open-Load-Reciprocal calibration. This calibration technique is similar to SOLT but with a general 'Thru' standard where reciprocal thru S_{12} = S_{21} and tolerant to high loss or highly reactive insertion standard. The technique is not available on network analysers, it requires Cascade Microtech software (WinCal) and it still needs accurate calibration standard models.

3.4.3 LMMR Calibration

LMMR calibration is defined as Line-Reflect-Reflect-Match calibration and is available in WinCal software and only requires a match standard on one port. It also uses off-wafer standards. LRRM provides a very high degree of repeatability in one-port and two-port measurements.

The LRRM technique is an integral feature of Cascade Microtech's WinCal VNA calibration software, which measures the characteristics of a device connected to the measurement reference plane. The calibration is said to be good only when the S_{11} plot is well within ±0.10 dB, as shown in Figure 3.15.

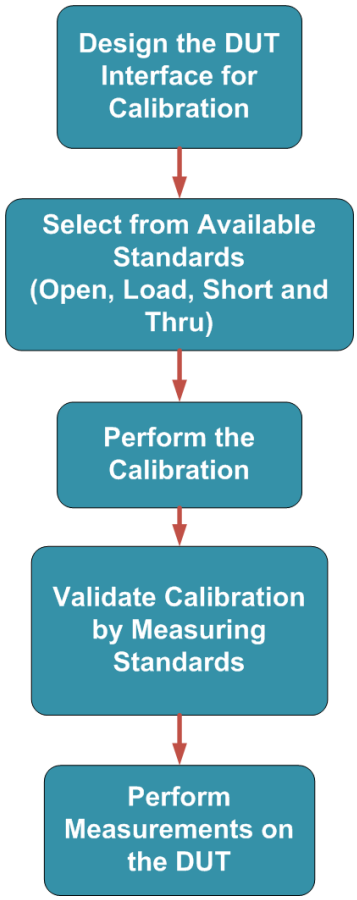


Figure 3.14: Flow chart of the calibration procedure.

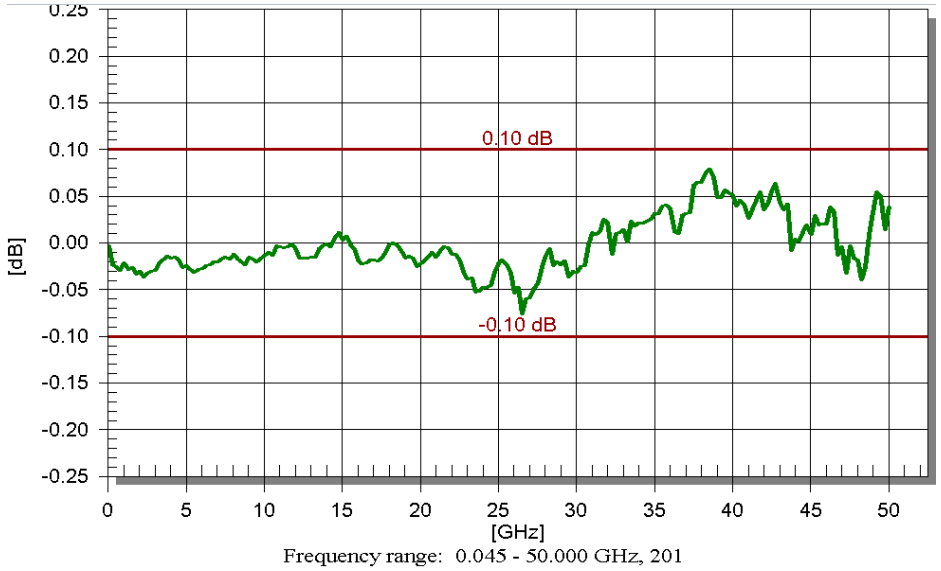


Figure 3.15: Magnitude (S_{11}) corresponding to a good calibration.

If the plot deviates too much from the ±0.10 dB range, then the calibration procedure has to be repeated. WinCal provides a unified calibration and measurement environment within one software application. After calibration, measurements may be taken from WinCal or directly from the VNA.

3.5 Multilayer MMIC Fabrication

Due to the monolithic nature of MMICs, they are manufactured as small parts of a whole wafer of semiconductor material. The processing of the wafers involves forming microscopic features on their surface; therefore, for this reason, all equipment is installed in a clean room environment to prevent moisture from affecting the features. This makes the fabrication process very time-consuming and costly, and often the correct functionality of the circuit cannot be checked until the whole process is complete. Therefore, it is imperative that the design of the chip is made right first, before committing to the fabrication process.

The most common choices of dielectrics used in MMIC applications are silicon nitride (Si_3N_4), silicon dioxide (SiO_2) and polyimide. Polyimide dielectric can be formed by spinning on the substrate surface and then being cured afterwards. In theory, any polyimide thickness can be formed by changing the viscosity of the material. Thus, thick polyimide can be obtained without the cracking problems encountered in Si_3N_4 or SiO_2 films through a careful curing process [16]. Polyimide has high dielectric breakdown strength, high

resistivity and a low dielectric constant, thereby making this dielectric suitable for a variety of MMIC fabrications [16].

Three-dimensional multilayer fabrication was carried out in the School of Electrical and Electronic Engineering clean room at the University of Manchester. In this work, a mask set (ver.5) with both active and passive components is fabricated on a GaAs wafer. The mask set (ver.5) is made up of five layers, namely three metal conductor layers and two dielectric layers, as shown in Figure 3.16.

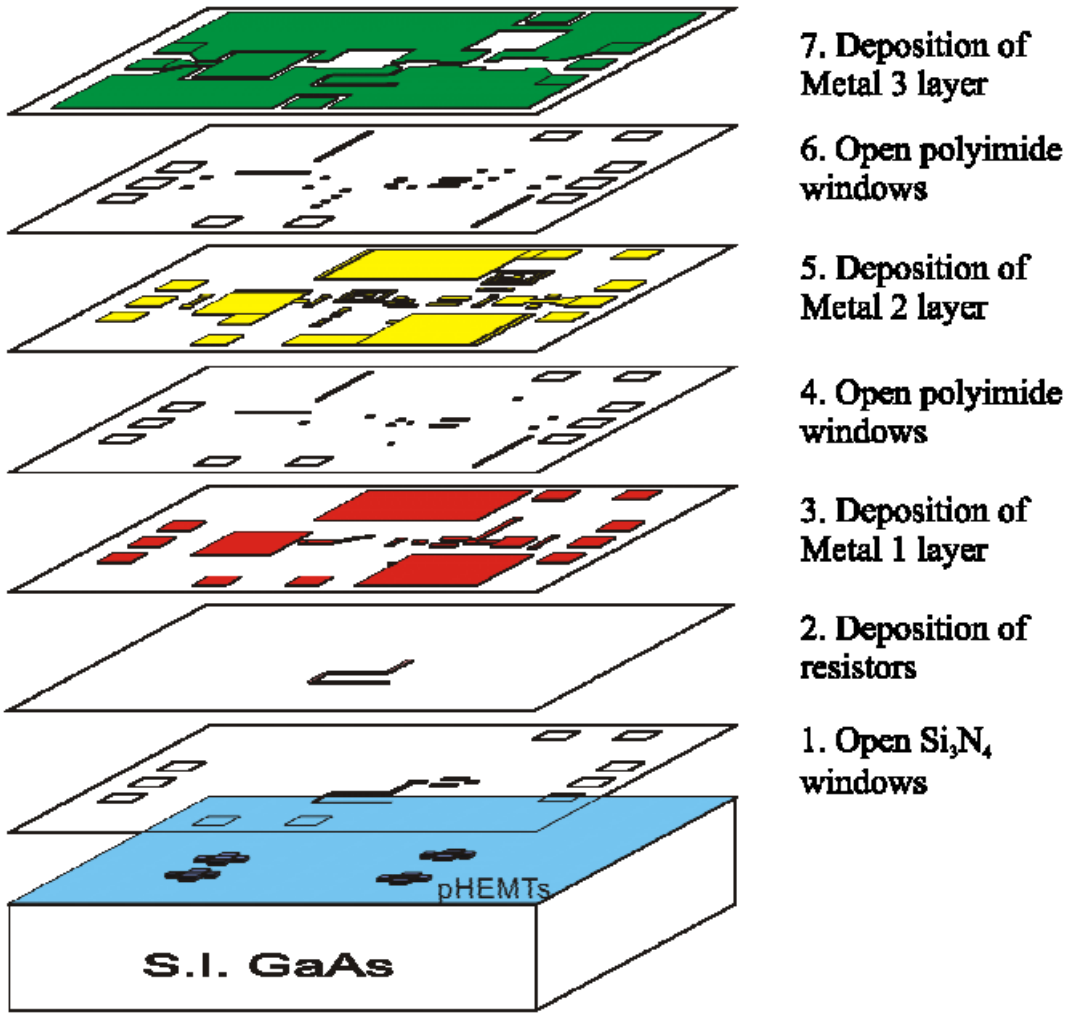


Figure 3.16: 3D multilayer mask set (ver.5) layout.

3.5.1 Multilayer MMIC fabrication procedure for active and passive components

The fabrication procedure involves four main processes:

- Photolithography
- Metal deposition
- Polyimide deposition
- Etching

The deposition process is additive, the etching process is subtractive and the curing or doping processes are for modification purposes.

One of the first steps in any form of fabrication is wafer preparation. The surface of the GaAs wafer substrate is thoroughly cleaned using chemicals such as acetone or methanol to remove organic dielectrics. The wafer can also be cleaned using an ultrasonic bath while in a beaker of acetone. De-ionised water is used finally to wash away the cleaning chemicals.

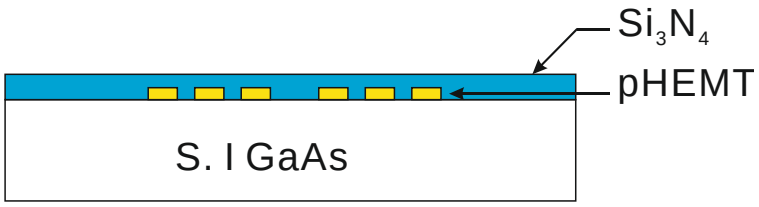


Figure 3.17: GaAs substrate wafer with pHEMTs.

The GaAs substrate wafer with pHEMTs is supplied by the Filtronic semiconductor foundry.

3.5.1.1 Opening Si_3N_4 windows

Opening the Si_3N_4 window on the GaAs substrate with pHEMT transistors is the first step undertaken during the multilayer fabrication process. This is done by etching away the Si_3N_4, and great care should be taken, as a poor Si_3N_4 etch would result in poor metal contact.

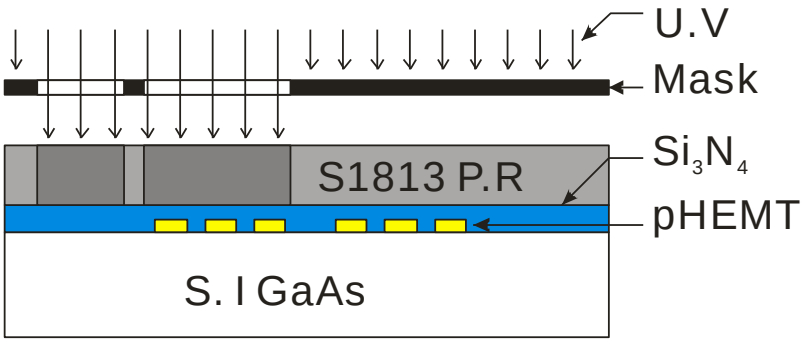


Figure 3.18: Applying photoresist for photolithography to open Si_3N_4 window.

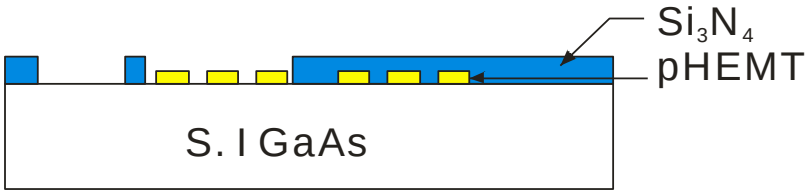


Figure 3.19: GaAs wafer is opened Si_3N_4 window.

The sample is baked for 10 minutes at 110˚C to dry. Thin photoresist (S1813) is then spun at 5200rpm for 30 seconds. Soft-baking is done at 90˚C for 30 minutes, after which the back of the wafer is checked to make sure there is no photoresist residue. The sample is then exposed for 45 seconds and developed in a 1 Microdev to 1 D.I. water mixture for 50 seconds. A 30-minute post-bake at 110˚C follows. Buffered HF is used to remove Si_3N_4 for 120 to 140 seconds. At this stage, no Si_3N_4 should be found in the opened pattern. Finally, acetone is used to remove the remaining photoresist and the sample is then rinsed in D.I. water.

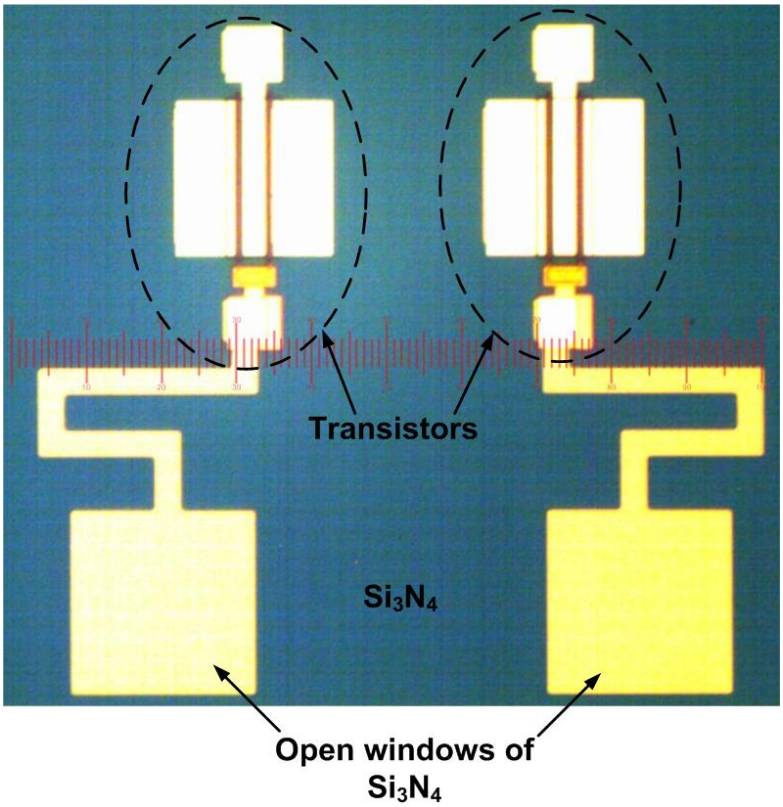
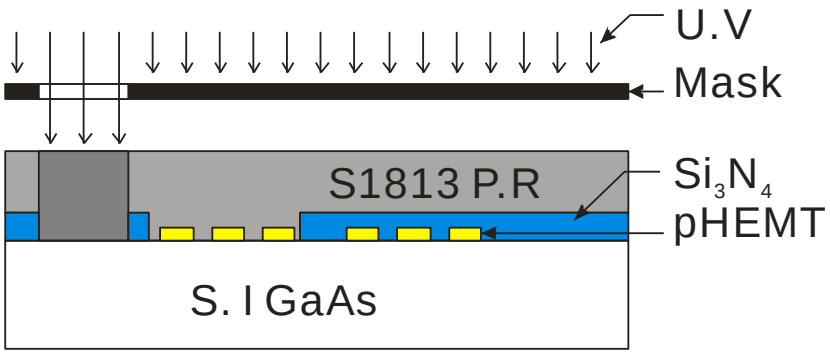


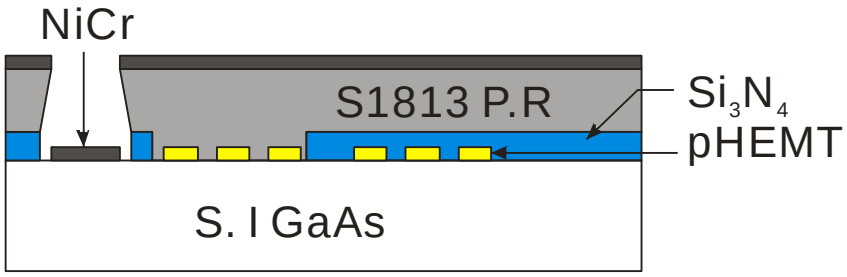
Figure 3.20: Micrograph showing opened Si_3N_4 widows.

3.5.1.2 Thin-film resistor deposition

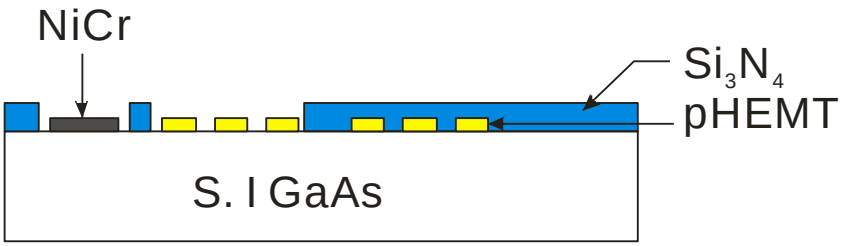
During fabrication, resistors can be produced using deposited thin metal films, such as NiCr or TaN. In this work, a nickel chrome wire alloy, at a ratio of 80% nickel to 20% chromium, is evaporated to form a thin film resistor. The sheet resistance of the thin film resistor depends on the ratio of Ni and Cr.



(a)



(b)



(c)

Figure 3.21: Thin film NiCr resistor deposition process; (a) photolithography, (b) NiCr deposition and (c) NiCr lift-off.

The sample is first cleaned and then dried at 110˚C for 10 minutes. Photoresist is spun on to the wafer at 5200rpm for 30 seconds, followed by a soft bake at 70˚C for 30 minutes. The back of the sample is then checked to make sure that there is no photoresist residue. After that, the sample undergoes a 45-second exposure and is developed in a 1 Microdev to 1 D.I. water mixture for 50 seconds. The sample is then cleaned for 15 seconds using HCL (10%) to remove the metal oxide. Finally, the metal is lifted off using acetone.

After opening the Si_3N_4 and deposition of the thin film NiCr resistors, the steps that follow are similar to the ones in the passive component fabrication from step 1 in Figure 3.23.

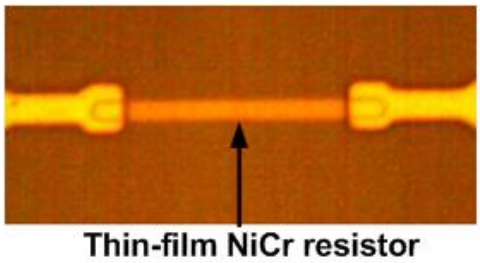


Figure 3.22: Thin film NiCr resistor micrograph after deposition.

3.5.1.3 Metal deposition

The process in this work involves the thermal evaporation of titanium (Ti) and gold (Au) on the wafer.

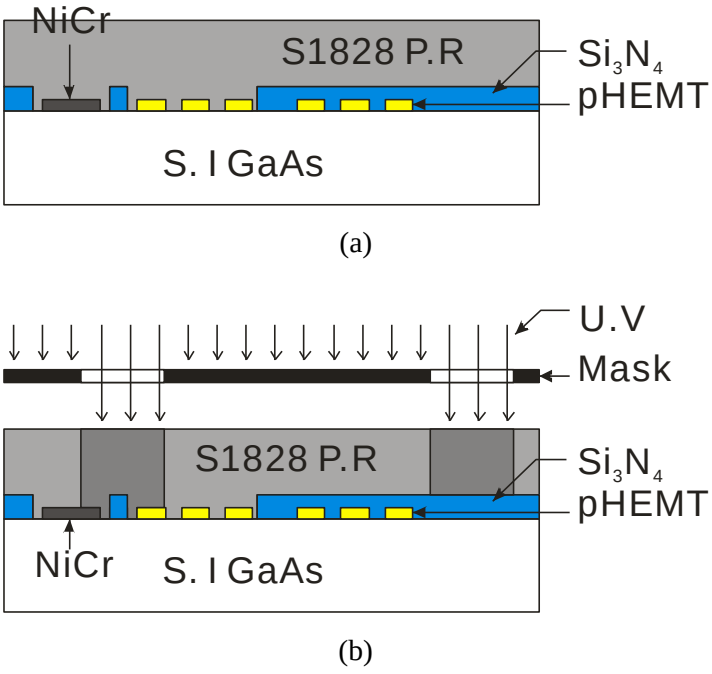


Figure 3.23: Multilayer fabrication process: (a) photoresist deposition. (b) Photolithography.

The GaAs wafer is cleaned and then photoresist S1828 is spun on at 5200rpm for 30 seconds. After spinning the photoresist, the wafer undergoes a soft bake for 20 minutes at 70ºC. This helps to drive off most of the solvent in the resist and to establish exposure characteristics.

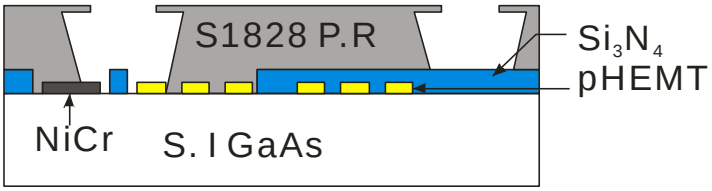


Figure 3.24: Developed profile of photoresist ready for metal evaporation.

Chlorobenzene is then used to harden the photoresist for one minute, after which the sample is post-baked at 70ºC for 5 minutes. The photoresist is developed using a mixed solution of two parts Microdev and one part water. Plasma etching is used to remove photoresist residue for 30 seconds at 30W. Thereafter, the sample is cleaned using hydrochloric (HCL) acid at 10% concentration for 15 seconds and finally rinsed using de-ionised water.

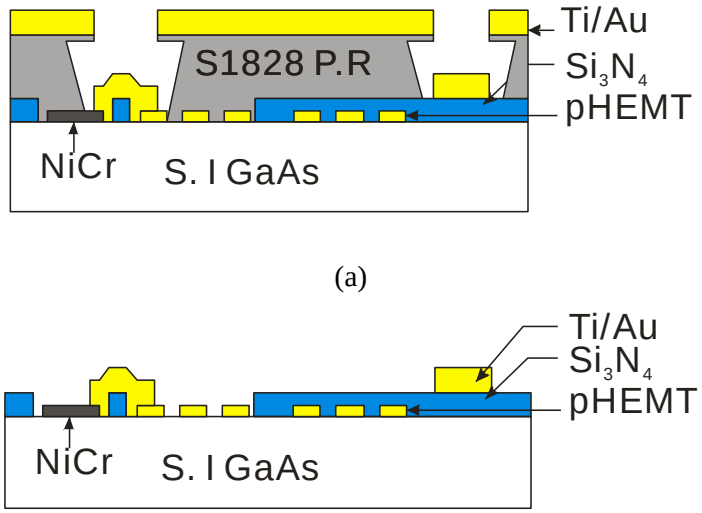


Figure 3.25: Metal deposition: (a) Titanium and gold evaporated. (b) Metal lift-off.

During thermal evaporation, titanium is slowly evaporated at a rate of 0.1nm/s to prevent the photoresist overheating. Dirt on the titanium rods is evaporated first before opening the shutter. After evaporating a thin-film of titanium, gold is evaporated with an adjusted speed of 1nm/s. Evaporation is stopped for 10 minutes for every 150nm of gold deposited, to avoid the photoresist overheating. The sample is placed in a photoresist stripper 1165 (NMP) to lift off the unwanted metal by removing the photoresist. Finally, the sample is rinsed in de-ionised water and cleaned with acetone.

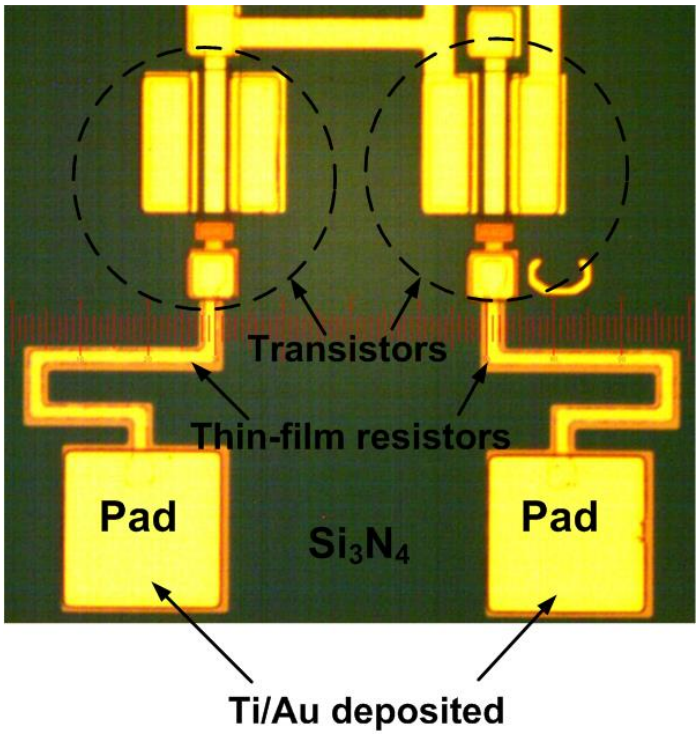


Figure 3.26: Micrograph of deposited Ti/Au on a developed pattern.

3.5.1.4 Polyimide deposition

In this work, polyimide is used as an interlayer dielectric in multilayer fabrication. The polyimide is typically spin coated onto the wafer, allowing for a flat uniform thickness coating of resin material. The resin is then cured into a smooth structural layer that can be patterned using a photolithographic process [83]. Although some polyimides contain light-sensitive chemicals, meaning they can be patterned without the use of a photoresist, and hence making fabrication a bit simpler, in this work the PI-2610 polymer liquid used would require a photoresist for patterning. A 2.5µm thick polyimide layer of PI-2610 polymer liquid, purchased from HD Microsystems, is spin coated onto a GaAs wafer, cured and then patterned. The processing steps that follow below are found to give repeatable results.

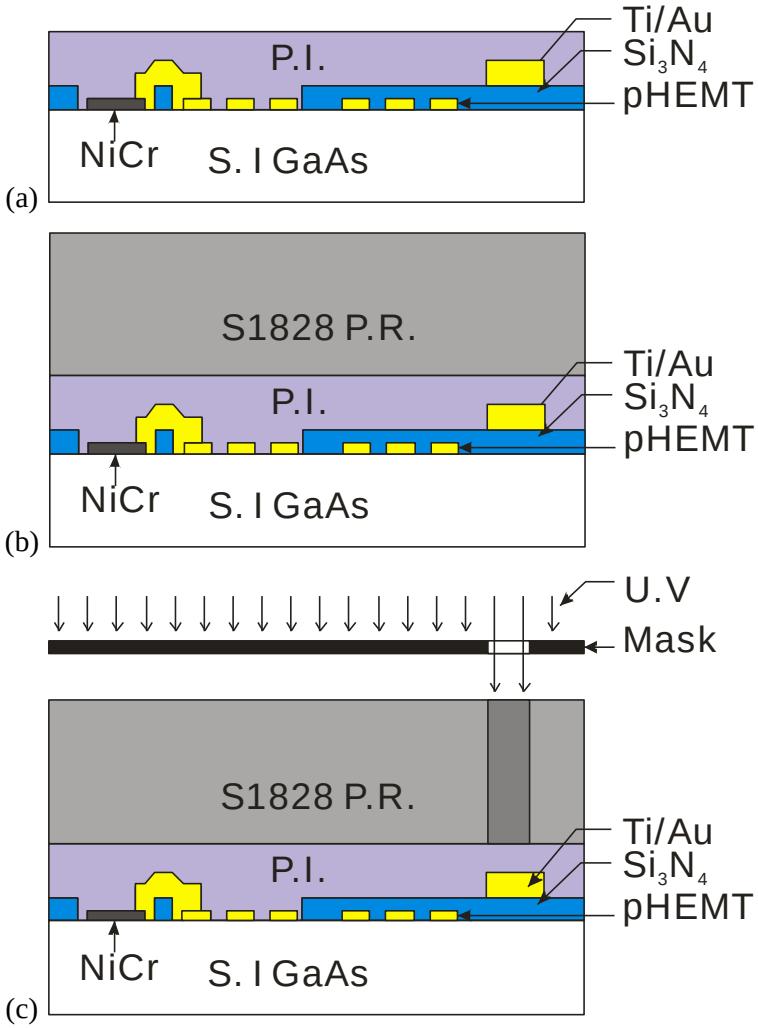


Figure 3.27: Multilayer fabrication steps of polyimide deposition: (a) applying polyimide, (b) applying photoresist and (c) mask alignment and exposure.

The GaAs wafer is cleaned using a standard semiconductor wafer cleaning procedure that involves an acetone soak and rinse, followed by an isopropyl rinse, a rinse in de-ionised (DI) water and finally blow drying the wafer with nitrogen gas. As polyimide has a short shelf life at room temperature, the polyimide resin material is kept refrigerated, as recommended by the manufacturer. It is therefore essential to bring the polyimide up to room temperature before opening the container, in order to guarantee that water vapour does not contaminate the resin [83].

Initially, the polyimide resin is brought to room temperature in its original container and carefully poured onto the wafer centre and allowed to settle while making sure that no bubbles are added to the resin. The sample is then spun at 2600rpm for 30 seconds, in order to achieve a polyimide thickness of 2.5µm. The polyimide is then soft-cured at 110ºC for 30 minutes in an oven. After soft curing, care is taken to remove any polyimide residue from the rear of the wafer using a Microposit developer. This is followed by the final curing of the polyimide at 200ºC for 4 hours in a vacuum oven.

After the sample has cooled down to room temperature, it then undergoes a semiconductor cleaning procedure. Once cleaning is done, S1828 type photoresist is spun on the sample at 4000rpm for 30 seconds. After spin coating, the wafer undergoes a soft bake at 90ºC for 20 minutes, in order to drive off most of the solvent in the resist and to establish the exposure characteristics. The rear of the sample is checked for any photoresist residue that may require removal. The sample is then carefully aligned with the mask, which is followed by an exposure of 250 seconds.

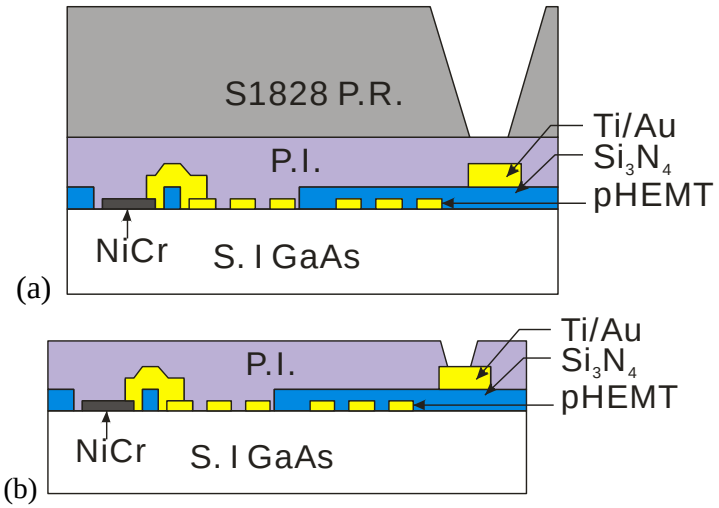


Figure 3.28: Multilayer fabrication steps of polyimide deposition: (a) developed photoresist pattern and (b) etched away polyimide profile.

A solution of two parts Microdev and one part water is used to develop the photoresist pattern on the sample for about 90 seconds. The sample is then post-baked at 110ºC for 20 minutes to harden the photoresist before etching. The rear of the wafer is checked for any photoresist residue. Plasma etching of the sample is carried out at 50scm of oxygen, 100W and 100mTorr for 10 to 12 minutes. The sample is then rinsed in NMP to remove any photoresist, and one minute of plasma etching at 50W follows, to improve metal adhesion. To remove any polyimide residue, the sample is rinsed in Microposit developer and finally in de-ionised water.

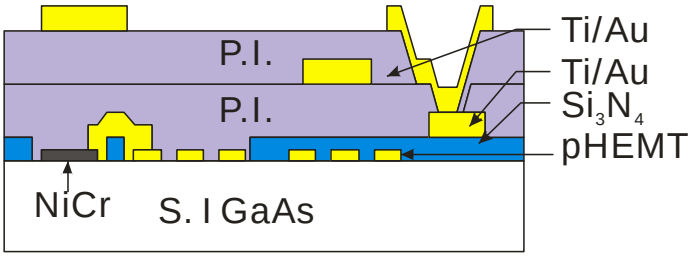


Figure 3.29: Cross-sectional view of all multilayer fabricated layers.

After the deposition of the NiCr thin-film resistor layer, five fabrication layers follow, including three metal (Ti/Au) depositions and two polyimide depositions. The polyimide layers are sandwiched between the metal layers. All three metal depositions and two polyimide depositions follow the same fabrication steps described previously. Therefore, the cross-section of the finished sample will be similar to the one in Figure 3.29.

3.5.2 Fabrication Challenges Encountered and Possible Solutions

During the fabrication process applied to this work, not all went according to plan, and there were a number of challenges that were encountered, as detailed below. Further possible solutions that were used to overcome these challenges, for the successful completion of the whole wafer fabrication process, are also provided.

The main challenges encountered involved:

- Small bubbles trapped in the polyimide layer after the curing process.
- GaAs wafer breaking while using the ultrasonic bath.
- Metal lift-off.
- Underdeveloped photoresist pattern.

3.5.2.1 Possible Solutions

Ultrasonic bath

During any wafer cleaning process, one might decide to use an ultrasonic bath, though carrying this out in a glass beaker may make GaAs wafers prone to breaking. It is therefore recommended to use a plastic beaker instead of a glass beaker, and bath time should not exceed more than 5 minutes. During the metal lift-off process, an ultrasonic bath can certainly be used, albeit under the same conditions as when using a plastic beaker.

Polyimide curing

During the plasma etching process for polyimide on one of the test samples, it was observed that after etching off approximately 1µm from an approximately 2 µm-thick polyimide layer, some grey spots start to appear on the surface of the polyimide, as shown in Figure 3.30. After a number of tests on different samples, it was further observed that the grey spots disappeared if the wafer with the polyimide were etched further. At first it was thought the spots were a wafer contamination issue or an oxygen plasma etcher problem, though this was not the case – it was later found that these spots were due to bubbles trapped in the polyimide film.

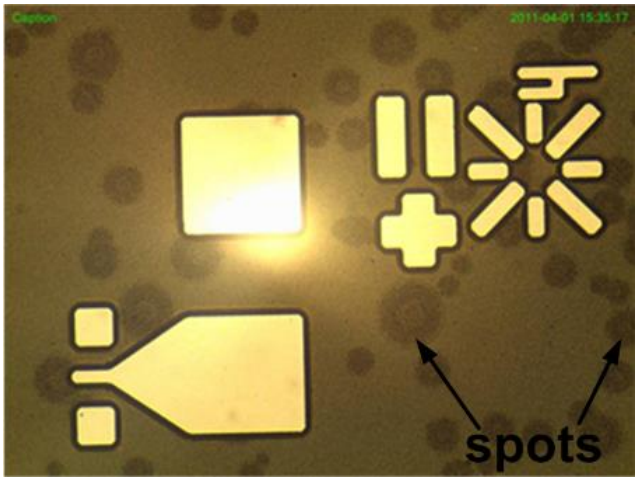


Figure 3.30: Polyimide surface after plasma etching off 1 µm.

After the curing process, observable small bubbles trapped in the polyimide layer cause problems with photolithography. In this case, the possible solution is to bring the resin up to room temperature in its original container, then de-gas the polyimide just prior to applying it to the wafer surface. Polyimide from the freezer is brought up to room temperature overnight while in its original sealed container. A small amount of the

polyimide is poured into a glass beaker, and the beaker is then placed into a mini vacuum desiccator, as shown in Figure 3.31. The polyimide is de-gassed for several hours just prior to using it, which helps to avoid trapped bubbles in the final polyimide liquid.

Figure 3.31: Image of the desiccator setup [83].

Development of the photoresist pattern

The underdevelopment of a photoresist pattern is mainly the result of setting the wrong development time in relation to exposure time. One has to determine the right exposure time for the applied resist which will not result into over-exposure and hence distort the resist patterns. Once an appropriate exposure time has been determined, the developing of the resist patterns on the sample is carried out with the right amount of Microdev solution. For this work, a solution of two parts Microdev and one part water is used for developing the resist and is carried out into phases: the mixed solution is divided into two beakers, in order to develop the sample into two parts, and the development takes place in one of the beakers for half of the development time and the other half of the time in the second beaker. The last rinse in the second beaker helps remove any extra unwanted resist residue.

Since chlorobeneze is used in the photolithography process that leads to metal deposition, great care should be taken in its use, as it hardens the surface of the photoresist; therefore, one should not leave the sample in the solution for too long (maximum 1 minute), as an over-hardened photoresist surface will make it harder to develop. One would also find it useful to use wafer samples with a big enough surface area for the multilayer fabrication

process, as this helps with the uniform distribution of photoresist during spinning and also helps the developing process. A good minimum wafer area recommendation would be approximately 12.25 cm^2. Figure 3.32 shows micrographs of both an underdeveloped pattern and a well-developed photoresist pattern.

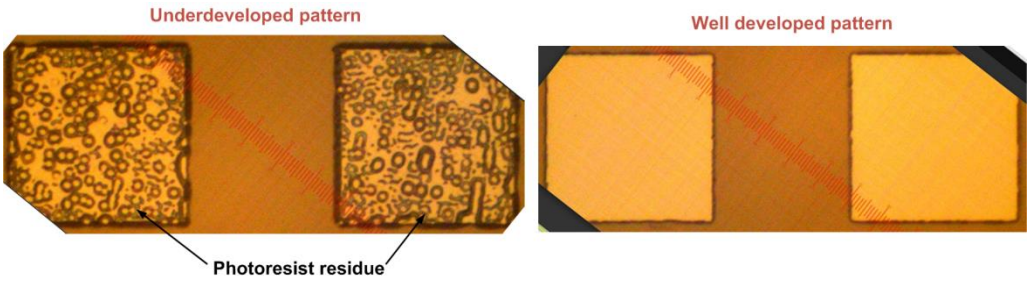


Figure 3.32: Micrographs of an underdeveloped pattern and a well-developed photoresist pattern.

Metal lift-off

The metal lift-off problem in the multilayer fabrication process is a serious issue and is caused mainly by poor adhesion between the two metal surfaces or poor adhesion between the wafer surface and the metal (Ti/Au). Adhesion can be improved by taking good care of the following:

- Making sure the surface of the wafer is cleaned very well following the semiconductor cleaning procedure described earlier. Adhesion between two metal layers can be improved by cleaning the sample in a diluted hydrochloric acid (10%) solution. It is also used to remove metal oxide.

- Great care should be taken during the development of the photoresist pattern, because if unwanted photoresist residue remains in the developed patterns, this will bring about an adhesion problem between the metal layers.

- By achieving a good vacuum during thermal evaporation, one can also improve metal adhesion. By pre-heating up the chamber, using the heater on the evaporator system, one can de-gas the system and hence help it to pump down faster. To have good evaporation with no adhesion problems, the system should be pumped down to below $1.5x10^{-6}$ Torr. A very clean chamber, and ensuring that the glass bell jar is well cleaned, will improve the system vacuum. Care must also be taken when

switching off the system, and after evaporation the rotary pump should be left on for a while until it cools down after switching off the diffusion pump. Figure 3.34 confirms that with a longer pre-pump-down of the diffusion pump, pressure in the bell jar can fall $1x10^{-6}$ mbar faster compared to a short pre-pump-down.

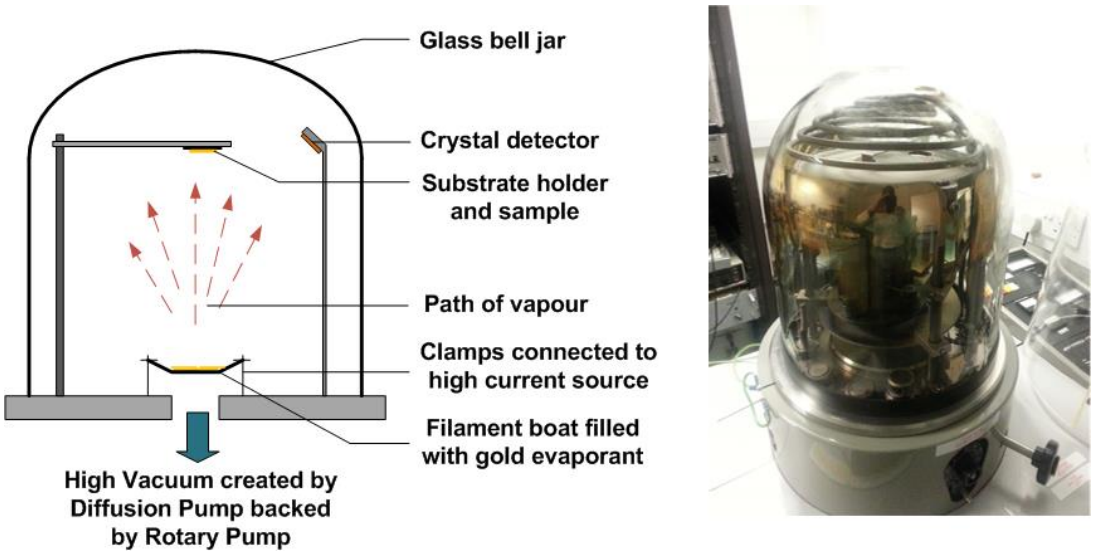


Figure 3.33: Sketch and actual photo of the thermal evaporator.

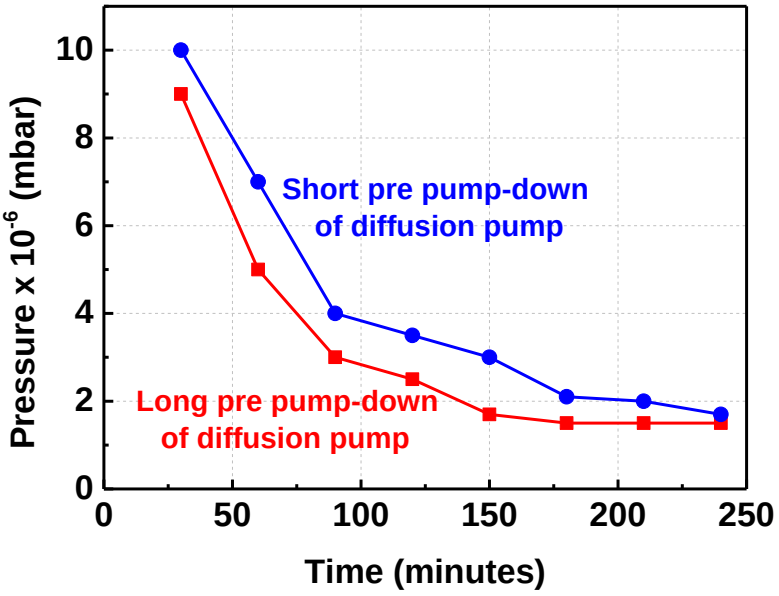


Figure 3.34: Thermal evaporator pump-down.

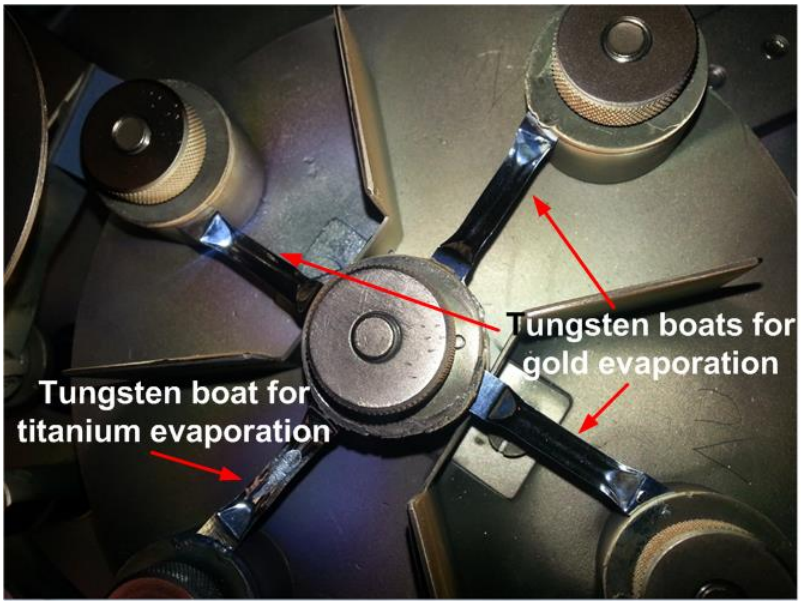


Figure 3.35: Actual photo of tungsten boats on the electrodes inside the thermal evaporator.

In this work, three tungsten boats are used for gold thermal evaporation, and one boat is used for titanium evaporation. Three tungsten boats are used for gold due to the amount of metal needed to achieve a thickness 0.8µm. This in turn helps distribute the gold evenly between the different boats, to prevent them from breaking during the evaporation due to overloading if one boat is used for all the gold. This further prevents overheating of the photoresist on the sample, which would otherwise make good metal lift-off difficult to achieve.

Figure 3.36: Tungsten boats of different sizes.

Great care must also be taken in choosing the right size boat to use during thermal evaporation. For this work, both boats shown in Figure 3.36 above were tested for thermal evaporation, and it was found that although the large boat can take a big load of gold strips, it would require a lot of current to achieve evaporation. Therefore, the smaller boats were found to be more suitable, as they require less current and hence prevent overheating the photoresist on the sample.

Chapter 4 MMIC Fabrication Results and Discussions

4.1 *Fabrication process calibrations*

Fabrication of MMIC components enables one to test and compare simulated design results with the actual measured results on fabricated wafers. In particular, with 3D multilayer fabrication, one can employ several layers of metals sandwiched by insulators, thereby allowing both thin-film microstrip lines and coplanar techniques to be used. This gives microwave engineers great flexibility in designing multilayer structures along with improved circuit performance.

4.1.1 Tooling Factor

The tooling factor is a way of correcting for differences in the material deposited on the quartz crystal sensor versus the substrate, as any difference in distance between the sensor and substrate might cause an incorrect reading on the thermal evaporation system, as illustrated in Figure 4.1.

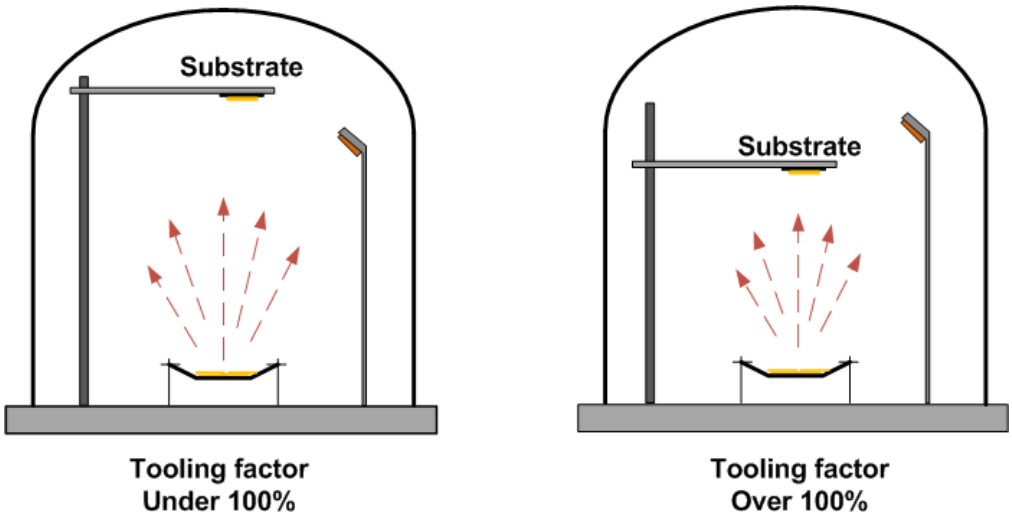


Figure 4.1: Thermal evaporator with the substrate at different distances from crystal sensor.

In order to determine the tooling factor of a material, the substrate and crystal sensor are placed in their normal positions. Approximate tooling is set to an approximate value or, if it is unknown, to 100%. The density of the material is also set and then we deposit 1µm or more of the material, then the thickness is read off the thickness monitor meter. A

profilometer, AFM or Tayler-step machine is then used to measure the actual film thickness of the substrate. This procedure is repeated a number of times, in order to increase the accuracy of the tooling factor.

The tooling factor is calculated using the following expression [84]:

$$Tooling\ Factor_{Actual} = Tooling\ Factor_{Approximate} \times \frac{Thickness_{Actual}}{Thickness_{FTM6\ meter}}$$

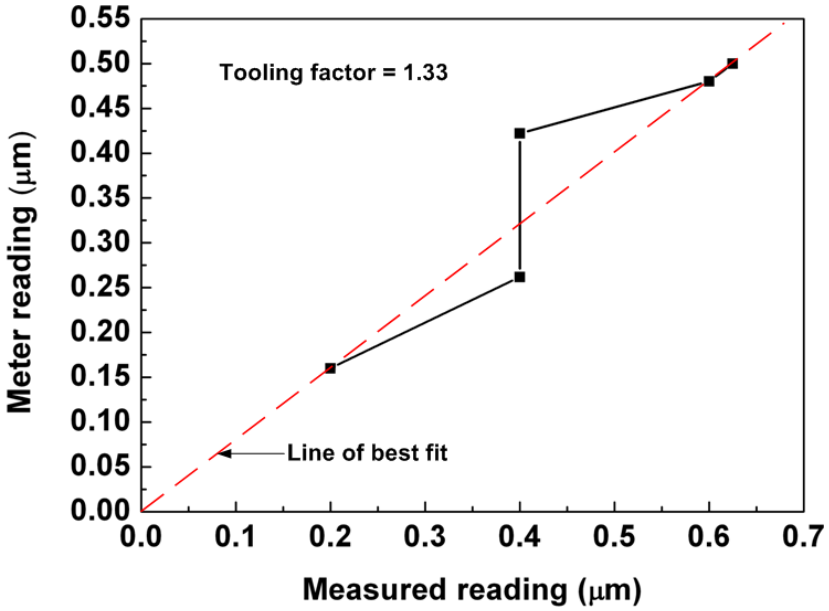


Figure 4.2: Graph showing the tooling factor of the evaporated Ti/Au metals.

This means that the actual measured thickness of the metal is 1.33 times the value indicated by the thickness monitor. In Figure 4.2, the line starts from the zero mark because it is assumed that with a properly calibrated FTM meter, the actual measurement reading and the FTM meter reading should be identical. The metal deposition of both gold and titanium is performed for the same particular purpose.

When reading the FTM6 meter during thermal evaporation, it was noticed that the meter reading stopped short of the targeted 0.8 μm, which was due to the amount of gold (number of strips) being evaporated and the tooling factor being over 100%. The number of gold strips evaporated is directly proportional to metal thickness, in that the less the strips evaporate, the lower the thickness of the metal – and vice versa.

4.1.2 Photoresist and polyimide deposition

In this work, calibration steps were taken for the photoresist and polyimide depositions to ensure that the right amount of resist was deposited onto the wafer for a particular step, such as for polyimide etching and metal lift-off. In order to apply a uniform coat of resist or polyimide onto the wafer, spin speed must be on the level out position, as illustrated in Figure 4.3(b).

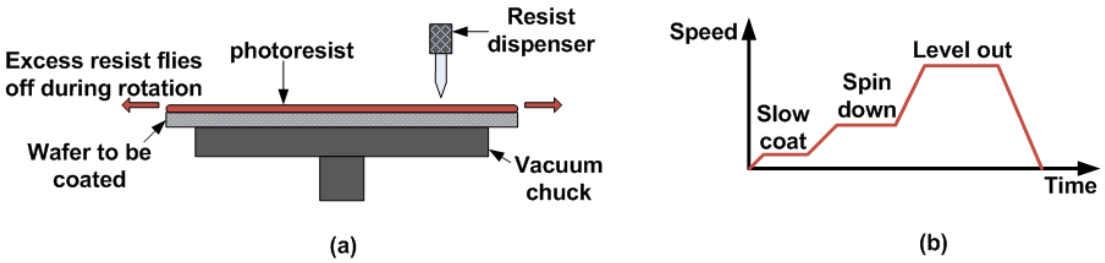


Figure 4.3: Spin coating: (a) sketch of a wafer on vacuum chuck with photoresist being applied; (b) plot of speed against time.

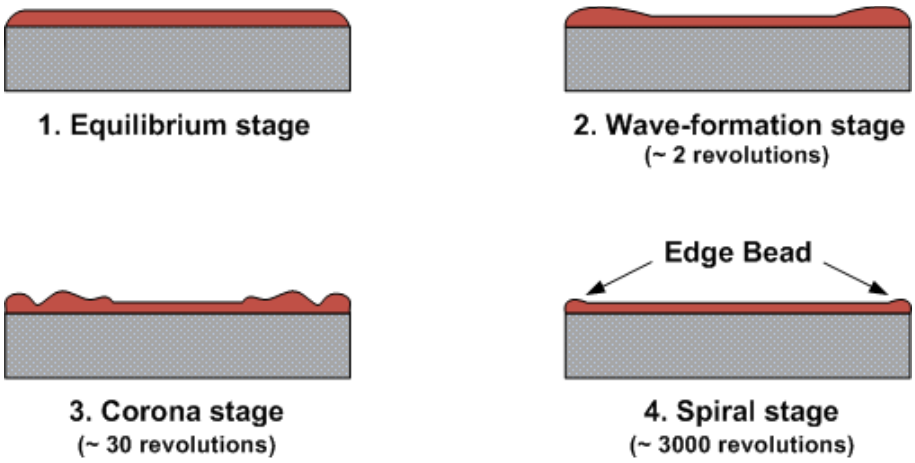


Figure 4.4: Stages of photoresist coating [85].

When the substance reaches the spiral stage during spin coating, the residue of the substance forms an edge bead on the outer regions of the wafer, as illustrated in Figure 4.4. It is therefore important to remove the edge bead by performing a lithography process on the edge bead areas while keeping the middle part of the wafer covered (not exposed to ultraviolent light).

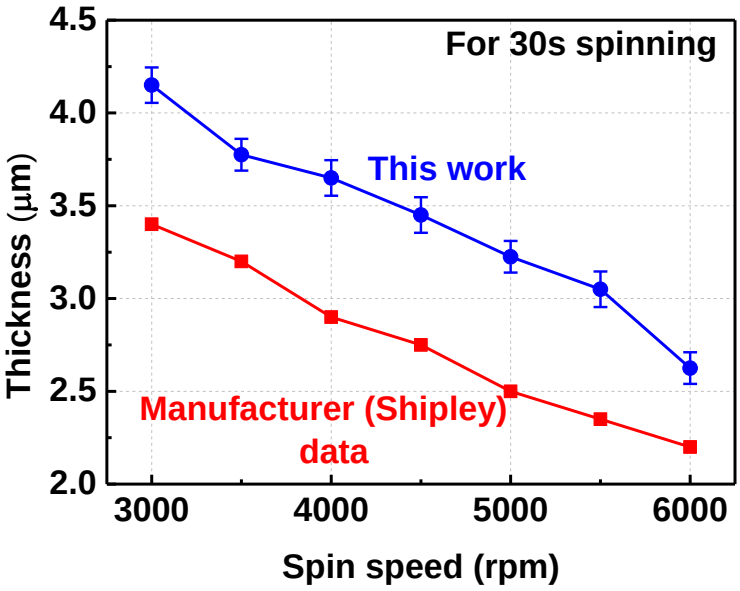


Figure 4.5: The thickness of S1828 photoresist as a function of spinning speed.

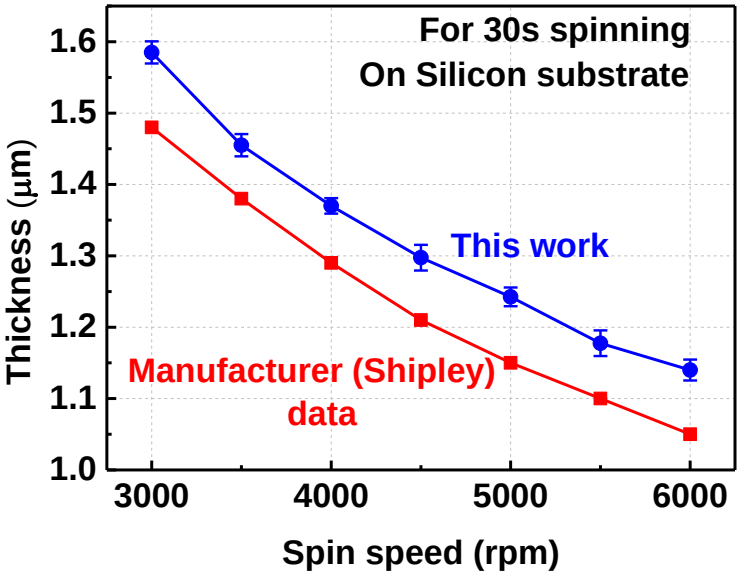


Figure 4.6: The thickness of S1813 photoresist as a function of spinning speed on silicon substrate.

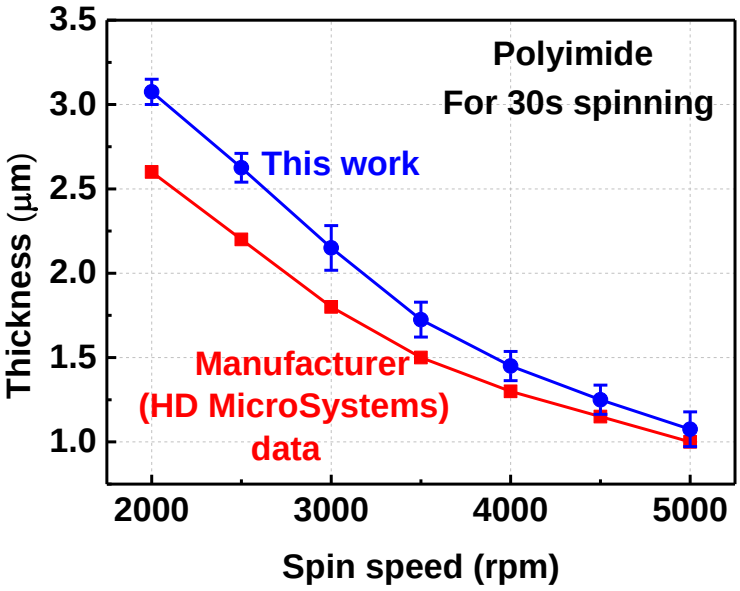


Figure 4.7: The thickness of polyimide as a function of spinning speed on GaAs substrate.

In order to confirm if the manufacturer's data for spin speeds with thickness of the photoresists match with those used for this work, both S1828 and S1813 resists were spun on at different spin speeds to re-plot the manufacturer's data, as illustrated in Figures 4.5 and 4.6. It was observed that both the manufacturer's data and this work's data follow a similar inversely proportional trend. The difference in the data was noticed in the thickness levels of the resist at the same spin speeds. This work's data showed an increase in thickness of about 0.75 µm for the S1828 resist and a 0.1 µm increase for the S1813 resist, because the resist solvent thickens up over time, if stored and then used after a long period compared to that of the manufacturer whose data are produced straight from the production line. The comparison between the manufacturer's data and this work for polyimide thicknesses against different spin speeds is illustrated in Figure 4.7. The reason for the difference in both datasets is the similar to that given for the resist discussion above.

4.1.3 Pre-Bake (Soft-Bake)

Soft baking is a step used to evaporate the coating solvent and to densify the photoresist after spin coating. The photoresist mainly becomes photosensitive or image-able only after soft baking. In this work we carry out some soft bake calibration tests from 60ºC to 100ºC of resist spun at 3000rpm and 5000rpm. A conventional oven was used for the soft-baking process, because it allows the heat to build up slowly, which is essential for avoiding solvent burst effects [85].

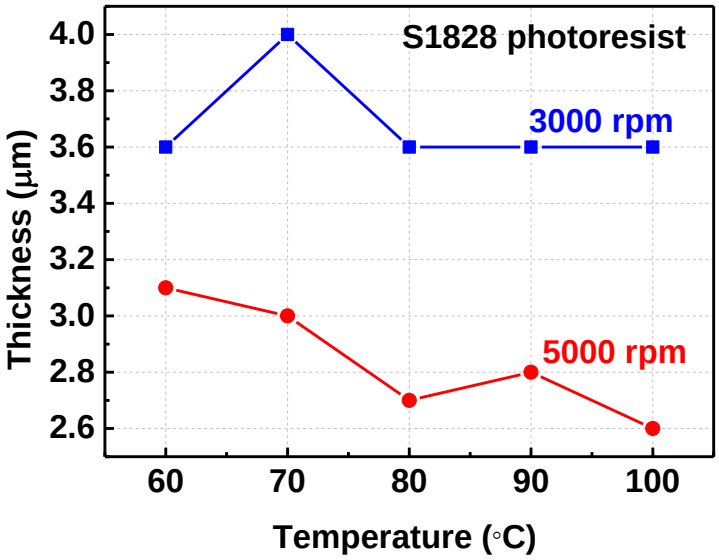


Figure 4.8: S1828 photoresist thickness as a function of temperature for spin speeds 3000rpm and 5000rpm.

The data in Figure 4.8 show the thicknesses of S1828 photoresist against temperature at 3000rpm and 5000rpm spin speeds. Photoresist at both speeds was spun for 30 seconds, and the baking time was set at 20 minutes for each temperature. By comparing the results in Figure 4.5 with those in Figure 4.8, it is evident that the thickness of the resist decreases by about 15% during the soft bake process. It is therefore very important to get the temperature calibration for the soft bake right, because over- baking would degrade the photosensitivity of the resist by reducing the developer solubility and less baking would prevent UV light from reaching the sensitiser, thus increasing the development rate.

4.1.4 Polyimide Curing

Polyimide curing involves removing solvents and other unwanted volatiles from the resin slowly and with the help of heat. This causes the resultant imidisation of the polymer resin into a durable polyimide film [83].

The curing of the polyimide is performed in a number of steps, whereby after spinning the liquid polyimide onto the wafer, it is placed in a 90ºC conventional oven for 90 seconds and then moved to another conventional oven at 110ºC for a soft cure of 30 minutes. After soft curing, the wafer is placed in the middle of a three chamber vacuum oven for a post cure. The vacuum oven is turned on and set to 200ºC and then held at that temperature for 2 hours. The oven is then turned off and the wafer is allowed to cool to room temperature in the oven. It can be left in the oven to cool overnight, if need be. A sketch of the full post curing process of the polyimide film is illustrated in Figure 4.9.

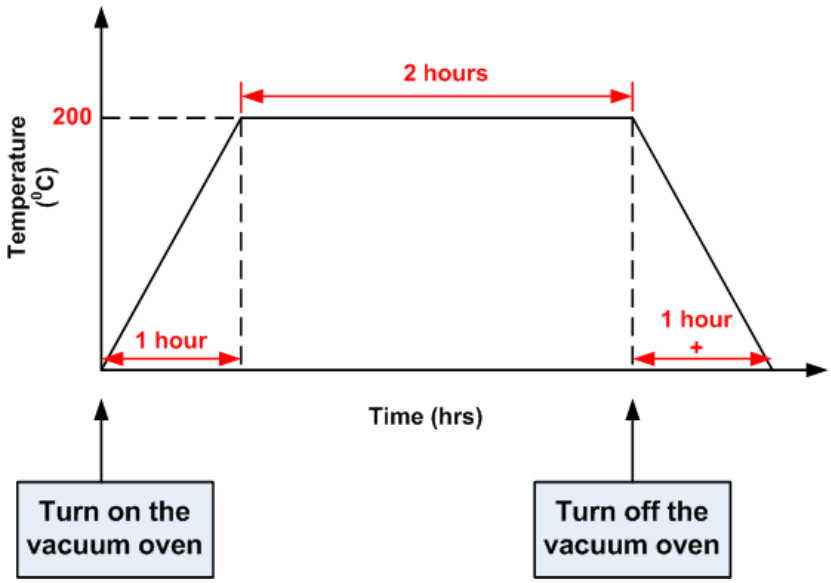


Figure 4.9: Sketch of a plot of temperature against time for the post curing process.

The rate of temperature rise in the vacuum oven is verified by recording the temperature of the oven at certain time intervals and then by repeating this process five times for accuracy, as tabulated in Table 4.1 and average plotted in Figure 4.10.

Table 4.1: Vacuum oven temperature rise.

	Temperature (ºC)					
Time (minutes)	**Run: 1**	**Run: 2**	**Run: 3**	**Run: 4**	**Run: 5**	**Average**
15	50	49	50	51	51	**50**
30	100	98	100	101	101	**100**
45	145	142	143	145	144	**144**
60	180	178	178	180	179	**179**
75	195	194	196	195	194	**195**
90	197	197	197	198	198	**197**
105	198	198	198	198.5	198	**198**
120	198	198	198	199	199	**198**
135	198	198	198	199	199	**198**
150	198	198	198	199	199	**198**

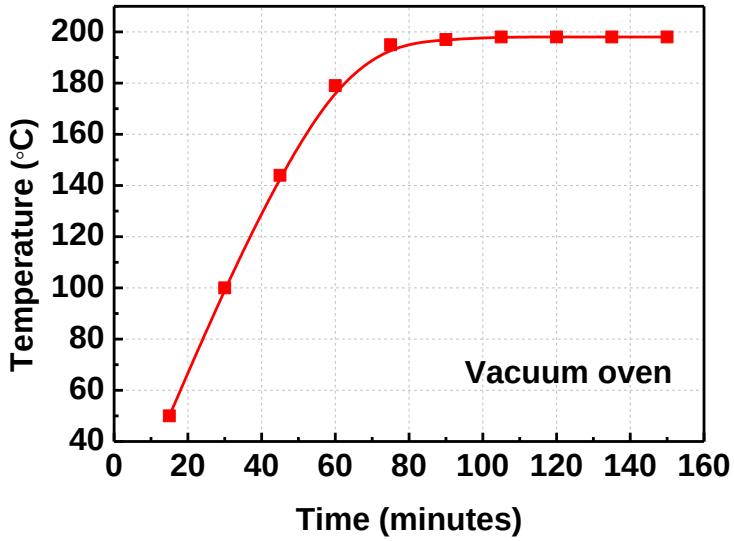


Figure 4.10: Temperature rise rate of the vacuum oven.

The slope of the linear part of the plot helps us calculate the rate of temperature rise.

$$\text{Slope} = \frac{\Delta Temperature}{\Delta Time} = \frac{144-50}{45-15} = \frac{94}{30} = 3.13\ ^{o}\text{C/min}$$

Therefore, the rate of temperature rise of the vacuum oven was found to be 3.13 ºC/min.

4.2 Mask Set Description and History

A photolithographic mask contains many features, each of which can be repeated in what is called a ‘unit cell’. For multilayer MMIC designs, each metal layer or dielectric layer needs its own mask, and each mask is aligned to other masks with the help of alignment marks. In this work, two mask sets, which were designed by previous researchers in the group, were fabricated and analysed. These mask sets are named ‘mask Ver.2’ and ‘mask Ver.5’. Mask Ver.2 comprised mainly passive components and mask Ver.5 comprised both passive and active components.

4.2.1 Description of Mask set Ver.2

Mask set Ver.2 shown in Figure 4.11 is a five-layer mask set which was designed with the aim of studying the effect of the geometric parameters of various passive components such as different multilayer CPW transmission lines, EM properties of planar and multilayer CPW inductors, capacitances of multilayer capacitors with various geometries and CPW couplers [86]. Metal interconnects, de-embedding kits and a power divider are other components found in the mask set. The mask layers of the designed components are tabulated in Table 4.2. In this work, mask set Ver.2 is also used as an initial stepping stone to develop and improve a multilayer fabrication procedure for the more advanced mask set Ver.5, which has both passive and active components.

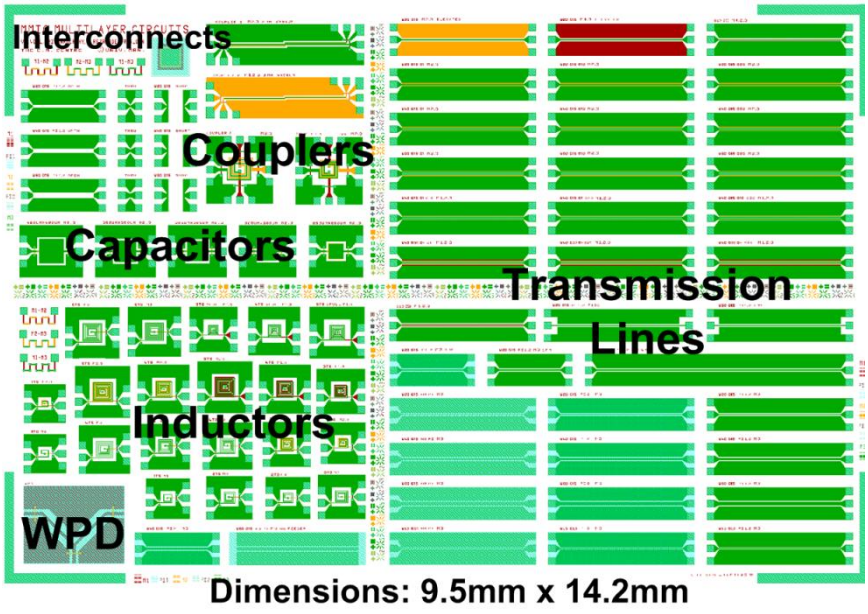


Figure 4.11: Layout of a cell in mask set Ver.2 with passive components.

Table 4.2: Various component structures designed in Mask set Ver.2.

			Masks				
			M1	**PI1**	**M2**	**PI2**	**M3**
Transmission Lines	Elevated	M2, M3		●	●	●	●
		M1, M3	●	●		●	●
	Two layer overlapping				●	●	●
	V-shaped			●	●	●	●
	Planar	No PI					●
		PI 2				●	●
		PI 3		●		●	●
Capacitors				●	●	●	●
Couplers	Single overlap			●	●	●	●
	Double overlap		●	●	●	●	●
Inductors	Planar						●
	Offset	M1, M3	●	●		●	●
		M2, M3		●	●	●	●
	Directly overlayed		●	●		●	●
Processing Validation Module (PVM)			●	●	●	●	●
Interconnects	M1 – M2		●		●		
	M2 – M3				●		●
	M1 – M3		●				●

4.2.2 Description of Mask set Ver.5

Mask set Ver.5, shown in Figure 4.12, is a seven-layer mask set which was designed with the aim of demonstrating the integration of compact multilayer CPW passive components with high-performance transistors such as pHEMTs. One cell of the mask consists of multilayer CPW transmission lines, CPW inductors and capacitors, de-embedding kits, amplifiers, switches, limiters, phase shifters, digitally tuneable capacitors/filters, diodes and pHEMT test structures. The mask layers of these designed components are listed in Table 4.3.

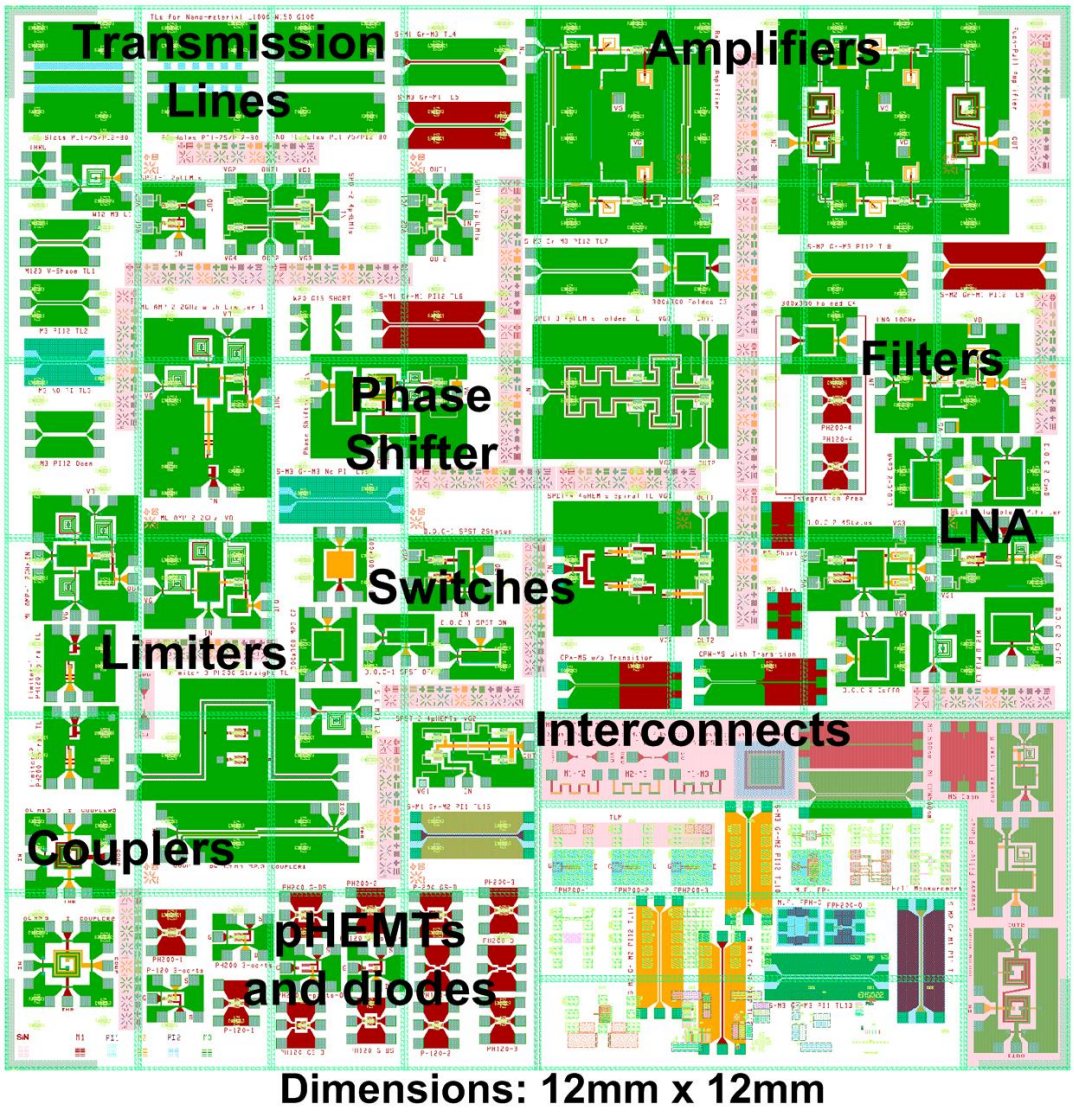


Figure 4.12: Layout of a cell in mask set Ver.5 with both active and passive components.

Table 4.3: Various component structures designed in Mask set Ver.5.

			Masks						
			Si_3N_4	**R**	**M1**	**PI1**	**M2**	**PI2**	**M3**
Transmission Lines	Elevated	M2, M3				●	●	●	●
		M1, M3			●	●		●	●
	CPW – TFMS transition				●	●		●	●
	V-shaped					●	●	●	●
	Planar	No PI							●
		PI 2						●	●
		PI 3				●		●	●
Capacitors						●	●	●	●
Couplers	Single overlap					●	●	●	●
	Double overlap				●	●	●	●	●
Inductors	Planar								●
	Offset	M1, M3			●	●		●	●
		M2, M3				●	●	●	●
	Directly overlayed				●	●		●	●
Processing Validation Module (PVM)					●	●	●	●	●
Interconnects	M1 – M2				●		●		

	M2 – M3					●		●
	M1 – M3			●				●
pHEMT test structures		●		●	●	●	●	●
Amplifiers		●	●	●	●	●	●	●
Switches		●	●	●	●	●	●	●
Limiters		●		●	●	●	●	●
Phase Shifters		●	●	●	●	●	●	●
Digital tuneable capacitors/filters		●	●	●	●	●	●	●

4.2.3 Interconnect Resistances

In order to determine whether there is a connection between the intermediate metals in a fabricated structure, interconnect test modules between M1 and M2, M1 and M3 and between M2 and M3 are used. Interconnect resistances between the metal layers are measured with the aim of obtaining very low resistance values, as this ensures good conductivity between the metal layers.

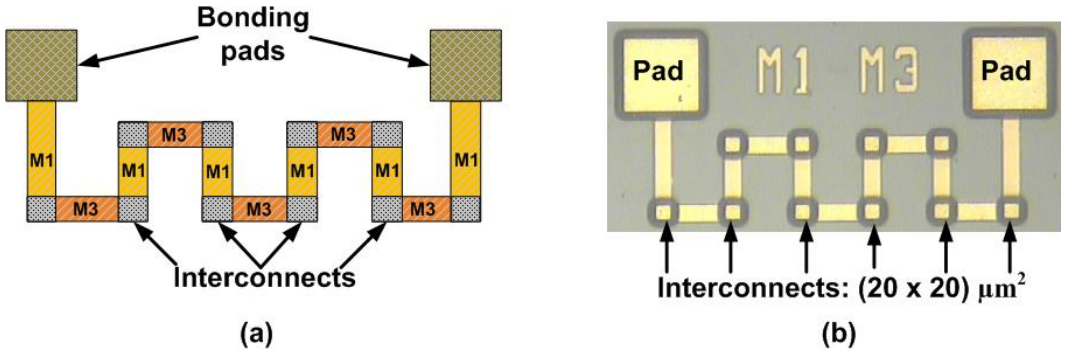


Figure 4.13: Top view of the M1-M2 interconnect (a) sketch, (b) micrograph of the fabricated sample.

Figure 4.14 shows a sketch of an interconnect test module between metal layer 1 and metal layer 3. Each test sample has ten interconnects on it, and therefore the total resistance measured is divided by ten to get the resistance value of each interconnect.

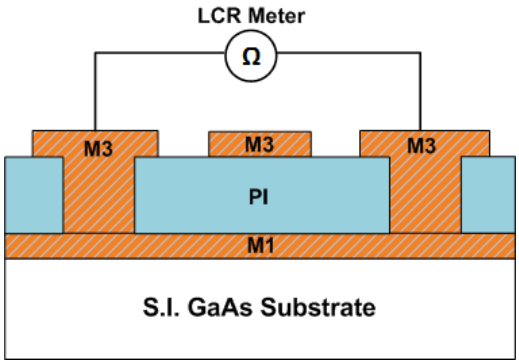


Figure 4.14: Sketch of an M1 – M3 interconnect test.

4.2.4 Thin film GaAs Resistors

The GaAs resistor relies on the linearity of the semiconductor's current-field characteristic at low electric field values. Hence, it is important to consider how much current will be passed through a resistor when modelling one. In this work, 80:20 NiCr alloy is used to produce the thin film resistors, because its temperature coefficient is low compared to that of other types of alloys [55]. Gold/titanium alloy is used as the contact pad metal, and the resistivity of the NiCr thin film of 30nm thickness is derived to be $(1.53 \times 10^{-6})\Omega$m.

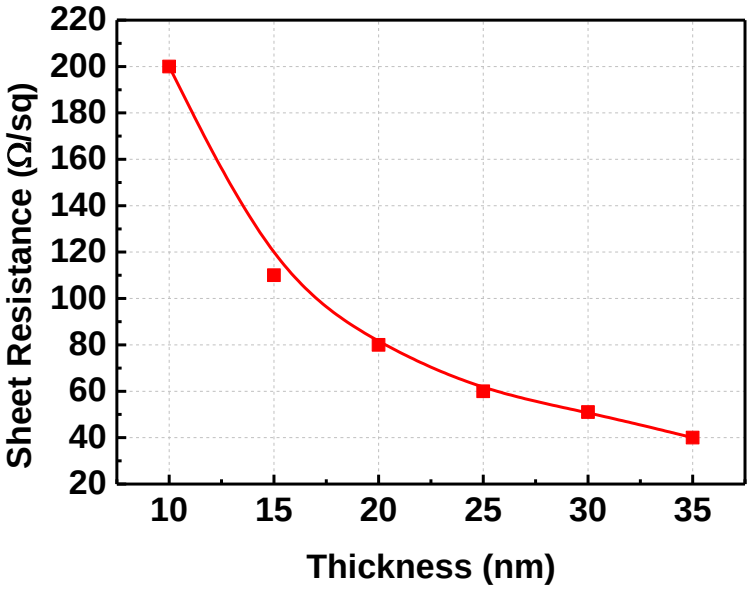


Figure 4.15: Measured sheet resistance against NiCr film thickness.

Sheet resistance is the ratio of resistivity of the NiCr film to the thickness of the NiCr film. It is therefore independent of the size of the square and is given by:

$$R_{sh} = \frac{\rho_{NiCr}}{t}$$

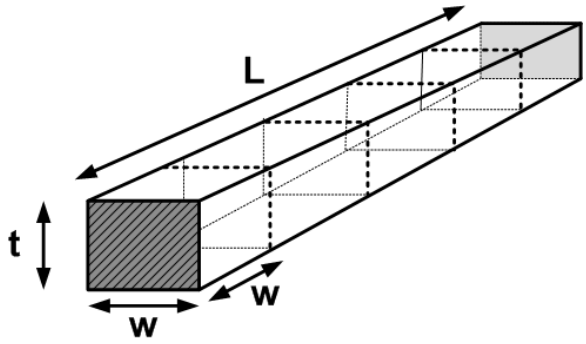


Figure 4.16: 3D cross-sectional sketch of an integrated resistor.

Resistance = Sheet resistance x number of squares $= \left(\frac{\rho}{t}\right) \times \left(\frac{L}{w}\right)$

where ρ is the bulk resistivity, L is the length of the resistive film, w is the width of the resistive film and t is the thickness of the resistive film.

The sizes of the resistors were 1 and 5 squares, and the resistive film had a thickness of 30nm. A multimeter was used to measure the resistance of the resistors. The Ni-Cr resistors were deposited on GaAs substrates and measured at room temperature. The micrographs of the fabricated thin film resistors are shown in Figure 4.17.

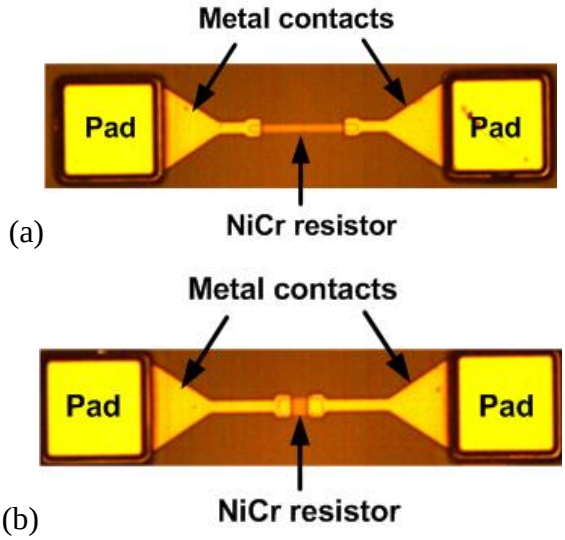


Figure 4.17: Micrographs of thin film resistors: (a) 500 Ω, (b) 50 Ω.

The theoretical value for a thin-film resistor with a width of 10µm and a length of 100 µm can be calculated as:

$$R = \left(\frac{1.5 \times 10^{-6}}{30 \times 10^{-9}}\right) \times \left(\frac{100 \times 10^{-6}}{10 \times 10^{-6}}\right) = 500\Omega$$

The resistivity, ρ of the NiCr metal is 1.5×10^{-6} [87].

4.2.5 Processing Validation Module (PVM)

The process validation module is a test structure designed on each mask set with the aim of verifying the thickness of the metal and polyimide layers after fabricating a sample. A sketch and the fabricated PVM are shown in Figures 4.18 and 4.19, respectively.

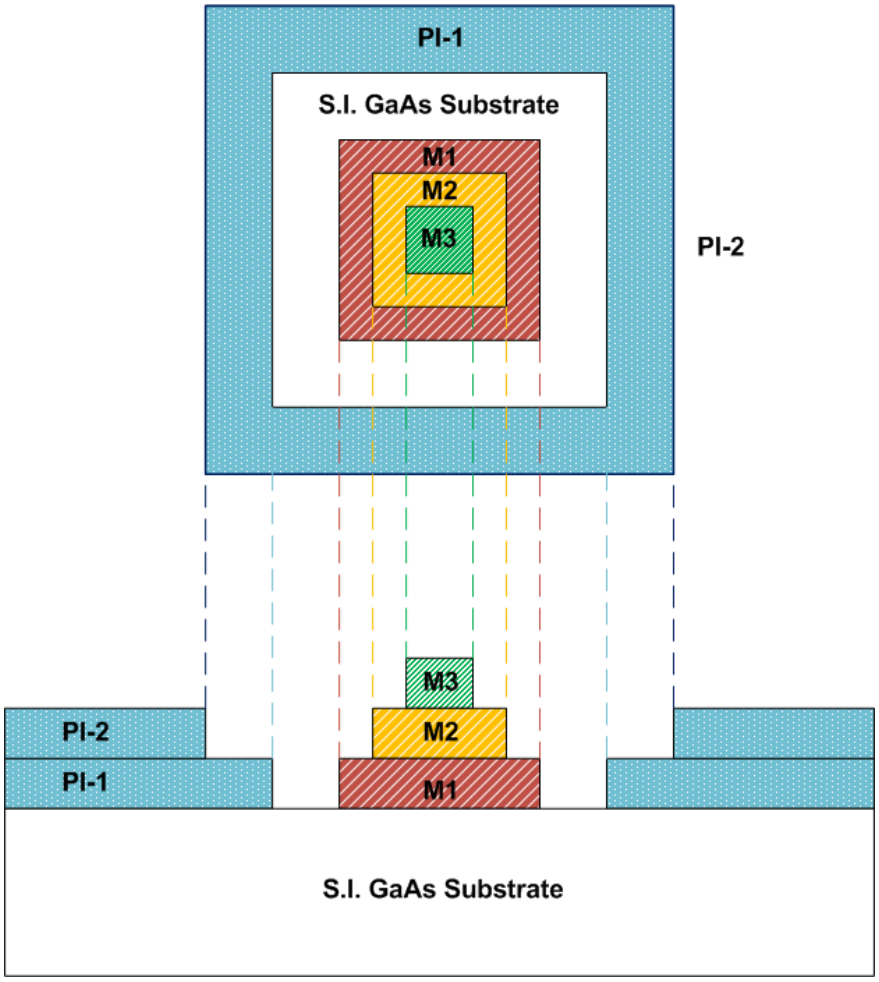


Figure 4.18: Sketch of the Processing Validation Module (PVM).

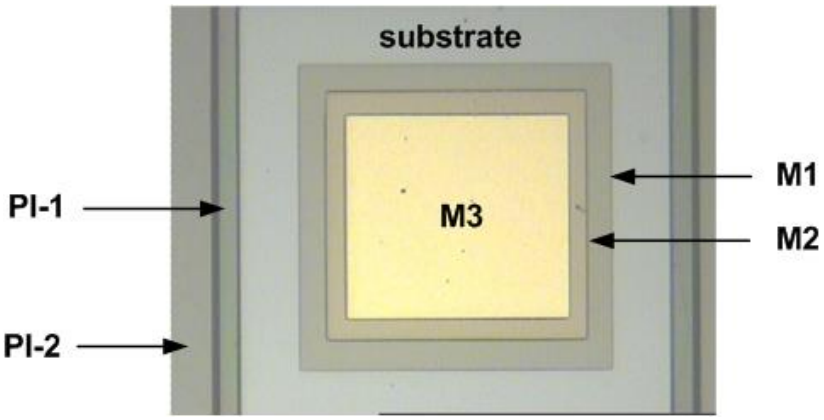
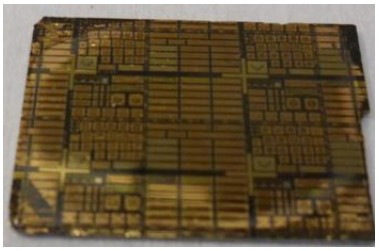


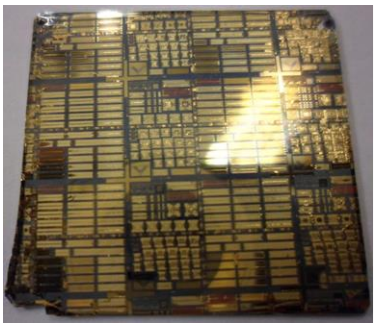
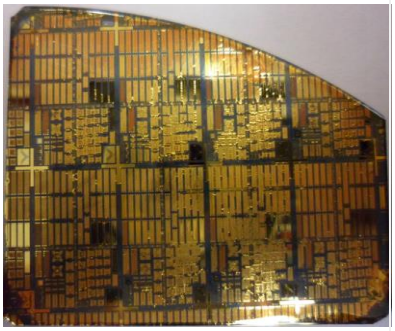
Figure 4.19: Micrograph of the fabricated Processing Validation Module (PVM) area.

4.2.6 Fabrication History for Mask set Ver.2

Three GaAs substrate samples were fully fabricated using the passive components mask Ver.2, as shown in Table 4.4. Although MMIC technology promises high repeatability for individual foundries, it is difficult to fabricate samples with good reproducibility using the same mask set in the university's clean room due to lab facility limitations, manual operation and even the dielectric material's properties. However, the fabricated samples provided another way to study the fabrication effect and the tolerance of the fabrication technology on the components' performances.

Table 4.4: History of fabricated multilayer samples using Mask set ver.2.

Sample No.	Sample Size (cm^2)	Metal Thickness (Ti/Au) (μm)	Interconnect Resistance (Ω)
1	2.5 x 2 	0.4	High (Due to poor polyimide etching)

2	2.5 x 3 	0.4	0.4 -1 (Relatively low resistances)
3	4.2 x 3 	0.6-0.7	0.3 – 0.5 (Very low resistances)

The measurement results obtained from the PVM for sample 2 are listed in Table 4.5. The interconnect resistances presented in Table 4.6 are measured from three samples of mask Ver.2, and from each sample a certain number of functional cells have two test modules (A and B).

Table 4.5: Measured polyimide and thin metal thicknesses measurement on PVM for sample 2 of Mask set of Mask set Ver.2.

Cell	PI - 1(µm)	PI - 2(µm)	M1 (µm)	M2 (µm)	M3 (µm)
2	1.4	3.6	0.4	0.4	0.4
3	1.4	3.6	0.4	0.4	0.36
4	1.6	3.4	0.4	0.4	0.4
5	1.6	3.4	0.4	0.3	0.4
Average	**1.5** ± 0.12	**3.5** ± 0.12	**0.4** ± 0	**0.38** ± 0.05	**0.39** ± 0.02

Table 4.6: Measured interconnect metal resistances on test sample 2 of Mask set Ver.2.

Sample	Cell	M1 – M2 (Ω)		M2 – M3 (Ω)		M1 – M3 (Ω)	
		A	B	A	B	A	B
2	1	-	-	-	-	-	-
	2	13M	4.7	6.4	9.2	5.4	5.9
	3	5.6	5.3	10.4	13.7M	5.8	6.3
	4	5.3	4.5	6.4	9.9	6.1	7
	5	4.9	4.5	16.1	62	4.3	6.6
	6	-	-	-	-	-	-
	7	-	-	-	-	-	-
	8	-	4.7	-	6.6	-	5.9
	9	-	12.4M	-	-	-	-

4.2.7 Fabrication History for Mask set Ver.5

After a number of trials fabricating mask set Ver.2 and improving the multilayer fabrication procedure, a decision was made to move on to the fabrication of mask set Ver.5. Initially, this posed a lot of challenges, which led to the fabrication of four samples using this mask set. The first two samples, 1 and 2, had a lift-off problem of the top conductor metal (metal 3), but these were used to study and rectify the problem. Sample 3 was fabricated with half of the target metal thicknesses (Au = 0.4 μm), in order to limit material wastage in case something went wrong in the middle of the process. With sample 3 successfully fabricated with half of the target metal thicknesses, skills and confidence allowed us to fabricate another sample, albeit this time with the target metal thicknesses (Au = 0.8 μm). Sample 4, shown in Figure 4.20 with 12 cells, was therefore successfully fabricated and later tested. Its validation results are listed in Tables 4.7 and 4.8.

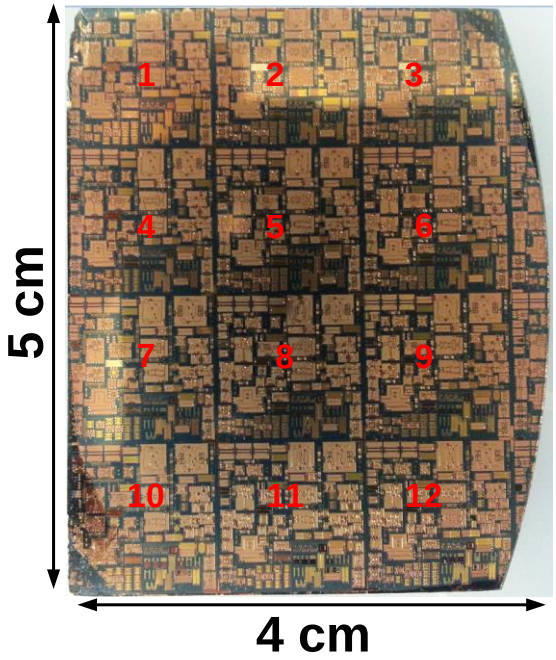


Figure 4.20: Micrograph of fabricated wafer sample no. 4 containing twelve cells.

Table 4.7: Measured interconnect metal resistances and resistors for sample no. 4 of Mask set Ver.5.

Cell No.	M1 – M2 (Ω)	M2 – M3 (Ω)	M1 – M3 (Ω)	W20, 50 Ω	W10, 500 Ω
1	2.2	2.4	2.6	53.5	190
2	2.2	2.4	2.5	54.5	180.5
3	2.3	2.4	2.9	54.7	185
4	2.4	2.2	2.4	52	144.8
5	2.4	2.2	2.4	51.3	174
6	2.4	2.3	2.3	52	180
7	2.1	2.7	2.4	52.6	-
8	2.1	2.1	2.2	52	193
9	2.1	2.3	2.4	48.5	193
10	-	-	2.4	38.4	74
11	-	-	2.2	57.7	247.2
12	2.2	2.4	2.6	53.1	225.1
Average	**2.2** ± 0.13	**2.3** ± 0.16	**2.4** ± 0.19	**51.7** ± 4.73	**180.6** ± 44.18

Table 4.8: Thickness measurement results for sample 4 of Mask set Ver.5.

Cell	**M1** (µm)	**M2** (µm)	**M3** (µm)	**PI – 1** (µm)	**PI – 2** (µm)
1	0.8	-	0.8	1.2	3.8
2	0.6	0.8	0.9	1.3	3.6
3	0.6	0.8	0.7	1.2	3.5
4	0.6	0.7	0.8	1.3	3.6
5	0.8	0.7	0.6	1.2	3.7
6	0.8	0.7	0.9	1.6	3.8
7	0.7	0.7	0.8	1.5	3.5
8	0.7	0.7	0.8	1.4	3.6
9	0.8	0.7	0.8	0.7	3.7
10	0.7	0.6	0.8	1.3	3.9
11	0.8	0.7	0.9	1.2	3.8
12	0.8	0.7	0.7	1.3	3.8
Average	**0.73** ± 0.09	**0.71** ± 0.05	**0.79** ± 0.09	**1.3** ± 0.22	**3.7** ± 0.13

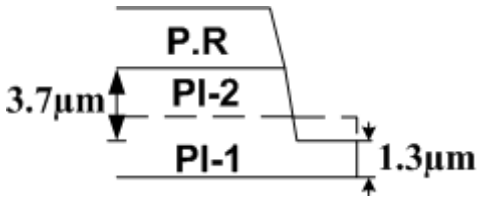


Figure 4.21: Measured profile of polyimide following dry etching in the PVM area.

After polyimide etching, the PVM layer test sample was measured using a Tayler step. It was evident that the thickness of the first polyimide layer (PI-1) was 1.3 µm and that of the second polyimide layer (PI-2) was 3.7 µm – as opposed to the expected value of 2.5 µm for each of the polyimide layers. This was then investigated and found to be due to the etching of polyimide. When the second polyimide layer (PI-2) is etched, part of the first polyimide layer is also etched off (as shown in Figure 4.21) when the photoresist on top of the second polyimide layer is etched. Hence, this makes the thickness of PI-1 smaller than that of PI-2.

Chapter 5 Microwave Characterisation of 3D MMIC Components

5.1 CPW to Thin-Film Microstrip (TFMS) Transition

The need for the transition from CPW probe pads to the microstrip line is mainly due to the demand for integrating of various circuit structures on one semiconductor wafer, in order to achieve the highest possible integration while maintaining each circuit's effective performance [17]. There are two main coupling techniques for transitioning vertically between two transmission lines, either through electromagnetic coupling or physical contact. This work presents design guidelines for the development of compact, wideband multilayer coplanar waveguide to thin-film microstrip (TFMS) transitions using an experimental 3D multilayer MMIC technology developed on GaAs substrate. This work employs an electromagnetic coupling technique.

5.1.1 Choosing CPW-to-TFMS Transition Transmission Line Design Parameters

This sub-chapter discusses why different parameters were chosen for the transition transmission line design, which consists of three main regions, namely the CPW region, transition region and thin-film microstrip (TFMS) region as shown in Figure 5.1. In this subchapter, these regions are analysed, and discussions are undertaken on why a tapered design was used for the transition and why a footprint on the CPW region was considered as a design aspect.

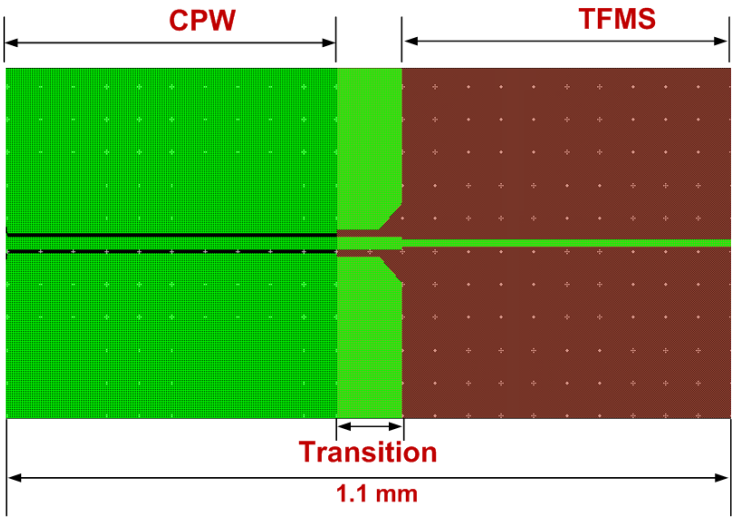


Figure 5.1: Top view layout of the CPW-to-TFMS transition transmission line without probing pads.

5.1.2 Coplanar Waveguides

A coplanar waveguide (CPW) is used in the analysis of the transition, because it accounts for most of the right hand side of the transition design structure as shown in Figure 5.1. In this work, we aim to employ multilayer technology to design a compact CPW line that has characteristic impedance (Z_0) of 50Ω. Therefore, this in consideration, two types of CPW lines were designed and discussed, one with a footprint (metal 2 under metal 3), as shown in Figure 5.2(b), and one with no footprint, as shown in Figure 5.2(a).

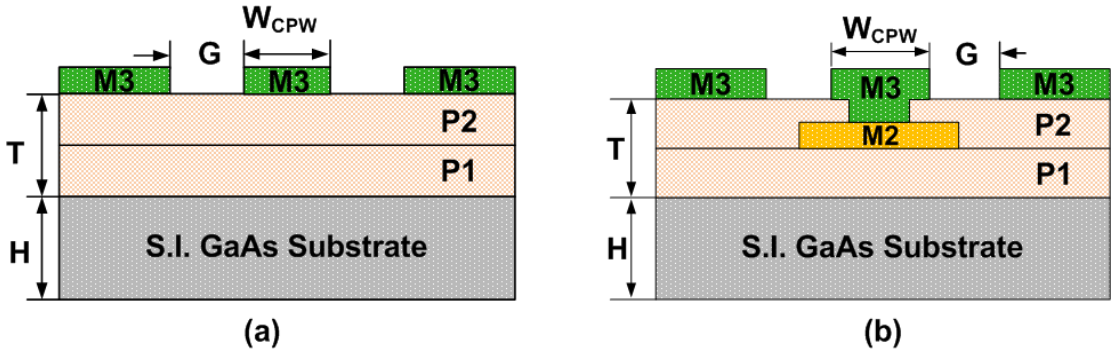


Figure 5.2: Cross-sectional view of the multilayer Coplanar Waveguide (CPW) transmission lines with (a) no footprint and (b) a footprint.

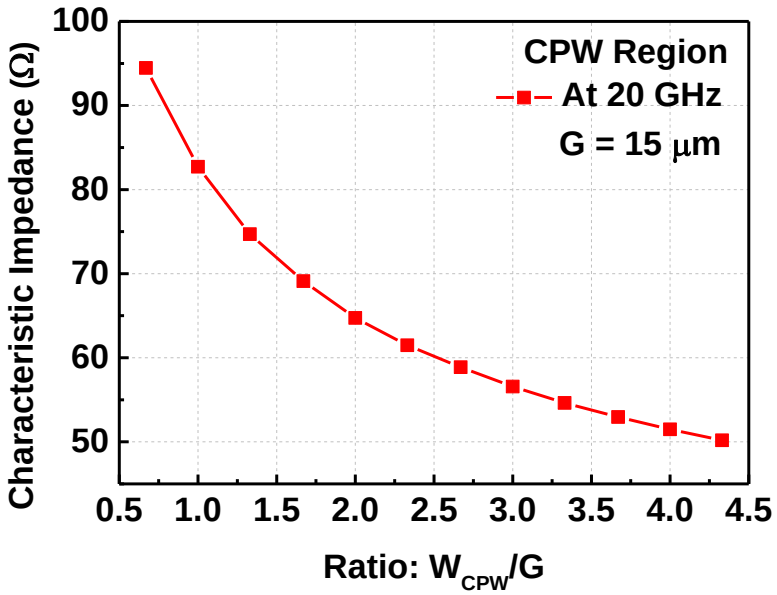


Figure 5.3: Simulated impedances of CPW lines with different width and gap parameters.

Simulated CPW line impedances with different signal width and gap parameters are compared in Figure 5.3. With a signal line width to gap width ratio (W_{CPW}/G) higher than unity, a characteristic impedance of lower than 80Ω can be obtained, and with a ratio less

than unity, one can obtain impedances higher than 80Ω. Since the planar CPW line employs multilayer technology, the impedance of the line will be much higher than 50Ω due to the line becoming less capacitive. Therefore, in order to lower the characteristic impedance of the line, the signal width is made wider, hence a ratio of about 4 to achieve 50Ω.

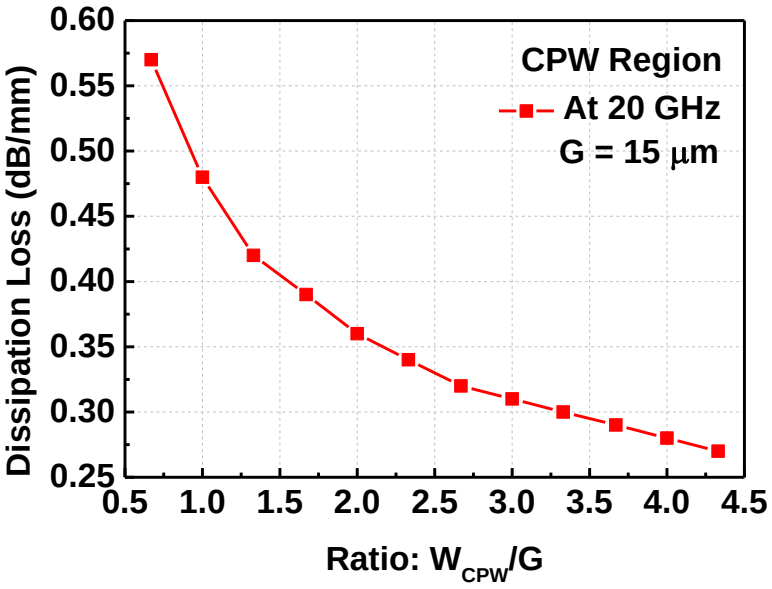


Figure 5.4: Simulated dissipation losses of CPW lines with different width and gap parameters.

Simulated CPW line dissipation losses with different width and gap parameters are compared in Figure 5.4. It is observed that dissipation loss stays relatively low (below 1 dB/mm) for the ratios (W_{CPW}/G) from 0.5 to 4.5 of the transmission lines. This means that minimal losses are dissipated through the signal line. Since a more compact multilayer design is desired while maintaining a 50Ω impedance match, the CPW line is designed with a footprint (metal 2) under the signal line (metal 3), the analysis for which is given in the following subsection.

5.1.3 CPW Transmission Line with a Footprint (Metal 2)

The CPW design structure discussed in this subchapter is modelled with a footprint (metal 2) under the signal line (metal 3), as shown in Figure 5.5. This compact multilayer CPW transmission line structure is modelled to have characteristic 50Ω impedance, as shown in the analysis that follows.

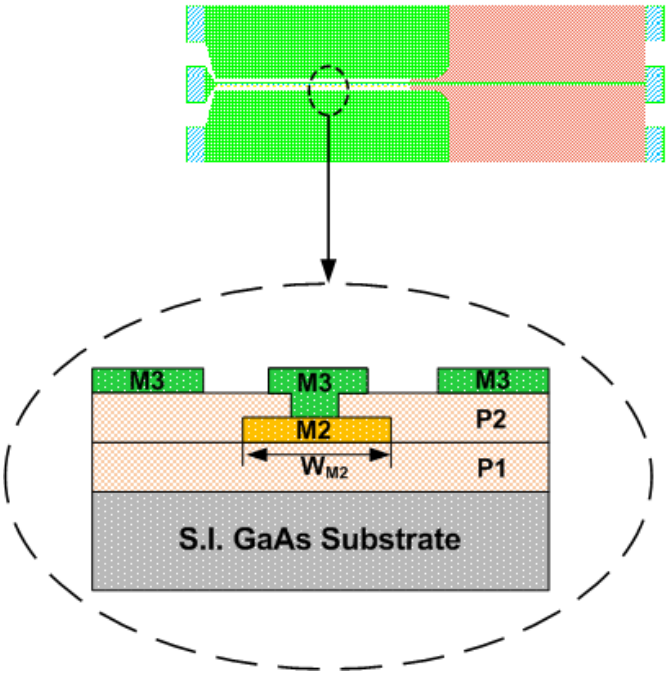


Figure 5.5: Cross-sectional view of the CPW of the transition elaborating the width of Metal 2.

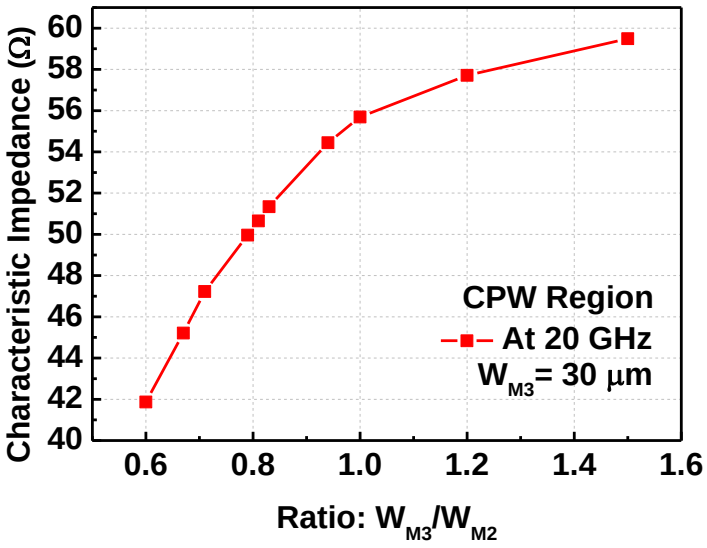


Figure 5.6: Simulated impedances of CPW lines with different values of metal 2 widths.

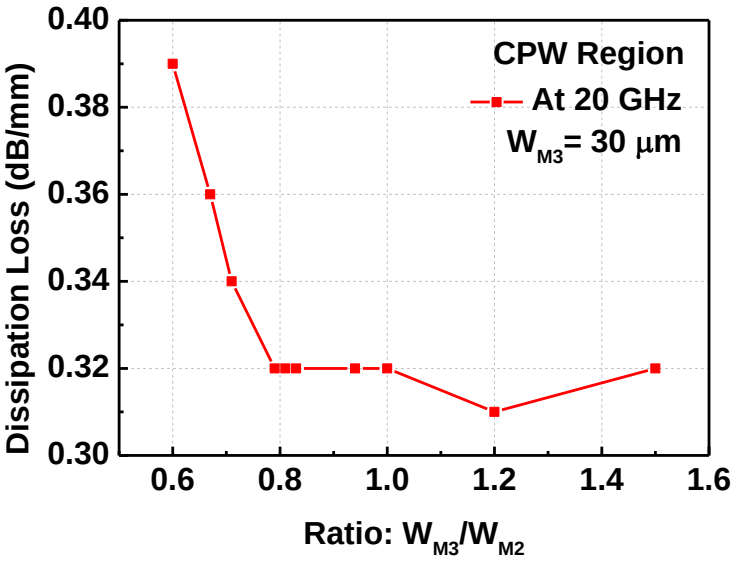


Figure 5.7: Simulated dissipation losses of the CPW line with different ratios of metal 3 to metal 2 widths.

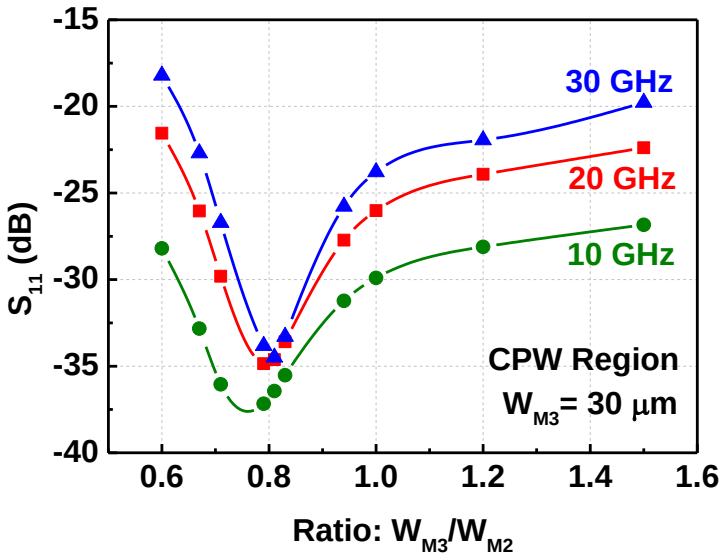


Figure 5.8: Simulated S_{11} parameters versus ratios of metal 3 to metal 2 widths for different frequencies.

Simulated CPW line impedances with different metal 3 to metal 2 width ratios at 20 GHz are compared in Figure 5.6. During the simulations, the metal 3 width was left constant at 30µm. Since the planar CPW line employs multilayer technology, the impedance of the line will be much higher than 50Ω due to the line becoming less capacitive. Therefore, in order to lower the characteristic impedance of the line, a footprint (metal 2) is added under the signal line (metal 3). Hence, this lowers the impedance of the transmission line, and at

a ratio (W_{M3}/ W_{M2}) of about 0.8, 50Ω characteristic impedance is achieved. Furthermore, losses in this design structure are analysed in Figures 5.7 and 5.8.

The simulated dissipation losses of the CPW line with different ratios of metal 3 to metal 2 widths are shown in Figure 5.7. It is observed that the dissipation losses stay relatively low (below 0.4) for all ratios between 0.6 and 1.6. It also noticed that at a ratio of about 0.8, the losses remain constant, therefore implying that at this ratio CPW line losses are minimal, which is also verified in the S_{11} parameters plot in Figure 5.8.

Figure 5.8 shows the simulated return loss for different ratios of metal 3 to metal 2 widths at 10, 20 and 30 GHz. Lower reflections are obtained with a ratio of about 0.8 for all the three frequencies shown. At this ratio, the metal 2 width slightly overlaps the metal 3 width by about 8 µm. Hence, the CPW line with a footprint (metal 2) offers better losses (reduced current crowding effect) compared to the one with no footprint.

5.1.4 Thin-Film Microstrip Line

The thin-film microstrip (TFMS) transmission line in this study has a 5 µm polyimide dielectric between the signal line (metal 3) and the ground plane (metal 1), as shown in the 3D cross-section in Figure 5.9. A number of alterations on the line are made and analysed in a bid to match the transmission line to an impedance of 50Ω, as shown in Figures 5.10 and 5.11.

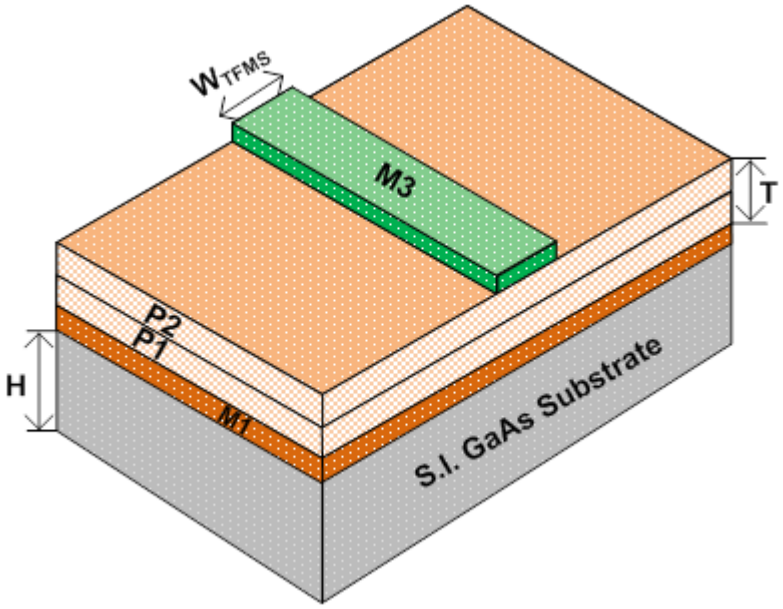


Figure 5.9: 3D cross-sectional view of a thin-film microstrip line.

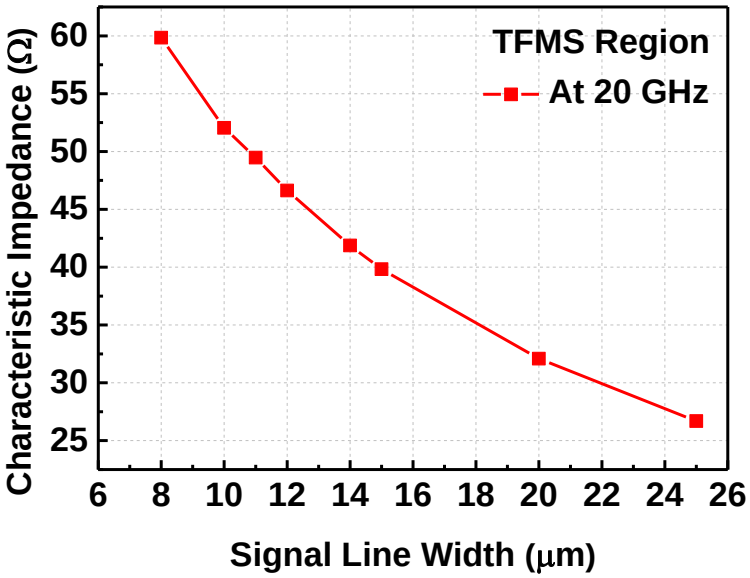


Figure 5.10: Simulated characteristic impedances of thin-film micostrip lines with different signal width parameters.

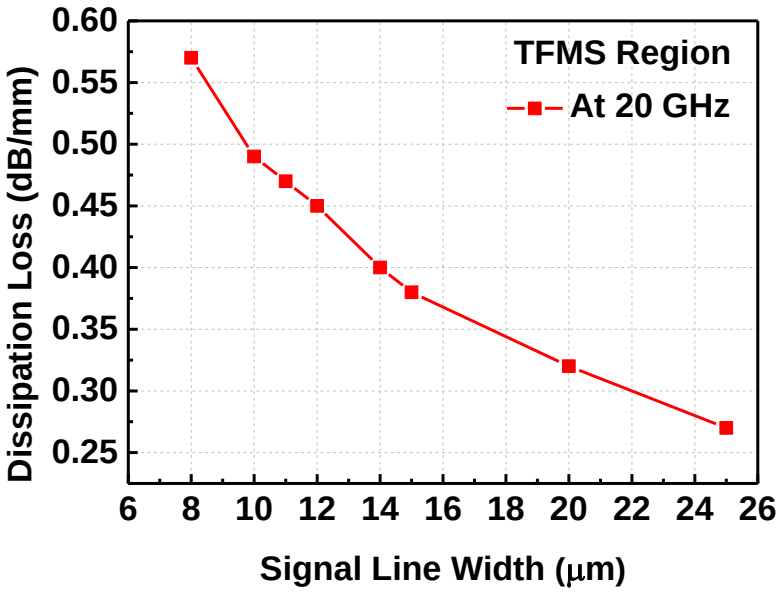


Figure 5.11: Simulated dissipation losses of thin-film micostrip lines with different signal width parameters.

Figure 5.10 compares the characteristic impedances of thin-film microstrip lines with different signal line widths at 20 GHz. In order to obtain an impedance of around 50Ω, the signal line width is reduced, which in turn causes the line to be less capacitive. Therefore, from Figure 5.10, 50Ω is achieved with a signal width of about 11 μm. Great care must also be taken not to reduce the width extensively, because this would bring about the current-crowding effect – losses are investigated at this value in Figure 5.11.

The simulated dissipation losses of the thin-film microstrip line with different signal line widths at 20 GHz are shown in Figure 5.11. As the signal line width becomes narrower, less current is dissipated through the line, therefore making the line more lossy due to the current-crowding effect. For the preferred signal width of 11 µm, which offers an impedance of 50Ω, dissipation loss remains well below 0.6 dB/mm. This signal width is verified by the S_{11} parameters plot in Figure 5.12.

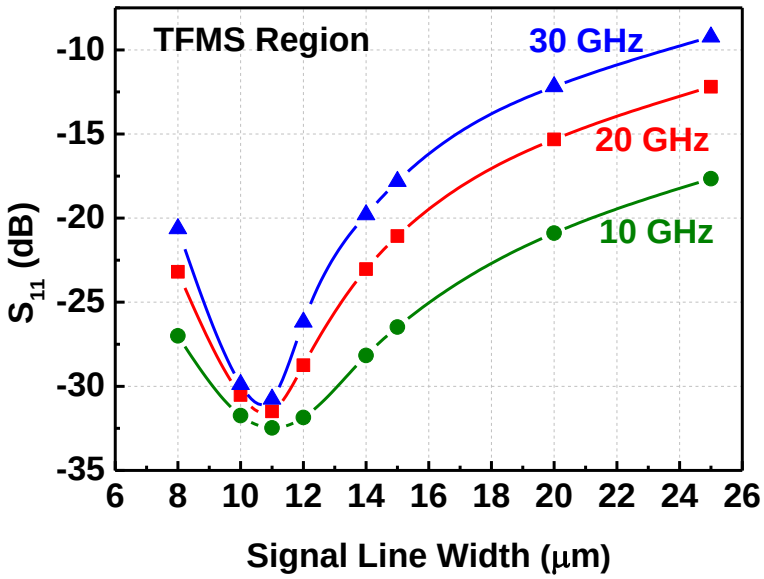


Figure 5.12: Simulated S_{11} parameters of thin-film microstrip lines with different signal width parameters.

A comparison of return loss for the thin-film microstrip lines with different signal line widths at 10, 20 and 30 GHz is shown in Figure 5.12. Lower reflections of better than 30dB are obtained when the signal line width is about 11 µm for all three frequencies as observed in Figure 5.12. Since we maintain a better return loss than 30dB at 11 µm signal width thickness, this verifies the value as the preferred design parameter for the thin-film microstrip signal width.

5.1.5 Transition Region

The transition region section of the CPW-to-TFMS transmission line shown in Figure 5.1, is a critical region of the line and requires careful design considerations in order to minimise mismatches between the CPW and the TFMS sections of the transmission line. Figure 5.13 shows a 3D cross-sectional view of the transition region. The characteristic

impedance and dissipation losses of the transition section have been simulated using equations 3.1 and 3.3d, respectively.

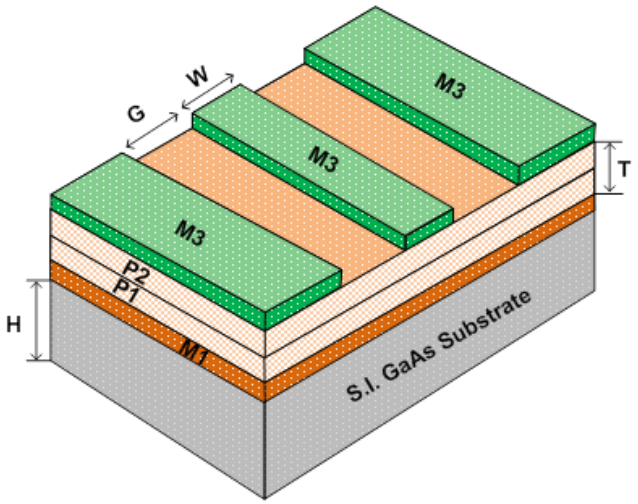


Figure 5.13: 3D cross-sectional view of the transition region for a CPW-to-TFMS transition transmission line.

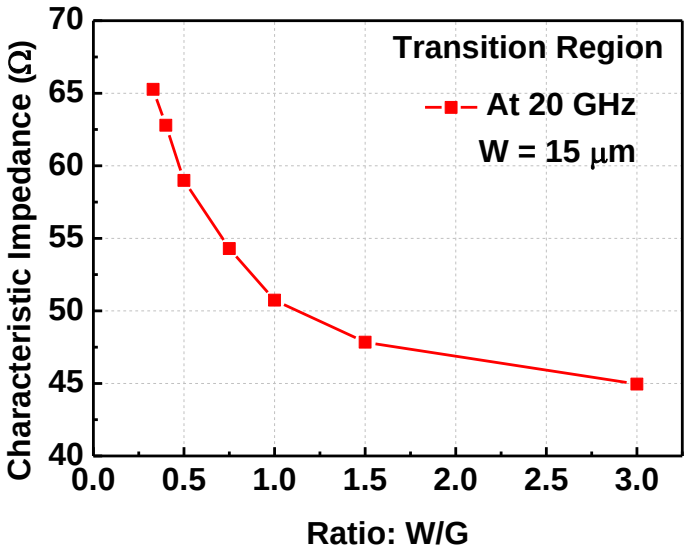


Figure 5.14: Simulated characteristic impedances of the transition region with different width and gap parameters.

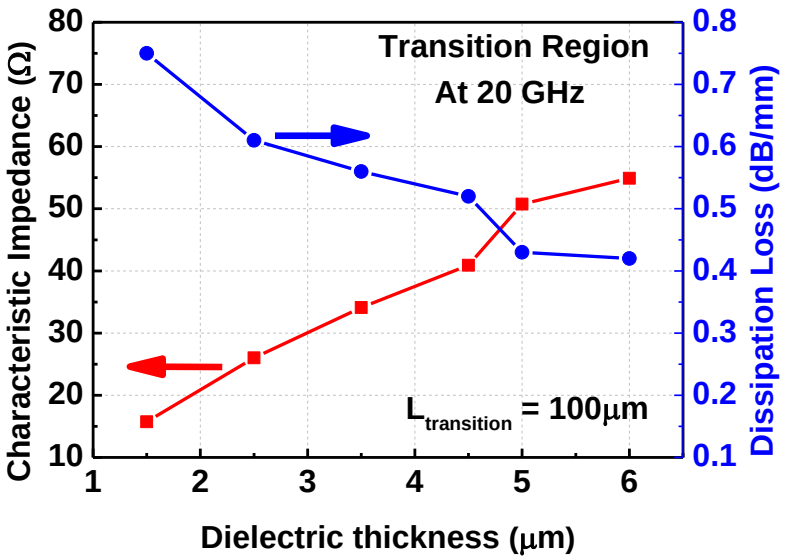


Figure 5.15: Simulated characteristic impedance and dissipation loss of the transition against dielectric thickness.

Figure 5.14 shows the simulated characteristic impedances of the transition region with different signal width and gap parameters. At 20GHz, and with a signal width to gap ratio less or equal to unity, the characteristic impedance of the transition region is approximately 50Ω, and with a higher ratio than unity, low impedance values are achieved. In order to impedance match the whole transmission line, we aim for a 50Ω line. Therefore, the best ratio to achieve this would be approximately unity, as using a ratio lower than unity would create a current-crowding effect on the transmission line. We further determine the dielectric thickness required to achieve the 50Ω impedance match in relation to the dissipation losses, as shown in Figure 5.15.

The increase in the impedance of the line with the increasing thickness of the polyimide dielectric layer, as shown in Figure 5.15, indicates a direct relationship – as one would expect. This is due to an increase in the distance between the metal conductor plates (M3 and M1) which reduce the capacitance of the line and hence result in an increase in impedance. The decrease in dissipation loss is associated with the lower effective dielectric constant as the thickness of the dielectric material increases. With transition section design parameters of 100µm in length, a width (W) of 15µm, a gap (G) of 15µm and a dielectric thickness of 5µm, one can achieve a Z_0 = 51Ω with a very low dissipation loss of about 0.42dB/mm at 20GHz. Further analysis is carried out on the effects of varying the transition region lengths on both characteristic impedance and dissipation loss, as shown in Figures 5.16 and 5.17, respectively.

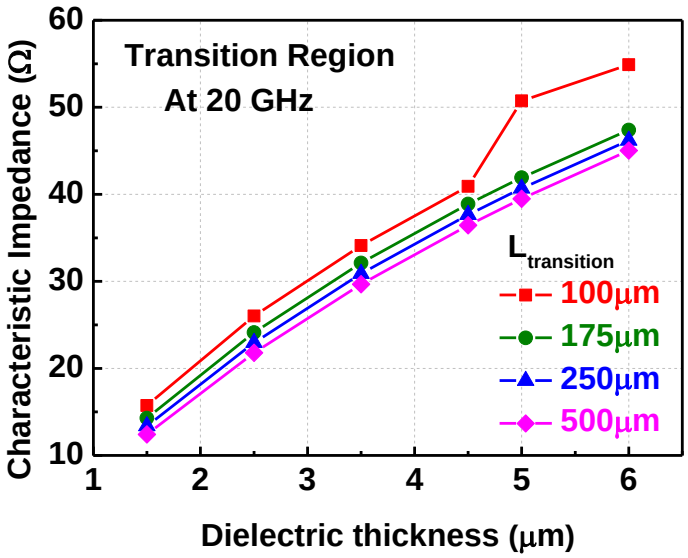


Figure 5.16: Simulated characteristic impedance against dielectric thickness at different transition lengths.

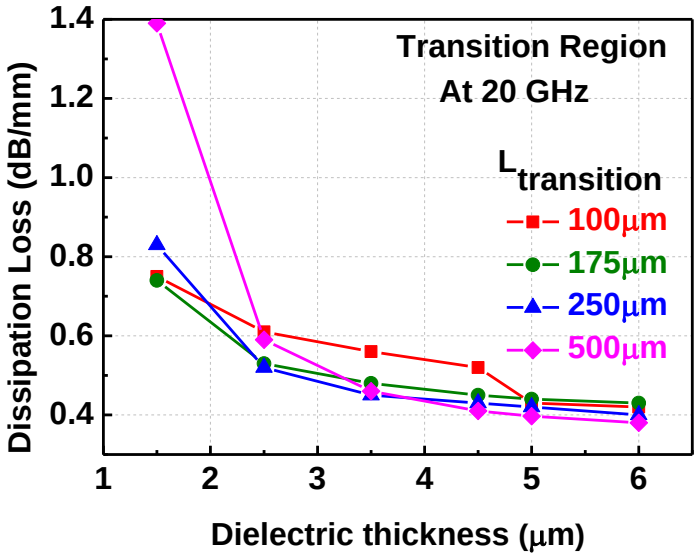


Figure 5.17: Simulated dissipation loss against dielectric thickness at different transition lengths.

Figures 5.16 and 5.17 illustrate that the transition becomes more capacitive when it is longer, hence the decrease in characteristic impedance. Dissipation losses increase as the length of the line increases, as observed in Figure 5.17. This is due to the parasitics that are associated with having a longer conductor line. It is further observed that the shortest length (100μm) transition has slightly higher losses due to the bonding pads being nearer to the DUT than when the transition length is longer. Hence, this introduces some parasitics into the line. In order to improve reflections of the transition section, CPW ground planes are tapered, the effect of which is shown in Figure 5.18.

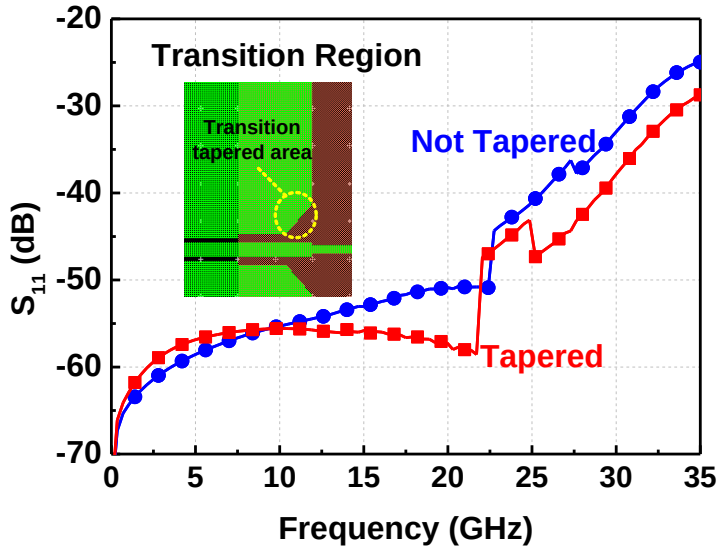


Figure 5.18: Simulated S_{11} parameters of the transition region with and without tapered CPW ground planes.

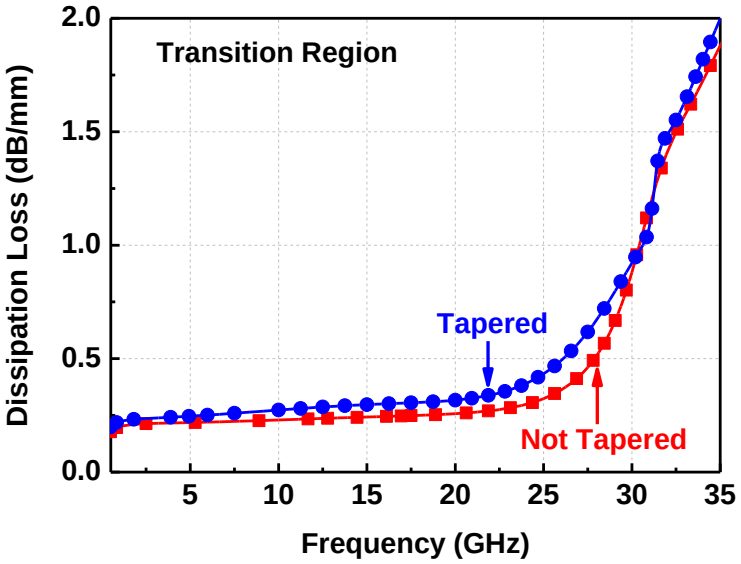


Figure 5.19: Simulated dissipation losses of the transition region, with and without tapered CPW ground planes.

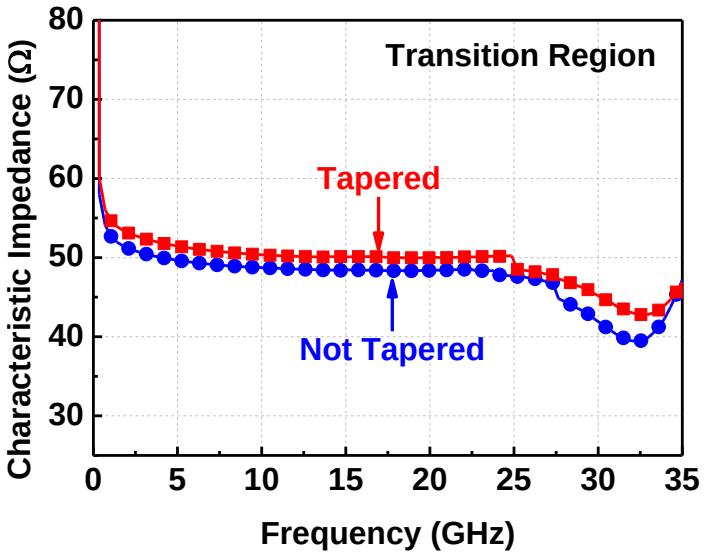


Figure 5.20: Simulated characteristic impedances of the transition region with and without tapered CPW ground planes.

The simulated return losses in the transition region, with and without tapered CPW ground planes, are shown in Figure 5.18. In the figure, it is clearly illustrated that a transition with tapered CPW ground planes has less reflections compared to a transition which is not tapered. As a result, this prompted us to taper the CPW ground planes on the transition region of the transmission line design. In order to verify that the tapering of the CPW ground does not have a significant effect on the line characteristics, the analysis is shown in Figures 5.19 and 5.20.

In Figures 5.19 and 5.20 comparisons between the simulated dissipation losses and characteristic impedances of the transition region, with and without tapered CPW ground planes, are made, respectively. Both the dissipation loss plots and the characteristic impedances of the tapered and non-tapered transition regions show no significant differences between the tapered and non-tapered transition CPW ground planes. Dissipation loss is maintained below 1 dB/mm, up to about 30 GHz, and the characteristic impedance of the transition section is also maintained at approximately 50Ω.

5.1.6 Transition Effect on the Transmission Line

In this subchapter, an in-depth transition effect on the CPW-to-TFMS transition transmission line is analysed, which includes the study of the CPW ground plane tapered region, return loss and a bandwidth analysis of the transition length of the different transition designs. The fully impedance-matched modelled structure of the CPW-to-TFMS transition transmission line, with cross-sectional views, is shown in Figure 5.21.

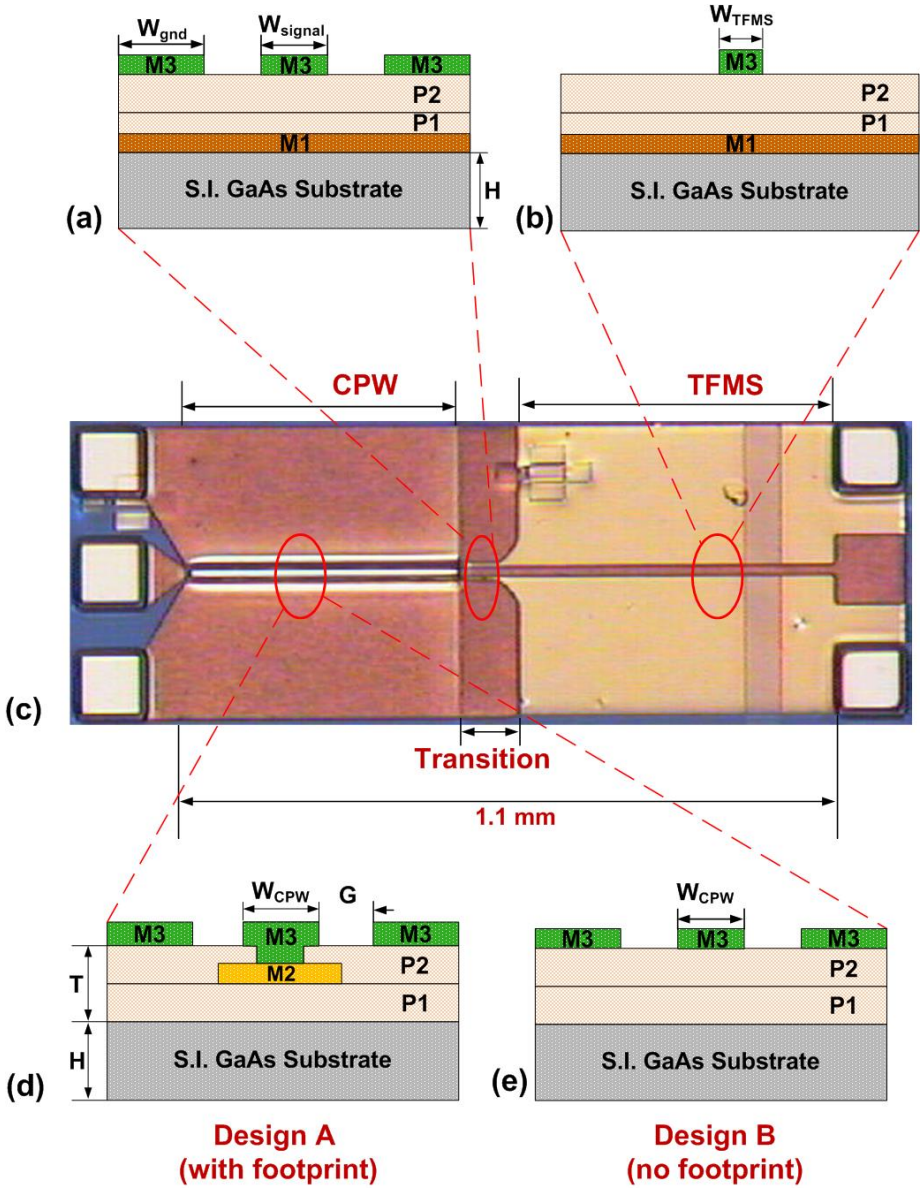


Figure 5.21: CPW to thin-film microstrip transition structure (a) cross-sectional view of the transition, (b) cross-sectional view of the TFMS end which does not have a footprint, (c) top view of the fabricated structure with bonding pads (d) cross-sectional view of the CPW line end with a footprint (design A) and (e) cross-sectional view of the CPW line end with no footprint (design B).

In this work we investigate two transition structures, design with a footprint on the CPW end (design A) and then design without a footprint (design B), as shown in Figure 5.21. Using the flexibility of multilayer technology, design A was modelled, fabricated and characterised. These structures do not require any vias between the CPW ground strips and the TFMS backside ground plane. Design A has a transition in the CPW section line with a footprint using (metal two, M2) as shown in Figure 5.21(d). In the transition section, the CPW ground plane is tapered in order to match the two parts of the line-minimising reflections. In Figure 5.21(c), both the CPW and TFMS sections have a length of 500 µm each, the transition section has a length of 100 µm and the left- and right-hand probing pads account for a total length of 125 µm each. All the design parameters for the two initial design structures are shown in Table 5.1.

Table 5.1: Dimensions for the CPW to TFMS transition transmission line for designs A and B [17]

Parameter	Design A (with a footprint) µm	Design B (no footprint) µm
H: Substrate thickness	600	600
T: Dielectric thickness	5	5
W_{gnd} : Ground plane width	248.5	248.5
G: CPW gap	10	5
$W_{(CPW)}$: Track width	15	20
$W_{(TFMS)}$: TFMS track width	15	10
W_{M2}: footprint width	25	----
(G-S-G): Pitch size	200	200

5.1.7 Choosing the Transition Design Parameters

This subchapter discusses why different parameters were chosen for the CPW-to-TFMS transition transmission line design. It analyses why a tapered design is used for the transition, the effect of the length of the CPW and TFMS section on the transition and the effects of a footprint on the full transition transmission line design.

5.1.8 Transition tapered region

CPW and the TFMS line characteristic impedance in the integrated structure is kept at 50Ω, while the transition section with the design parameters given in Table 5.1 has a impedance of only 51Ω. Therefore, great care has to be taken in the design of the transition area, to minimise signal reflections. In this work we have tapered the CPW grounds, and Figure 5.22 shows the effect of tapering on the signal line reflections.

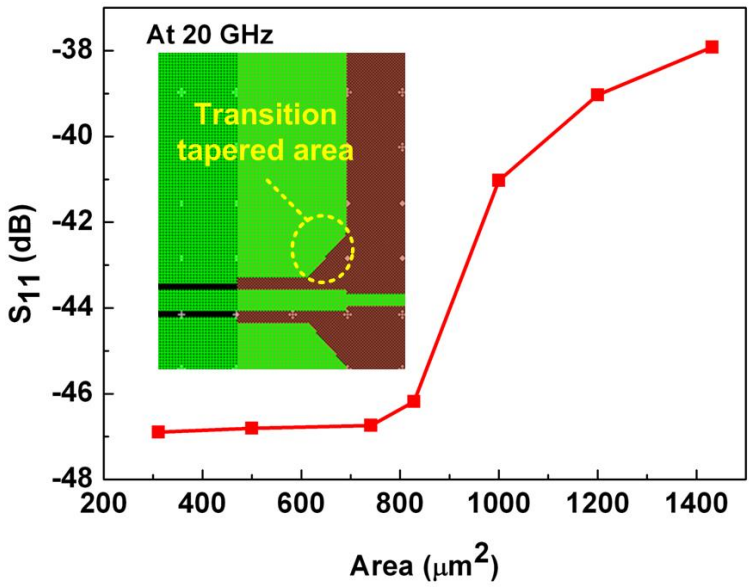


Figure 5.22: Simulated return loss of the transition tapered section at different CPW ground plane areas for design B (without a footprint).

In Figure 5.22 the simulated return loss of the transition tapered section at different CPW ground tapered-off areas at 20 GHz is shown. As shown in the Figure 5.22, when the tapered-off area is increased, the reflections in the line increase. The best return loss is achieved by tapering off an area between 300μm^2 and 900 μm^2.

5.1.9 Transition length analysis in relation to integrated transmission line length

This section investigates the design guidelines on how the performance of a transition structure will be affected at different ratios of the fully integrated transmission line length (L_{TL}) to the transition length ($L_{transition}$). The Design B's structure (without a footprint) is used for this investigation.

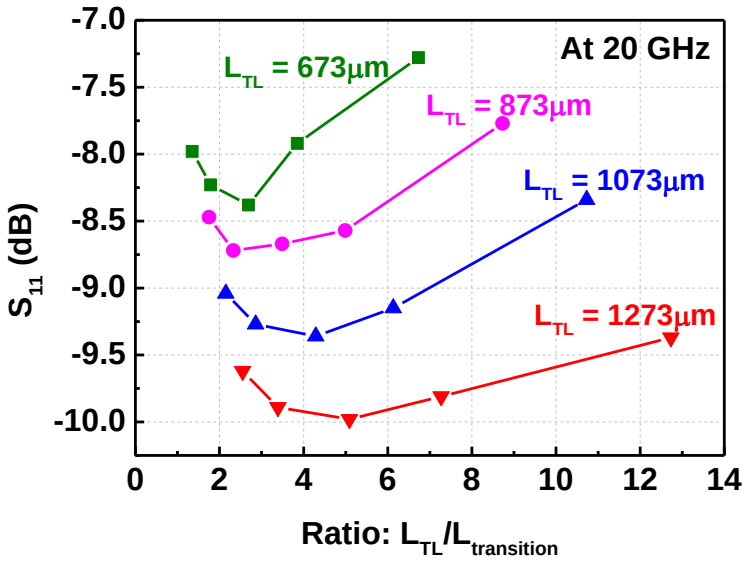


Figure 5.23: Return loss simulation analysis of the ratio of the transmission line length to transition length.

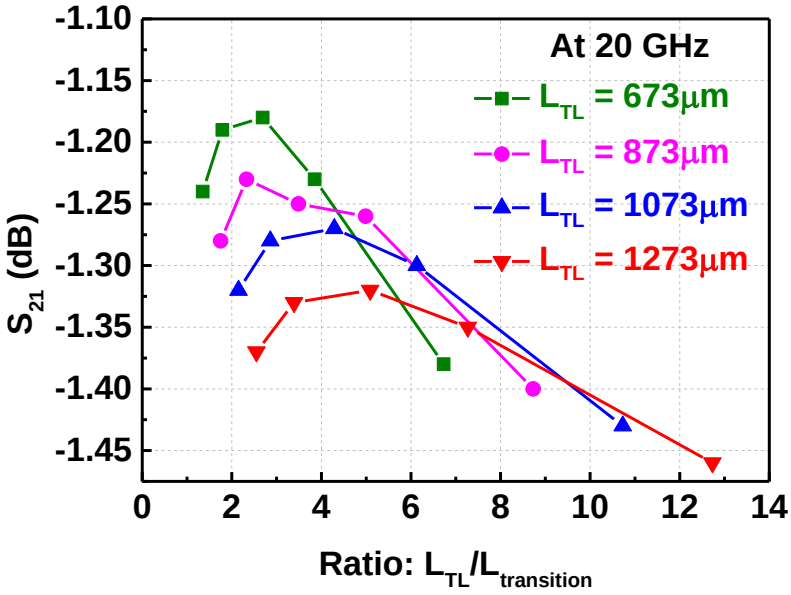


Figure 5.24: Insertion loss simulation analysis of the ratio of the transmission line length to transition length.

Signal line reflections are reduced following an increase in the full transmission line length (L_{TL}), as shown in Figure 5.23, while minimal reflections are achieved with a transition length ($L_{transition}$) of 250 µm at 20 GHz. It is observed in Figure 5.24 that the shortest transmission line gets more power transmitted through the signal line compared to the other three transmission lines, mainly due to conductor losses, which are greater in longer lines. Good insertion losses are achieved with a transition length ($L_{transition}$) of 250 µm at 20 GHz.

In conclusion, one would find it best to design a better performing CPW-to-TFMS transition with a transition length of 250 µm and with a full transmission line length of about 1mm. In the next section, the ideal lengths of both the CPW and TFMS regions are analysed, and the ideal ratio of the CPW length, L_{CPW}, to thin-film microstrip line length, L_{TFMS}, is obtained.

5.1.10 CPW and TFMS Length Optimisations

In this section, we investigate the performance of the transition structure on the length of the CPW and TFMS lines, by varying the lengths of the CPW and TFMS sections in design B (without footprint) while keeping constant the transition section length at 100um.

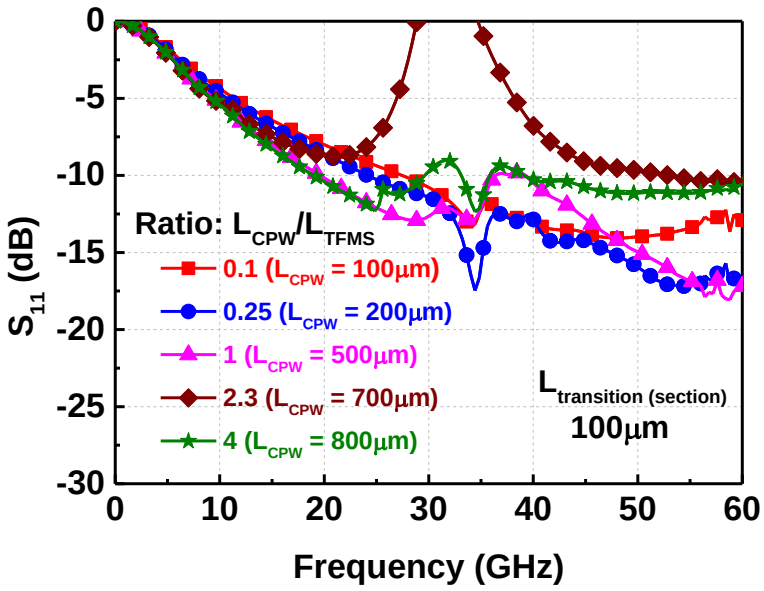


Figure 5.25: Simulation analysis of return loss for various ratios of the CPW length section to the TFMS line length section (L_{CPW}//L_{TFMS}) for a transition length of 100µm (design B).

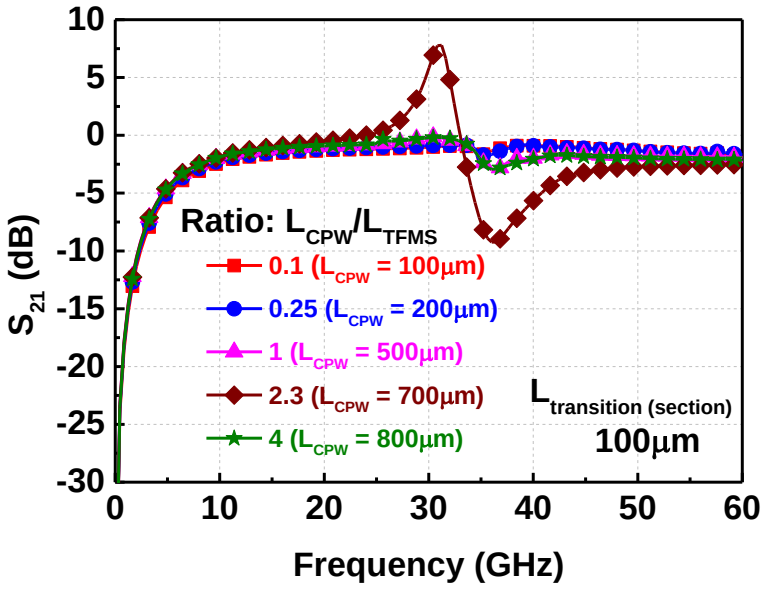


Figure 5.26: Simulation analysis of insertion loss for various ratios of the CPW length section to the TFMS line length section (L_{CPW}/L_{TFMS}) for a transition length of 100µm (design B).

Simulated return and insertion losses at different CPW length to TFMS line length ratios for design B (without footprint), with 1.1mm total transmission line length (bonding pads not included), are shown in Figures 5.25 and 5.26. In this study the transition section length is kept constant at 100µm while varying the CPW and TFMS lengths. From this investigation it is observed that when the CPW and TFMS have a similar length (unity), the transmission line maintains a good return loss along with a wider bandwidth. The transition demonstrates an insertion loss of less than 1dB over the frequency range 10 - 40 GHz, which further confirms that the CPW-to-TFMS transition transmission line is less length-dependent. With the ideal lengths of the transmission line sections analysed and obtained, the effects of the transition region lengths are discussed in the next subsection.

5.1.11 Effects of the transition region length

This section investigates the design guidelines on how the performance of a transition structure will be affected with different transition region lengths ($L_{transition}$). The transition region length is varied from 100µm to 350µm. The Design B's structure (without a footprint) is used for this investigation.

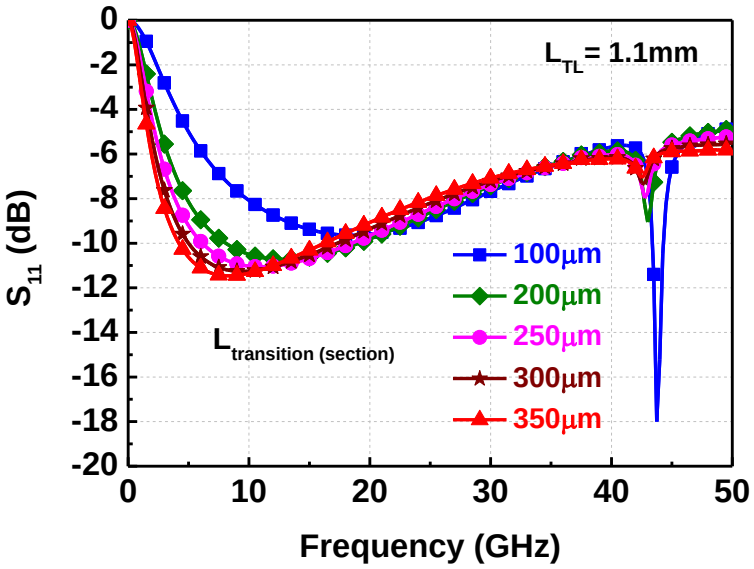


Figure 5.27: Simulation analysis of return losses of design B with different transition section lengths.

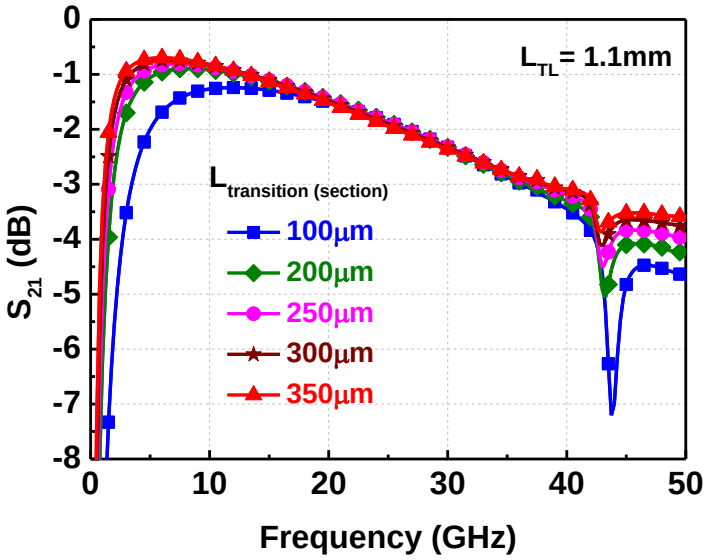


Figure 5.28: Simulation analysis of insertion losses of design B with different transition section lengths.

Simulated return and insertion losses at different transition section lengths line length for design B (without footprint), with 1.1mm total transmission line length (bonding pads included), are shown in Figures 5.27 and 5.28. In this study the transition section lengths are varied from 100μm to 350μm while maintaining the transmission line length at 1.1mm. From this investigation it is observed that when $L_{transition}$ is increased, both the performances of return and insertion losses would improve at frequencies below 15 GHz.

That is, less reflections and more power transmitted. It is also observed that the parasitic resonance peak distortion at around 45 GHz is reduced when $L_{transition}$ is increased.

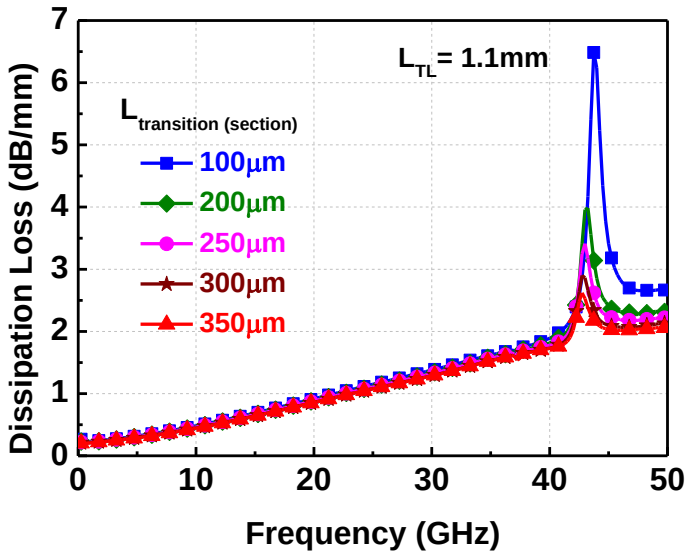


Figure 5.29: Simulation analysis of dissipation losses of design B with different transition section lengths

Simulated dissipation losses at different transition section lengths line length for design B (without footprint), with 1.1mm total transmission line length (bonding pads included), are shown in Figure 5.29. It is observed that the dissipation losses remain the same for all structures because the total transmission line length, L_{TL} remains unchanged. Similar to both the return and insertion loss plots, it is again observed that the parasitic resonance peak distortion at around 45 GHz is reduced when $L_{transition}$ is increased. The parasitic resonance of the transmission line is caused by ground planes of the CPW not being electrically connected to that of the TFMS. With the transition design guidelines analysed and obtained, the effect of having a transition region is discussed in the next subsection.

5.1.12 Comparison of Design A with and without transition region

A comparison of both measured and simulated return and insertion losses for design A (with a footprint), with and without a transition section, is shown in Figures 5.28 and 5.29. Figure 5.27 shows the fabricated design A (with a footprint) structure with no transition region.

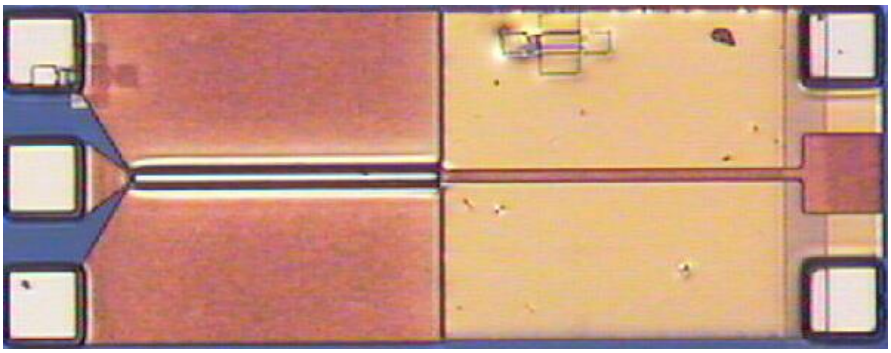


Figure 5.30: Fabricated design A, transmission line structure with no transition region.

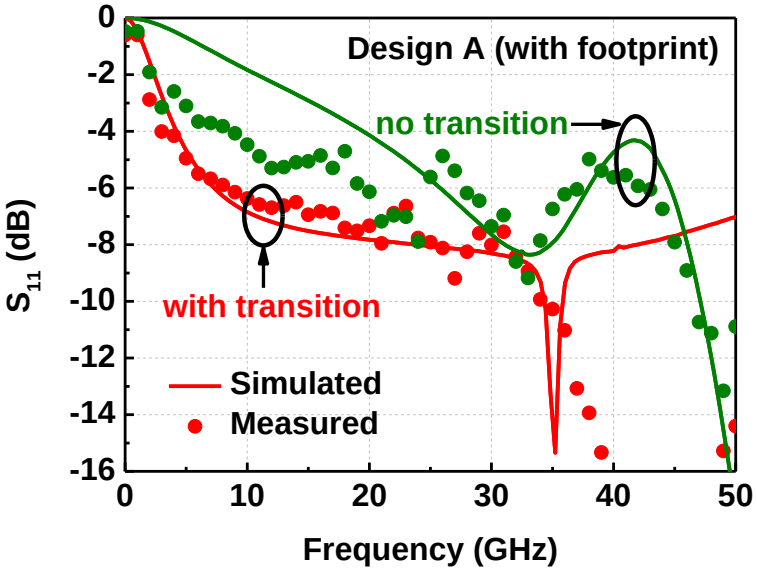


Figure 5.31: Measured and simulated return loss for design A, with and without a transition section.

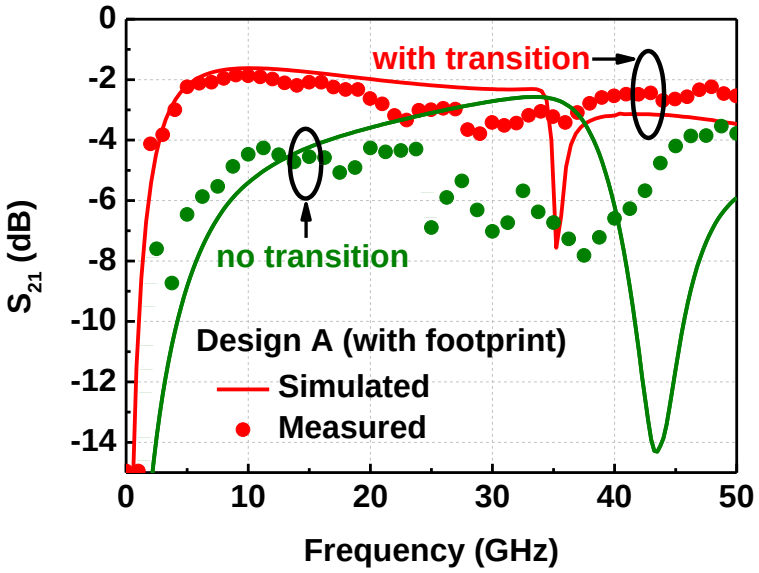


Figure 5.32: Measured and simulated insertion loss for design A with and without a transition section.

The design structure with a transition is observed to have a return loss better than 7 dB, from 9 to 34 GHz, and the design structure with no transition has a return loss better than 5 dB, from 19 to 38 GHz, as shown in Figure 5.28. From this analysis it is clear that the design structure with a transition has better return loss and hence less reflections on the line and a much wider bandwidth.

Both the measured and simulated insertion losses of design A, with and without a transition section in the design structure, are shown in Figure 5.29. It is observed that with a transition in the design structure, more power is transmitted through the transmission line than when we apply a design structure without a transition section. The structure with a transition demonstrates an insertion loss of 3 dB, from 4 to 22 GHz, while one with no transition demonstrates an insertion loss of 6 dB, from 5 to 25 GHz. After verifying the need to have a transition as part of the design structure, in order to assure better performance, a comparison is made in Figures 5.30 and 5.31 between two design structures: design A (with a footprint) and design B (no footprint).

5.1.13 Comparison of Designs A and B

A comparison of both simulated return and insertion losses in design structures A (with a footprint) and B (no footprint) is made, and the measured return and insertion losses of design A are compared to the simulated results, as shown in Figures 5.30 and 5.31.

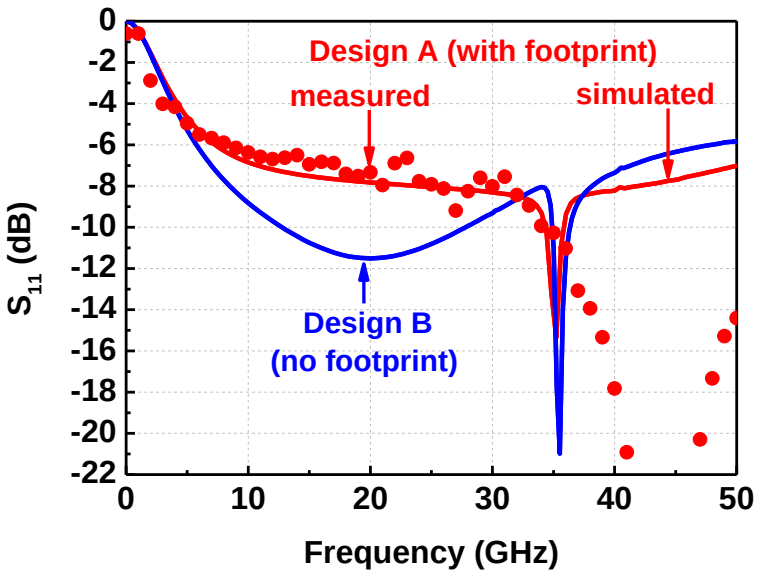


Figure 5.33: Measured and simulated return loss for design A and the simulated data for design B.

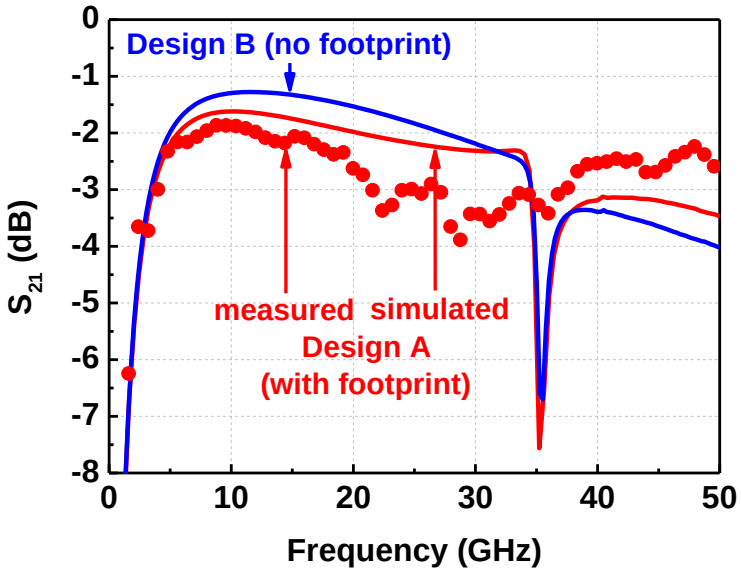


Figure 5.34: Measured and simulated insertion loss for design A and the simulated data for design B.

In Figure 5.30 it is observed that for design B (with no footprint) the return loss is better than 8 dB for the frequency range from 8 to 35 GHz, and for design A (with a footprint) its measured return loss is better than 7 dB, from 9 to 34 GHz, while its simulated return loss is better than 7 dB, from 12 to 34 GHz. From this analysis it is clear that design B has a better return loss of 8 dB as compared to 7dB for design A.

The measured insertion loss of design A, along with the simulated return loss for design B, is illustrated in Figure 5.31. It is observed that in design B more power is transmitted through the line than design A, which demonstrates an insertion loss of 3 dB, from 4 to 22 GHz. In both Figures 5.30 and 5.31 there is distortion at about 35 GHz, due to the parasitic resonance of the transmission line which caused by grounds of the CPW not being electrically connected to that of the TFMS. A further investigation is undertaken on the compactness of the transition and how to get rid-of the distortion at 35 GHz, and this analysis is discussed in the next subsection.

5.1.14 Compact Transitions

Compact transitions can also be achieved by redesigning the structure in design B (without a footprint). In order to achieve this goal, signal-to-ground spacing (pitch spacing) is reduced from 200 µm to 150 µm and to 100 µm while at the same time shortening the lengths of the CPW and TFMS lines to half of the original length, 250 µm each, making the new total length of the transition transmission line (including the probing pads) equal to 0.806 mm.

From Figure 5.32, it is observed that compact structures with 100 µm and 150 µm pitch sizes have better return losses compared to the 200 µm pitch-sized structure. Of the two compact design structures in Figure 5.32, the 150 µm pitch-sized structure offers less reflections in the signal line and much wider bandwidth with a return loss better than 10 dB, from 15 GHz to 60 GHz, compared to the 100 µm pitch-sized structure with a return loss better than 10 dB, from 25 GHz to 60 GHz. This is further verified with the insertion losses in Figure 5.33.

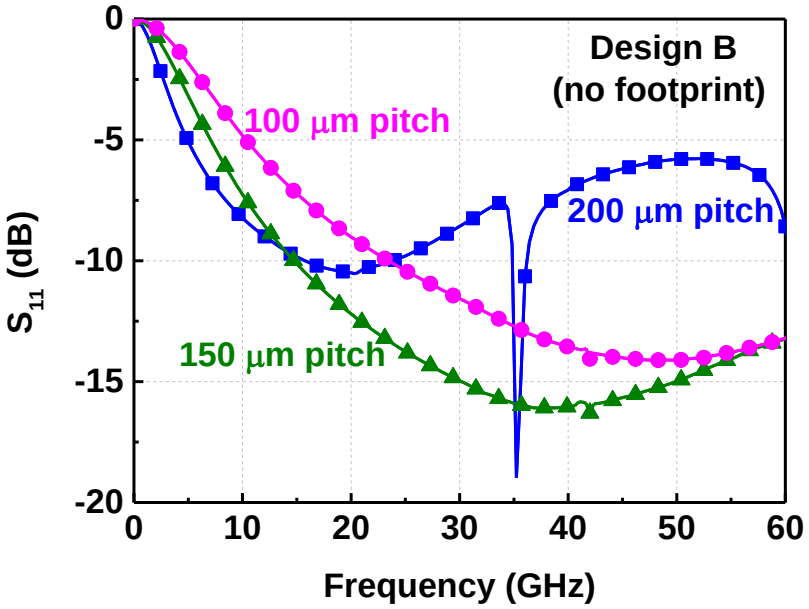


Figure 5.35: Simulated return loss comparison for design B with 200 µm, 150 µm and 100 µm signal-to-ground (pitch) spacing.

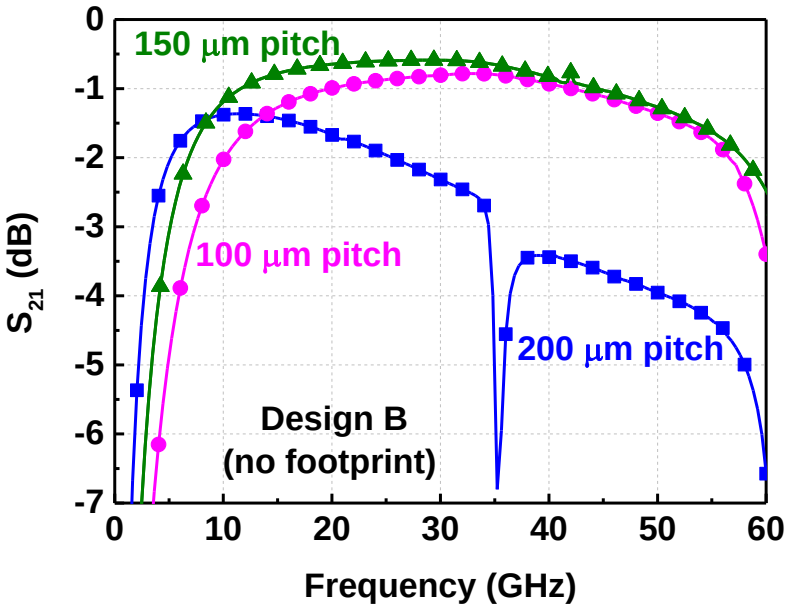


Figure 5.36: Simulated insertion loss comparison for design B with 200 µm, 150 µm and 100 µm signal-to-ground (pitch) spacing.

The compact design structures with 100 µm and 150 µm pitch sizes transmit more power through the signal line as compared to the 200 µm pitch-sized structure, as seen in Figure 5.33. Of the two compact design structures, the 150 µm pitch-sized design maintains a slightly wider bandwidth with an insertion loss of 1.5 dB, from 8 to 54 GHz, compared to the 100 µm design with an insertion loss of 1.5 dB, from 13 to 52 GHz. Hence, this verifies that the 150 µm pitch-sized probing pads would offer better performance in the design of a compact CPW-to-TFMS transition transmission line.

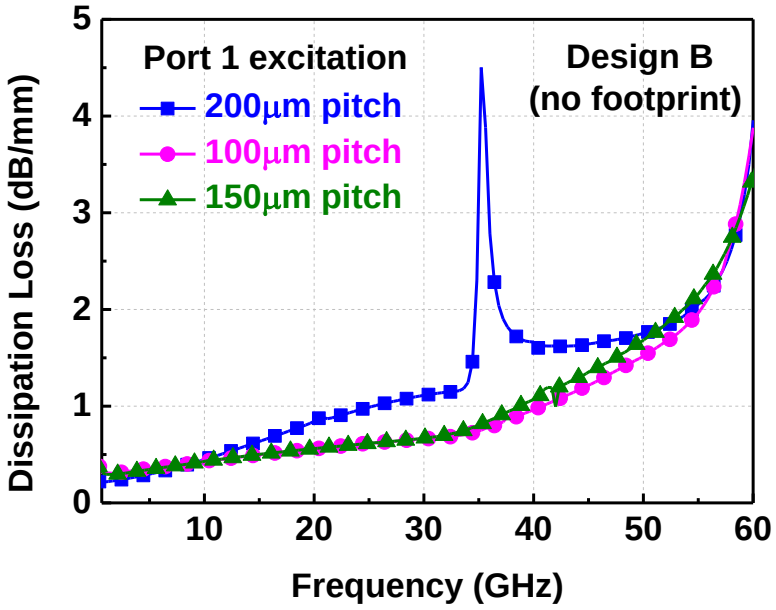


Figure 5.37: Simulated dissipation loss for design B with 100 µm, 150 µm and 200 µm signal-to-ground (pitch) spacings at port 1 (CPW end) excitation.

A dissipation loss comparison between the compact structures (100 µm, 150 µm) and 200 µm pitch-sized designs, for both ports 1 and 2 excitations, is shown in Figures 5.34 and 5.35. Port 1 refers to the CPW end and Port 2 refers to the TFMS end. It is observed that there is a significant difference in dissipation loss between the two compact designs (100 µm and 150 µm) which both maintain a dissipation loss below 1 dB/mm, up to 40 GHz. The compact design structures at Port 1 (CPW end) excitation demonstrate lower dissipation losses as compared to the 200 µm pitch-sized structure. This is mainly due to higher parasitic (conductor) losses in the conductor line, caused by having a wider signal-to-ground spacing. At Port 2 (TFMS end) excitation, there is no significant difference in losses for all three design structures, as shown in Figure 5.35. The EM current distribution interpretation of the structures in Figure 5.36 verifies the dissipation loss results in this section.

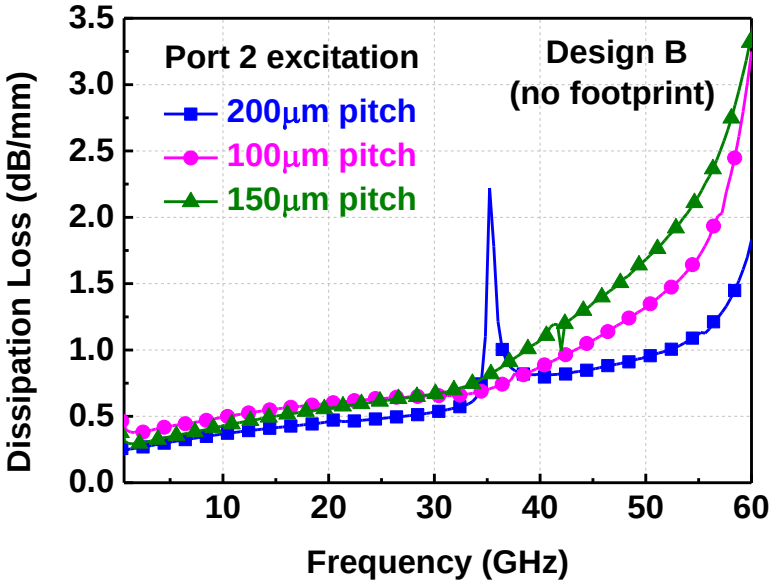


Figure 5.38: Simulated dissipation loss for design B with 100 µm, 150 µm and 200 µm signal-to-ground (pitch) spacings at Port 2 (TFMS end) excitation.

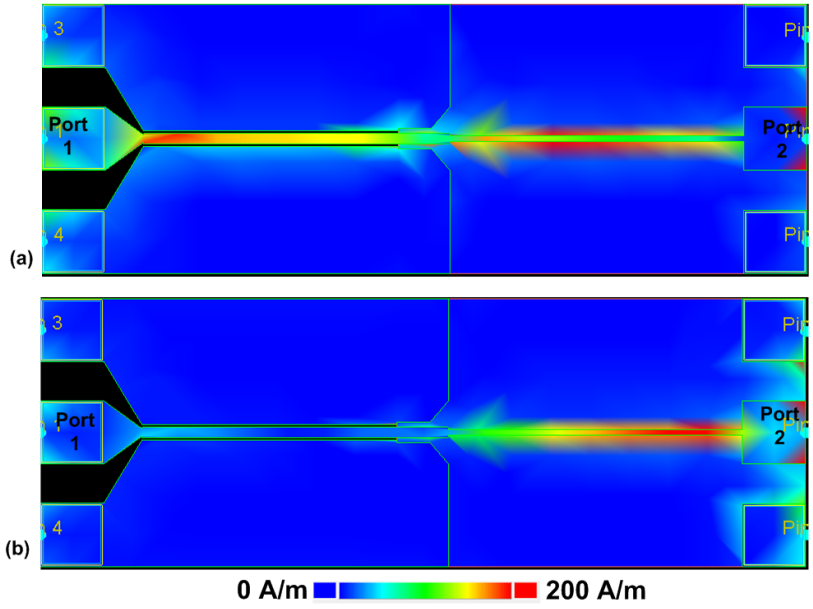


Figure 5.39: EM current distribution in CPW-to-TFMS transition at 20 GHz with; (a) Port 1 excitation and (b) Port 2 excitation (design B with 200 µm pitch).

Figure 5.36 illustrates the simulated EM current distribution for the CPW-to-TFMS transition at 20 GHz, and it is observed that the transmission line structure with Port 1 excitation shows relatively more losses as compared to the excitation from Port 2 (Figure 5.36b). In both figures the current distribution is concentrated mainly on the signal line, most of which is around the TFMS structure due to the current-crowding effect [1]. The EM current distribution observations in Figure 5.36 verify dissipation losses for design B with a 200 µm pitch, as shown in Figures 5.34 and 5.35.

5.1.15 New Wideband Compact Transition Designs

After analysing and discussing in the previous sections the different parameters that make up the CPW-to-TFMS transition transmission line, new and improved design structures for both design A (with a footprint) and design B (no footprint) are proposed in Figure 5.37. These new design structures are compact multilayer structures and demonstrate much better performance than the old designs, as shown in Figures 5.38, 5.39 and 5.40. Table 5.2 compares the design parameters between the old and new design structures of A and B.

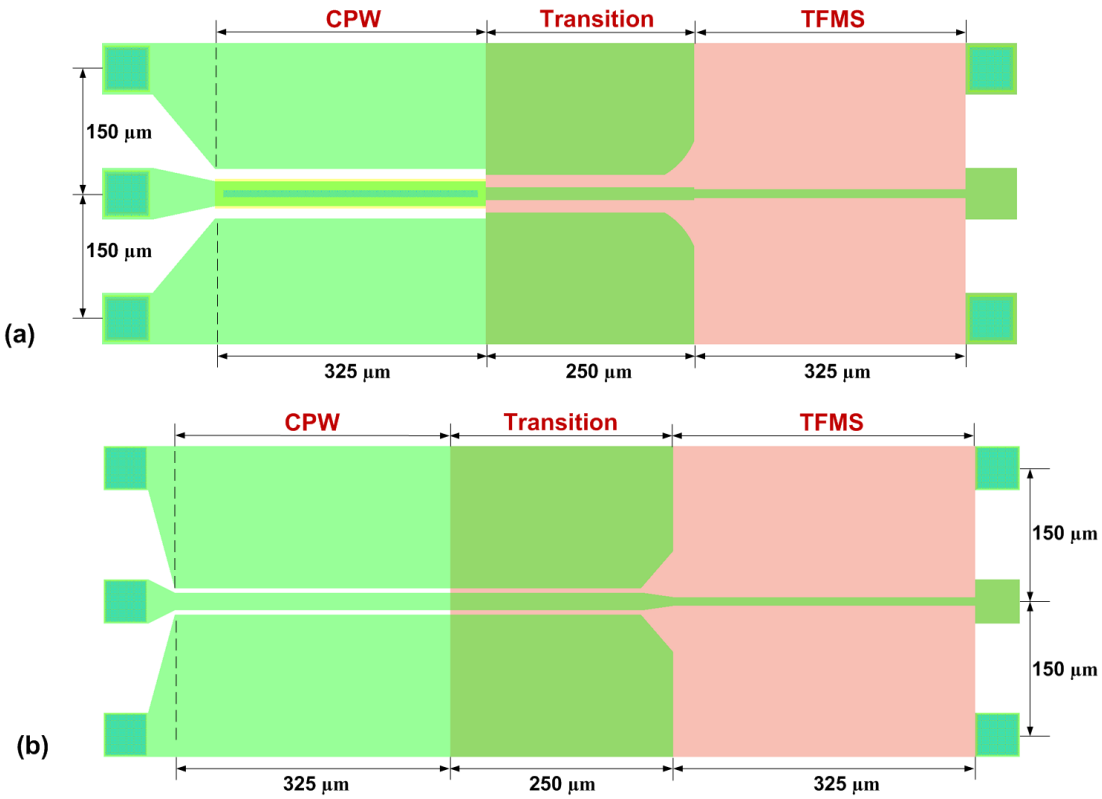


Figure 5.40: Top view of the new compact CPW-to-TFMS transition design structures; (a) design A (with a footprint) and (b) design B (no footprint).

Table 5.2: Design parameter comparison between old and new A and B transmission line structure designs.

Parameter	**Old Designs**		**New Designs**	
	Design A (µm)	**Design B (µm)**	**Design A (µm)**	**Design B (µm)**
H (substrate thickness)	600	600	600	600
T (dielectric thickness)	5	5	5	5
G (gap width)	10	5	15	5
$\mathbf{W_{signal\ (CPW)}}$	15	20	30	20
$\mathbf{W_{signal\ (TFMS)}}$	15	10	11	11
$\mathbf{W_{signal\ (transition)}}$	15	10	15	20
W (footprint width, M2)	25	---	36	---
Pitch size (G-S-G)	200	200	150	150
$\mathbf{L_{transition}}$ (transition section length)	100	100	250	250
$\mathbf{L_{CPW}}$ (CPW section length)	500	500	325	325
$\mathbf{L_{TFMS}}$ (TFMS section length)	500	500	325	325

In Table 5.2 the old designs refer to the 200 µm pitch-sized transition transmission lines, while the new designs refer to the more compact, improved transition transmission lines with a 150 µm pitch and a shorter length. The performances of these design structures are compared in Figures 5.38 and 5.39.

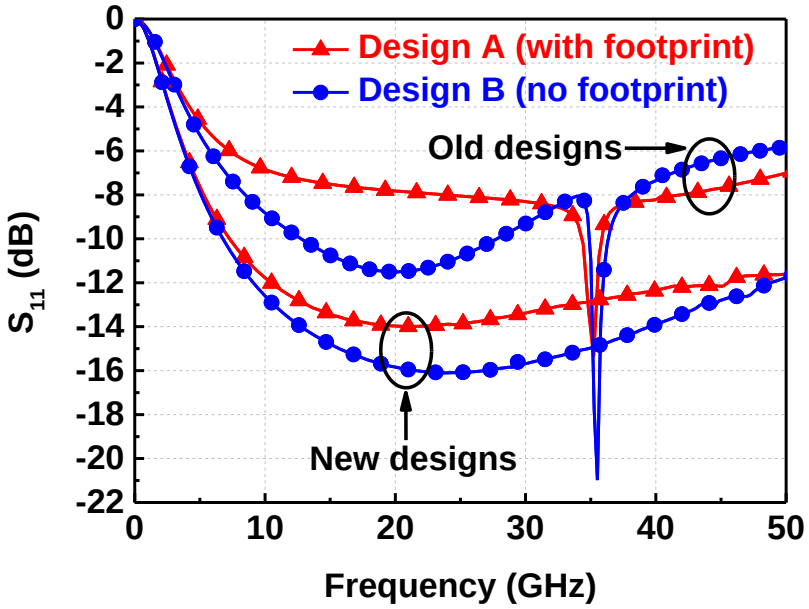


Figure 5.41: Simulated return losses for old and new A and B transmission line structure designs.

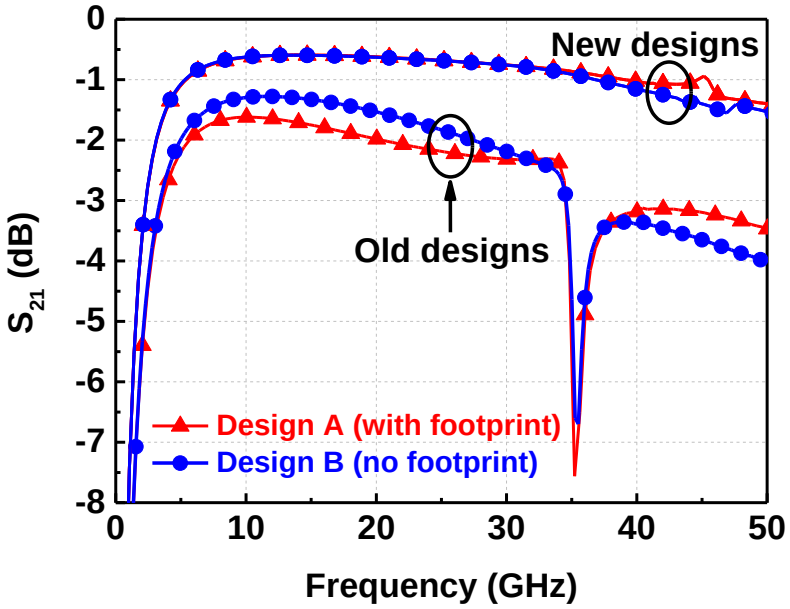


Figure 5.42: Simulated insertion losses for old and new A and B transmission line structure designs.

The old design structures demonstrate return losses better than 6 dB, from 7 to 50 GHz, while the new compact designs demonstrate return losses better than 12 dB, from 10 to 50 GHz, as shown in Figure 5.38. Hence, reflections in the new compact designs are observed to be minimal as compared to the ones of the old designs. Of the two new compact design structures, design B (no footprint) demonstrates a slightly better return loss of about 2 dB

than design A (with a footprint). The performances of these design structures are further verified by the S_{21} parameters simulations in Figure 5.39.

The old design structures demonstrate insertion losses below 2.5 dB, from 4 to 34 GHz, while the new compact designs demonstrate insertion losses below 1.5 dB, from 4 to 47 GHz, as shown in Figure 5.39. Hence, more power is observed to be transmitted through the new compact designs over a wider bandwidth than the old design structures. The two new compact design structures, design A (with a footprint) and design B (no footprint) have no significant differences in insertion losses. The superior performances of the new compact design structures are further verified using the dissipation loss characterisation shown in Figure 5.40.

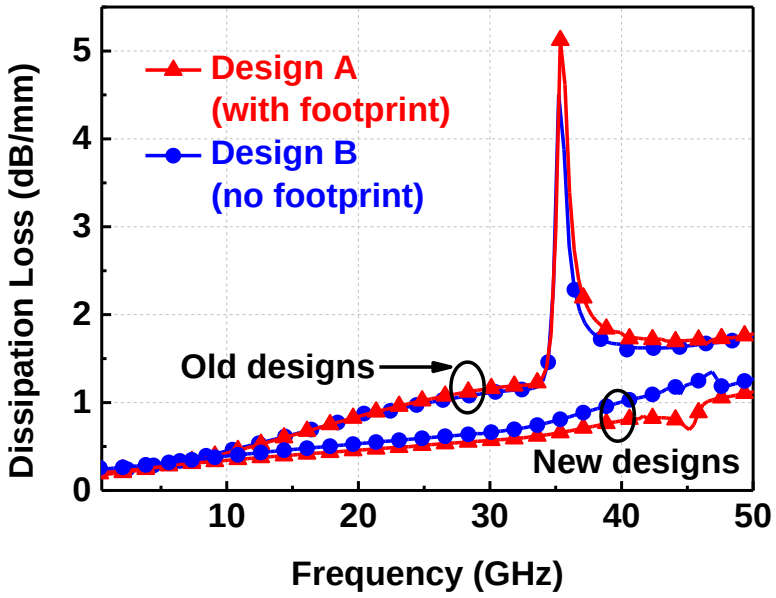


Figure 5.43: Simulated dissipation losses for old and new designs A and B transmission line structures.

The new and improved design structures of designs A and B are observed in Figure 5.40 to have lower dissipation losses of below 1 dB/mm, from 0 to 40 GHz, compared to the old design structures with losses below 1 dB/mm, from 0 to 26 GHz. As a result, this provides a significant bandwidth difference of 14 GHz, mainly due to higher parasitic (conductor) losses in the conductor line caused by having a wider signal-to-ground spacing in the old design structures. EM current distribution in Figure 5.41 is used to verify and explain these results.

The electromagnetic current distribution of the new compact design structures A and B at 20 GHz, with Port 1 excitation, is illustrated in Figure 5.41. In both figures the current distribution is mainly concentrated on the signal line, most of which is around the TFMS structure due to the current-crowding effect. There is not much current-crowding in the CPW region in design A, as shown Figure 5.41(a), which is mainly due to the footprint (metal 2) employed by the design, in that it evenly distributes the current as it passes through the line. This is not the case for the CPW region in design B (with no footprint), as observed in Figure 5.41(b). Therefore, the low current distribution seen in the CPW region of design A explains and verifies the slightly lower dissipation losses in Figure 5.40 that the design offers compared to those of design B.

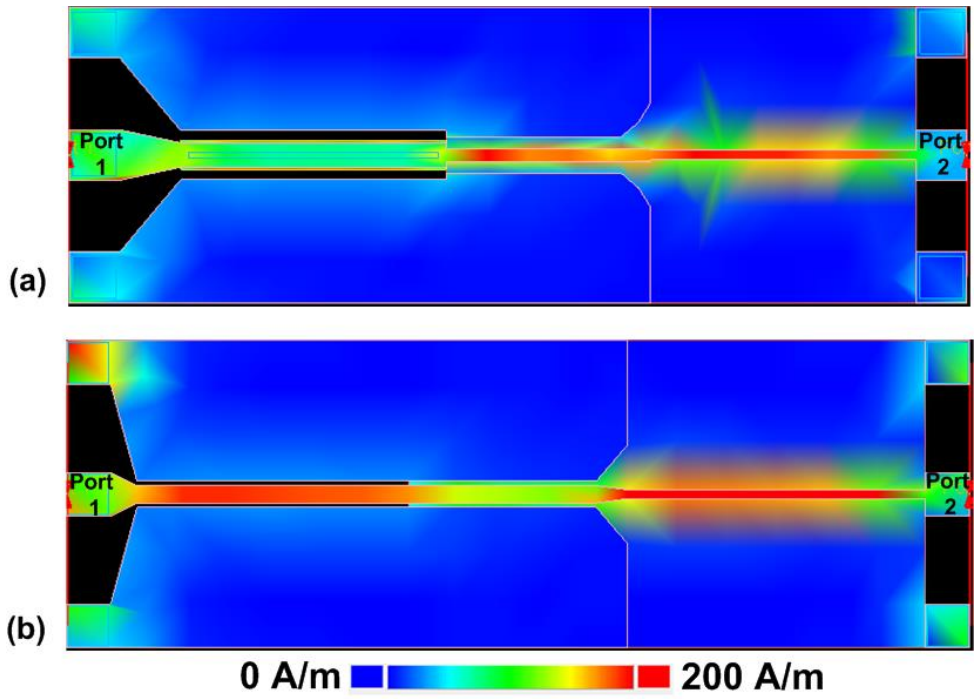


Figure 5.44: E.M current distribution at 20 GHz with port 1 excitation of; (a) new compact design A (with footprint) and (b) new compact design B (no footprint).

5.2 MMIC-Active Components and Circuits Interconnection

5.2.1 pHEMT Characterisation

The two pHEMT structures under investigation in this work are AlGaAs/InGaAs/GaAs pHEMTs. The first pHEMT has a gate length, L_g, of 0.5 µm and a gate width, W_g, of 100 µm. It consists of two gate fingers, making it a (0.5x200 µm^2) pHEMT. The second pHEMT structure has a gate length, L_g, of 0.5 µm and a gate width, W_g, of 60 µm. It also consists of two gate fingers, making it a (0.5x120 µm^2) pHEMT. Both the top and cross-sectional views of the (0.5x200 µm^2) pHEMT are shown in Figure 5.45. Probing pads at the gate and drain have been fabricated for the purpose of characterising this pre-processed virgin pHEMT. The micrographs of both the virgin and post-processed multilayer (0.5x200 µm^2) pHEMTs are shown in Figure 5.46.

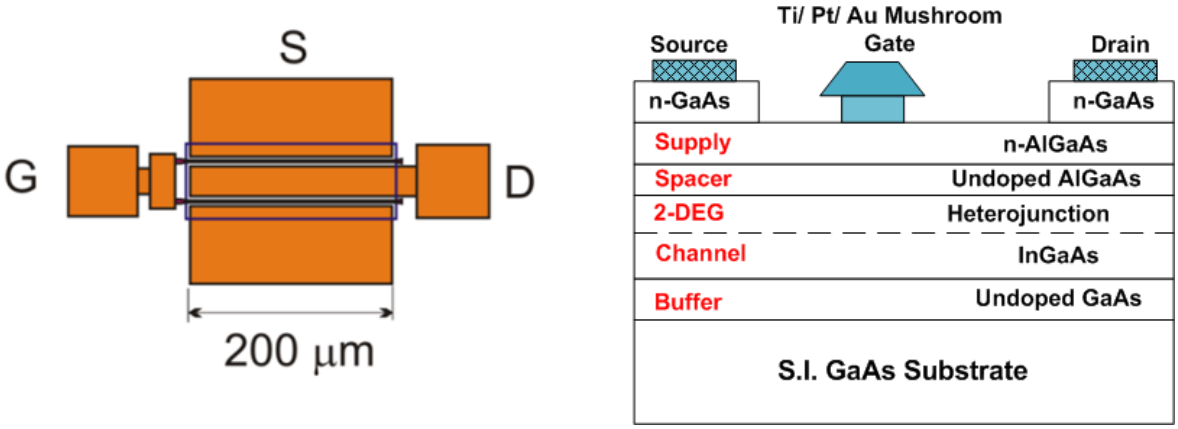


Figure 5.45: Top and cross-sectional view of the AlGaAs/InGaAs pHEMT.

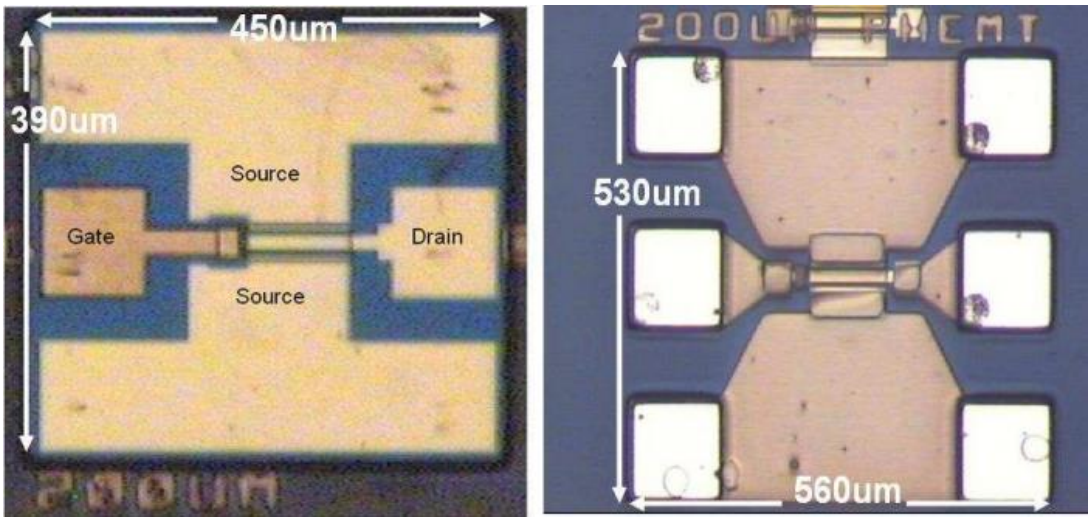


Figure 5.46: Micrographs of the fabricated pre- (virgin) and post-multilayer processed (0.5x200µm^2) pHEMTs.

The effect of multilayer processing on the active devices is investigated in this work. Probing pads have been designed and fabricated on both the virgin and post-multilayer pHEMTs, to compare and study the effects of multilayer processing.

The pHEMTs incorporated in multilayer CPW MMIC technology have polyimide and metal layers fabricated on top of the pHEMTs. A conceptual drawing of how the pHEMTs are positioned in the multilayer MMIC is shown in Figure 5.46.

5.2.2 Multilayer pHEMT Modelling

In this section multilayer-processed pHEMTs are characterised by first looking at the DC characteristics. A comparison between the virgin and multilayer pHEMTs, in order to study the effects of multilayer processing, is made here; furthermore, small-signal parameter extraction is achieved using a direct S-parameter measurement technique. The technique has been created as an automated procedure with the aid of Agilent's IC-CAP.

5.2.3 DC Characterisation a (0.5x200 µm^2) pHEMT

During DC characterisation, drain source voltage (V_{ds}) is varied at different gate biasing points (V_{gs}), and the respective drain source current (I_{ds}) is measured. Gate voltage is varied and the drain source current is measured for a fixed drain source voltage. DC and RF measurements are carried out using HP8510C VNA, along with Agilent's IC-CAP as the controlling platform.

It should be noted that the results shown in Figures 5.47 and 5.48 are taken as the average of five pHEMTs for both the virgin and multilayer devices. It is observed that although there are some slight differences between the virgin and multilayer pHEMTs, such as the pinch-off voltage, and the maximum attainable g_m, they are still considered to be very much similar to each other. The discrepancy in the results is well within tolerance range.

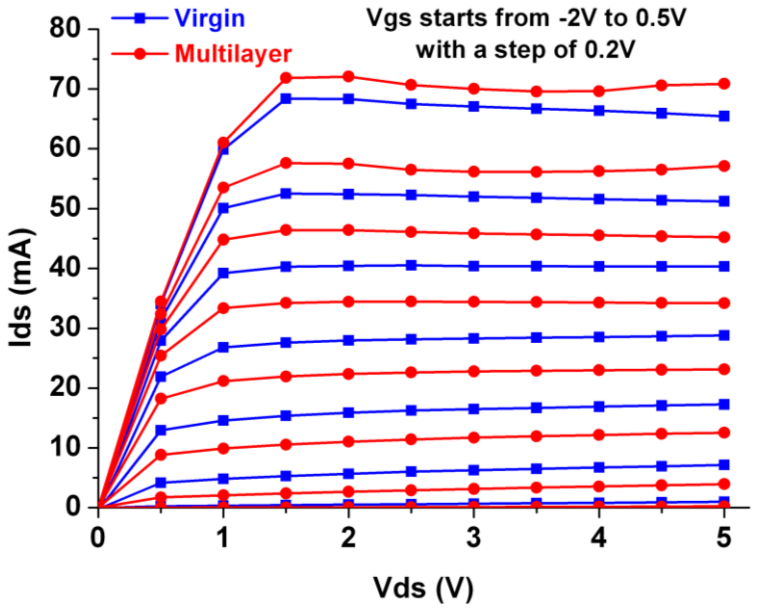


Figure 5.47: Comparison of output characteristics between virgin and multilayer (0.5×200 µm^2) pHEMTs.

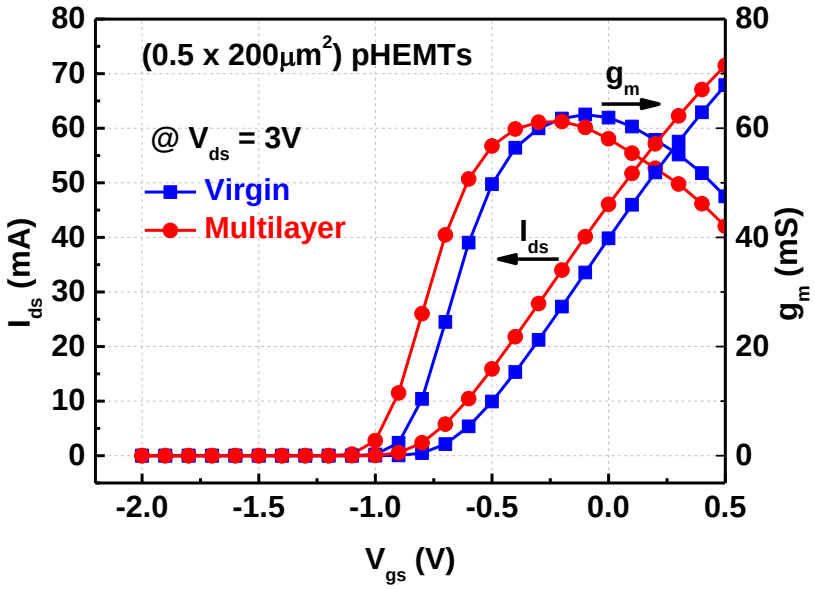


Figure 5.48: Comparison of measured I_{ds} and g_m characteristics between virgin and multilayer (0.5×200 µm^2) pHEMTs.

From Figure 5.47 it is evident that with a zero V_{ds} and V_{gs}, a very low drain to source current I_{ds} (normally less than the reverse leakage current) flows between the drain to the source. As the input gate voltage (V_{gs}) increases, higher drain currents (I_{ds}) are obtained. This figure can be divided into two regions – in the first region the drain current increases and then in the second region it remains almost constant. The region where the current increases linearly is referred to as the 'triode region', in which the output current increases

almost linearly in line with an increase in drain voltage. For larger V_{ds}, the channel is pinched-off from the drain side, and hence the maximum current flowing through the channel is limited or saturated and therefore remains almost constant.

It is seen from Figures 5.47 and 5.48 that there is a slight difference between the virgin and multilayer pHEMTs. These discrepancies are within the tolerance level, and therefore it can be concluded that multilayer processing does not introduce any significant degradation of performance in relation to pHEMT devices.

The highest transconductance peak for the (0.5 x 200 μm^2) pHEMT is found to be 61 mS at V_{gs} = -0.2 V and V_{ds} = 3 V. At these bias-operating conditions, the drain source current I_{ds} is found to be 34 mA.

5.2.4 DC Characterisation of a (0.5x120 μm^2) pHEMT

The micrograph of the (0.5x120 μm^2) pHEMT is shown in Figure 5.49 and it DC characteristics are given in Figures 5.50 and 5.51.

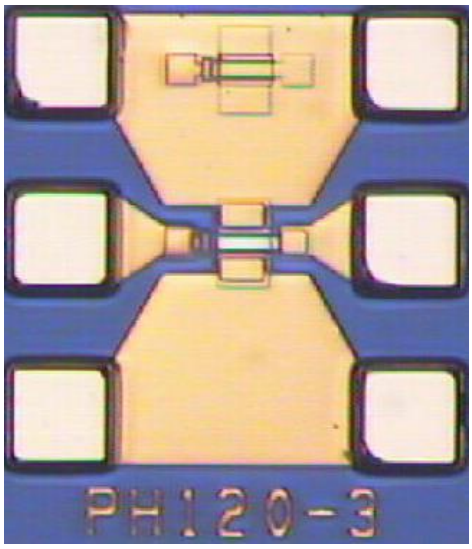


Figure 5.49: Micrograph of a fabricated multilayer (0.5x120 μm^2) pHEMT.

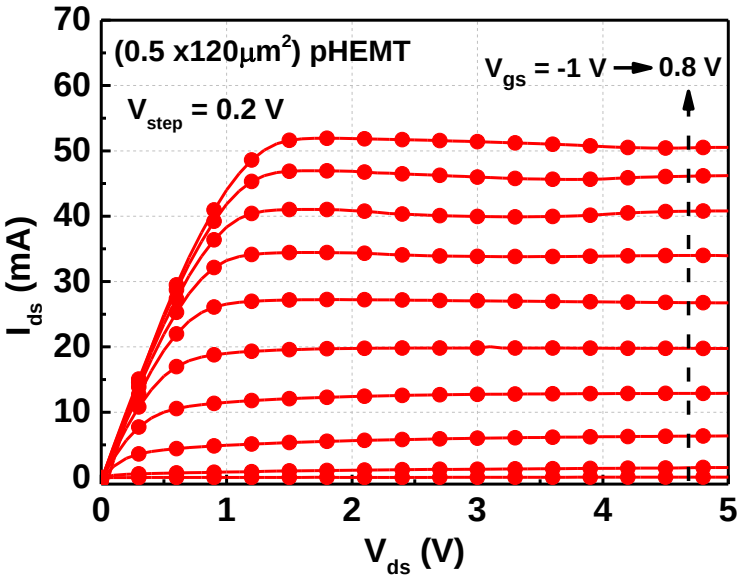


Figure 5.50: Measured output characteristics of the fabricated two-gate fingered (0.5 x 120 μm^2) pHEMT.

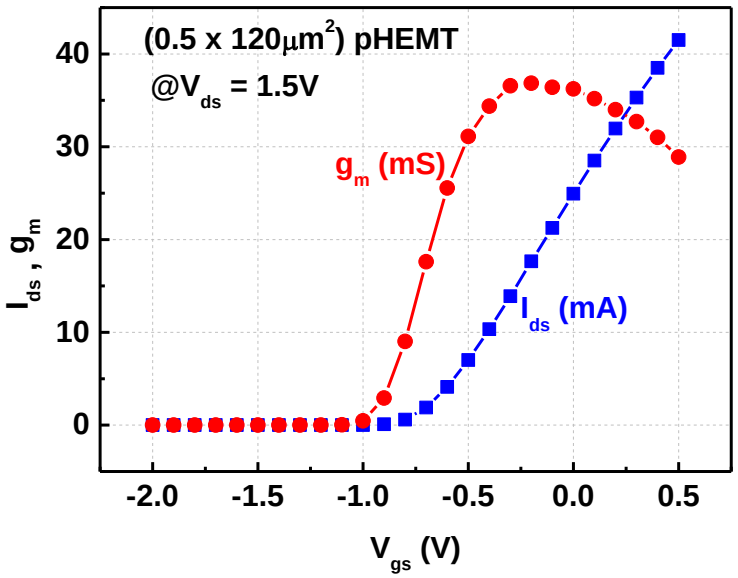


Figure 5.51: Measured transfer characteristics of the fabricated two-gate fingered (0.5 x 120 μm^2) pHEMT.

The highest transconductance peak for the (0.5 x 120 μm^2) pHEMT is found to be 37 mS at V_{gs} = - 0.2 V and V_{ds} = 1.5 V. At these bias-operating conditions, the drain source current I_{ds} is found to be 18 mA.

5.2.5 RF Parameter Extraction Procedure

Small-signal equivalent circuit model parameters are vital for characterising and analysing device performance. The development of a small-signal model is normally started off by carrying out both DC and RF S-parameter measurements, the data from which are then used in a procedure called 'parameter extraction'.

In this section the step-by-step procedure for direct small-signal parameter extraction for a pHEMT device is presented. In order to make this technique work, DC and RF measurements are taken at different biasing conditions. The cold (pinch-off) bias is required, in order to determine the extrinsic parameters, and Agilent's Integrated Circuit Characterisation and Analysis Program (IC-CAP) is used to perform the extraction. An equivalent circuit pi-model, like the one shown in Figure 5.52, is adopted as the small-signal model for the pHEMT device. The equivalent circuit is divided into two parts, namely the intrinsic and the extrinsic parts.

- The intrinsic elements g_m, g_d, C_{gs}, C_{gd}, C_{ds}, R_i and τ are bias-dependent elements.
- The extrinsic elements L_g, R_g, C_{pg}, L_s, R_s, R_d, C_{pd} and L_d are independent of the biasing condition.

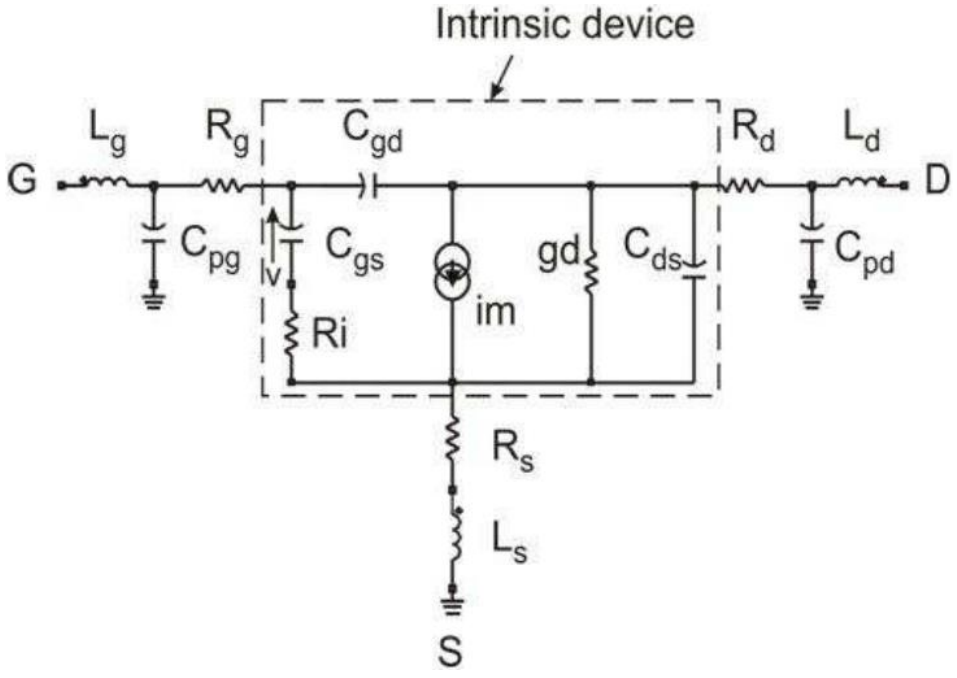


Figure 5.52: Small-signal equivalent circuit of a pHEMT in a common source configuration [53].

5.2.5.1 Cold Bias Extraction

Two different operating bias conditions are needed in order to extract the extrinsic parameters shown in Figure 5.53, and these are off-state (V_{ds} = 0 and V_g = 0) and use on-wafer measurements. The S-parameters are then converted to Z-parameters. The flow chart in Figure 5.53 shows the steps followed to extract the corresponding extrinsic values.

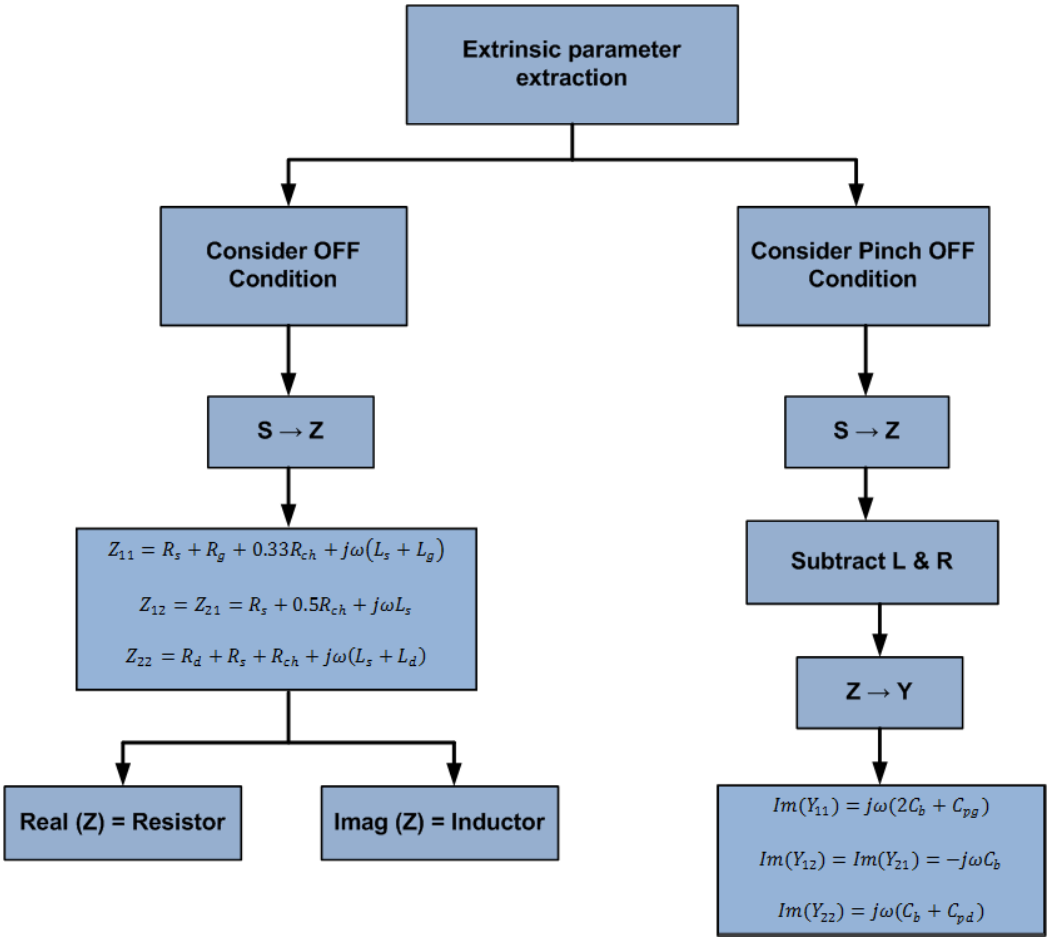


Figure 5.53: Flow chart for determining pHEMT extrinsic parameters.

The following expressions are for Z-parameters at off-state:

$$Z_{11} = R_s + R_g + 0.33R_{ch} + j\omega(L_s + L_g) \tag{5.1}$$

$$Z_{12} = Z_{21} = R_s + 0.5R_{ch} + j\omega L_s \tag{5.2}$$

$$Z_{22} = R_d + R_s + R_{ch} + j\omega(L_s + L_d) \tag{5.3}$$

where R_{ch} is channel resistance under the gate when V_g = 0V and V_{ds} = 0V. The parasitic inductances L_s, L_d and L_g are computed using the imaginary parts of equations (5.1), (5.2) and (5.3).

$$Im(Z_{12}) = j\omega L_s \rightarrow L_s = \frac{Im(Z_{12})}{\omega} \tag{5.4}$$

$$Im(Z_{22}) = j\omega(L_s + L_d) \rightarrow L_d = \frac{Im(Z_{22})}{\omega} - L_s \tag{5.5}$$

$$Im(Z_{11}) = j\omega(L_s + L_g) \rightarrow L_g = \frac{Im(Z_{11})}{\omega} - L_s \tag{5.6}$$

The parasitic resistances R_s, R_d and R_g can be extracted from the real parts of equations (5.1) – (5.3). An additional expression is required, since there are four unknowns with only three equations for the resistance extraction. This equation is derived by biasing the pHEMT under a strong pinch-off condition (V_{ds} = 0 and V_g is much lower than pinch-off voltage V_{po}) and measuring the S-parameters. The measured S-parameters are then converted to Z-parameters to give the fourth equation as:

$$Re\left[Z_{11(V_{po})}\right] = R_s + R_g \tag{5.7}$$

Thus, the four parasitic resistances can be extracted using equations (5.1) – (5.3) and (5.7), and they are calculated as:

$$Re\left[Z_{11(V_{po})}\right] = R_s + R_g \; and \; Re[Z_{11}] = R_s + R_g + 0.33R_{ch} \tag{5.8}$$

$$R_{ch} = 3 \times \left\{Re[Z_{11}] - Re\left[Z_{11(V_{po})}\right]\right\} \tag{5.9}$$

$$Re[Z_{12}] = 0.5R_{ch} + R_s \rightarrow R_s = Re[Z_{12}] - 0.5R_{ch} \tag{5.10}$$

$$R_g = Re[Z_{11}] - R_s - 0.33R_{ch} \tag{5.11}$$

$$R_d = Re[Z_{22}] - R_s - R_{ch} \tag{5.12}$$

For the parasitic capacitances C_{pg}, C_{pd} and C_b, the measured S-parameters of pHEMT under a strong pinch-off condition are converted to the respective Z-parameters. According to the topology of the equivalent circuit model, the inductances and resistances computed in the previous section are subtracted to eliminate their effect:

$$Z_{11} - R_s - R_g - j\omega(L_s + L_g) \tag{5.13}$$

$$Z_{12} - R_s - j\omega L_s \; or \; Z_{21} - R_s - j\omega L_s \tag{5.14}$$

$$Z_{22} - R_d - R_s - j\omega(L_s + L_g) \tag{5.15}$$

The resultant Z-parameters are transformed to the respective Y-parameters, which can be expressed as:

$$Y_{11} = j\omega(2C_b + C_{pg}) \tag{5.16}$$

$$Y_{12} = Y_{21} = j\omega C_b \tag{5.17}$$

$$Y_{22} = j\omega(2C_b + C_{pd}) \tag{5.18}$$

The capacitances are then extracted using equations (5.16) – (5.18) as:

$$C_b = \frac{Im(Y_{12})}{\omega} \tag{5.19}$$

$$C_{pg} = \frac{Im(Y_{11})}{\omega} - 2C_b \tag{5.20}$$

$$C_{pd} = \frac{Im(Y_{22})}{\omega} - C_b \tag{5.21}$$

Using the above equations, the extrinsic parameters of a pHEMT can be calculated. The results are listed in Table 5.3, for the (0.5×200 μm^2) pHEMT, and Table 5.4, for the (0.5×120 μm^2) pHEMT.

5.2.5.2 Hot Bias Extraction

The intrinsic elements g_m, g_d, C_{gs}, C_{gd}, C_{ds}, R_i and τ are bias-dependent elements and therefore need to be extracted in hot (non-zero) biasing conditions. A flowchart for the extraction of the intrinsic parameters is presented in Figure 5.54.

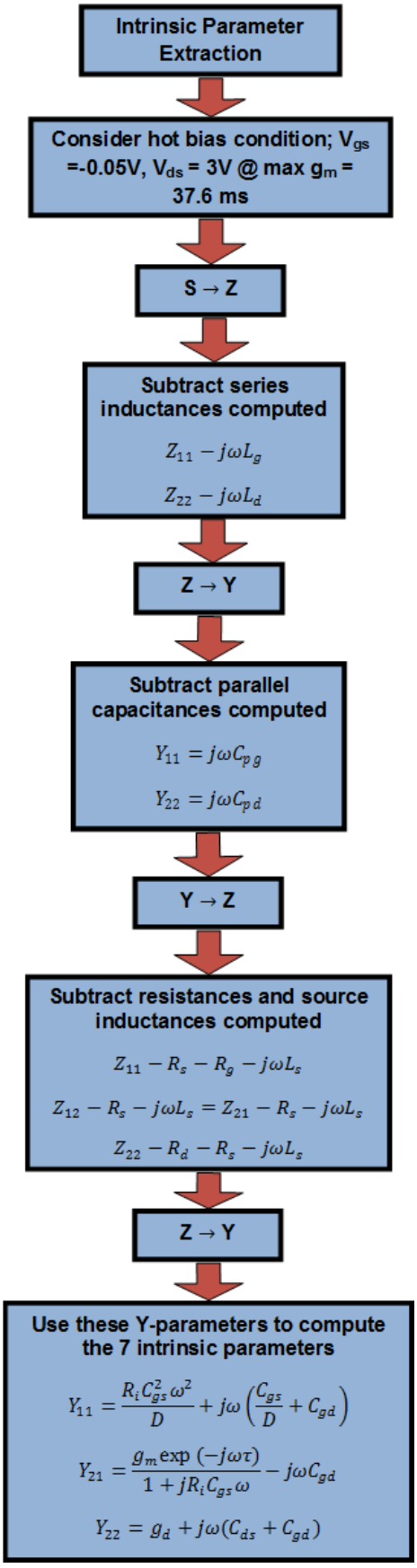


Figure 5.54: Flowchart for the intrinsic parameter extraction of the pHEMT.

During 'hot' measurements V_{gs} = -0.2V, V_{ds} = 3V, I_{ds} = 32mA, g_m = 66mS are chosen for a (0.5×200 μm^2) pHEMT. To determine the intrinsic parameters, the computed extrinsic parameters are first de-embedded or removed from the S-parameters measured under 'hot' biasing conditions. This is performed by the following:

1. Transform the S-parameters of the chosen bias point into Z-parameters. From the Z-parameters subtract the gate and the drain parasitic series inductances computed from extrinsic extractions.

$$Z_{11} - j\omega L_g \tag{5.22}$$

$$Z_{22} - j\omega L_d \tag{5.23}$$

2. The resulting Z-parameters are then converted to Y-parameters and then the effects of the two parasitic capacitances are eliminated:

$$Y_{11} - j\omega C_{pg} \tag{5.24}$$

$$Y_{22} - j\omega C_{pd} \tag{5.25}$$

3. The resulting Y-parameters are then converted back to Z-parameters and the series resistances and source inductances are subtracted, thus completing the de-embedding process. As we can observe, we are moving from the outer side of the device towards the intrinsic part of the device by eliminating all the extrinsic element effects.

$$Z_{11} - R_s - R_g - j\omega L_s \tag{5.26}$$

$$Z_{12} - R_s - j\omega L_s = Z_{21} - R_s - j\omega L_s \tag{5.27}$$

$$Z_{22} - R_s - R_d - j\omega L_s \tag{5.28}$$

4. The obtained Z-parameters are then converted to Y-parameters, which are now ideal for intrinsic parameter extraction. The intrinsic parameters are determined through the following equations:

$$C_{gd} = -\frac{Im(Y_{12})}{\omega} \tag{5.29}$$

$$C_{gs} = \frac{[Im(Y_{11}) - \omega C_{gd}]}{\omega}\left[1 + \frac{Re^2(Y_{11})}{[Im(Y_{11} - \omega C_{gd})]^2}\right] \tag{5.30}$$

$$g_{ds} = Re(Y_{22}) \tag{5.31}$$

$$C_{ds} = \frac{Im(Y_{22}) - \omega C_{gd}}{\omega} \tag{5.32}$$

$$R_i = \frac{Re(Y_{11})}{Re^2(Y_{11})+\left[Im(Y_{11})-\omega C_{gd}\right]^2} \tag{5.33}$$

$$\tau = \frac{1}{\omega} arcsin\left[\frac{-Im(Y_{21})-\omega C_{gd}-\omega C_{gs}R_i Re(Y_{21})}{g_m}\right] \tag{5.34}$$

$$g_m = \left[\left[Im(Y_{21}) + \omega C_{gd}\right]^2 + Re^2(Y_{21})\right]^{1/2}\left(1 + \omega^2 R_i^2 C_{gs}^2\right)^{1/2} \tag{5.35}$$

The Y-parameter equations for the intrinsic parameters are inputted into ADS momentum software to obtain the values of these parameters.

Table 5.3: Extracted small-signal parameters for the multilayer (0.5x200μm^2) pHEMT.

Device Parameter (V_{ds} = 3V, V_{gs} = -0.2V)	**Value**	**Description**
L_s (pH)	1.03	Source inductance
L_d (pH)	82.1	Drain inductance
L_g(pH)	144.6	Gate inductance
R_{ch} (Ω)	2.2	Channel resistance
R_s (Ω)	3.8	Source resistance
R_g (Ω)	1.0	Gate resistance
R_d (Ω)	6.5	Drain resistance
R_{ds} (Ω)	584.8	Output resistance
R_i (Ω)	1.2	Input resistance
C_{pg} (fF)	25.1	Parasitic gate capacitance
C_{pd} (fF)	69.3	Parasitic drain capacitance
C_{gd} (fF)	25.6	Gate-drain capacitance
C_{ds} (fF)	91.4	Drain-source capacitance
C_{gs} (fF)	372.2	Gate-source capacitance
G_m (mS)	71.4	Intrinsic transconductance
τ (pS)	2.2	Signal delay

5.2.5.3 RF Small-Signal Characterisation for a (0.5 x 200 μm^2) pHEMT

In this section the RF S-parameters results are shown and discussed. A comparison between the virgin and multilayer pHEMTs is also shown in Figures 5.55 – 5.58. These results are the average of four pHEMTs measured from the mask sample Ver.5.

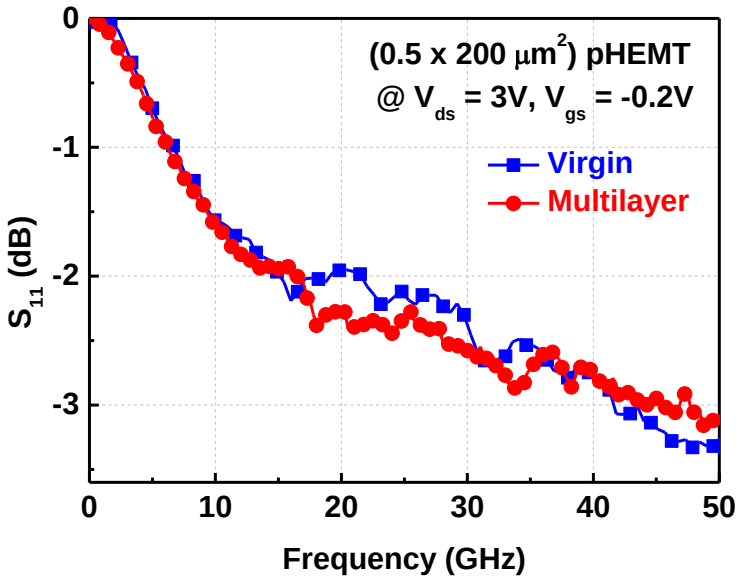


Figure 5.55: S_{11} parameter comparison between a virgin and a multilayer (0.5×200 μm^2) pHEMT.

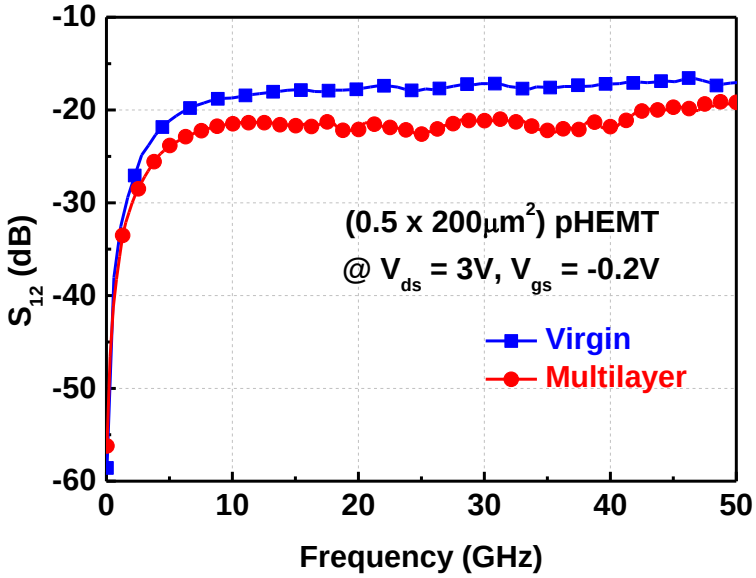


Figure 5.56: S_{12} parameter comparison between a virgin and a multilayer (0.5×200 μm^2) pHEMT.

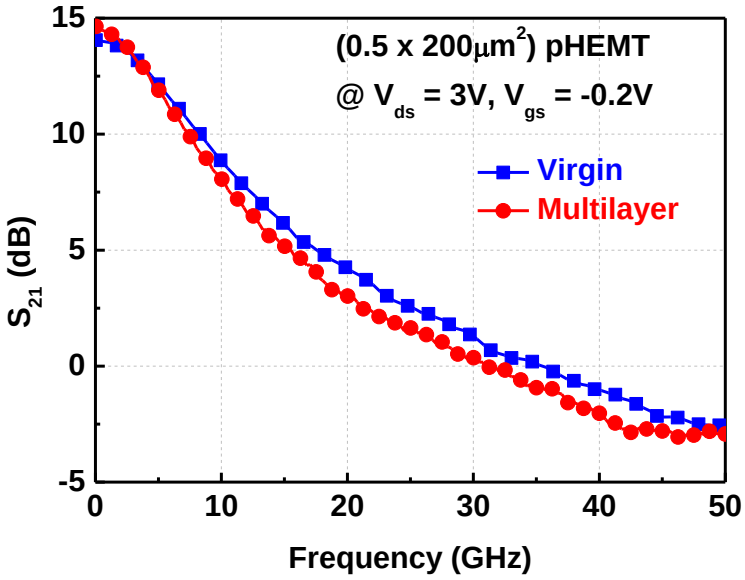


Figure 5.57: S_{21} parameter comparison between a virgin and a multilayer (0.5×200 μm^2) pHEMT.

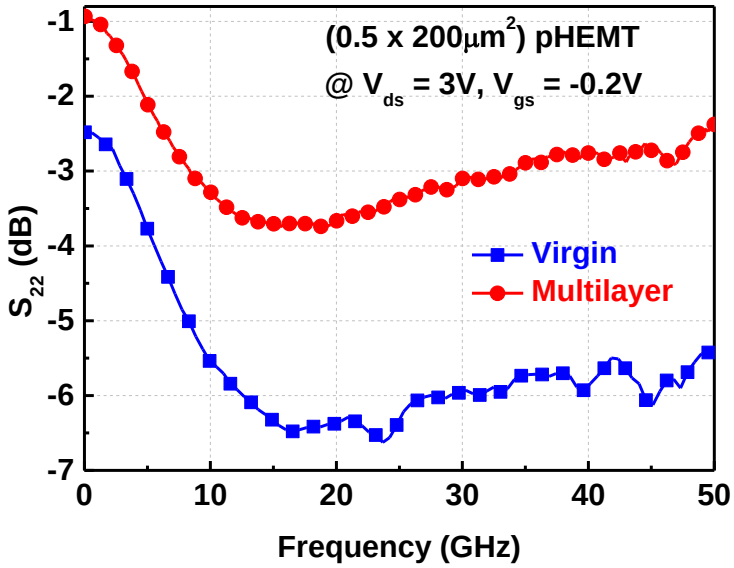


Figure 5.58: S_{22} parameter comparison between a virgin and a multilayer (0.5×200 μm^2) pHEMT.

After extracting all of the small-signal parameters, the next step is to determine the f_t and f_{max} of the pHEMT from both the measured and simulated results, which gives the figure of merit of the pHEMT device. f_t is the transition frequency of the device, where the current gain of the device is equal to unity and f_{max} is the frequency where the device's MAG or unilateral gain is equal to zero. From Figure 5.58 it is evident that there is a large difference between the measured and simulated S_{22} because of its high sensitivity compared to the other S-parameters.

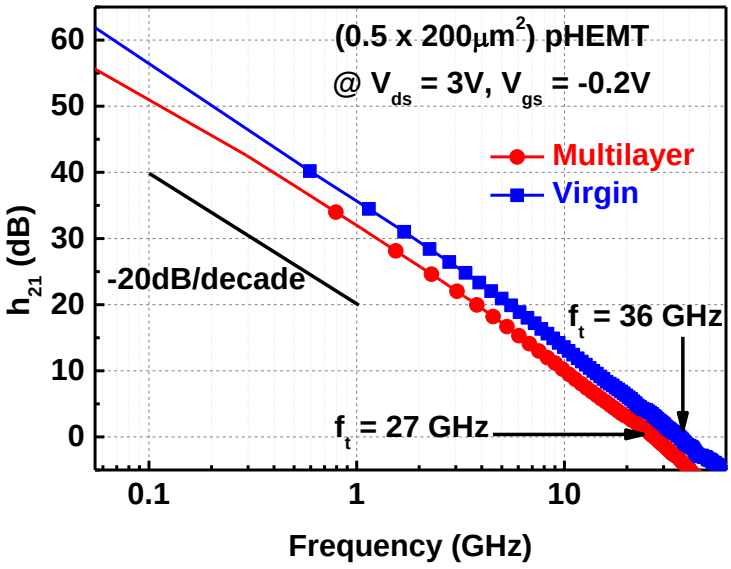


Figure 5.59: Comparison of h_{21} parameters for a virgin and a multilayer (0.5×200 μm^2) pHEMT.

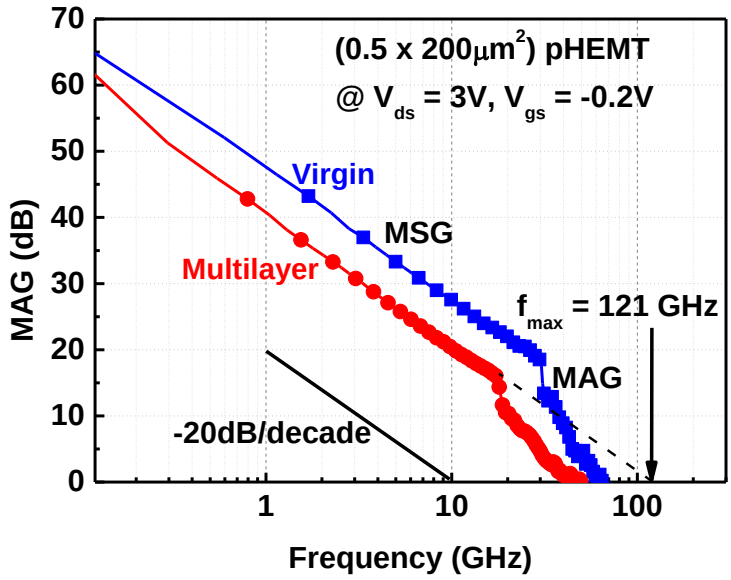


Figure 5.60: Comparison of MAG for a virgin and a multilayer (0.5×200 μm^2) pHEMT.

Using Figure 5.59 we read off f_t for the virgin pHEMT as 35.8 GHz, and f_t for the multilayer pHEMT as 27 GHz. The transition frequency, f_t, is the frequency at which h_{21} (current gain) reaches zero. The transition frequency can also be estimated using an analytical formula, which is given as:

$$f_t = \frac{G_m}{2\pi(C_{gs}+C_{gd})} \tag{5.36}$$

From the multilayer pHEMT, extracted parameters from Table 5.3 are:

G_m = 71.4 mS, C_{gs} = 372.2 fF and C_{gd} = 25.6 fF.

Substituting the values in the f_t equation 4.36, we get f_t = 28.6 GHz.

Maximum available gain (MAG) can be estimated using the following relation:

$$MAG = 10 \times log \frac{|S_{21}|}{|S_{12}|} + 10 \times log\left|K \pm \sqrt{K^2 - 1}\right| \tag{4.37}$$

where

$$K = \frac{1+|D_s|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|} \tag{4.38}$$

$$D_s = S_{11}S_{22} - S_{12}S_{21} \tag{4.39}$$

and the maximum stable gain (MSG) is given by $\frac{|S_{21}|}{|S_{12}|}$.

The analytical formula for f_{max} is given as:

$$f_{max} = \frac{f_t}{2\sqrt{r_1+f_t\tau}} \tag{4.40}$$

where

$$r_1 = \frac{R_g+R_i+R_s}{R_{ds}} \tag{4.41}$$

$$\tau = 2\pi R_g C_{gd} \tag{4.42}$$

From the multilayer pHEMT, extracted parameters from Table 5.3 are:

R_g = 1Ω, R_i = 1.2 Ω, R_s = 3.8Ω, R_{ds} = 584.8 Ω, C_{gd} = 25.6fF

f_t = 28.6 GHz (obtained using the analytical method)

Therefore, f_{max} is obtained as 118.3 GHz

The calculated transition frequency f_t and maximum oscillation frequency f_{max} are both almost identical to the modelled ones obtained from Figures 5.59 and 5.60. The modelled f_t and f_{max} are 27 GHz and 121 GHz, respectively.

5.2.5.4 RF Characterisation for a (0.5 x 120 µm^2) pHEMT

In this section the RF characterisation for a (0.5 x 120 µm^2) pHEMT is presented. The S-parameters of the fabricated pHEMT were measured using Agilent HP8510C VNA and Keithley DC source. The on-wafer measurements were carried out within the frequency range 45 MHz to 50 GHz at a DC bias of V_{ds} = 1.5 V and V_{gs} = - 0.2 V. The small-signal parameter extraction procedure for this pHEMT is similar to the one described in subchapter 5.2.5. The small-signal extracted parameters are tabulated in Table 5.4, and the equivalent circuit is provided in Figure 5.61. The TOM3 equivalent circuit model is also provided in Figure 5.62. The measured TOM3 model and small-signal S-parameter results are compared in Figures 5.63 – 5.66. Furthermore, both the current gain (h_{21}) and the maximum available gain (MAG) are extracted, and their results are compared as illustrated in Figures 5.67 and 5.68.

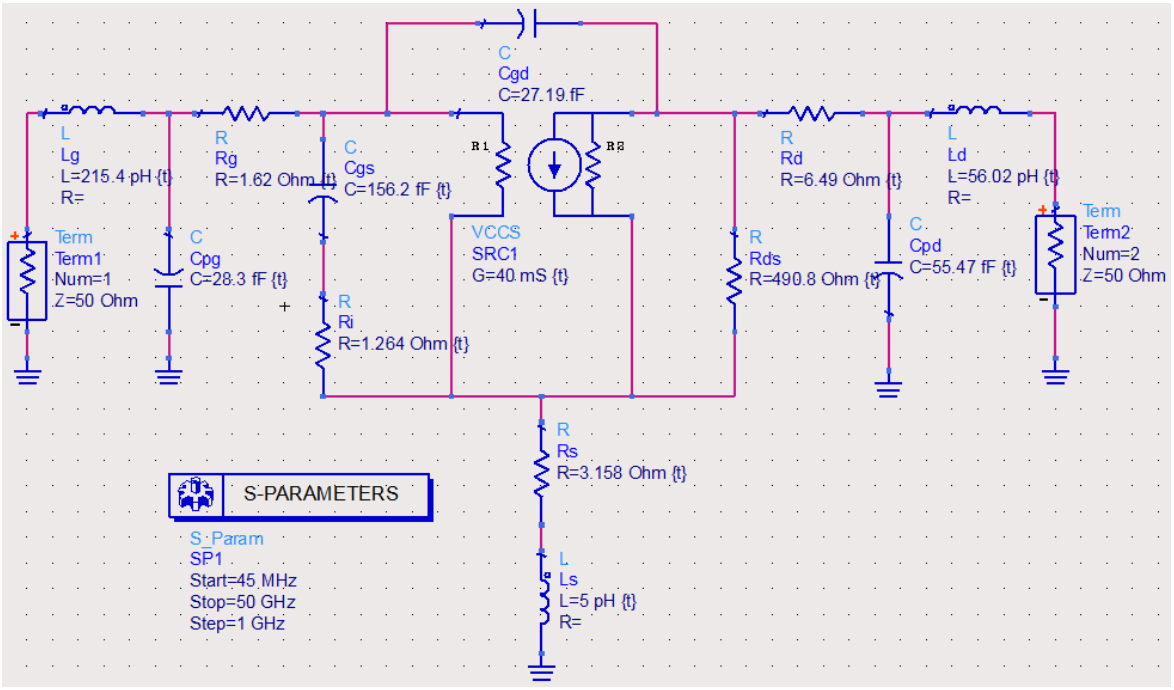


Figure 5.61: Schematic model of the small-signal pi circuit for the fabricated (0.5 x 120 µm^2) GaAs pHEMT.

Table 5.4: Extracted small-signal parameters for the fabricated (0.5 x 120 µm^2) GaAs pHEMT.

Device Parameter (V_{ds} = 1.5V, V_{gs} = -0.2V)	Value	Description
L_s (pH)	5.96	Source inductance
L_d (pH)	56.02	Drain inductance
L_g(pH)	215.4	Gate inductance
R_s (Ω)	3.16	Source resistance
R_g (Ω)	1.62	Gate resistance
R_d (Ω)	6.49	Drain resistance
R_{ds} (Ω)	490.8	Output resistance
R_i (Ω)	1.26	Intrinsic resistance
C_{pg} (fF)	28.3	Parasitic gate capacitance
C_{pd} (fF)	55.47	Parasitic drain capacitance
C_{gd} (fF)	27.19	Gate-drain capacitance
C_{gs} (fF)	156.2	Gate-source capacitance
G_m (mS)	40	Intrinsic transconductance
τ (pS)	0.8	Signal delay

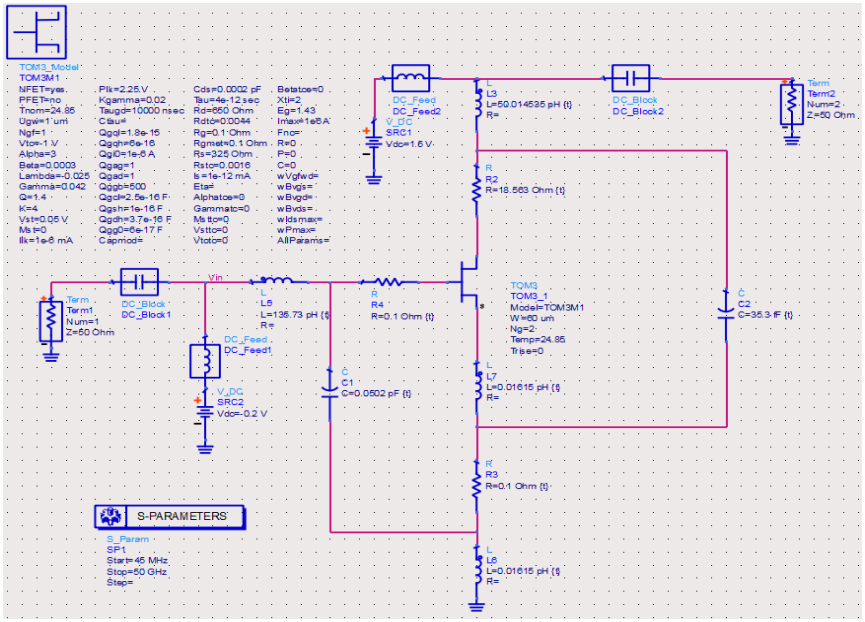


Figure 5.62: Schematic equivalent circuit of the TOM3 large-signal model for the (0.5 x 120 µm^2) GaAs pHEMT.

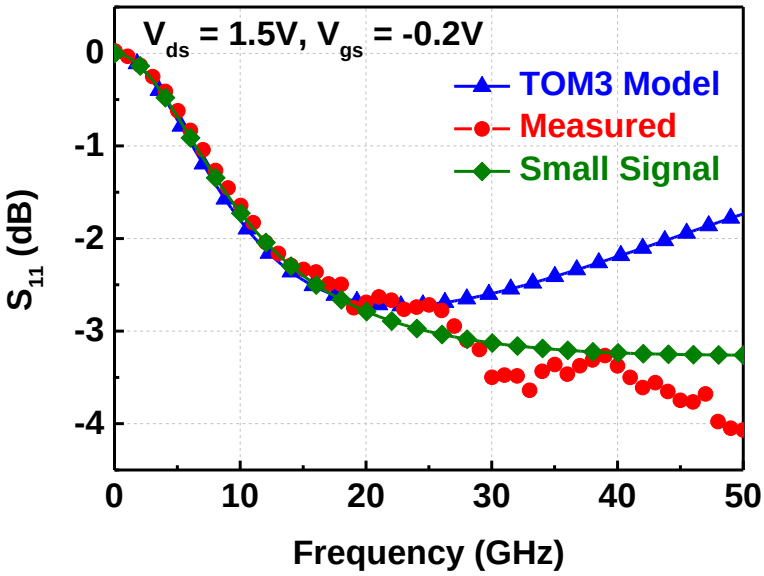


Figure 5.63: Comparison of S_{11} parameters between the TOM3 large-signal model, small-signal model and the measured (0.5 x 120 µm^2) GaAs pHEMT.

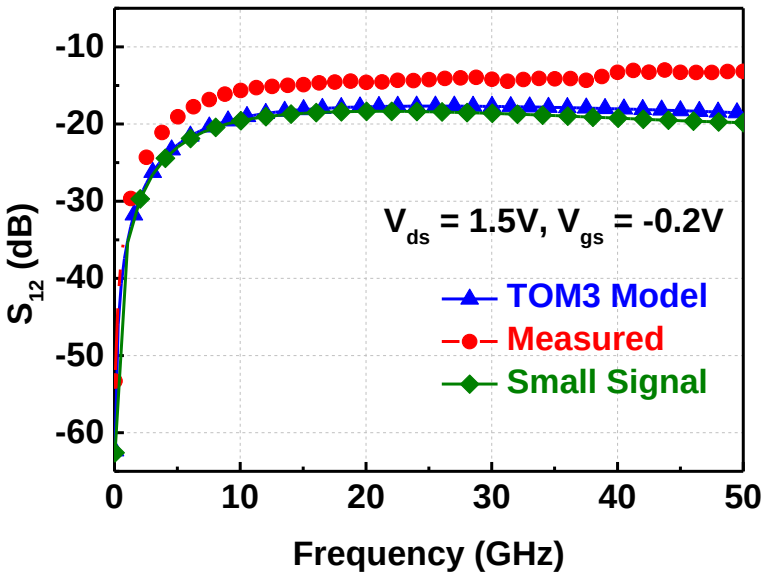


Figure 5.64: Comparison of S_{12} parameters between the TOM3 large-signal model, small-signal model and the measured (0.5 x 120 µm^2) GaAs pHEMT.

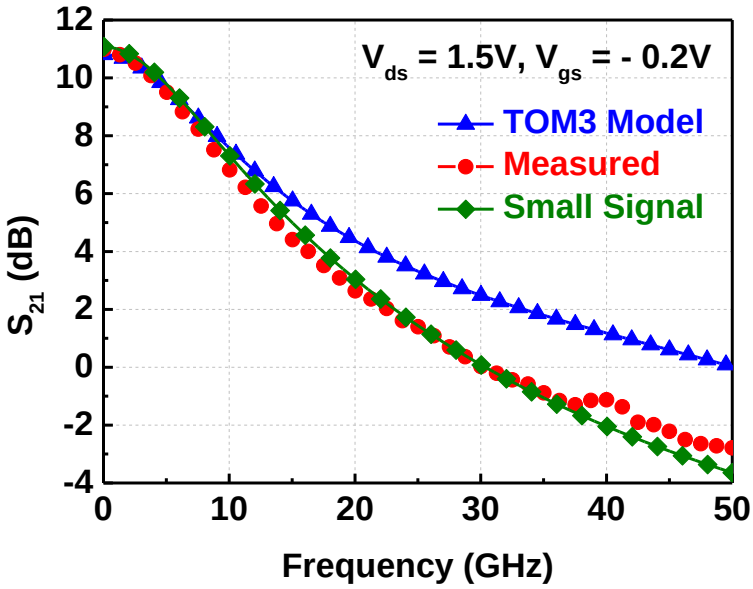


Figure 5.65: Comparison of S_{21} parameters between the TOM3 large-signal model, small-signal model and the measured (0.5 x 120 µm^2) GaAs pHEMT.

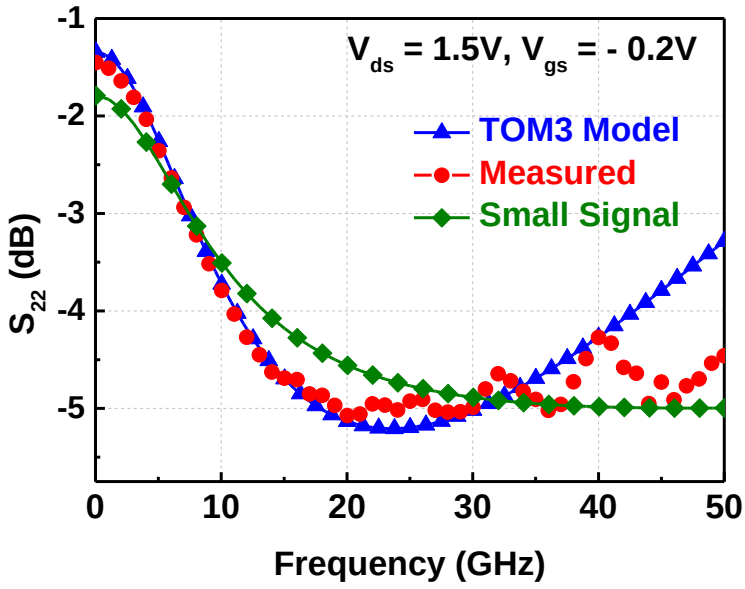


Figure 5.66: Comparison of S_{22} parameters between the TOM3 large-signal model, small-signal model and the measured (0.5 x 120 µm^2) GaAs pHEMT.

Both the TOM3 large-signal and small-signal models show good agreement with the measured S-parameter results in the frequency range 45 MHz to 25 GHz, as observed in Figures 5.63 – 5.66. A difference in the S-parameter results of the TOM3 model with the measured and small-signal model after about 25 GHz is also observed. This is mainly due

to the very ideal nature of the TOM3 model block from Filtronic [60, 88]. Hence the TOM3 model block doesn't have the input and output parasitic components which are added on the small-signal model and parasitics introduced by the probing pads during the measurements. Furthermore, the small-signal extraction and computation processes allow one to understand the intrinsic and extrinsic parameters of the pHEMT, before it is used in any amplification application.

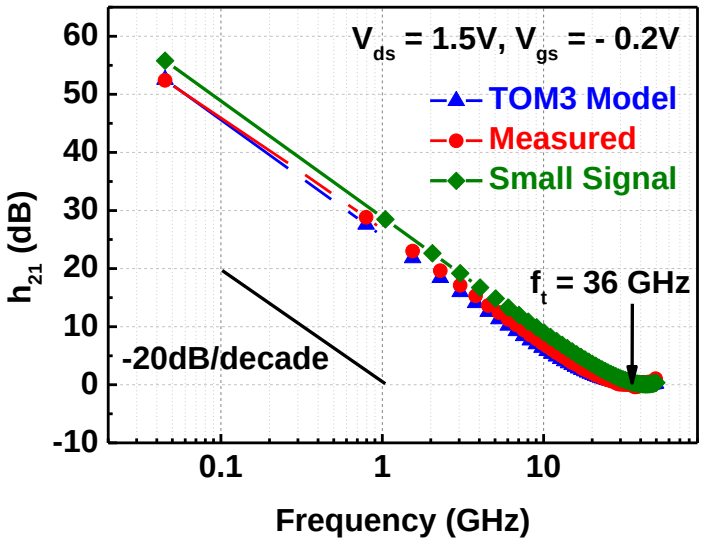


Figure 5.67: Comparison of current gain, h_{21} between the TOM3 large-signal model, small-signal model and the measured (0.5 x 120 µm^2) GaAs pHEMT.

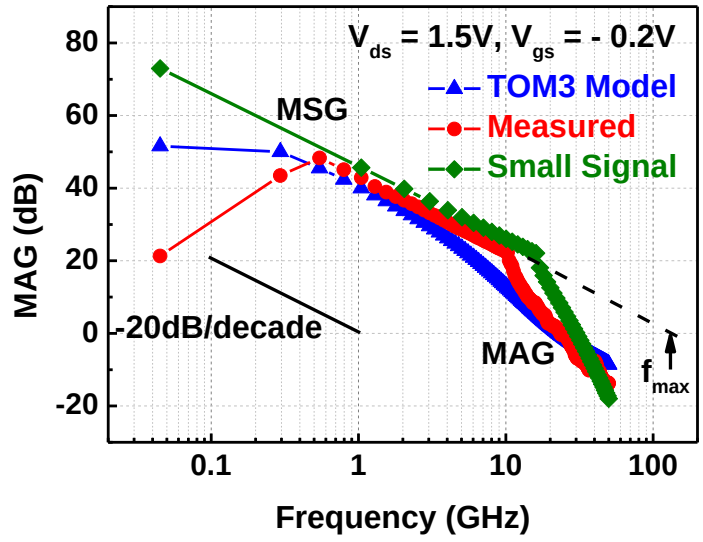


Figure 5.68: Comparison of maximum available gain, MAG between the TOM3 large-signal model, small-signal model and the measured (0.5 x 120 µm^2) GaAs pHEMT.

The cut-off frequency, f_t, is computed using the analytical formula [55]:

$$f_t = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{5.43}$$

Using the tabled data in Table 5.4, g_m = 40 mS, C_{gd} = 27.19 fF and C_{gs} = 156.2 fF. Therefore, substituting these values into expression 5.43 gives f_t as 34.7 GHz, which is approximately similar to the extrapolated value in Figure 5.67.

The maximum available gain, MAG, is estimated using the analytical formulae [46]

$$f_{max} = \frac{f_t}{2\sqrt{r_1+f_t\tau}} \tag{4.44}$$

where $r_1 = \frac{R_g+R_i+R_s}{R_2}$ and $\tau = 2\pi R_g C_{gd}$

Using the tabled data in Table 5.4, R_g = 1.62 Ω, R_i = 1.26 Ω, R_s = 3.16 Ω, R_2 = 490.8 Ω and C_{gd} = 27.19 fF. Therefore, substituting these values into the above expressions gives f_{max} as 117 GHz. The computed value of f_{max} is found to be similar that of the extrapolated parameter in Figure 5.68.

The TOM3 model shows very good agreement with the measured data, and these results validate the accuracy of both the small-signal and TOM3 models for further circuitry modelling, which includes limiters or a low-noise amplifier.

5.2.6 pHEMT DIODES

In this work, Schottky diodes are designed and fabricated using existing fabricated pHEMT structures for RF power detection. To design the two-pin network of a diode, the drain and source of the pHEMT are connected together to form the output port (ohmic contact) while the gate is the input port (Schottky contact) as shown in Figure 5.69. The diodes are fabricated on a 600µm-thick semi-insulating GaAs substrate using three metal layers and two dielectric layers sandwiched in between the metal layers. The metal layers are made up of Ti/Au, and each has a thickness of about 0.8µm (the Ti is a very thin layer of about 10nm). The fabrication uses the same process during pHEMT fabrication. The fabricated pHEMT diodes are shown in Figure 5.70. Although the pHEMT diodes are included in this chapter, it is to be noted that they are strictly passive components and cannot convert dc power into RF power [36].

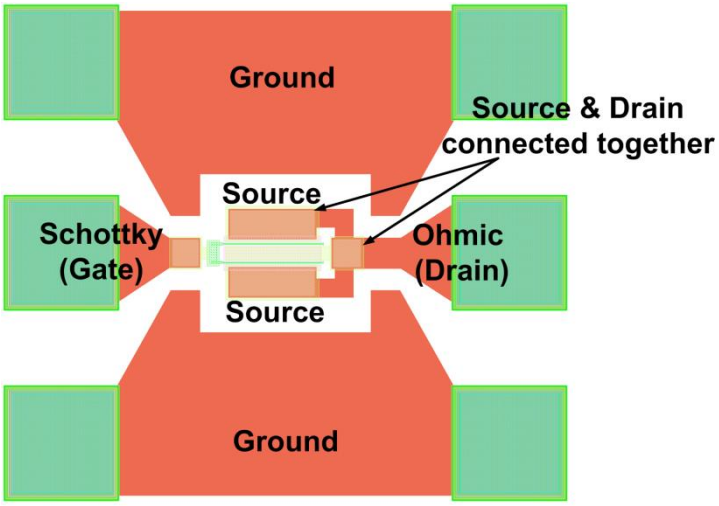


Figure 5.69: Layout of a multilayer pHEMT diode.

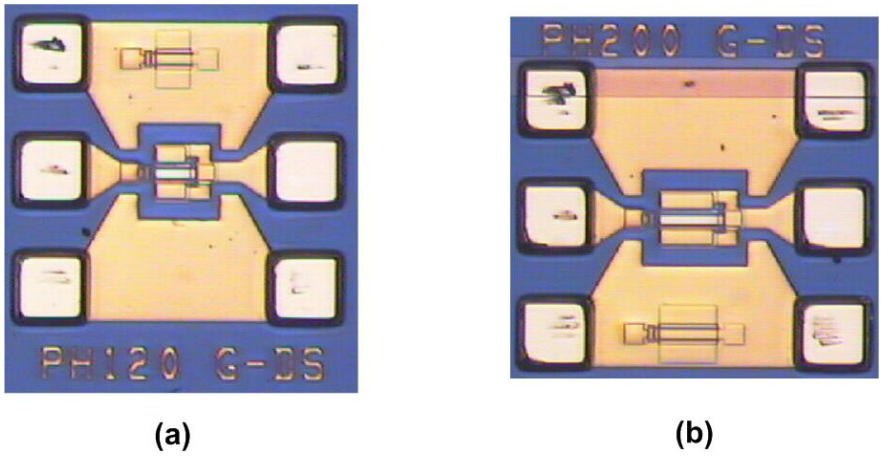


Figure 5.70: Micrograph of fabricated pHEMT diodes; (a) 0.5 µm x (2x60) µm diode. (b) 0.5 µm x (2x100) µm diode.

The pHEMT diode utilises a Schottky contact along the edge of a two-dimensional electron gas (2-DEG) structure. This new configuration allows one to combine very low series resistance, due to the excellent transport properties of the electric field varying in two dimensions (2-DEG) compared to the one-dimensional field variation in an abrupt-junction diode. A much higher breakdown voltage caused by the two-dimensional electric field spreading in the depletion region can be achieved [89]. The 2-DEG layer that makes up the pHEMT diode also provides higher electron mobility [90].

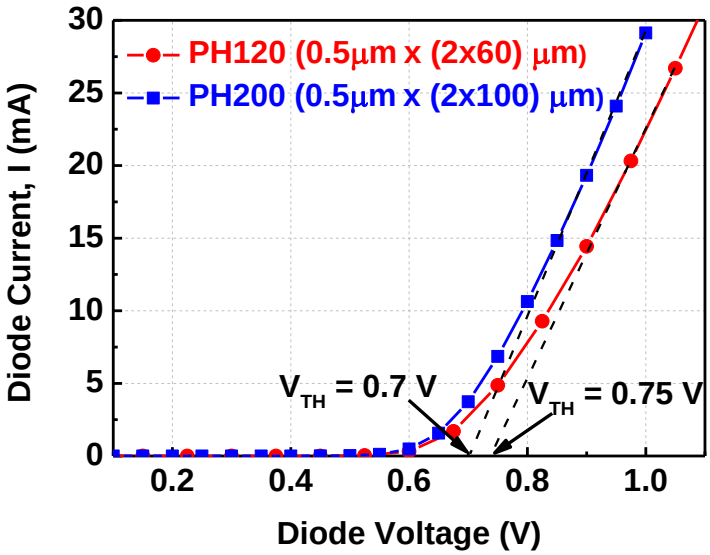


Figure 5.71: Measured I-V characteristics of the pHEMT diodes.

The threshold voltages, V_{TH} (turn-on voltages), of the PH120 and PH200 are estimated to be 0.75V and 0.7V, respectively. The PH200 diode with a wider gate width has more current passing through it compared to the PH120 diode when switched on. This is mainly due the larger Schottky contact area of the PH200 diode.

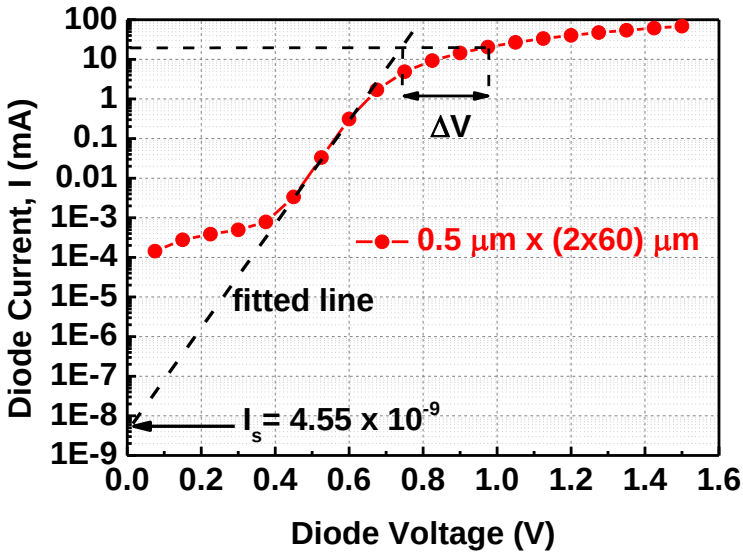


Figure 5.72: Measured I-V characteristics of the 0.5 µm x (2x60) µm PH diode in a semi log scale.

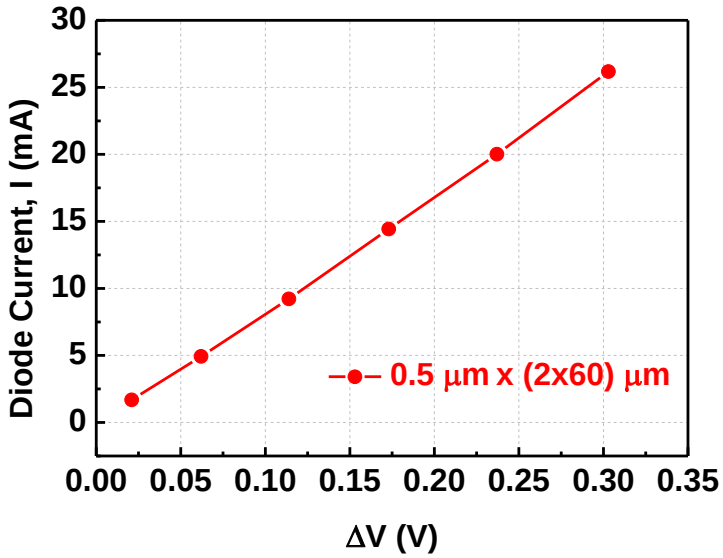


Figure 5.73: Diode current against a change in diode voltage of the 0.5 µm x (2x60) µm PH diode, using data from Figure 4.90.

Figure 5.73 shows a series resistance, $R_{Series} = \frac{\Delta V}{I} = \frac{0.173\ V}{14.429\ mA} = 12\ \Omega$

The ideality factor, η, is derived from equation 2.31:

$$I_d(V_j) = I_S\left(e^{\frac{qV_j}{\eta k_B T}} - 1\right)$$

Therefore, using the value from Figure 4.90, the ideality factor is expressed as;

$$\eta = \frac{q}{k_B \cdot T} \cdot \frac{\Delta V}{\Delta \mathrm{In} I} \cong \frac{\Delta V}{0.05783}$$

since $\frac{k_B \cdot T}{q} \approx 0.025V$ at room temperature and $\Delta V = 0.0714V$.

The ideality factor for the PH120 diode is therefore obtained as $\eta = 1.23$

In Figure 5.72 the saturation current of the PH120 diode is read off as $I_S = 4.55 \times 10^{-9}$ mA. Using the saturation current expression in equation 2.31, we can calculate the barrier height ϕ_b as:

$$I_S = AA^{**}T^2\left(e^{\frac{-q\phi_b}{k_B T}}\right)$$

$$\phi_b = \frac{k_B \cdot T}{q} \times In\left(\frac{A \cdot A^{**} \cdot T^2}{I_S}\right)$$

The barrier height of the PH120 diode is obtained as $\phi_b = 0.648\ eV$.

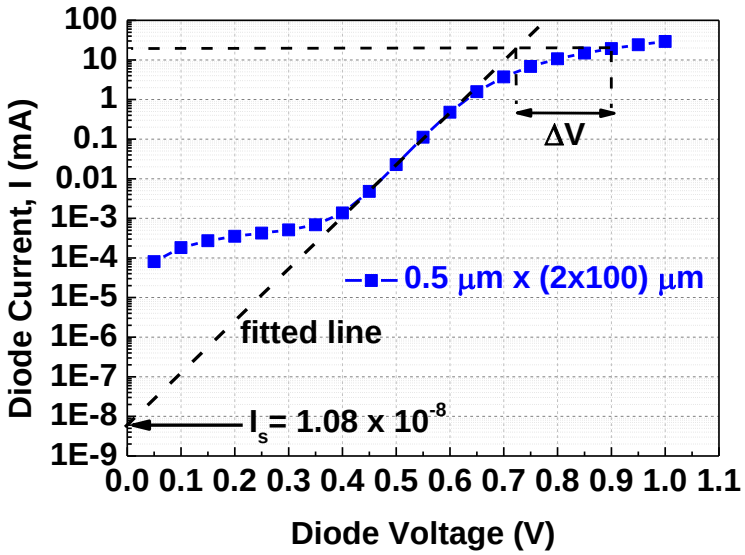


Figure 5.74: Measured I-V characteristics of the 0.5 µm x (2x100) µm PH diode in a semi log scale.

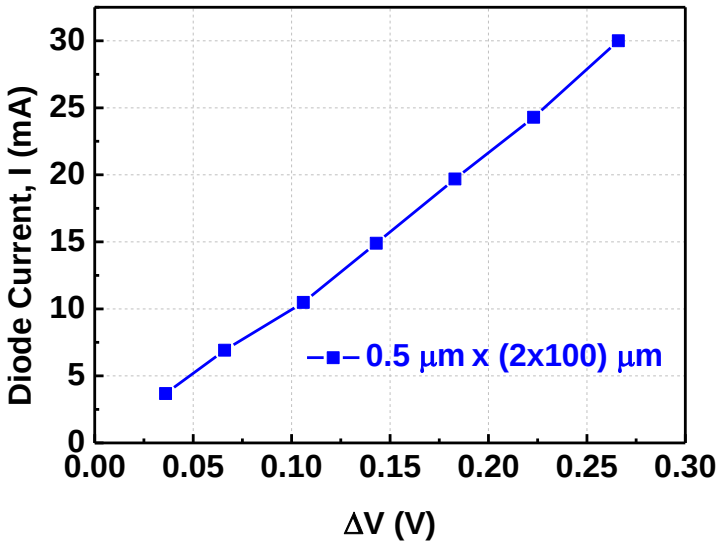


Figure 5.75: Diode current against a change in diode voltage of the 0.5 µm x (2x100) µm PH diode, using data from Figure 4.92.

Figure 5.75 shows a series resistance, $R_{Series} = \frac{\Delta V}{I} = \frac{0.183\ V}{19.685\ mA} = 9.23\ \Omega$

From the results of the series resistances of the two pHEMT diodes, it verifies that the PH200 diode has a lower series resistance (9.23Ω) compared to the PH120 diode with 12Ω allows more current to pass through it because of its wider channel width.

The ideality factor, η of the PH200 diode is derived from equation 2.31. Therefore using the values from Figure 5.74, the ideality factor is expressed as:

$$\eta = \frac{q}{k_B \cdot T} \cdot \frac{\Delta V}{\Delta \ln I} \cong \frac{\Delta V}{0.05783}$$

And where $\Delta V = 0.075V$, the ideality factor for the PH200 diode is therefore obtained as $\eta = 1.29$.

In Figure 5.74 the saturation current of the PH200 diode is read off as I_S = 1.08 x 10^{-8} mA. Using the saturation current expression in equation 2.31, we obtain the barrier height of the PH200 diode as $\phi_b = 0.639\ eV$.

5.2.6.1 C-V Characteristics of the pHEMT Diodes

In this work, the C-V characteristics of the diodes are derived from the DC measurements using an Agilent E4980A precision LCR meter with a frequency range from 20 Hz to 2 MHz.

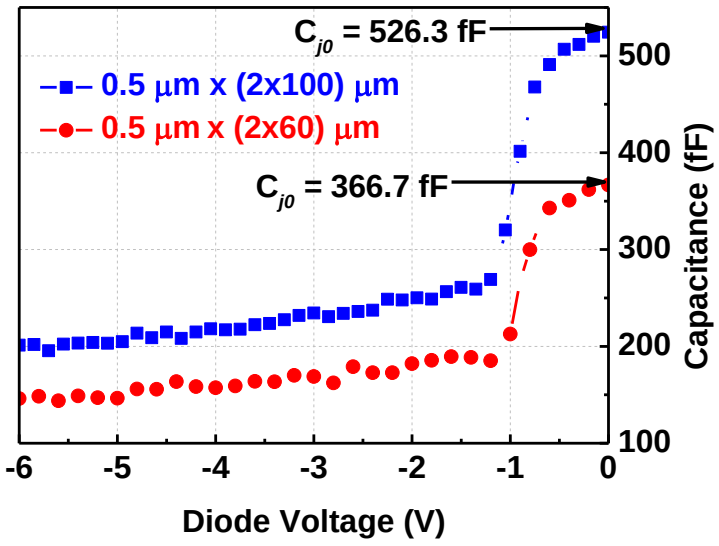


Figure 5.76: Measured C-V characteristics of both 0.5 µm x (2x100) µm and 0.5 µm x (2x60) µm pHEMT diodes.

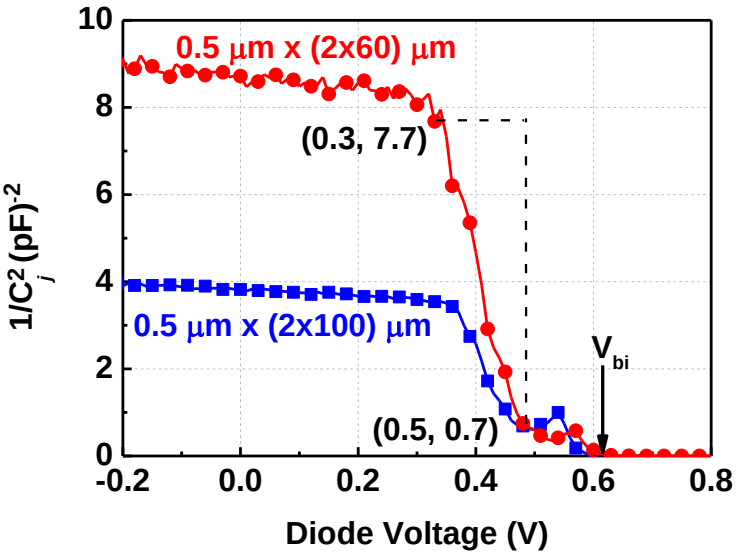


Figure 5.77: Measured C-V characteristics of both 0.5 µm x (2x100) µm and 0.5 µm x (2x60) µm pHEMT diodes showing the built-in voltage.

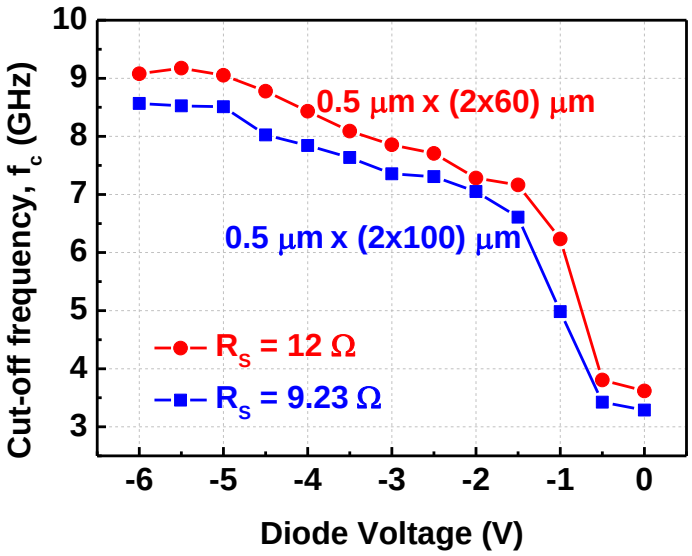


Figure 5.78: Cut-off frequency of both 0.5 µm x (2x100) µm and 0.5 µm x (2x60) µm pHEMT diodes.

With the junction capacitances and the series resistances (R_s), the cut-off frequencies (f_c) of the two pHEMT didoes can be obtained. The diode cut-off frequency is a figure of merit that describes the upper limit of the diode frequency response, and it is given as:

$$f_c = \frac{1}{2\times\pi\times R_S\times C_{j0}} \tag{5.45}$$

where $R_{Series} = 9.23\Omega$ and $C_{j0} = 526.3$ fF.

Therefore, the cut-off frequency of the 0.5 µm x (2x100) µm pHEMT diode is found to be 3.28 GHz.

Cut-off frequency of 0.5 µm x (2x60) µm pHEMT diode

Using equation 5.45, where $R_{Series} = 12\Omega$ and $C_{j0} = 366.7$ fF, the cut-off frequency of the 0.5 µm x (2x60) µm pHEMT diode is found to be 3.62 GHz.

Since the diode cut-off frequency is proportional to $(1/R_S C_{j0})$, we then conclude that the cut-off frequency is also proportional to $(1/A)$, where A is the diode area. The two different diode areas, each giving different capacitances, lead to slightly different cut-frequency values. Using equations 2.33 and 2.34, we can obtain the donor concentration N_d of the pHEMT diodes as

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_s N_d} V_{bi} - \frac{2}{q\varepsilon_s N_d} V_{app}$$

$$N_d = \frac{2}{q\varepsilon_0 \varepsilon_r A^2} \times \left[\frac{-1}{d(1/C^2)/dV}\right]$$

where $d(1/C^2)/dV$ is the slope of the pHEMT diode plot in Figure 5.77 which can be obtained as (-3.5e25), ε_s is the dielectric permittivity and ε_r is the relative permittivity of GaAs (12.9). Therefore, the donor concentration of the pHEMT diodes can be obtained as 8.68 x 10^{17} cm^{-3}. This is rather nearer to the expected doping concentration (n=10^{18} cm^{-3}) for a typical n-AlGaAs supply layer in a pHEMT.

Table 5.5: Summary of parameters from IV and CV pHEMT diodes characteristics.

	Diodes	
Parameter	**0.5 µm x (2x60) µm**	**0.5 µm x (2x100) µm**
V_{TH} (V)	~ 0.75	~ 0.7
R_{Series} (Ω)	12	9.23
C_{j0} (fF)	366.7	536.3
f_c (GHz)	3.62	3.28
I_S (mA)	4.55 x 10^{-9}	1.08 x 10^{-8}
η	1.23	1.29
ϕ_b (V)	0.65	0.64
V_{bi} (V)	0.64	0.61
N_d (cm^{-3})	8.68 x 10^{17}	

Chapter 6 Integration of Multilayer CPW Passive Components with Active Components

As part of the GaAs pHEMT applications and the integration between multilayer passive components with active components, miniaturised multilayer MMIC limiters, pHEMT diodes and a low-noise amplifier have been developed, fabricated and characterised. In subsection 5.2.6 we analysed the fabricated pHEMT diodes which are employed in the modelling of the multilayer MMIC limiters. The final part of this section details how a pHEMT is used to model a miniaturised low-noise amplifier at a specific operating frequency.

6.1 Multilayer MMIC Limiters

In this work, three limiter designs were designed, modelled and fabricated on the same wafer as the other active components on the S.I. GaAs substrate. The three designs are:

- straight (PH200) limiter with two (0.5 x 200 μm^2) pHEMT diodes
- spiral (PH200) limiter with two (0.5 x 200 μm^2) pHEMT diodes
- spiral (PH120) limiter with two (0.5 x 120 μm^2) pHEMT diodes

The multilayer limiter investigation begins with the ideal case, which is shown in Figure 6.2.

6.1.1 Limiter Mode of Operation

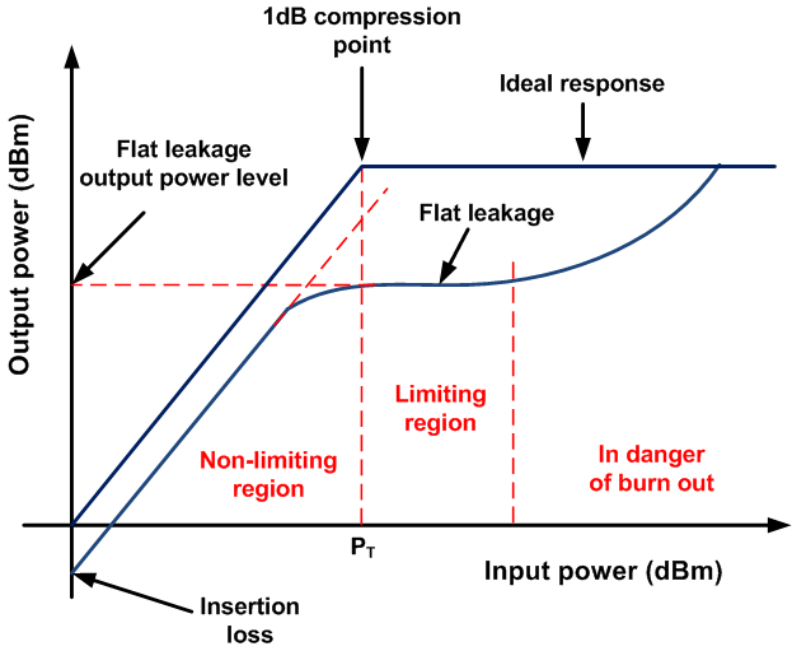


Figure 6.1: Typical output power profile of a microwave power limiter.

When the limiter receives an RF signal of a power level higher than its limiting threshold (P_T), indicated in Figure 6.1, the shunt-mounted pHEMT diode will self-generate a dc current from the incoming signal, lowering its impedance. The circuit acts like a closed switch and the incident power is reflected back. In an ideal response, the transition from high reverse to low forward impedance is not abrupt; however, there is a short finite period required for the limiting action to be activated. The portion of undesirable RF energy that is able to penetrate into the circuit in this short finite period is known as 'spike leakage' [69], and when the limiter is fully operational, the RF energy exceeding the limiting threshold is known as 'flat leakage', which acts as a safety margin for the device connected at the output of the limiter. The incoming power level reaches a point where it no longer exceeds the limiting threshold, and a finite measureable time period elapses during which the limiter returns to a high impedance low loss state – a period known as 'recovery time' [69, 74]. For most limiter applications, assuming the limiter is lossless, the flat leakage level is the same as the power threshold. The attenuation required to provide flat leakage is a straight linear line with a unity gradient.

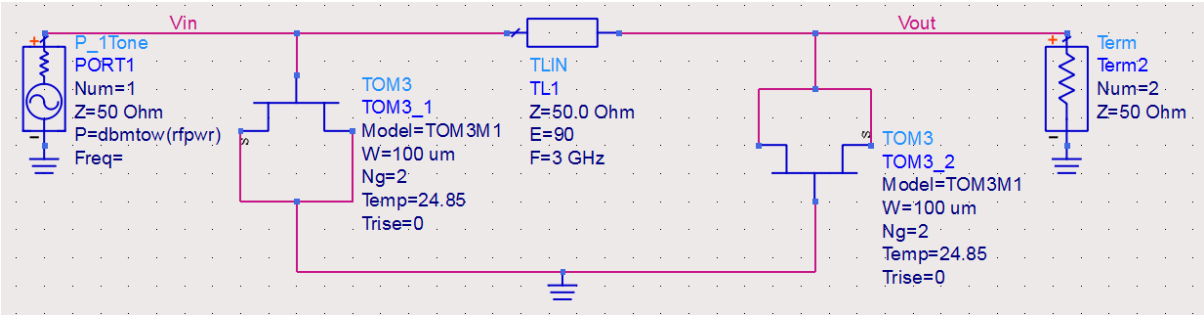


Figure 6.2: Schematic circuit of an ideal limiter.

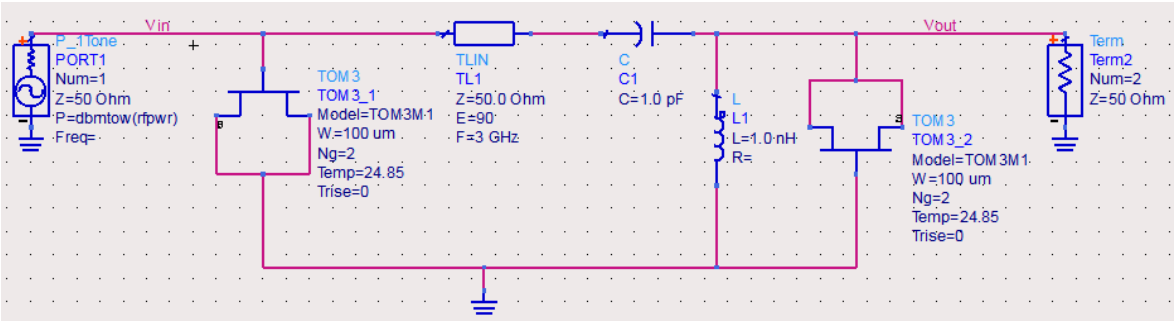


Figure 6.3: Schematic circuit of an ideal limiter with LC components.

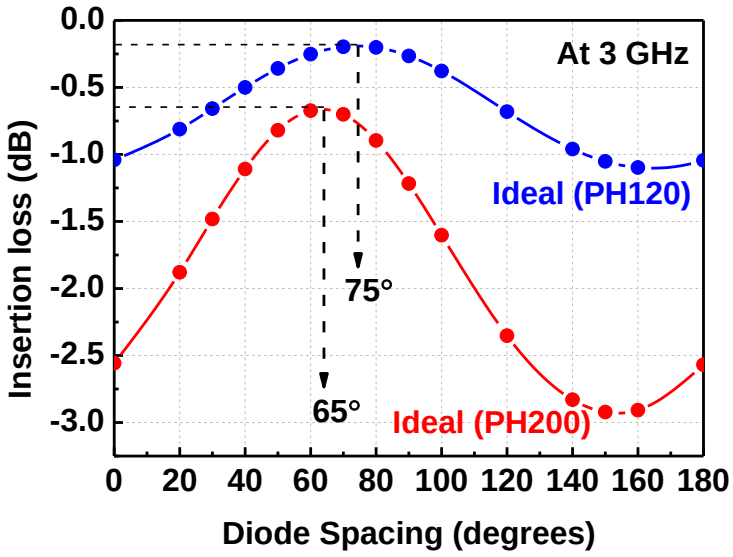


Figure 6.4: Simulated insertion loss of both the ideal (PH200) and (PH120) limiters at 3 GHz.

Since the electrical length or phase length is typically expressed as *N* wavelengths or as the phase φ expressed in degrees or radians, the diode spacing in Figure 6.4 can be converted to physical lengths as follows:

For the ideal (PH120) limiter, φ = 75º

where $\varphi = 360^0 \cdot N$ and $N = L/\lambda$, where L is a distance along the conductor. The wavelength is given by $\lambda = c/f$, where c is the speed of light and f is 3 GHz. Therefore, we obtain the physical diode spacing of the ideal (PH120) as 20mm.

For the ideal (PH200) limiter with φ = 65º, we obtain the physical diode spacing as 18mm.

Table 6.1: Ideal limiter diode spacing at 3 GHz.

Limiter	Insertion loss (dB)	Diode Spacing (degrees)	Diode Spacing (mm)
Ideal (PH120)	-0.2	75	20
Ideal (PH200)	-0.6	65	18

In the layout of the limiter circuit the spacing between the diodes must be carefully considered, because it helps in achieving the lowest insertion loss for the limiter circuit. The diode spacing is also referred to as the 'electrical length', which is the length of a transmission medium expressed as the number of wavelengths of the signal propagating in the medium. It is sometimes expressed in radians or degrees [91].

From Figure 6.4 the ideal (PH120) limiter is observed to have the lowest insertion loss of approximately (- 0.2dB) when the two pHEMT diodes have an electrical length spacing of 75º between each other at 3GHz. The lowest insertion loss of (-0.6dB) for the ideal (PH200) limiter is observed when the two pHEMT diodes have an electrical spacing of 65º between each other. It is also noticed that of the two ideal limiters, the (PH120) limiter with a diode of narrower channel width exhibits a lower insertion loss than the (PH200) limiter.

A high-quality limiter circuit comprises three main characteristics, namely low insertion loss, high isolation and fast switching speed. To achieve all the three desired responses, two diodes are employed instead of one, which would likely be too lossy or slow in switching response. Therefore, mounting multiple shunt diodes along a transmission line will overcome the problems that a single diode limiter might encounter [69]. Spacing between the diodes must be carefully considered, because it determines the effective isolation of the limiter and, if not chosen carefully, the device can be damaged easily [69]. The micrographs of the fabricated spiral (PH120), straight (PH200) and spiral (PH200) limiters are shown in Figure 6.5.

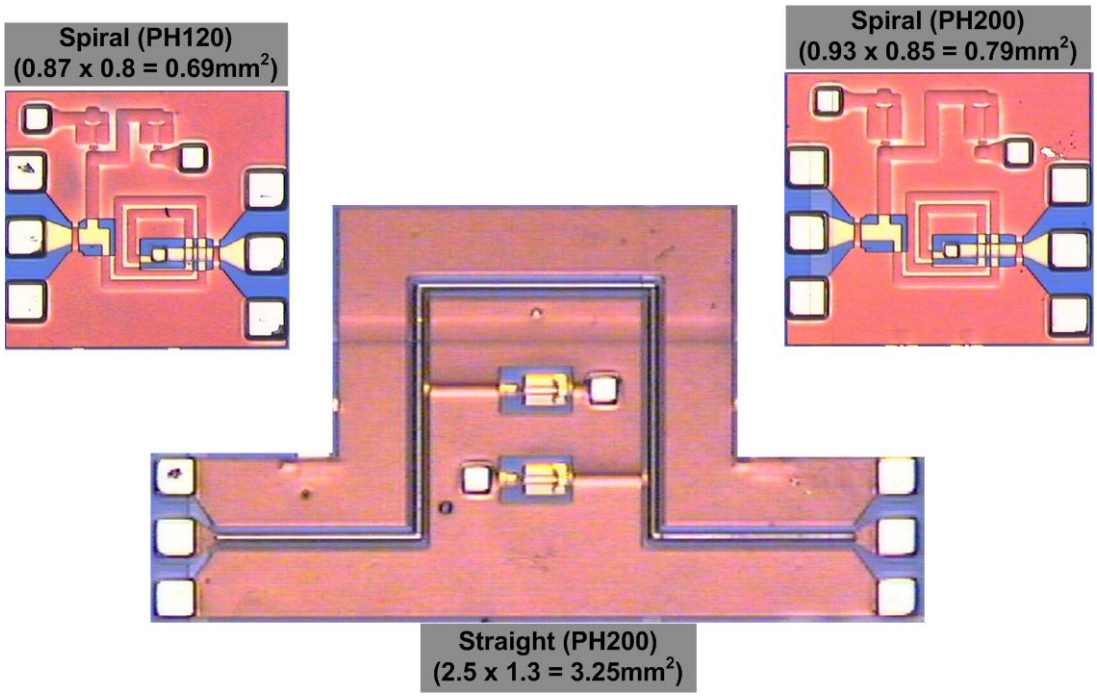


Figure 6.5: Micrographs of the fabricated spiral (PH120), straight (PH200) and spiral (PH200) limiters.

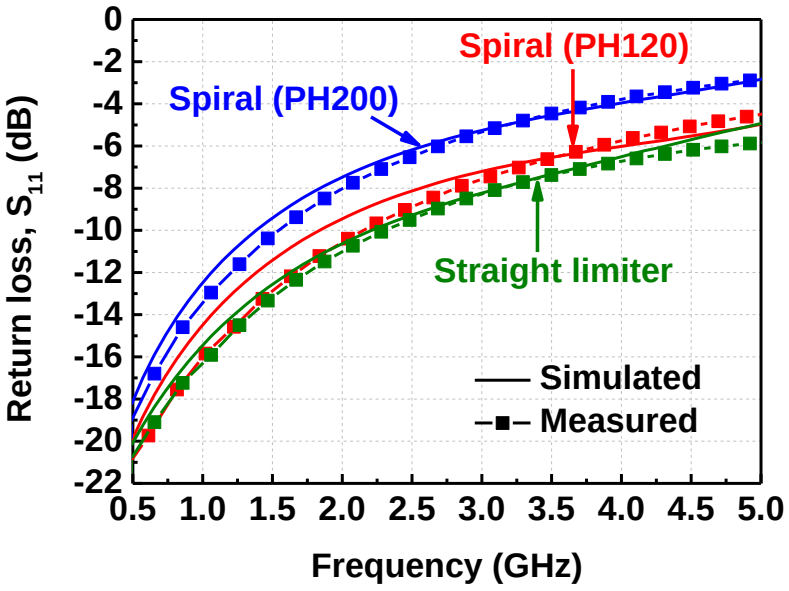


Figure 6.6: Comparison of measured and simulated return loss of three MMIC limiter circuits at zero biasing conditions.

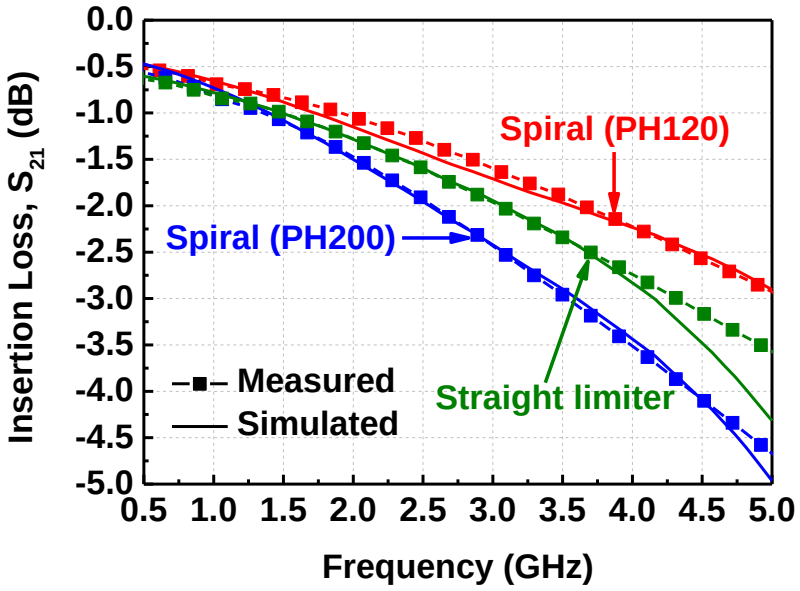


Figure 6.7: Comparison of measured and simulated insertion loss of three MMIC limiter circuits at zero biasing conditions.

The measured and simulated S-parameters for all three limiters are shown in Figure 6.6 and Figure 6.7. The measured results seem to agree reasonably well with the simulated results, in that all three limiters exhibit the classical band-pass filter frequency response with a drop in insertion loss, which is caused by transmission line attenuation losses at higher frequencies. At 3 GHz, the straight limiter exhibits less than 1.89dB of insertion loss, while the spiral (PH120) and spiral (PH200) limiters exhibit 1.63dB and 2.44dB of insertion loss, respectively. The return loss of the three limiters is better than 5dB across the 3 GHz band. The insertion loss comparison of the three limiters shows that both the spiral (PH200) and the straight limiter have some extra insertion loss compared to the spiral (PH120), due to the two both having longer total transmission line length which causes more attenuation and is dominated by the skin effect at higher frequencies, which in turn serves to increase the effective resistance of the transmission line in proportion to the square root of the frequency.

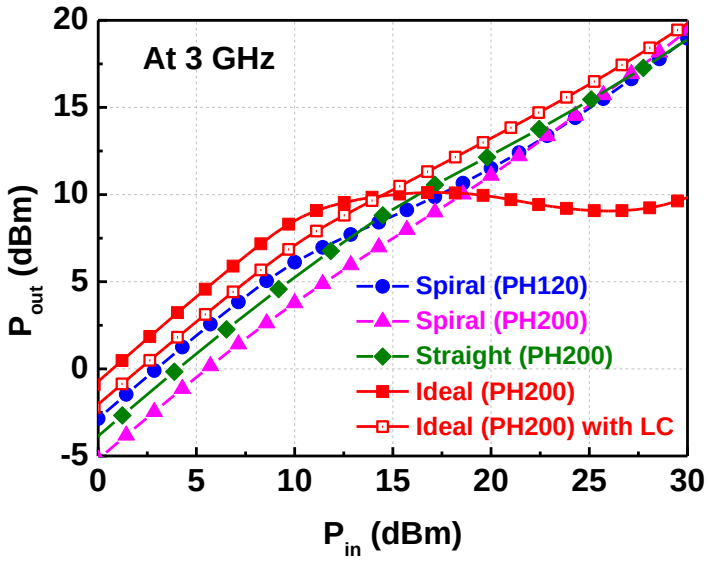


Figure 6.8: Simulated output power response of the three MMIC limiter circuits as well as the ideal limiter circuit at 3GHz.

The results shown in Figures 6.7 and 6.8 are for the three modelled limiter circuits compared with the ideal limiter case. The data were generated from the harmonic balance simulation setup in an ADS simulator. Furthermore, to prove that inductive and capacitive parasitics are responsible for the short, flat leakage level of the three modelled limiters, LC components were added to the ideal limiter circuit, as shown in Figure 6.3. In power response plots in Figure 6.8, it is evident that the ideal limiter with LC components showed a similar short flat leakage level response as the other three modelled limiters. The gain in this investigation also refers to the insertion loss, S_{21}.

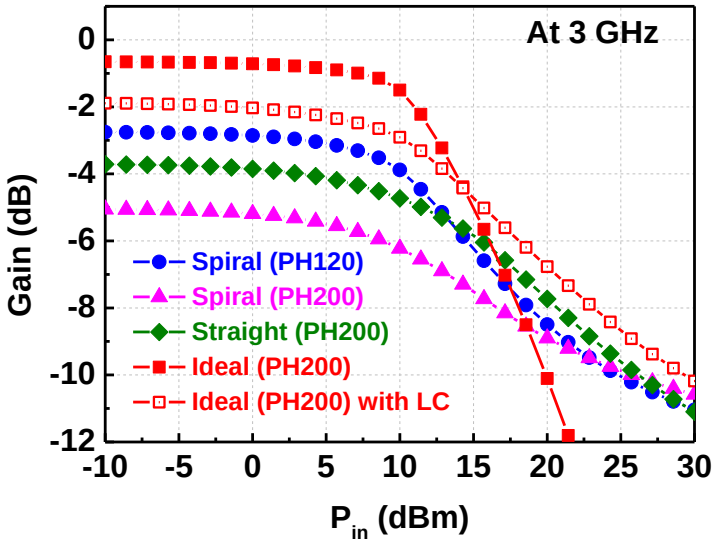


Figure 6.9: Simulated gain response of three MMIC limiter circuits as well as the ideal limiter circuit at 3GHz.

Table 6.2: Summary of 1dB compression power ratings at 1 GHz.

Limiter	Input Power, P_{in} (dBm)	Output Power, P_{out} (dBm)	Attenuation, ($P_{in} - P_{out}$) (dBm)	Insertion Loss (dB)
Ideal (PH200)	10.13	8.83	1.30	-0.30
straight (PH200)	9.85	8.35	1.50	-0.77
spiral (PH200)	9.48	7.43	2.05	-0.72
spiral (PH120)	9.51	7.78	1.73	-0.65

Table 6.3: Summary of 1dB compression power ratings at 2 GHz.

Limiter	Input Power, P_{in} (dBm)	Output Power, P_{out} (dBm)	Attenuation, ($P_{in} - P_{out}$) (dBm)	Insertion Loss (dB)
Ideal (PH200)	11.61	10.04	1.57	-0.57
straight (PH200)	8.33	5.35	2.98	-1.31
spiral (PH200)	9.57	5.80	3.77	-1.54
spiral (PH120)	9.59	7.05	2.54	-1.13

Table 6.4: Summary of 1dB compression power ratings at 3 GHz.

Limiter	Input Power, P_{in} (dBm)	Output Power, P_{out} (dBm)	Attenuation, ($P_{in} - P_{out}$) (dBm)	Insertion Loss (dB)
Ideal (PH200)	10.36	8.72	1.64	-0.65
straight (PH200)	7.52	4.58	2.94	-1.96
spiral (PH200)	9.10	3.06	6.04	-2.44
spiral (PH120)	9.54	5.80	3.74	-1.72

The spiral limiter design structures are found to have better attenuation than the straight limiter across all frequencies as shown in Tables 6.2 – 6.4, which means that they offer more protection (limit more power) to the output circuit. The insertion loss of the spiral (PH120) limiter is lower at all three frequencies in Tables 6.2 – 6.4 compared to the other limiters, which could be due to low microstrip attenuation losses in the spiral (PH120) limiter design. Both the spiral (PH200) and straight (PH200) limiters have a large diode contact area, and this introduces capacitive parasitics into the circuit which lead to losses. Since a limiter is used as a front-end device in telecommunication radar systems, any loss that is exhibited by the limiter is considered noisy for the overall receiver, which makes the insertion loss a very important characteristic when designing a power limiter.

From the tabulated results above, it can be concluded that the spiral (PH120) limiter offered the best performance with a flat leakage level less than 10 dBm, a maximum insertion loss of 2 dB from 50 MHz to 3.6 GHz and a return loss better than 6 dB. These advantages, together with a much smaller circuit layout, make the PH120 diode-based spiral limiters suitable candidates for efficient radar and other communication systems demanding lower cost and lower weight considerations.

6.1.2 MMIC Power Measurement Set-up

In order to test how well the fabricated limiters in this work help to block high power level signals from damaging a power-sensitive device, the set-up in Figure 6.10 is used to carry out power measurements.

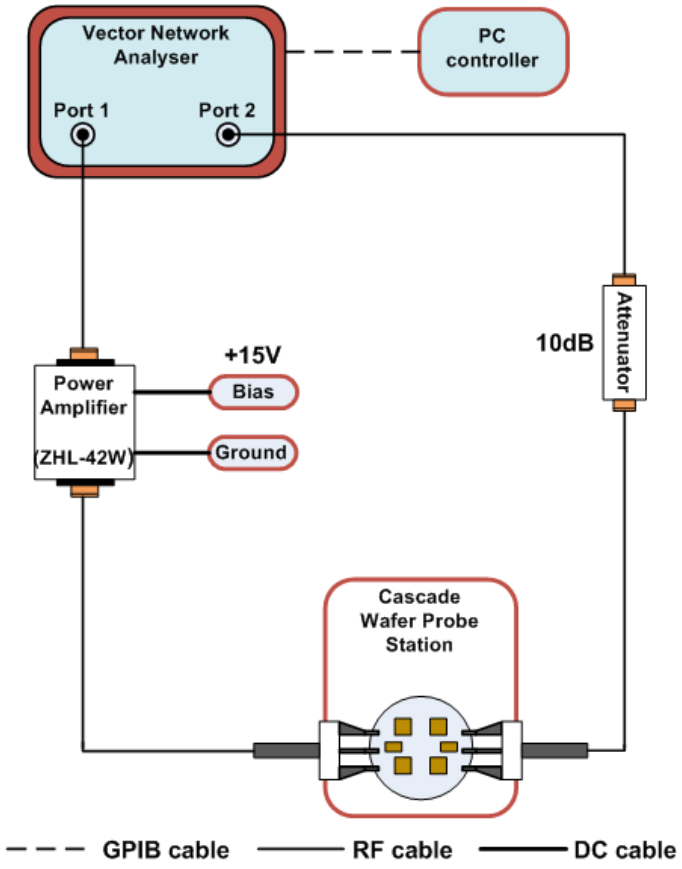


Figure 6.10: Simplified block diagram measurement set-up for the MMIC power limiters.

The on-wafer power measurements on a MMIC power limiter made for 3 GHz applications will require a power amplifier that operates in the 3 GHz frequency range. The amplifier used in this work is from Mini-Circuits, with a measured gain of 30 dB, maximum output power of 38 dBm, minimum 1dB compression of 28 dBm and noise figure of 8 dB at 15V DC bias. The amplifier operating frequency range is from 10 MHz to 4.2 GHz, and the DC bias is manually controlled. In order to protect the VNA, a 10 dB attenuator is placed between the VNA and the device under test (DUT) for the high power measurements. The constant attenuation of 10 dB is provided by a high-quality broadband coaxial attenuator. The measurements were completed and automated with the aid of a PC controller connected to the network analyser through a GPIB interface.

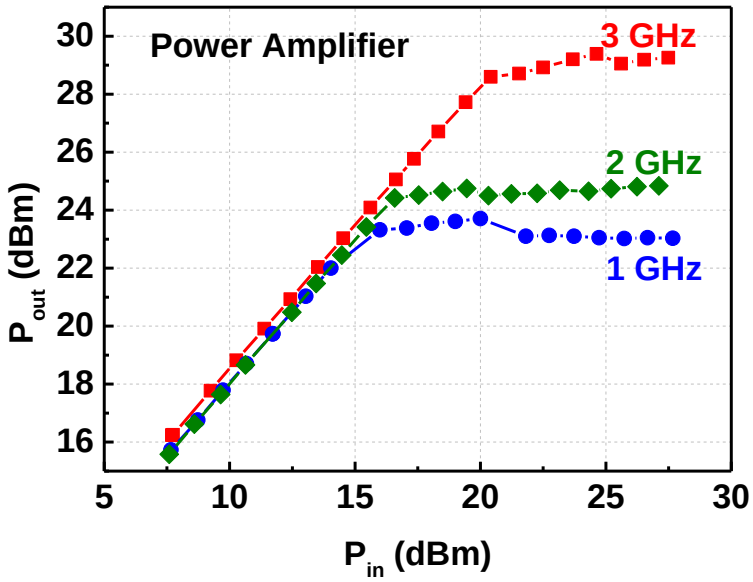


Figure 6.11: Comparison of measured output power response of a Mini-Circuits coaxial power amplifier (ZHL-42W) at different frequencies.

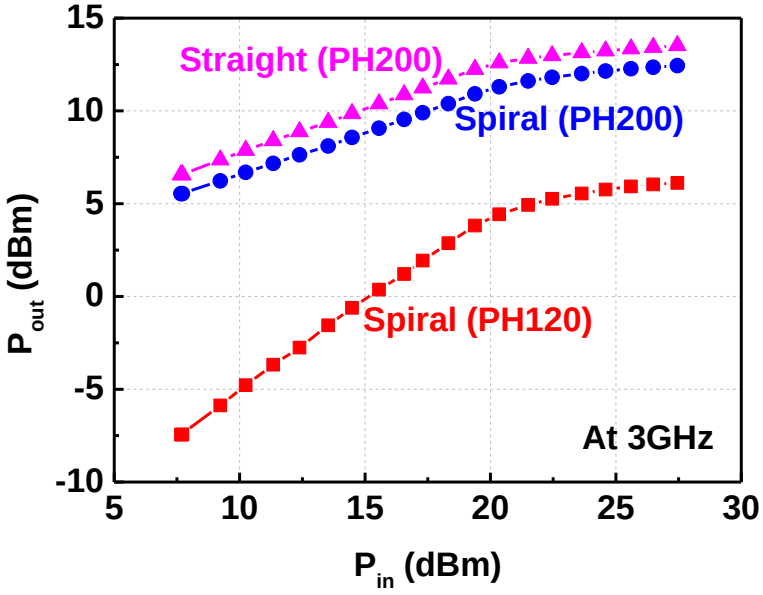


Figure 6.12: Measured output power response of three MMIC limiter circuits at 3GHz.

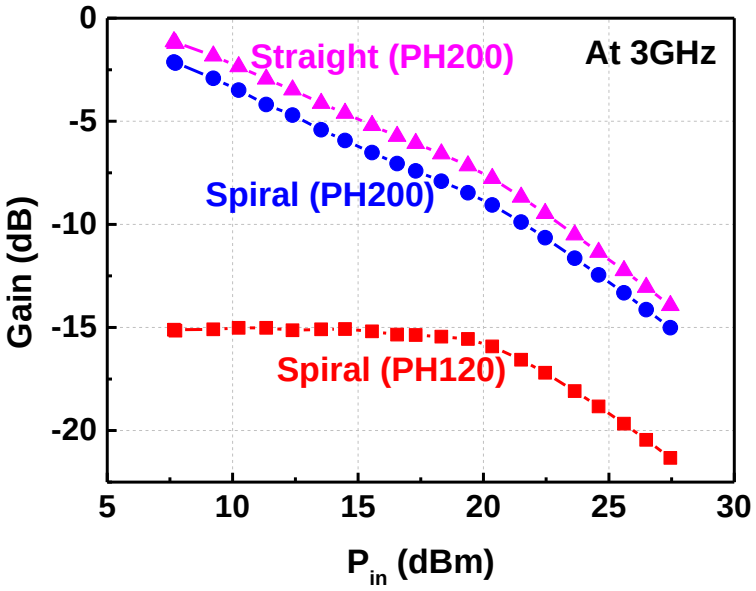


Figure 6.13: Measured gain response of three MMIC limiter circuits at 3GHz.

The limiting threshold power of all three limiters is approximately 20dBm of input power at 3GHz, as illustrated in Figure 6.12. The spiral (PH120) limiter exhibits an attenuation of about 15dB at an input power of 15dBm and zero output power. The spiral (PH200) and straight (PH200) limiters exhibit attenuations of about 7dB and 5dB, respectively, at an input power of 15dBm, and 8dBm and 10dBm output power, respectively. With an attenuation of approximately 15dB, the spiral (PH120) limiter looks clearly the more desirable one, because it reflects more of the high input power wave. The limiter reflects more high input power at the expense of an increase in insertion loss, which is not the case for the spiral (PH200) and straight (PH200) limiters.

In Figure 6.13 it is evident that both straight (PH200) and spiral (PH200) limiters with gate width diodes of (2 x100) µm have much higher gain than the spiral (PH120) limiter with gate width diodes of 60µm. The gains are negative because the limiters' circuits are using diode components, and positive gains are usually associated with transistors. A wider gate means more DC and RF current, the depletion width becomes larger and the trans-conductance increases, therefore resulting in an increase in gain to support high-frequency operation. Having a wider gate also means more power capability.

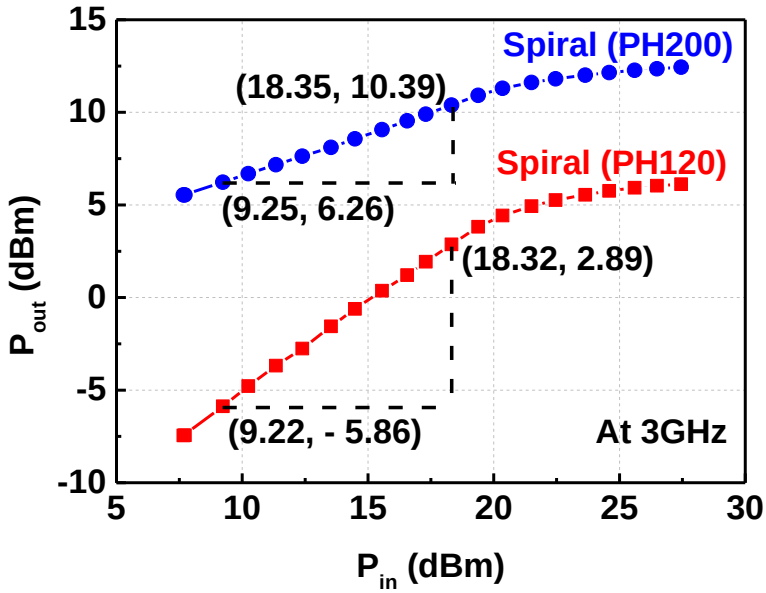


Figure 6.14: Slopes of the measured output power response of the spiral (PH120) and spiral (PH200) limiters at 3GHz.

The slope for the spiral (PH200) limiter in Figure 6.14 is given as:

$$\text{Slope} = \frac{\Delta y}{\Delta x} = \frac{(10.39 - 6.26)}{(18.35 - 9.25)} = 0.45$$

The slope for the spiral (PH120) limiter in figure 6.14 is given as:

$$\text{Slope} = \frac{\Delta y}{\Delta x} = \frac{(2.89 - -5.86)}{(18.32 - 9.22)} = 0.96$$

During the analysis of the output power response of the three limiter circuits, it was found that the non-limiting region (resistive region) of the limiters (spiral PH200 and straight PH200) with a wider diode channel width showed a less steep slope of around 0.45 compared to the 0.96 slope of the spiral PH120 limiter. This confirms that the PH120 diode is more resistive compared to the PH200 diode, and consequently, less current flows through the PH120 diode because of a narrower channel width, which is verified by a series resistance of about 12Ω for the PH120 diode compared to that of the PH200 diode of 9Ω. Therefore since the two series resistances of the diodes are not so different, this also confirms that the limiters are very sensitive to the series resistance of the diodes.

Table 6.5: 1dB compression power ratings at 1 GHz.

Limiter	Input Power, P_{in} (dBm)	Output Power, P_{out} (dBm)	Gain /Attenuation (dB)
Power Amplifier	19.00	23.64	4.64
Straight (PH200)	9.72	8.60	1.12
Spiral (PH200)	9.74	8.36	1.38
Spiral (PH120)	22.73	7.26	15.47

Table 6.6: 1dB compression power ratings at 2 GHz.

Limiter	Input Power, P_{in} (dBm)	Output Power, P_{out} (dBm)	Gain /Attenuation (dB)
Power Amplifier	17.54	24.50	6.96
Straight (PH200)	7.97	6.66	1.31
Spiral (PH200)	7.99	5.83	2.16
Spiral (PH120)	21.66	5.73	15.93

Table 6.7: 1dB compression power ratings at 3 GHz.

Limiter	Input Power, P_{in} (dBm)	Output Power, P_{out} (dBm)	Gain /Attenuation (dB)
Power Amplifier	20.41	28.56	8.15
Straight (PH200)	10.23	7.75	2.48
Spiral (PH200)	10.19	6.45	3.74
Spiral (PH120)	21.50	4.68	16.82

Of the three fabricated limiters, the spiral (PH120) has a much better attenuation (difference between the input power and output power) of over 10dB for frequency range of 1GHz to 3GHz, as shown in Tables 6.5 to 6.7, mainly due to the contact areas of these devices. That is to say, too small a contact area would limit the maximum amount of power a limiter can detect before the diodes burn out [93], which makes diode area a very important design parameter, because most of the other parameters, such as the work functions of the semiconductor and metal, are predetermined by the process as shown in the Richardson-Dushman expression for thermionic current [94]. Table 6.8 compares the

performance of this work's limiter results with other published MMIC limiters. Due to employing multilayer technology, this work's limiter offers a better reduced total chip size while maintaining a low insertion loss.

Table 6.8: Summary of the performance comparison of the MMIC Limiters.

Ref.	Technology	Frequency (GHz)	Insertion Loss (dB)	Pout (dBm)	Return Loss (dB)	Total Area (mm^2)
[95]	GaAs Dual VPIN	0.5 - 20	< 0.8	@ Pin =10dBm 15 – 16.5	---	---
[74]	GaAs VPIN	10	< 0.39	@ Pin =28dBm 21	> 13	0.79
[96]	GaAs VPIN	1-6	< 0.5	@ Pin >30dBm 16	> 12	4
[97]	GaAs VPIN	2-4.5	< 0.5	@ Pin >30dBm 15	> 15	5.5
This Work	GaAs pHEMT	3	< 1.61	@ Pin =10dBm 6.13	> 7.59	0.69

6.2 A 10 GHz Low-noise Amplifier (LNA)

In this section we continue the investigation into the integration of multilayer CPW passive components such as inductors and capacitors with active components such as pHEMTs, in order to form compact 3D multilayer MMICs. Passive components are employed to design a conjugate matched amplifier at the maximum available gain. The conjugate matched amplifier's maximum gain is traded off in return for better noise performance at an operating frequency of 10 GHz, which therefore leads to the creation of a compact 10 GHz low-noise amplifier. The schematic and layout simulations are compared and analysed with the measured data.

6.2.1 Stability Considerations of an Amplifier

The first requirements that an amplifier circuit design must meet is stable performance over the entire frequency range. This is of particular concern when dealing with RF circuits which tend to oscillate, depending on the operating frequency and termination [98].

The best way for a designer to determine whether a device is unconditionally stable or not is by calculating the Rollett's stability factor (K) [99], which is given as:

$$K = \frac{1+|D_s|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|} \tag{6.1}$$

Where:

$$D_s = S_{11}S_{22} - S_{12}S_{21} \tag{6.2}$$

For stability, if K is greater than one (K > 1), then the transistor is considered to be unconditionally stable at the given bias point for any combination of source and load impedance. If K is less than one (K < 1), the transistor is then considered to be unstable and will oscillate for certain source and load impedances. Therefore, one must take great care while choosing the source and load impedances, as well as their relative positions on the stability circles. With an unconditionally stable transistor, one is able to conjugate match the input and output ends, in order to achieve maximum gain. The transistor's input and output reflection coefficients must be plotted on the Smith chart and manipulated into the 50Ω point with suitable matching networks [55].

The stability measure is represented as [55]:

$$b = 1 + |S_{11}|^2 - |S_{22}|^2 - |D_s|^2 \tag{6.3}$$

If b is greater than zero (b > 0), then the transistor is considered to be unconditionally stable, and if (b < 0), the transistor is considered to be unstable and will oscillate for certain source and load impedances.

The stability technique employed in this work is the same as the one discussed in Krishnamurthy's thesis [55], where the designs are based on a series and shunt resistive loading technique. In this technique, a small series resistor, or a large shunt resistor, is added to the input and (or) output ports to ensure good stability, as shown in Figure 6.15.

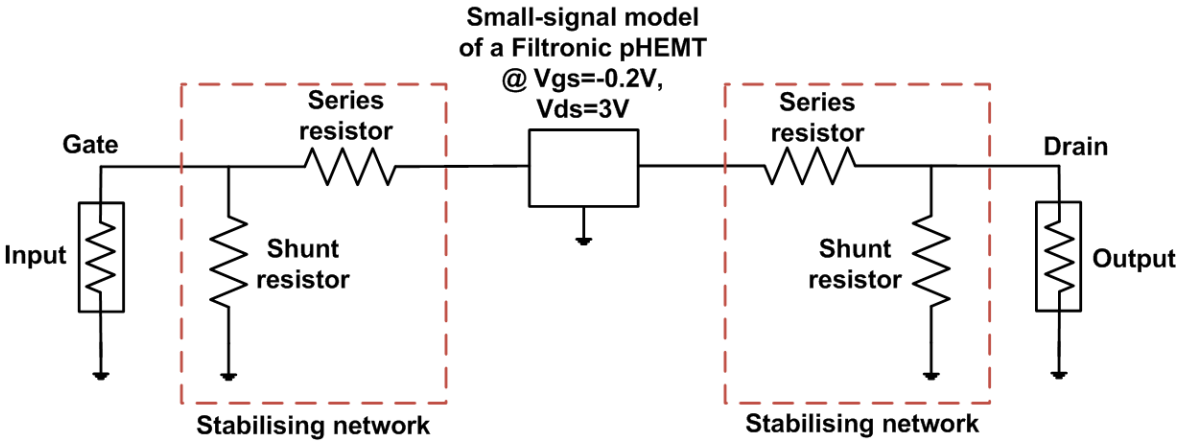


Figure 6.15: Small-signal pHEMT model with the stabilising resistor networks at both input and output ports.

6.2.2 Stability of Small-Signal pHEMT Model

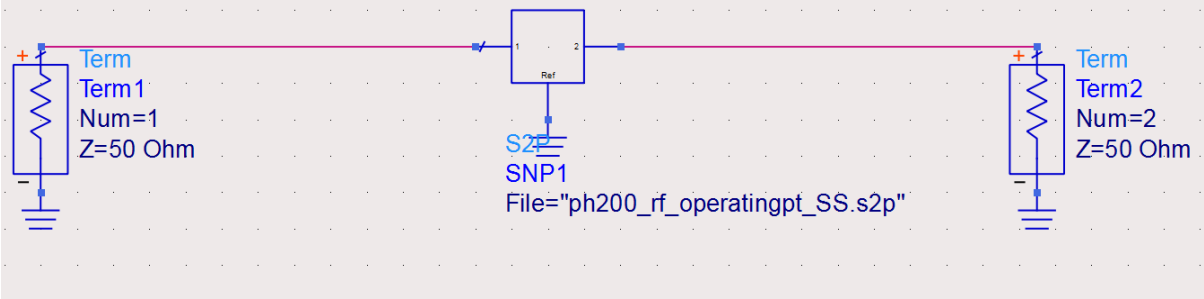


Figure 6.16: Small-signal model pHEMT without stabilising resistors.

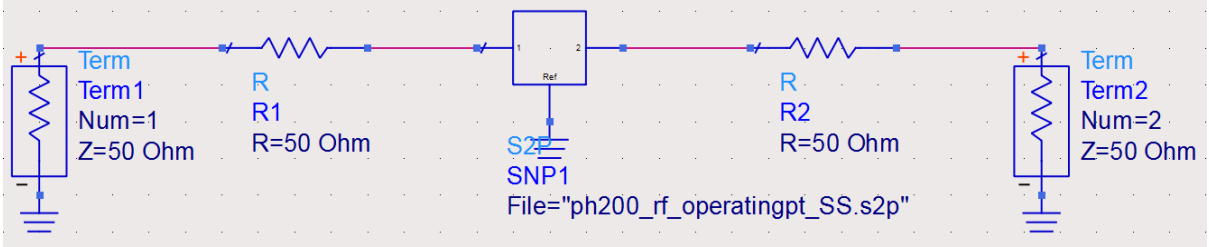


Figure 6.17: Small-signal pHEMT model with stabilising resistors.

The resistor values are tuned until the stability factor (K) is greater than unity. The method described is a simple and more economical way of making an amplifier unconditionally stable, rather than employing feedback circuits which would occupy a large circuit area [100].

It is observed in Figure 4.114 that the pHEMT is unstable without the stabilising resistors, because its stability factor, K, is below unity. When the 50Ω series input and output stabilising resistors are added to the network, the pHEMT becomes unconditionally stable, with the stability factor being greater than one (K > 1) starting from very low frequency values and increasing linearly. The stability measure, b, shown in Figure 6.18, remains above zero (b > 0) for both cases, with and without the stability resistors, hence confirming the unconditionally stable condition of the transistor. The stability factor, stability measure, minimum noise figure and pHEMT gain, with and without the 50Ω stability resistors at 10 GHz, are summarised in Table 6.9.

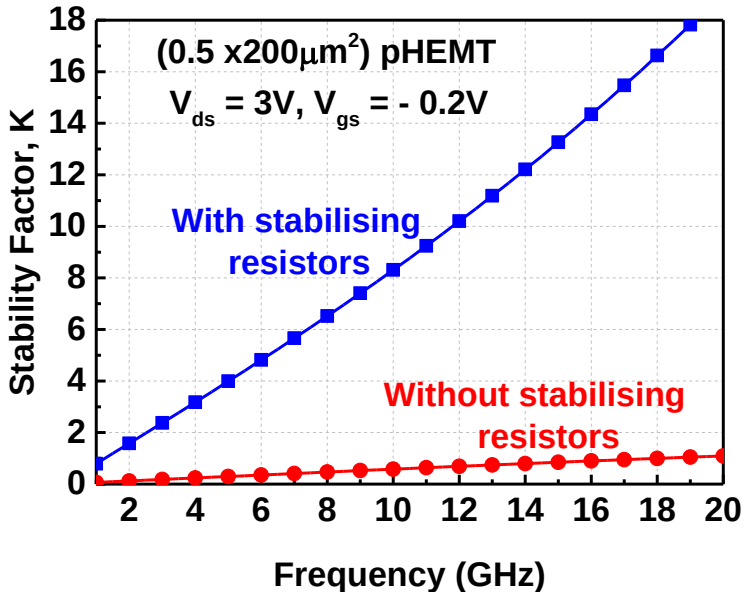


Figure 6.18: Stability factor of the small-signal model for a GaAs pHEMT, with and without stabilising resistors.

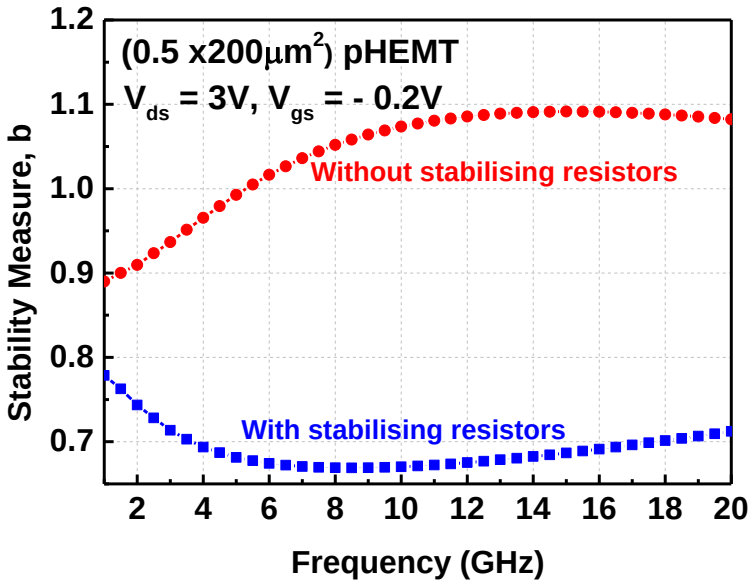


Figure 6.19: Stability measure of the small-signal model for a GaAs pHEMT, with and without stabilising resistors.

Table 6.9: Stability factor, stability measure, noise figure and gain of the pHEMT, with and without stabilising network at 10 GHz.

Circuit Network	Stability factor, K	Stability measure, b	Noise Figure (dB)	Gain (dB)
Without stabilising resistors	0.58	1.07	1.05	7.16
With stabilising resistors	8.31	0.67	4.02	0.24
With optimised resistors	1.07	0.97	1.48	6.47

One disadvantage observed while using this stabilising method is degradation in the noise performance and gain of the transistor, as shown in Table 6.9. Therefore, in order to improve noise performance and gain, the series resistors need to be tuned until the stability factor is just about unity over the frequency of interest, which in this case is 10 GHz. The series stability resistors are optimised at 4.2Ω each, and the noise performance and gain of the transistor are improved, as shown in the optimised values in Table 6.9.

6.2.3 Conjugate matched network design

Maximum gain can be realised when conjugate matches between the amplifier source or load impedance and the transistor are obtained.

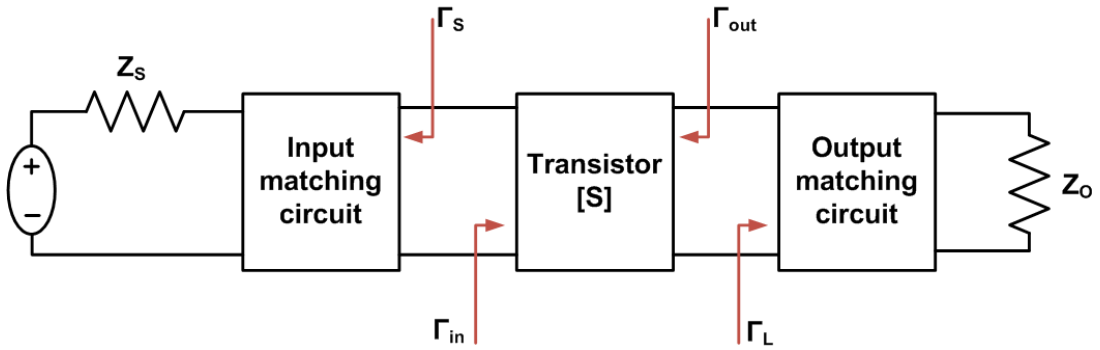


Figure 6.20: Block diagram for a single stage amplifier design.

The transducer power gain of an amplifier is given as [32]:

$$G_T = G_S G_O G_L = \frac{P_L}{P_{avs}} = \frac{1-|\Gamma_S|^2}{|1-\Gamma_S\Gamma_{in}|^2}|S_{21}|^2\frac{1-|\Gamma_S|^2}{|1-S_{22}\Gamma_L|^2} \quad (6.4)$$

where

G_S is the Gain factor for the input matching circuit;

G_O is the Gain factor for the transistor and

G_L is the Gain factor for the output matching circuit.

The transistor input/source and output/load reflection coefficients are shown in Figure 6.20, and they are obtained as follows [101]:

Source reflection coefficient, Γ_S

$$\Gamma_{in} = \Gamma_S^*$$

where Γ_S^* is the complex conjugate of the source reflection coefficient

$$\Gamma_S^* = \Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \quad (6.5)$$

$$|\Gamma_S| = \left|\frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1}\right| \quad (6.6)$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |D_S|^2$$

$$C_1 = S_{11} - D_S S_{22}^*$$

Load reflection coefficient, Γ_L

$$\Gamma_{out} = \Gamma_L^*$$

where Γ_L^* is the complex conjugate of the load reflection coefficient

$$\Gamma_L^* = \Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S} \quad (6.7)$$

$$|\Gamma_L| = \left| \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \right| \tag{6.8}$$

where

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |D_S|^2$$

$$C_2 = S_{22} - D_S S_{11}^*$$

Once the desired source and load reflection coefficients have been obtained, they are then plotted on the Smith chart to read off both the source and the load impedances, respectively. An alternative way of estimating the source and load impedances is by calculating them using the mathematical approach described in Krishnamurthy's thesis [55].

In this work, Krishnamurthy's [55] approach to conjugate matching is employed whereby shunt inductors and series capacitors are used to obtain a match between the source and the transistor as well as the load and the transistor at a designed operating frequency of 10 GHz. The shunt inductors and series capacitors values are estimated using:

$$Series\ L = \frac{Arclength \times 50}{2\pi f} \tag{6.9}$$

$$Shunt\ L = \frac{50}{2\pi f \times Arclength} \tag{6.10}$$

$$Shunt\ C = \frac{Arclength}{2\pi f \times 50} \tag{6.11}$$

$$Series\ C = \frac{1}{2\pi f \times Arclength \times 50} \tag{6.12}$$

where, f = 10 GHz is the operation frequency of the amplifier in this work.

The initially calculated capacitor and inductor values are assumed to be lossless and are applied to the input and output matching networks in the amplifier circuit shown in Figure 6.21. Lossy components (capacitors and inductors) replace the ideal circuit components, in order to include the realistic parasitics, as shown in Figure 6.22. The lossy components' values are tuned, in order to impedance-match the network. It can also be observed that the input network design is configured as a low pass filter, while the output network as a high pass filter to improve the frequency selectivity of the designed amplifier [86].

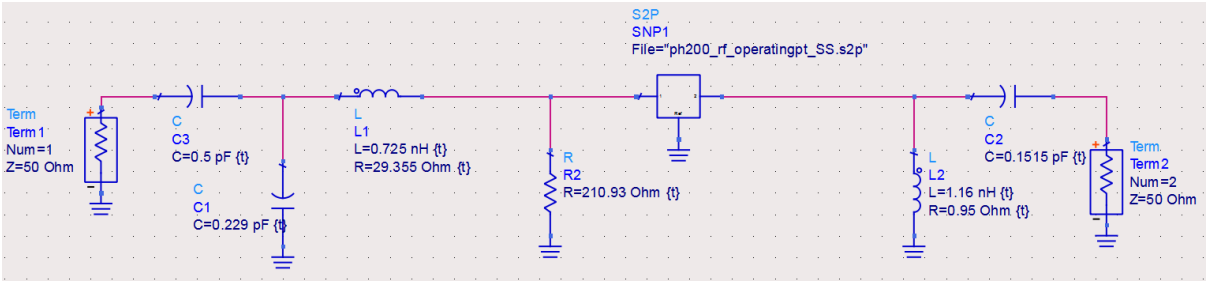


Figure 6.21: Schematic of a conjugate matched 10GHz low-noise amplifier with ideal L and C.

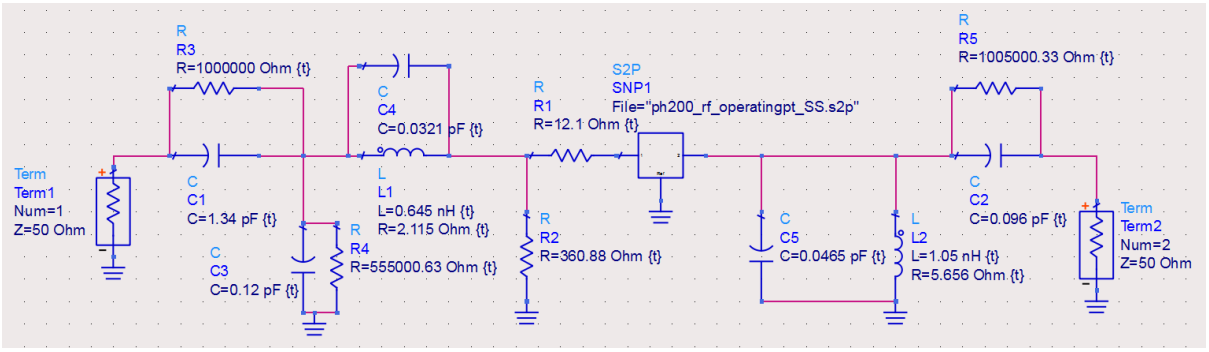


Figure 6.22: Schematic of a conjugate matched 10GHz low-noise amplifier with parasitics associated with the passive components (lossy L and C).

In this work, the 10 GHz matched amplifier is designed with a shunt stabilising network and enables the use of as many multilayer passive components in the design as possible. This helps to demonstrate one of the advantages of using multilayer components to save chip space. The comparisons of the simulated S-parameters of the 10 GHz LNA using ideal, lossy and optimised passive components are shown in Figures 6.23 – 6.26, and the noise factor comparison is shown in Figure 6.27.

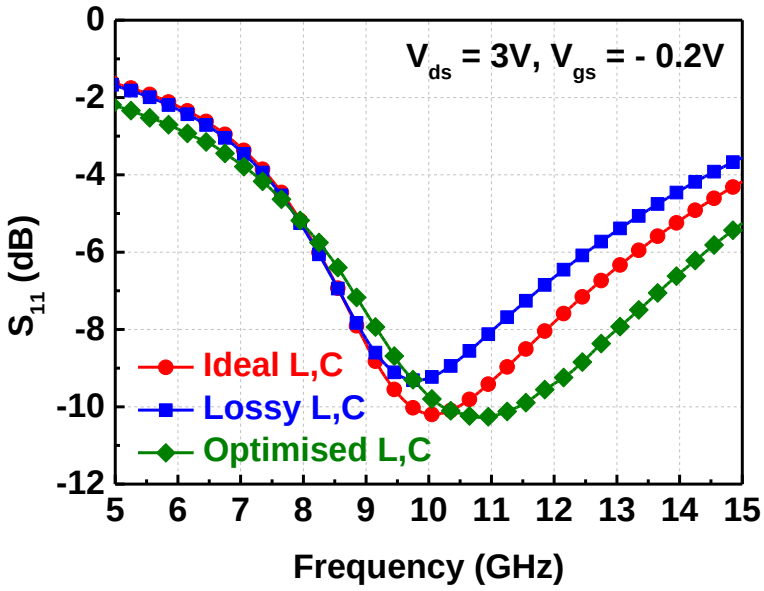


Figure 6.23: Comparison of the simulated S_{11} parameters of a 10 GHz low-noise amplifier using ideal, lossy and optimised passive components.

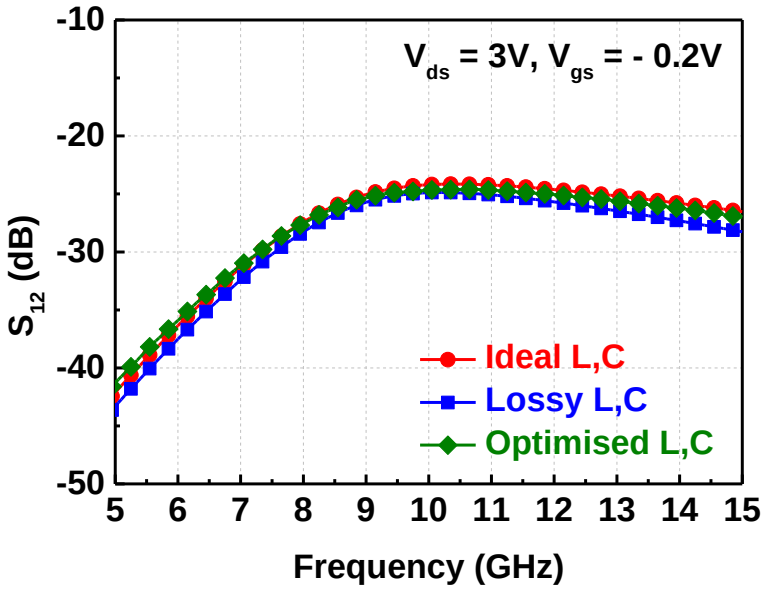


Figure 6.24: Comparison of the simulated S_{12} parameters of a 10 GHz low-noise amplifier using ideal, lossy and optimised passive components.

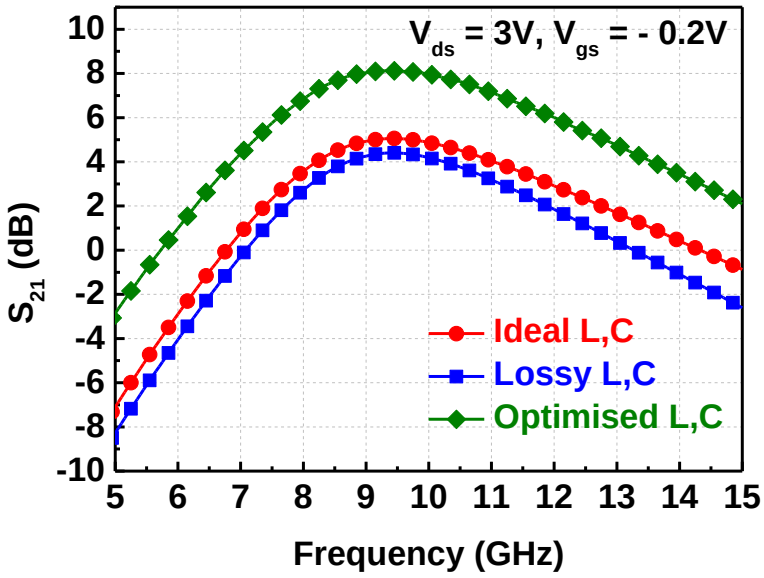


Figure 6.25: Comparison of the simulated S_{21} parameters of a 10 GHz low-noise amplifier using ideal, lossy and optimised passive components.

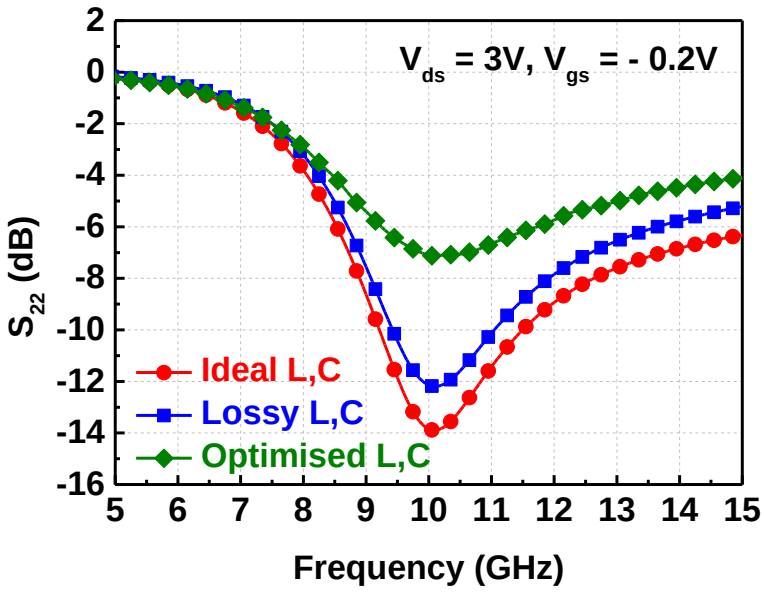


Figure 6.26: Comparison of the simulated S_{22} parameters of a 10 GHz low-noise amplifier using ideal, lossy and optimised passive components.

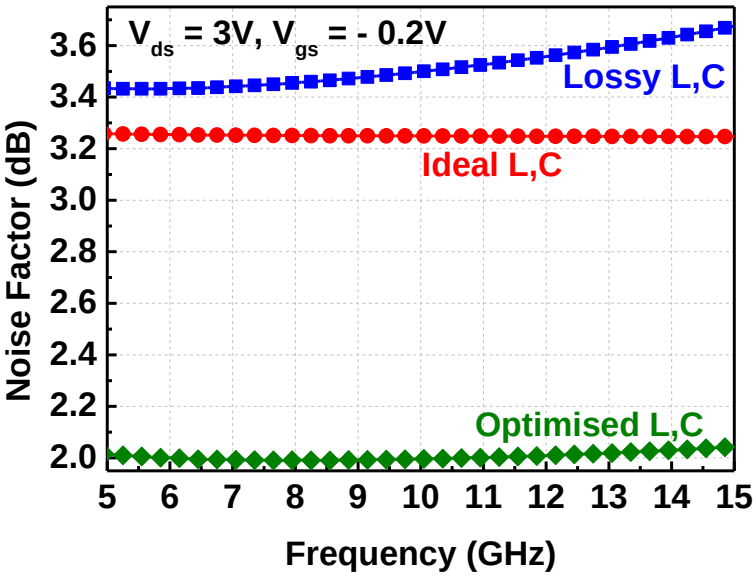


Figure 6.27: Comparison of the noise factors of a 10 GHz low-noise amplifier using ideal, lossy and optimised passive components.

Table 6.10: Comparison of the matching network values of a low-noise amplifier with ideal, lossy and optimised passive components at 10 GHz.

Circuit Network	L_1 (nH)	C_1 (pF)	L_2 (nH)	C_2 (pF)	Noise factor (dB)	Maximum Gain (dB)
Ideal L,C	0.73	0.23	1.02	0.13	3.25	7.36
Lossy L,C	0.73	0.23	0.73	0.15	3.49	6.18
With optimised L,C	0.62	0.12	1.04	0.13	1.99	7.97

In this work input and output networks are optimised to match perfectly, even with the addition of inductor and capacitor parasitics, as shown in Figures 6.23 – 6.26. From Table 6.10 it is evident that adding parasitic (lossy L, C) components to the amplifier circuit results negatively in gain loss of about 1.18 dB. This is caused mainly by the series resistance of the inductors and is taken into account in the final amplifier design. It also suffers a small increase in a noise factor of 0.24 dB due to the lossy parasitics introduced into the circuit. With some tweaking of the parasitic components, one can achieve much greater performance results for the gain and the noise factor of the amplifier. The gain performance improved by 1.79 dB and the noise factor decreased by 1.5 dB, as shown in Table 6.10.

6.2.4 10 GHz Low-Noise Amplifier (LNA) Layout design

A multilayer technology with directly overlaid, spiralled inductors and folded capacitors is employed in the 3D MMIC layout design of the amplifier. Three-dimensional CPW multilayer components are used in the layout design instead of the planar or microstrip components, because the 3D inductors occupy one quarter of the area that a planar inductor occupies, and 3D capacitors will occupy almost half the size of the planar capacitors [86, 102, 103]. When designing layout circuits, providing isolation between components or reducing cross-talk between the components is another important issue to be considered. From the analysis done in Vo's paper [2], it is found that a -30dB isolation between the components is achieved with a 150µm separation in a microstrip-based design, and the same isolation is achieved with a 90µm separation in CPW-based circuit designs.

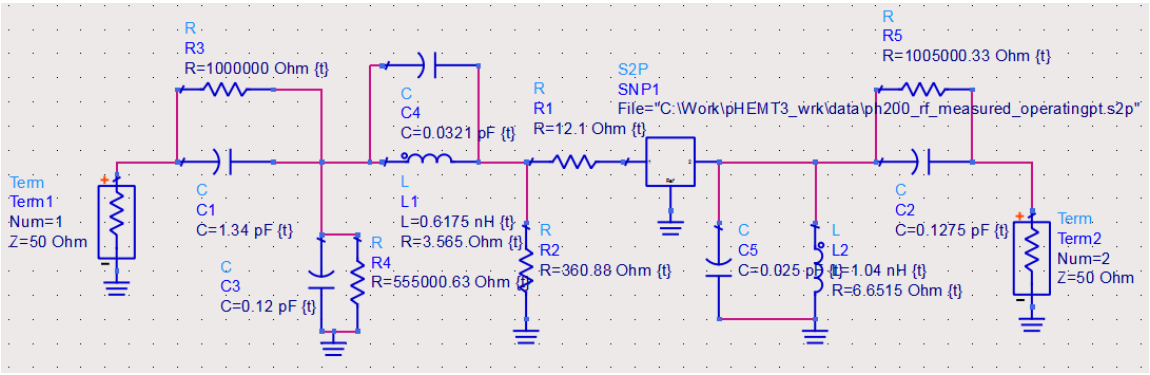


Figure 6.28: Schematic circuit of a 10GHz LNA.

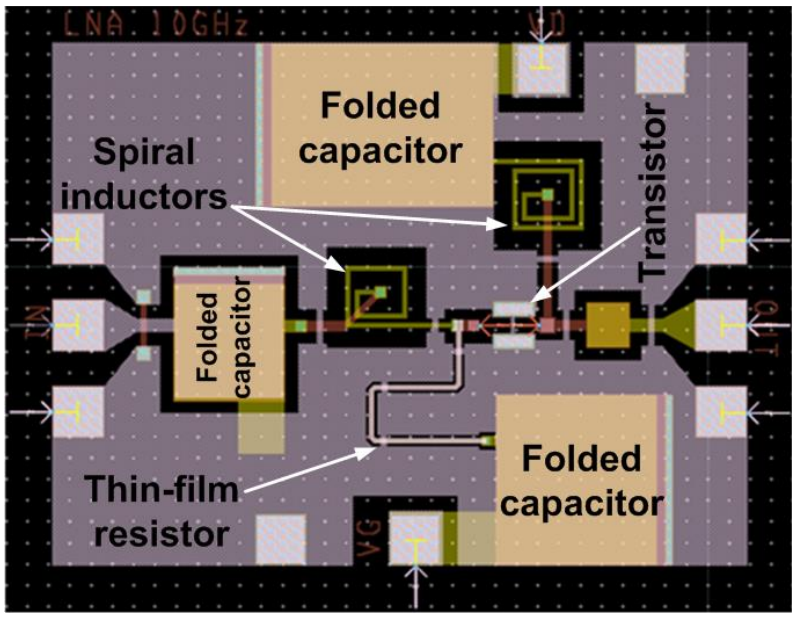


Figure 6.29: Layout design of a multilayer 3D MMIC 10 GHz LNA.

The 10 GHz low-noise amplifier shown in Figure 6.29 has been fabricated on the same wafer as other multilayer components and circuits.

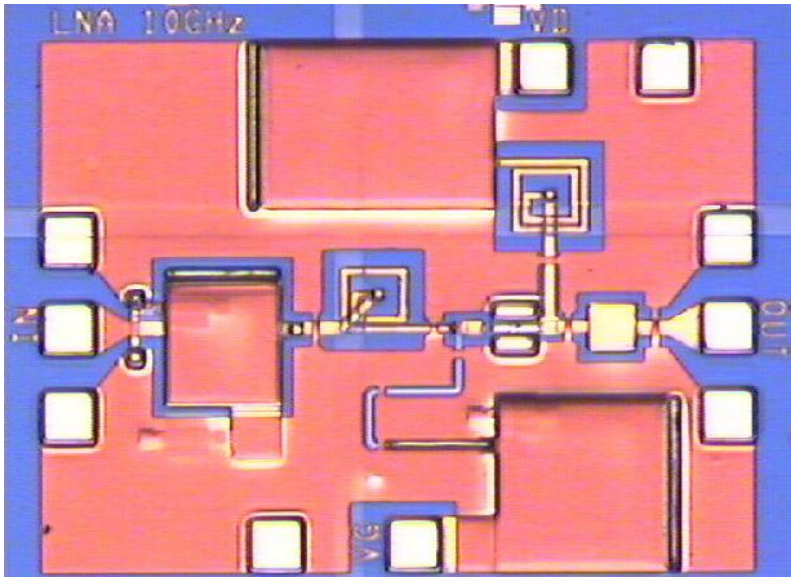


Figure 6.30: Micrograph of a fabricated multilayer 3D MMIC 10 GHz LNA.

In this work, the fabricated 10 GHz LNA is characterised using a Cascade Microtech on-wafer probe station and a Vector Network Analyser (VNA) from 5 GHz to 15 GHz. DC bias is applied to the amplifier using DC probes fed at the VD and VG pads, as shown in Figure 6.30. The comparisons of the S-parameters for the layout, fabricated and schematic designs of the 10 GHz LNA are shown in Figures 6.31 – 6.33.

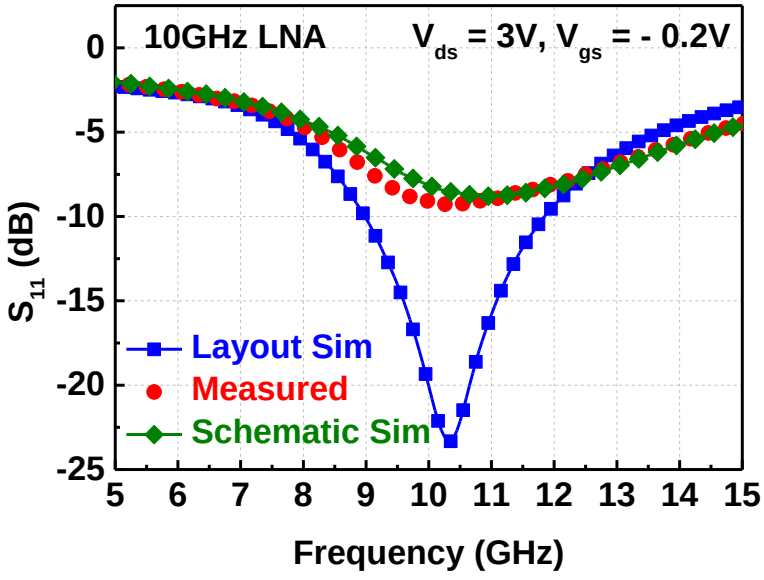


Figure 6.31: Return loss comparison for measured, layout simulation and schematic simulation of the 10 GHz LNA.

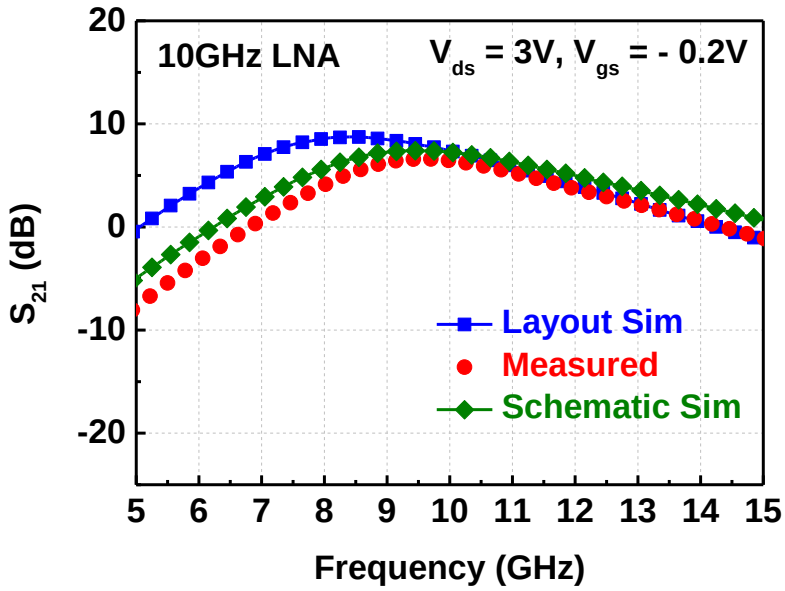


Figure 6.32: Gain comparison for measured, layout simulation and schematic simulation of the 10 GHz LNA.

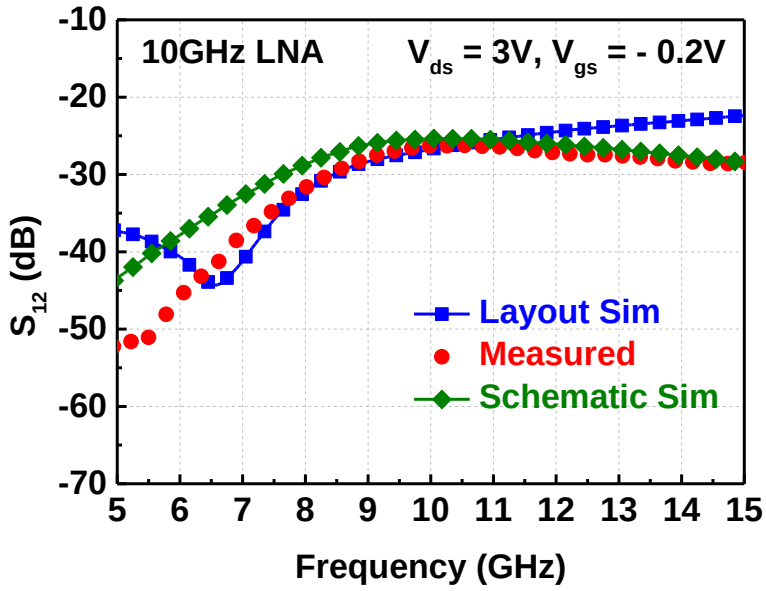


Figure 6.33: Reverse isolation comparison for measured, layout simulation and schematic simulation of the 10 GHz LNA.

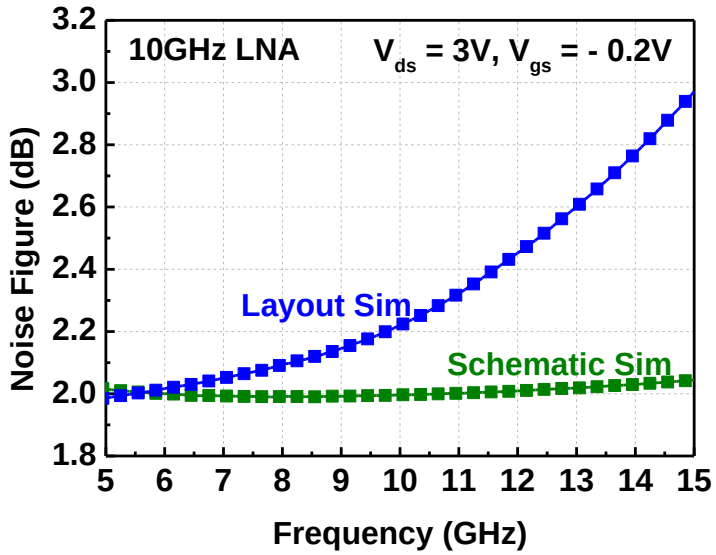


Figure 6.34: Noise figure comparison for layout simulation and schematic simulation of the 10 GHz LNA.

Table 6.11: Summary of the S-parameters and noise figure of the layout, schematic and measured results for the 10 GHz LNA.

Dataset	Return loss, S_{11} (dB)	Reverse Isolation, S_{12} (dB)	Maximum Gain, S_{21} (dB)	Noise Figure (dB)
Layout	- 20.06	- 26.65	7.40	2.22
Schematic	- 9.73	- 24.67	7.97	1.99
Measured	- 9.26	- 26.33	6.50	--

The layout and schematic simulations show good agreement with the measured results of the 10 GHz LNA, shown in Figures 6.31 – 6.33. The slight discrepancies in the results are mainly due to the inductive parasitics introduced by the DC probes on the measurement data. The increasing noise figure of the layout simulation shown in Figure 6.34 is due to the conductor losses in transmission lines employed in the layout design of the amplifier, which is not the case in the schematic design. From the results in Table 6.11, it is evident that the noise figure is relatively low (below 2.5 dB) at 10 GHz while maintaining a maximum gain of above 6.5 dB for all three compared datasets. Table 6.12 compares the performance of this work's LNA results with other published MMIC LNAs.

Table 6.12: Summary of the performance comparison of the MMIC LNAs.

Ref.	Technology	Frequency (GHz)	Gain (dB)	Noise factor (dB)	Return loss (dB)
[104]	0.15µm GaAs pHEMT	3-10	5	2.22	< -8.5
[105]	0.15µm GaAs pHEMT	9-25	20	3.3	< -10
[106]	0.15µm GaN FET	4-16	>10	< 2	< -10
[107]	0.15µm GaAs pHEMT	8-18	21	1.5	< -2
[108]	0.2µm GaAs pHEMT	8-18	11	2.3	--
[109]	0.15µm GaAs pHEMT	4-12	27	2	< -8
[110]	0.15µm GaAs pHEMT	0.4-12	>15	< 3	< -10
This Work	0.5µm GaAs pHEMT	10	6.5	* < 2.3	-9

*simulated

Chapter 7 Conclusions and Future work

7.1 Conclusions

In this research, a wide range of multilayer CPW structures have been designed, fabricated and characterised using on-wafer S-parameter measurements. These structures, which include both passive and active components, were fabricated at The University of Manchester. Three-dimensional multilayer technology was employed and consisted of three metal conductors and two dielectric layers. An alloy of Au/Ti was used for the conductor layers with an intended thickness of 0.8 μm. The two dielectric layers of polyimide of dielectric constant 3.7 were each of 2.5 μm thickness.

Multilayer CPW structures were characterised over a wide range of frequencies, from 45 MHz to 50 GHz. In designing the components, Momentum EM software in Agilent ADS was employed. Direct parameter extractions of the transmission lines were also developed, to facilitate the analysis of the multilayer components. The HP8251C Vector Network Analyser (VNA) was used to carry out all the RF S-parameter measurements. Different types of calibration techniques were studied and discussed. The Line-Reflect-Reflect-Match (LRRM) type of calibration, which is available in the WinCal software of the VNA, was used for calibration in this work, because it is a more accurate calibration than the conventional test and provides more reliable S-parameter measurements. Simulated and measured results were carefully compared and analysed.

An improved multilayer fabrication procedure was presented, giving an in-depth analysis of the main fabrication steps such as photolithography, metal deposition/lift-off, polyimide deposition and the etching process. The main problems encountered, which included metal lift-off, polyimide curing and an underdeveloped photoresist pattern, were discussed and possible solutions suggested. Fabrication process calibrations, such as tooling factors, spinning coatings, polyimide curing and pre-bake and post-bake times, were tabulated and illustrated in detail and then compared with the relevant manufacturer's data. The histories of the fabricated test samples, using the two mask sets were presented with tabulated test results from the processing validation module, resistor and interconnect measurements.

Transition from the CPW probe pads to the microstrip line was due mainly to the demand for integrating various circuit structures on one semiconductor wafer, in order to achieve the highest possible integration while maintaining each circuit's effective performance [17,

111, and 112]. In this research, design guidelines for the development of compact, wideband multilayer coplanar waveguide to thin-film microstrip (TFMS) transitions, using an experimental 3D multilayer MMIC technology developed on GaAs substrate, were presented. The three regions – the CPW region, the transition region and the thin-film microstrip (TFMS) region – that make-up this transmission line were all individually designed and analysed, to offer an impedance of 50 Ω. Two transition design types were considered, namely design A (with a footprint at the CPW end) and design B (with no footprint), and various parameter extractions were carried on both of these transition designs and their results compared. The fabricated transition structure demonstrated a maximum insertion loss of 3 dB, from 4 to 22 GHz, and a return loss better than 7 dB over the frequency range, from 9 to 34 GHz. Furthermore, the design criteria was discussed and presented for achieving compact transmission lines with improved performance for future high-performance, compact and multifunctional MMICs. The proposed improved compact transitions demonstrated return losses better than 12 dB, from 10 to 50 GHz, and insertion losses below 1.5 dB, from 4 to 47 GHz. This approach provides microwave engineers with the flexibility to design multilayer circuits with improved performance.

In this work, MMIC-active components were also modelled and realised. In this investigation, Filtronic pHEMTs were employed, which came pre-fabricated on semi-insulating GaAs substrate wafers. At the University of Manchester, multilayer processing was applied on the pre-fabricated pHEMT wafers, in order to achieve a multilayer processed pHEMT. Two types of pHEMTs were processed: (0.5x2x100) μm^2 pHEMT and (0.5x2x60) μm^2 pHEMT. These pHEMTs are used as active devices for integration with multilayer CPW passive components on a single substrate. The operating bias points of the (0.5x2x100) μm^2 pHEMT were found to be (V_{ds} = 3 V, V_{gs} = -0.2 V) and the (0.5x2x60) μm^2 pHEMT bias points were (V_{ds} = 1.5 V, V_{gs} = -0.2 V). DC and RF S-parameter measurements were carried out, and their DC and RF characteristics compared, in order to study the uniformity of both virgin and multilayer processed pHEMTs. It was observed that both the virgin and multilayer processed pHEMTs were relatively uniform for both DC and RF characteristics, and any slight discrepancies were within the tolerance level of the measurement system.

For the two pHEMTs' small-signal models were extracted from the measured S-parameter data using an automation extraction process that uses the Agilent IC-CAP simulator [55].

In the extraction process the intrinsic and extrinsic parameters of the pHEMTs were identified, which helped facilitate the design of accurate large-signal models. The (0.5x2x100) μm^2 pHEMT had its highest transconductance, g_m at 61 mS with an I_{ds} value of 34 mA, while the (0.5x2x60) μm^2 pHEMT had its highest transconductance, gm at 37 mS with an I_{ds} value of 18 mA. The (0.5x2x100) μm^2 pHEMT had f_t and f_{max} at 27 GHz and 118 GHz, respectively, while the (0.5x2x60) μm^2 pHEMT had f_t and f_{max} at 23 GHz and 85 GHz. The small-signal and large-signal models demonstrated similar values for f_t and f_{max} to the analytical calculations.

GaAs pHEMTs were used further in this work, to design and realise Schottky diodes for RF power detection purposes. To configure the pHEMT into a diode, the drain and source of the pHEMT were connected together to form the output port (ohmic contact) of the diode, while the gate acted as the input port (Schottky contact). The devices were facilitated with CPW transmission line structures on both sides of the input and output ports, which employed ground-signal-ground (GSG) pad structures for RF probe measurement purposes. Two different sized diodes were modelled, namely a (PH120) which is the (0.5 µm x 2x60) µm diode and (PH200) which is the (0.5 µm x 2x100) µm diode. The I-V and C-V characteristics of both diodes were generated, and the turn-on voltages of the PH120 and PH200 were estimated at 0.75 V and 0.7V, respectively, and the series resistances were 12Ω and 9.23Ω, respectively. Because of a larger Schottky contact area, the PH200 diode had more current passing through it compared to the PH120 diode. Diode junction capacitance at zero bias voltage (C_{j0}) for the PH120 diode was found to be approximately 366.7 fF, with a cut-off frequency of 3.62 GHz, while the C_{j0} for the PH200 diode was found to be approximately 526.3 fF, with a cut-off frequency of 3.28 GHz.

As part of the integration of active components with multilayer CPW passive components on a single substrate, MMIC limiters were designed and fabricated. These fabricated limiters employ multilayer technology and include a straight (PH200) limiter, a spiral (PH200) limiter and a spiral (PH120) limiter. These limiter circuits were each designed with the two pHEMT diodes discussed in this work. In order to test how well these fabricated limiters help to block high power level signals from damaging a power-sensitive device, a commercial 30 dB gain power amplifier, with an operating frequency range from 10 MHz to 4.2 GHz, was used in the measurement set-up. The extracted results show that both spiral limiters attenuated more power than the straight limiter. The miniaturised spiral (PH120) limiter design was found to be the most reliable one in providing the best

protection to power sensitive devices. The limiter offers a flat leakage level less than 10 dBm, a maximum insertion loss of 2 dB from 50 MHz to 3.6 GHz and a return loss better than 6 dB. This therefore verifies that with multilayer technology in the limiter modelling, not only can it reduce the circuit size by approximately 20% but it can also improve the performance of the circuit.

To further demonstrate the integration of active components with multilayer CPW passive components, and to highlight some advantages of multilayer technology, simple amplifiers were designed, fabricated and tested. The GaAs pHEMT transistor was first stabilised by employing a shunt resistance technique [55]. Passive components such as inductors and capacitors were employed to design a conjugate matched amplifier at the maximum available gain, which was then traded off in return for better noise performance at an operating frequency of 10 GHz and hence led to the creation of a 10 GHz low-noise amplifier with a maximum gain of above 6.5 dB. Good agreements among the measured, layout and schematic circuit results were achieved.

In conclusion, this research has shown that multilayer CPW technology is highly appropriate for novel compact MMIC applications. It has also shown that low-cost 3D multilayer fabrications can be realised for both passive and active components on the same substrate. The results and analysis of this research will help simplify the whole on-wafer chip production process for compact multifunctional 3D MMICs.

7.2 Future Work

Although the research in this thesis offers an in-depth and improved understanding of the design, modelling and characterisation of 3D multilayer MMIC components, further ideas and recommendations for the continuity of work in this same area of research are suggested.

- During the multilayer fabrication process, it was noticed that some interconnects for circuits such as amplifiers, had relatively very high resistances. This was due mainly to the narrow via-hole widths that connect two metal layers on different levels. In future, when designing interconnect via-holes, they should not be less than 15 μm in width, which would help reduce unwanted parasitic losses in the fabricated circuits.

- In subchapter 5.1 of this thesis, a number of new interconnect designs, including the thin-film microstrip, were designed and characterised up to 50 GHz. Therefore, it would beneficial to fabricate and test some of these new designs and compare the measured results with the modelled results. This research could also be extended by modelling these new structures, by using other polymer-based dielectric materials such as benzocyclobutene (BCB) in place of polyimide.
- New compact CPW-to-TFMS transitions were designed with greatly improved loss performance. It would therefore be useful to fabricate new designs and compare the measured results with their simulation results. Furthermore, one could develop a mathematical theorem for the transition and then later design an application structure to prove it.
- In this work, Schottky pHEMT diodes were briefly discussed and employed in the design of the limiter circuits. In future, it would be useful to develop a large-signal model for the pHEMT diodes. One could further study the Schottky pHEMT diodes integration with a planar/ multilayer dipole antenna to form an RF power detector.
- The low noise amplifier noise figure in this work has only been simulated because of the unavailability of a noise meter for higher frequency ranges. In future, it would be useful to measure its noise figure and compare it with published LNAs.
- Microwave limiter circuits were fabricated, tested and characterised in this work. Therefore future work involving an in-depth study of their non-linearity [113] would be a very useful contribution to microwave research.

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