Novel, Low-Cost, High-Capacitance Nanocomposite Dielectrics for Printed Electronics

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Abstract

Sheida Faraji,
"Novel, Low-Cost, High-Capacitance Nanocomposite Dielectrics for Printed Electronics"
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PhD
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Organic thin-film transistors (OTFTs) have been widely studied because of their promising potential for application in low-cost, large-area and flexible electronics. However, several challenges remain on the way towards practical OTFT devices, such as a high operating voltage (> 20 V) induced by the low charge carrier mobility of organic semiconductors and low capacitance of organic gate dielectrics. A low operating voltage is essential for various OTFTs applications, such as portable displays, radio frequency identification tags (RFIDs), smart textiles and sensors. The key to low voltage operation of OTFTs is reduction of the threshold voltage, inverse subthreshold slope which can be fulfilled by using a high-capacitance gate dielectric with superior interface properties. Since field-effect current is proportional to field-induced charge density, using a gate dielectric layer with high dielectric constant (high-*k*) enhances output current densities at much lower applied voltages. Very thin dielectric layers have reportedly suffered from poor dielectric properties, while very high-*k* gate dielectrics have led to inferior dielectric-semiconductor interface. As a result, unsatisfactory device performance, such as low charge carrier mobility and high gate leakage current, has been obtained. In addition, solution-processability on a variety of substrates and compatibility with most common semiconducting materials make high-*k* dielectric materials an unrivalled candidate for low-voltage, low-cost applications.

Consequently, the aim of this project was to produce a high-quality, high-capacitance gate dielectric with excellent properties which is consistent with cheap, basic solution-processing manufacturing techniques. With great promise in hybrid materials, a novel, high-*k* dielectric material based on alternative organic-inorganic nanocomposites that combine very high dielectric constant values intrinsic to ferroelectric ceramic materials (nanoparticles) with mechanical flexibility, low-cost and easy processing of polymers was developed. Both low- and high-*k* polymer matrices have been used in formulating high-*k* nanocomposite dielectric suspensions. The uniformity of suspensions has been improved by surface modification of nanoparticles in the case of low-*k* polymers, while a combination of polymer choice, solvents and nanoparticle-to-polymer ratio led to homogenous suspensions based on high-*k* polymers. The nanocomposite preparation technique was also unique to this work and gave reproducibly stable nanocomposite suspensions. Finally, ultralow-voltage (~ 1) OTFTs have been successfully demonstrated by integrating nanocomposite bilayer dielectrics using a high-*k* fluorinated polymer. Bilayer dielectrics were formed by (partially) capping the surface of the nanocomposite films with an ultrathin capping layer. The capping layer was the key to the operation of low-voltage OTFTs as it allowed remarkable and advantageous use of the nanocomposite surface roughness while improving the dielectric-semiconductor surface roughness. Ultimately, such nanocomposite bilayers have a potential to pave the way towards low-cost fabrication and integration of low-voltage components and circuits on flexible substrates.

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Acknowledgements

"Many of life's failures are men who did not realise how close they were to success when they gave up."

Thomas Edison

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S. Faraji, L. A. Majewski, "*Novel, Low-Cost, High-Capacitance Nanocomposite Dielectrics for Flexible Electronics"*, IEEE Electron Devices Poster Conference 2013, University of Manchester, Awarded the best poster prize.

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S. Faraji, L. A. Majewski, "*Novel, Low-Cost, High-Capacitance Nanocomposite Dielectrics for Flexible Electronics"*, PGR Poster Conference 2012, School of Electrical and Electronic Engineering, University of Manchester, Awarded 2nd best in EEE school and best industrial (National Grid) poster prizes

Chapter 1

Introduction

1-1- Background

For the past fifty years or so inorganic electronic materials, such as silicon (Si), silicon dioxide (SiO_2) and copper (Cu), have been the backbone of the semiconductor industry. Since the discovery in 1973 of polythiazyl $(SN)_x$, a synthetic polymer possessing inherently metallic conductivity [1, 2], and a decade later, the realisation of the first polymer-based thin-film transistor (TFT) [3], there has been tremendous interest in the development of electronic devices based on organic materials. There is irony in the fact an inorganic polymer, polythiazyl, opened the door to organic electronics.

More recently, great strides in organic electronics – also referred to as plastic or printed electronics- have been made, citing the light-emitting diode (OLED), organic solar cell (OSC) and the organic field-effect transistor (OTFT), as notable examples. However, due to the relatively low mobility of organic semiconductors, OTFTs are not suitable for use in applications requiring very high switching speeds, but could compete in applications requiring large-area coverage, structural flexibility and low-temperature processing. Nevertheless, over the past 25 years, impressive enhancements in device performance have been achieved either by improving the processes used for the fabrication of the transistors or by synthesising new organic materials [4]. Almost incessant research on OTFTs has greatly contributed to the understanding of the fundamental charge transport physics in organic semiconductors. Several important features have come to light, for instance the crucial role of the quality of the dielectric- semiconductor interface and that of the resistance of the source-drain contacts.

Moreover, recent advances, such as the discovery of many key materials, have demonstrated that field-effect mobilities matching that of benchmark amorphous silicon (a:Si) are obtainable. In some cases these mobility values have exceeded 10 cm^2/Vs in thin films of weakly van der Waals - bonded, flexible and solution-processable materials [5]. The improvements OTFTs have undergone with regards to material performance and

device structures have enhanced their current drive capability and switching speed and yielded significant applications, such as high-resolution, flexible displays based on electrophoretic ink, or “e-paper”, and integrated circuits, such as an 8-bit microcontroller [5, 6].

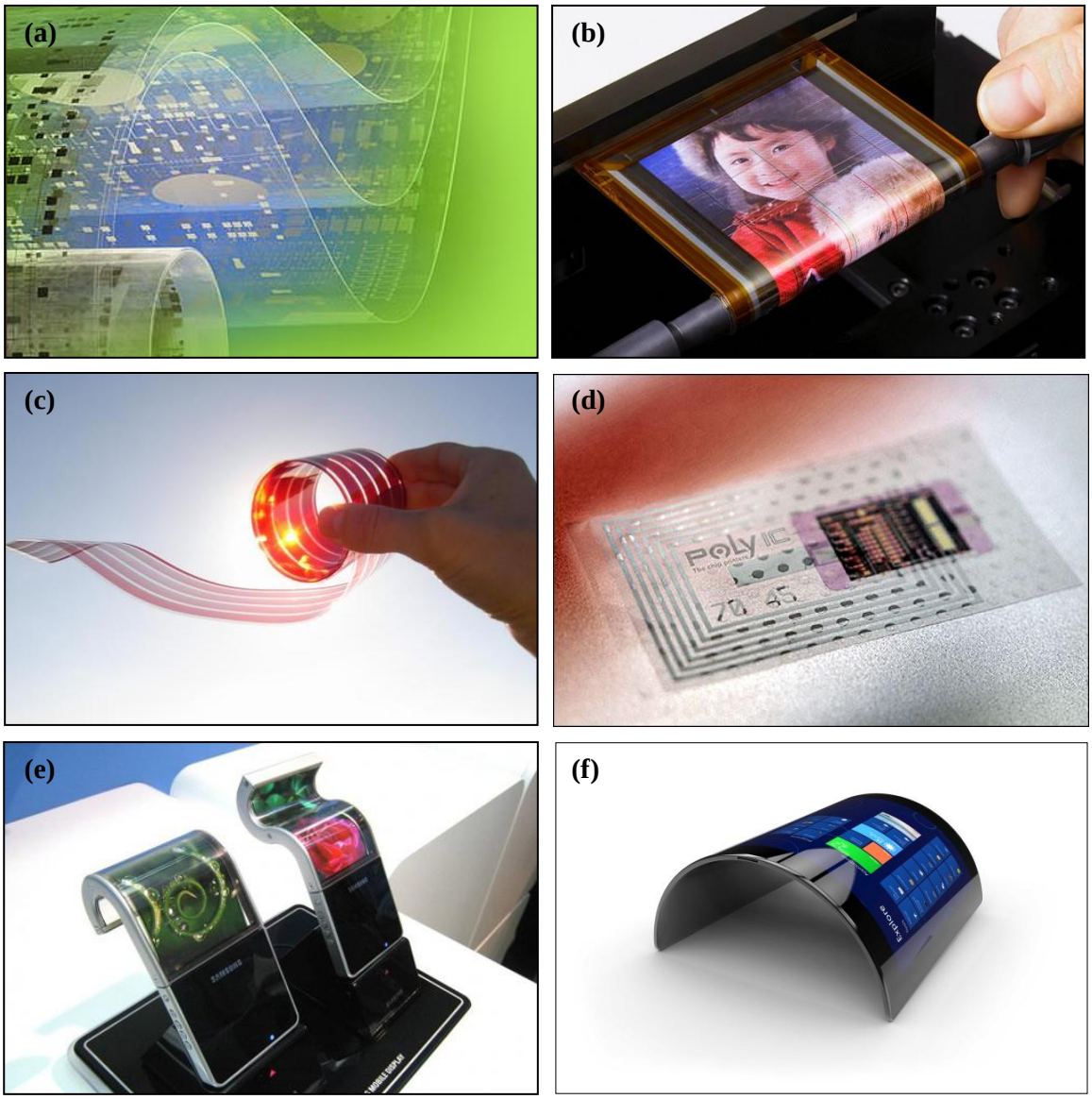


Fig. 1.1: (a) Printed electronics on flexible substrates, image by ASME [7], (b) Rollable OLED display, image by Sony [8], (c) Printed, plastic solar cell, image by Eight19 [9], (d) Printed, organic RFID, image by PolyIC [10], (e) Mobile phones with flexible displays, image by Samsung [11] and (f) Printed, organic curved mobile phone, image by SmartKem [12]

Alongside the development of new devices, notable advances have been made in industrial manufacturing technology. The technology that is believed to have the highest impact on manufacturing costs is the use of soluble organic semiconductors (in addition to dielectrics

and conductive electrodes), combined with large-area printing techniques that could eliminate lithography [4]. The ability to fabricate devices at low temperatures over large areas on materials, such as plastic or paper, has provided unique technologies and generated novel applications [13]. Nowadays, remarkable advances in OTFTs have been achieved and are being applied in emerging technologies (Fig.1.1). Flexible displays, logic circuits, solar cells, chemical and biological sensors, radio frequency identification (RFID) tags and light-emitting devices (LEDs) are some examples [5, 14, 15].

Most recently, OTFTs have also shown particular promise in sensing devices, including biosensors, gas sensors, vapour (aqueous) sensors and pressure sensors (for e-skin applications). Device structures for different sensors are depicted in the following Fig.1.2. In OTFT-based sensors, in which the channel currents can be changed by charge doping or trapping due to the analytes, the active semiconductor layer is exposed to the target analyte [14, 16].

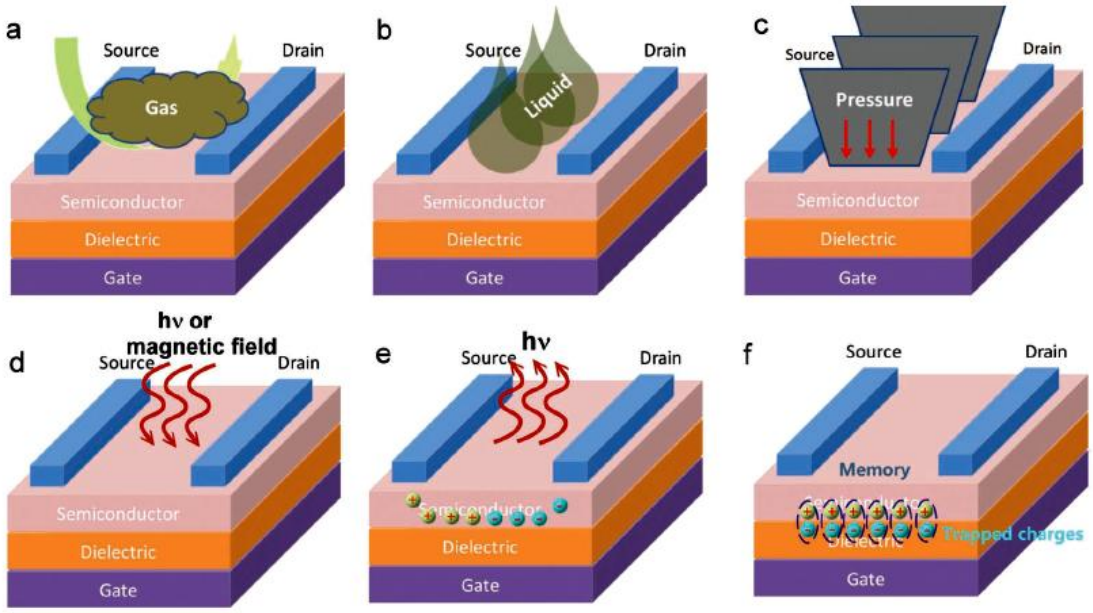


Fig. 1.2: Illustration of device structures and operating mechanisms of an OTFT-based (a) gas sensor, (b) liquid sensor, (c) pressure sensor and (d) a phototransistor or magnetic OTFT, (e) a light-emitting transistor, and (f) a memory cell [16]

OTFT-based sensors exhibit much lower operating voltages, normally less than 1 V, compared to sensors based on organic electrochemical transistors (OECTs). Furthermore, OTFTs can offer a more favourable platform than OECTs because they can be entirely

submerged in aqueous media without the need for an electrolyte medium and an external reference electrode [17]. Taking into account the concept of a pressure sensor, Someya *et al.* [18-20] used OTFTs to create the first flexible, bendable electronic artificial skin (e-skin). They demonstrated a flexible pressure sensor in which OTFTs active matrices were used to read out pressure data from sensors. As illustrated in Fig. 1.3, the researchers wrapped the material (comprising both pressure and temperature sensors) around a mechanical hand to demonstrate the potential applications of e-skin in robotics.

Fig. 1.3: Image of an e-skin demonstrated by Someya *et al.*; OTFTs were used to realise a flexible active matrix to read out pressure images from the sensors [18, 19].

As shown in Fig. 1.3, the device was bendable since all the layers apart from the electrodes were made of soft materials. Despite the low mobility of the organic semiconductors in comparison to that of poly- and single-crystalline silicon, Someya *et al.* reported that the slower speed was likely to be tolerable for most applications of large-area sensors [19, 20].

On the whole, the key challenge in the ubiquitous practicality of OTFTs is the relatively low charge carrier mobility of organic semiconductors and hence their high operating voltage (> 20 V) and subsequent high power consumption. As a result, OTFTs are generally not suitable for low-voltage applications such as aqueous sensors and wearable and portable devices [15]. In the following section, we take a deeper look at the necessity of low-voltage operation in OTFTs (and conventional TFTs) when used in commercial products. Strategies available to date to tackle high operational voltages are mentioned. Lastly, a discussion on the novelty and superiority of our developed material and technique is presented.

1-2- Motivation, Challenges and Research Aim

The search for high dielectric constant (so-called high-*k*) gate dielectric materials has stimulated important research activities in both conventional and unconventional electronics. The inevitable need to increase integrated circuit performance by shrinking the circuit components has required the conventional Si transistor dimensions to be scaled down at a rate according to "Moore's law" [21].

According to the International Technology Roadmap for Semiconductors (ITRS), 2014, the end of the road on transistor scaling is expected sometime around 2022 with a 5 nm node. Following the 22 nm node (in 2012), a 14 nm technology is expected to be reached by semiconductor companies in the 2014 framework. Getting down to 14 nm manifests major obstacles yet to be solved, such as increasing leakage current, increasing power consumption, less tolerance for process variation and increasing cost [22]. Increasing leakage current does not allow further reduction of threshold voltage, which subsequently hinders further operating voltage scaling for the historical speed improvement. As a result, the corresponding higher electric fields generated inside the transistor worsen device reliability and further increase leakage currents [23].

Further scaling down of transistors into the nanometre region is impeded by a number of factors, such as the increased costs of fabrication, the limits of lithography, and overall size of the transistor [23]. More importantly, the traditional materials (SiO_2 as the gate dielectric) used for TFT and capacitor fabrication have reached their fundamental material limits [21]. Therefore, continued downscaling will necessitate the adoption of new technologies and introduction of new materials.

The need for identifying and employing (new) high-*k* dielectric materials manifests its importance on a completely different level in organic electronics. Since the realisation of the first successfully operational organic transistor by Tsumura *et al.* [24], the semiconducting organic materials have been suffering from low charge carrier mobilities and hence could not compete with their inorganic counterparts in terms of charge transport, operational voltage performance and industrial development.

OTFTs, as components of commercial products, need to reliably operate at low voltages for prolonged periods of time [15]. Nevertheless, in spite of the significant progress in optimisation and improvement of performance, operational voltage of these devices is still often too high (> 20 V). This restricts their integration in low-cost, low-voltage electronics, in particular aqueous sensors, low-power electronics and wearable and portable electronics. The necessity of low-voltage operation for health, safety and power consumption concerns is dependent on the specific application [25]. However, for detection of chemical or biological species in aqueous media for environmental monitoring and medical diagnostics, a very low operating voltage (< 1 V) is highly critical to stable operation in aqueous media. This is to avoid electrolytic hydrolysis of water and high ionic conduction through the analyte solution which would happen at high operating voltages [26-28]. Furthermore, consideration must be given to the selection of the organic semiconductor to accommodate performance and stability requirements in aqueous solutions [26, 27].

The high operational voltage in most OTFTs has been attributed to dependence of mobility on the accumulated charge carriers in the OTFT channel. Since this charge is proportional to both the dielectric constant of the gate dielectric and the gate voltage, using high-*k* dielectric materials allows the necessary charge to accumulate at much lower voltages [4]. Lowering the operational voltage of OTFTs is generally achieved by reducing threshold voltage (V_T) and inverse subthreshold slope (subthreshold swing, SS) [29]. Both parameters are strongly controlled by the gate dielectric and the density of charge traps at the dielectric-semiconductor interface. A high-capacitance gate dielectric and a trap-free interface would enable greater charge density to be induced at lower voltages and increase drive capability [30]. Theoretically, high capacitance can be achieved by increasing the *k/d* ratio of the dielectric layer, i.e. reducing the dielectric thickness (*d*) or using dielectrics with high dielectric constant (*k*).

Moreover, one of the main fundamental issues with OTFTs is the lack of a reliable model for predicting the charge transport mechanism for a given semiconductor. It has been largely justified that the performance of OTFTs is mostly governed by morphology of the semiconductor film at the dielectric-semiconductor interface. Hence, the role of dielectric is as important as that of semiconductor. In conventional inorganic electronics, Si is the universal element used in microelectronics not so much because of its intrinsic properties but because of the almost perfect interface it forms with its thermally grown oxide [31, 32].

Thus, in addition to an increased k/d ratio of the gate dielectric layer, identifying suitable dielectric-semiconductor interfaces (rather than semiconductors alone) is a major challenge in the development of low-voltage OTFTs [31]. Moreover, it is necessary for the gate dielectric to be processable from solution and at low temperatures to enable compatibility with flexible plastic substrates and circuitry production via large-scale, roll-to-roll and other fabrication technologies.

To date, low-voltage OTFTs (down to several volts) have been achieved using ultrathin dielectric layers of self-assembled mono- and multi- layers, ultrathin cross-linked low-*k* polymer, solution-processed metal oxides, high-*k* ferroelectric polymers, and organic/inorganic hybrid dielectrics. However, all of these materials have limitations, such as high leakage and small output currents due to thin dielectric layers, and which conspire against achieving practical, flexible, low-voltage operating OTFTs (especially below 1 V). One emerging strategy to increase capacitance and mechanical flexibility in OTFTs is to use composite gate dielectrics consisting of a polymer host and high-*k* inorganic nanoparticles. However, the dielectric constants of these composite materials are generally dominated by the relatively low-*k* polymeric component. To increase composite *k* values, large nanoparticle loadings are necessary; however, this generally results in greatly enhanced surface roughness and subsequent poor electrical properties and mechanical flexibility [33].

Such matters are of particular concern to this research. The primary aim of the project was to develop a method to formulate high-*k* nanocomposites from scratch based on a low-*k* polymer matrix incorporated with various high-*k* nanoparticles, then to evaluate their dielectric properties and characterise the performance of subsequently fabricated OTFTs. Following accomplishment of our initial objective, we went on to present ultralow (< 1.5 V) OTFTs using a novel, high-capacitance nanocomposite dielectric bilayer that had been solution-processed from a suspension of high-*k* polymer matrix filled with high-*k* nanoparticles. By carefully identifying the best combination of fluorinated copolymer, solvents and nanoparticles-to-polymer volume ratio, a reproducible, uniform nanocomposite suspension was made without the need for nanoparticles surface modification. Such high-*k* dielectric layers have led to operation of both vacuum-deposited and solution-processed OTFTs at voltages as low as 1 V.

This achievement is likely to pave the ways towards realisation of various low-voltage devices by simple, cheap and large-area coverage solution-processing techniques which would be attractive to many relevant industries. For instance, most recently, the company Plastic Logic, has announced industrialisation of low power flexible electronics using materials with high *k*, developed by its partner, Solvay Speciality Polymer, and targeting a number of prominent industrial segments. These have included manufacturers of flexible active-matrix organic light-emitting diodes (AMOLEDs) and other displays for mobile phones, sensors, wearables and Internet of Things (IOT) [5].

1-3- Outline of the Thesis

This thesis is presented in such a way to allow easy appraisal of both the topic and the approaches methodically taken towards fulfilling the ultimate aim of this project: successful fabrication and characterisation of low-voltage OTFTs using high-capacitance nanocomposite gate dielectrics. Following this introductory chapter, relevant literature concerning theory of dielectrics, device physics and device operation is reviewed in chapter 2. Methodology and experimental work is thoroughly described in chapter 3, a large portion of which is allocated to nanocomposite preparation and then progressing into device structure and fabrication. Chapter 4 comprises complete results and discussions classified into two main subsections: (i) characterisation of nanocomposite dielectric layers and (ii) evaluation of fabricated OTFTs' performance using corresponding gate dielectrics. In each subsection, nanocomposite dielectrics using low- and high-*k* polymer matrix are separately presented and analysed. Finally, conclusions are presented in chapter 5 alongside discussions on potential future work.

Chapter 2

Literature Review

2-1- Theory of Dielectrics

2-1-1-Polarisation

Insulators or dielectric materials are generally regarded as materials with large band gap and characterised by bound charges and absence of charge transport. However, they exhibit a displacement in their charge distribution under the application of an electric field. The ability of dielectric materials to store energy is attributed to electric field-induced separation and alignment of electric charges, a phenomenon known as polarisation. When a dielectric material is placed in an electric field, its positive and negative charges will be displaced from their original position, electric dipoles are created and aligned with direction of applied field, and the dielectric becomes polarised.

Polarisation is characterised by dipole moments. Dipole moment (***p***) is a measure of the separation between field-induced, displaced positive and negative charges:

$$\boldsymbol{p} = q\boldsymbol{d}, \qquad \text{(Eq. 2.1)}$$

where both ***d*** (the displacement) and ***p*** are vectors pointing from the negative charge (-*q*) to the positive charge (+*q*) [34].

The polarisation vector ***P*** is the polarisation density, the dipole moment (***p***) of unit volume of a material or number of dipoles (*N*) in unit volume:

$$\boldsymbol{P} = N\boldsymbol{p}. \qquad \text{(Eq. 2.2)}$$

As schematically presented in Fig. 2.1, the origins of dielectric polarisation are generally described by four major microscopic mechanisms:

(i) Electronic (or atomic) polarisation

(ii) Vibrational (or ionic) polarisation

(iii) Orientational (or dipolar) polarisation and

(iv) Interfacial (or space-charge) polarisation.

Application of an electric field to each of these mechanisms displaces charges, resulting in a polarisation (induced or aligned dipole moments) in the direction of the applied field. Electronic polarisation occurs in neutral atoms when the electron cloud is displaced by an electric field giving rise to a dipole moment (Fig. 2.1 (a)). This polarisation which is common in all dielectric materials is not permanent and disappears upon removal of the applied electric field.

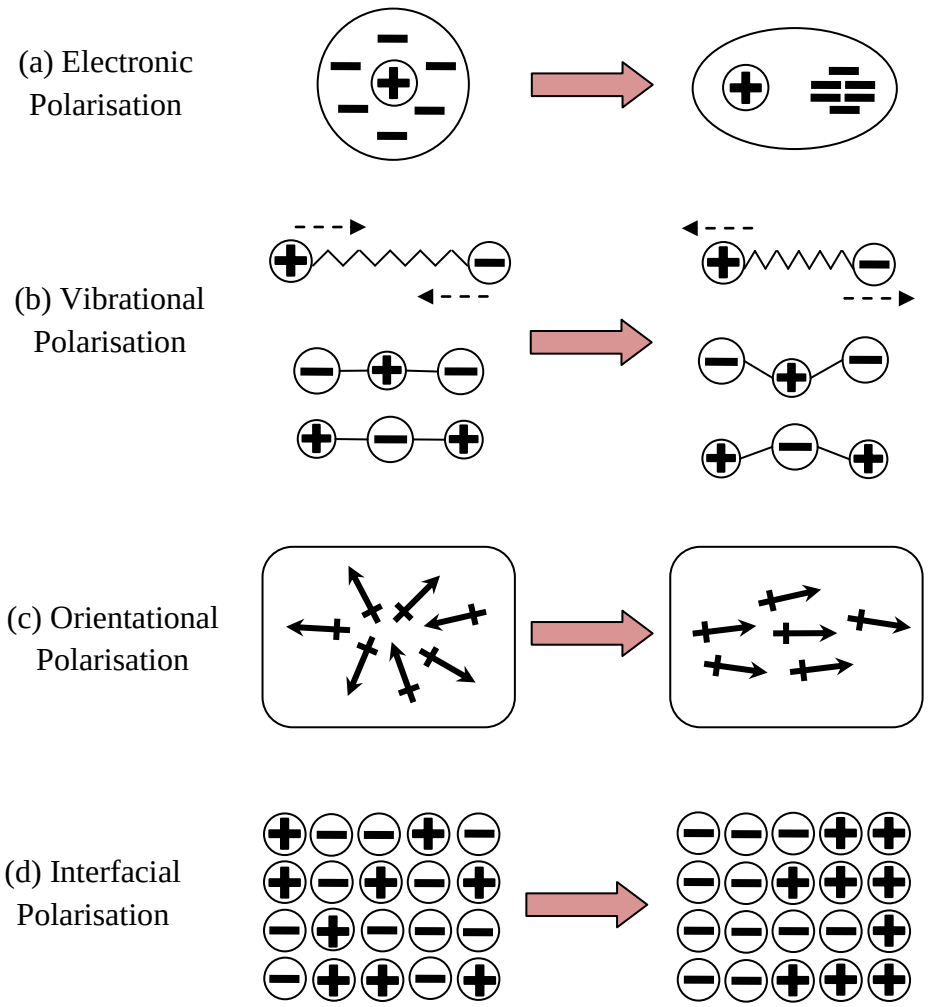


Fig. 2.1: Schematics of (a) Electronic, (b) vibrational, (c) orientational and (d) interfacial polarisation mechanisms.

Vibrational polarisation (Fig. 2.1 (b)), which usually occurs in ionic substances, is related to the displacement of positive and negative ions under applied electric field until the ionic bonding ceases the process and a dipole moment is induced. Similarly, the relative positions of the atoms in non-ionic molecules can be displaced by an applied electric field. Vibrational polarisation is prevalent in inorganic crystals, glasses and ceramics [35, 36].

Orientational polarisation (Fig. 2.1 (c)) is associated with permanent dipoles and is usually observed in polar (ceramic or polymer) dielectrics. In the absence of an electric field, dipoles present in polar dielectrics are randomly oriented with zero net dipole moment. Once an external field is applied, the dipoles tend to align themselves to the direction of applied field resulting in a non-zero net dipole moment and polarisation [37, 38].

Finally, interfacial polarisation (Fig. 2.1 (d)), is related to the presence of migrating charges (electrons or ions) over macroscopic distances in an applied field. These charges tend to be trapped and accumulated at physical barriers such as defects, impurities, grain/phase boundaries and the electrode interfaces where the material has different charge transport properties. The accumulated charges distorting the local electric field gives rise to a change in permittivity. Interfacial polarisation is especially crucial in heterogeneous or multiphase systems such as polymer-ceramic nanocomposites [37].

For a given dielectric material, total polarisation is considered as the collective contribution of all polarisation mechanisms [39]:

$$P_{Total} = P_{Electronic} + P_{Vibrational} + P_{Orientational} + P_{Interfacial}. \qquad \text{(Eq. 2.3)}$$

Depending on the dielectric material, overall polarisation can be accredited to a combination of all or some of these mechanisms. Frequency-dependent behaviour of each of these polarisation mechanisms is discussed in section 2-1-3.

2-1-2-Capacitance and Dielectric Constant

The dielectric constant (k) is an important property directly proportional to polarisation, $\boldsymbol{P}$. It quantifies the ability of an insulating material to store charge when subjected to an electric field [40].

The dielectric constant can be determined using a simple parallel-plate capacitor. Capacitors are one of the essential, dominant passive components with many applications and properties, including filtering, timing, alternating/direct current (AC/DC) conversion, termination, decoupling, and energy storage [41].

In its simplest form (Fig. 2.2), a capacitor consists of two parallel conducting electrodes of area *A* separated by a dielectric of thickness *d*. Applying a differential voltage (*V*) to the electrodes creates an electric field (*E*) between them and charge (*Q*) is stored on each of the conducting plates. The plate with positive charge is called the anode, while the plate with negative charge is referred to as the cathode.

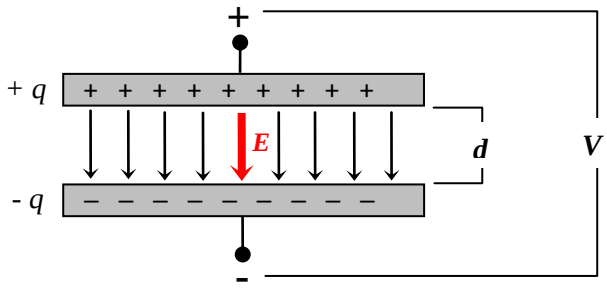


Fig. 2.2: Schematic of a simple parallel-plate capacitor.

The amount of charge (in coulomb) stored in a capacitor is linearly proportional to the electric potential difference *V* applied between the two plates such that:

$$Q = CV, \qquad \text{(Eq. 2.4)}$$

where capacitance *C* is the constant of proportionality.

Capacitance is defined as the charge transferred from one capacitor plate to the other to generate a potential difference of 1 V between the plates [41].

By ignoring the non-uniform electric fields near the edges of the plates (fringe effects), and treating the oppositely charged plates as infinite planes, Gauss's law can be used to calculate the electric field induced between the plates:

$$E = \frac{\sigma}{\varepsilon_o}, \qquad \text{(Eq. 2.5)}$$

where σ stands for charge density ($\sigma = \frac{Q}{A}$) and ε_o is the permittivity of free space (= 8.854 × 10^{-12} F/m). Here, we assume the plates are separated by a distance d in vacuum, i.e. no dielectric exists between the plates. Subsequently, the electric charge stored can be calculated as:

$$Q = \sigma A = \varepsilon_o AE. \quad \text{(Eq. 2.6)}$$

On the other hand, the voltage difference applied between the two electrodes can be expressed as the work done to move a $+q$ from the positive to the negative plate, spaced apart by d:

$$V = \frac{Fd}{q}. \quad \text{(Eq. 2.7)}$$

Considering the electric field at a location as the force experienced by a unit positive charge placed at that location (i.e. substituting $\frac{F}{q}$ by E) and rearranging equation (2.7), the (absolute) electric field induced between two plates of a capacitor as the result of applying a potential difference to them can be re-written as [21]:

$$|E| = \frac{V}{d}. \quad \text{(Eq. 2.8)}$$

The capacitance of a capacitor depends mainly on the geometry of the electrodes and the properties of the dielectric. Rearranging equation (2.4) and substituting with equation (2.8):

$$C_0 = \frac{Q}{V} = \frac{Q}{Ed} = \frac{Q}{\frac{Qd}{\varepsilon_o A}} = \frac{Q\varepsilon_o}{\frac{Qd}{A}} \quad \text{(Eq. 2.9)}$$

$$= \frac{\varepsilon_o A}{d}. \quad \text{(Eq. 2.10)}$$

where C_0 represents the capacitance without a dielectric material. Thus, capacitance is directly proportional to the area A of the conductive plates and inversely proportional to the distance d between them [21]. In real capacitors, the spacing between the two conductive plates is filled with a dielectric material.

In Fig. 2.3, two parallel-plate capacitors with and without a dielectric are depicted. In the absence of a dielectric, when a voltage is applied, an electric field is created inside the capacitor, directed away from the positively charged plate and towards the negatively charged plate. Once a dielectric material is inserted, application of an electric field polarises the dielectric, which in turn produces a secondary field ($\boldsymbol{E}_{Polarisation}$) in the opposite direction to $\boldsymbol{E}$ and decreases the overall effective field ($\boldsymbol{E}_{Effective}$) inside the dielectric (Fig. 2.3).

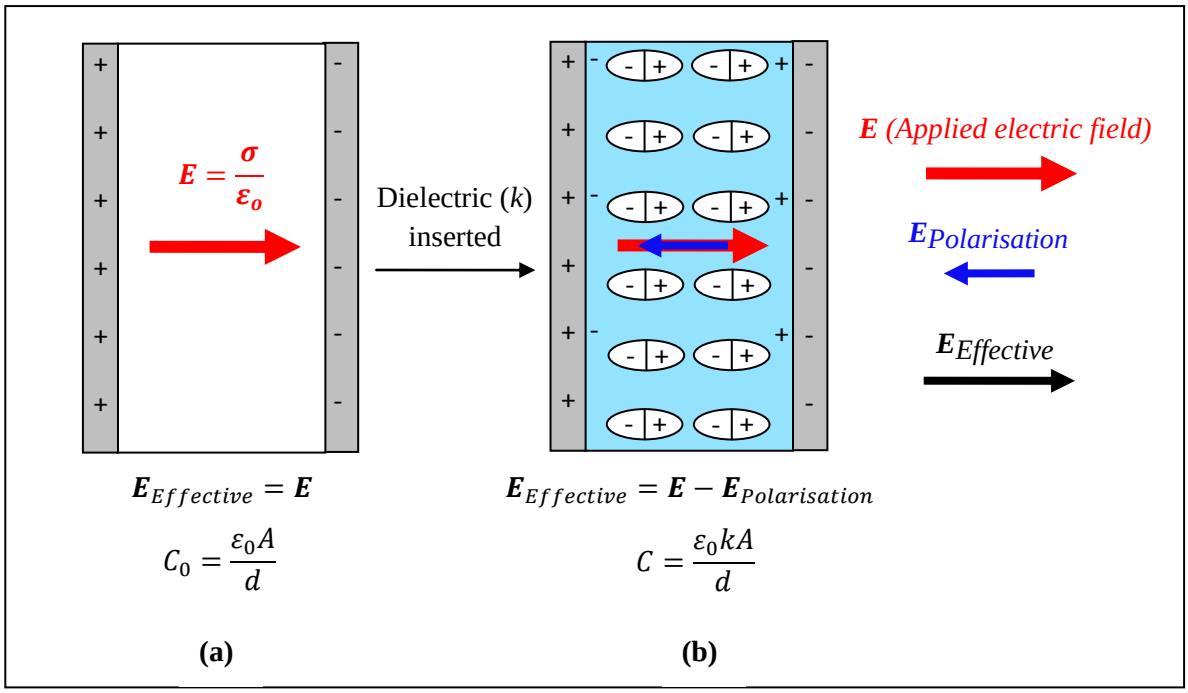


Fig. 2.3: Schematic of a parallel-plate capacitor (a) without and (b) with a dielectric under an applied electric field.

Reduced (effective) electric field inside the capacitor will reduce the potential difference V between the two plates. Since the net charge (Q) is fixed, the capacitance will correspondingly increase (according to equation (2.4)) proportionately by a factor known as the relative permittivity (ε_r) or dielectric constant k:

$$C = kC_0. \qquad \text{(Eq. 2.11)}$$

Since k is a positive value greater than 1, capacitance is supposed to increase in the presence of a dielectric and even further for a dielectric with higher value of k. Thus the dielectric constant (k) is a measure of a material's response to an external electric field and the reduction of the effective electric field inside a capacitor due to dielectric polarisation.

Each dielectric material is characterised by a *k* value intrinsic to that material which varies with temperature, bias, frequency, impurity, and crystal structure to some extent depending on materials' type [41]. The capacitance of a capacitor with a dielectric material between its electrodes can be expressed as:

$$C = \frac{\varepsilon_o k A}{d}. \qquad \text{(Eq. 2.12)}$$

According to this relationship, capacitance is directly proportional to area *A* of the electrodes and dielectric constant *k* of the dielectric, while inversely proportional to the dielectric thickness (or separation of the plates) *d*. Therefore, high capacitance is achievable by utilising dielectric materials of high dielectric constant (so-called high-*k* dielectrics) and/or by reducing the thickness of the dielectric layer. High capacitance is essential to maintain low operating voltages and high output currents in OTFTs and ultimately electronic circuits and systems.

2-1-3-Dielectric Materials in an Alternating Field

The (relative) permittivity of a dielectric material is constant in direct current (DC) field when there is no significant dielectric saturation. However, if a capacitor is driven with a frequency-dependent voltage, the dielectric constant of a dielectric will depend on the frequency of the induced alternating current (AC) [41]. The variation of dielectric constant with frequency is referred to as a dielectric dispersion somewhere in the electromagnetic spectrum, which is governed by dielectric relaxation processes such as Debye relaxation [41]. When a dielectric is placed in an alternating electric field, the dipoles attempt to maintain alignment with the field. This process requires a finite time, which is different for each polarisation mechanism (described in 2-1-1).

In Fig. 2.4, the variation of polarisation with frequency for a hypothetical material that exhibits all the four polarisation mechanisms is illustrated [42]. At small frequencies, all four polarisation mechanisms are present. At optical frequencies, only electronic polarisation is operative. Orientational and vibrational polarisations are small at high frequencies because of the inertia of the molecules and ions. The peaks occurring at ~ 10^{13} and ~ 10^{15} Hz are due to resonance effects, where the external field is alternating at the natural vibrational frequency of the bound ions or electrons respectively [40].

As shown in Fig. 2.4, in the frequency region above ultraviolet, electronic polarisation loses its response and k becomes ε_0.

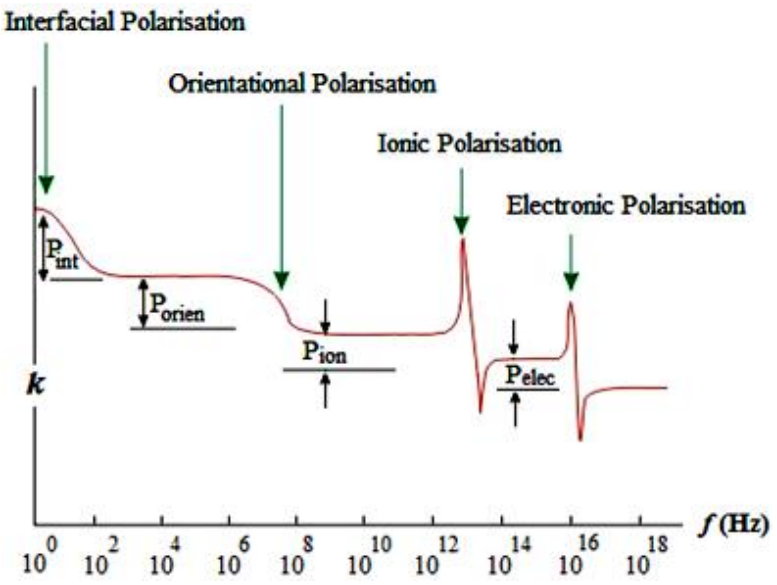


Fig. 2.4: Frequency dependence of dielectric constant. Redrawn from [42].

Under an AC field, the permittivity of a dielectric material can be expressed as a frequency-dependent complex number, which manifests the dielectric loss [43]:

$$\varepsilon = \varepsilon' - j\varepsilon'' = |\varepsilon| e^{-j\delta}, \qquad \text{(Eq. 2.13)}$$

where ε' denotes the real part of dielectric permittivity (often referred to as the relative permittivity, k), ε'' is the imaginary permittivity, so-called dielectric loss factor, and δ is the dielectric loss angle.

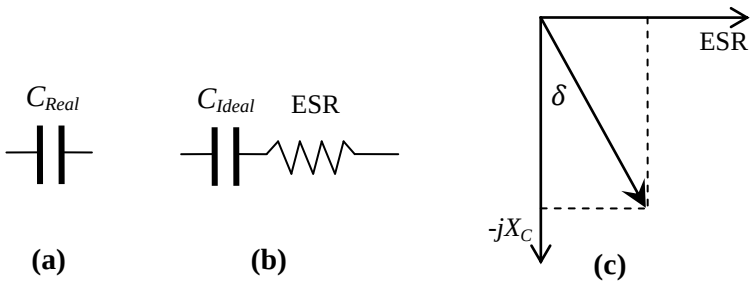


Fig. 2.5: Schematic of (a) real and (b) ideal capacitor, (c) schematic illustrating the dielectric loss angle.

As depicted in Fig. 2.5, δ is the angle between the ESR (equivalent series resistance representing losses in a real capacitor) and reactive (lossless) components in an impedance plane. Further discussion on dielectric loss and other characteristics of dielectric materials is given in the following section 2-1-4.

2-1-4-Other characteristics of a dielectric material

In addition to the dielectric constant, dielectric materials possess other important properties, which will considerably influence the overall performance of the capacitors, transistors and electronic systems in which those materials are utilised. Dielectric loss is one of the other characteristics of dielectric materials. According to Johnson *et al.* [43], almost all dielectric materials exhibit two kinds of dielectric loss. One is the conduction loss resulting from leakage of current through a (thin or porous) dielectric layer. The other one is the loss due to the rotation of the atoms/molecules in an alternating electric field.

At relaxation frequency (f_c), the dipoles are only just able to reorient themselves in time with the applied field. At this frequency, the dielectric becomes imperfect and the capacitor loses a fraction of energy by power dissipation, becomes a so-called lossy capacitor. The dielectric loss is at its maximum when the frequency of the external field coincides with the relaxation frequency of a given polarisation mechanism. At frequencies above the relaxation frequency, the diploes are no longer able to keep up with changes in the applied field. The contributing polarisation mechanism becomes effectively "frozen" and no longer contributes [39, 40].

The dielectric loss, which is a material property independent of the geometry of capacitor, is usually expressed as the loss tangent (tan δ) or dissipation factor (DF):

$$\tan\delta = \mathrm{DF}. \qquad \text{(Eq. 2.14)}$$

Loss tangent can be expressed as:

$$\tan\delta = \frac{\varepsilon^{"}}{\varepsilon'} + \frac{\sigma}{2\pi f \varepsilon'}, \qquad \text{(Eq. 2.15)}$$

where $\varepsilon' = \varepsilon_o \varepsilon_r$ and σ is the electrical conductivity and f is the frequency [36].

Dielectric breakdown strength is another important characteristic of dielectric materials. For any dielectric material, there is a threshold electric field, which can be applied while the material still maintains its insulating properties. Beyond this threshold electric field, irreversible (permanent) breakdown of the dielectric accompanied by the onset of an intensive, disruptive flow of charges occurs. The minimum electric field responsible for such dielectric breakdown phenomenon is called the breakdown field or breakdown strength (E_B) [41]. Various factors are considered to influence the dielectric breakdown strength, including temperature, defects, thickness, area and volume of the material, duration of time for which the dielectric is subjected to electric field, surface conditions and the method of placing the electrodes, area of the electrodes, composition of the electrodes, humidity and other contaminations, aging and mechanical stress [37].

Capacitors comprising dielectric materials are commonly used in energy storage applications. The electrical energy stored in a capacitor is equal to the work done to remove charges from the positively charged plate to the negatively charged plate, so that the maximum stored energy is:

$$W_{max} = \frac{1}{2}\frac{Q^2}{C} = \frac{1}{2}CV_B^2, \qquad \text{(Eq. 2.16)}$$

where V_B is the dielectric breakdown voltage of the capacitor. The maximum energy storage density (energy per volume) can be derived from equation (2.16) by substituting C and V with equation (2.8) and (2.12) respectively:

$$U_{max} = \frac{1}{2}\varepsilon_o k E_B^2. \qquad \text{(Eq. 2.17)}$$

Ideally, a dielectric material is expected to exhibit high dielectric breakdown strength, high dielectric constant and low dielectric loss and dissipation factor [21]. Such dielectric materials yield high-capacitance necessary for high energy storage applications and high-performance, low-voltage operations. According to equation (2.12), high capacitance can be obtained by using high-k dielectric materials or reducing the dielectric thickness d. Nonetheless, both maximising k and minimising d leads to practical problems.

A thin, fragile dielectric may lead to increased leakage currents through the insulation layer, and hence gives rise in power consumption and shortens the device lifetime. Whilst, high-*k* (polar) insulators introduce undesirable effects at the semiconductor-insulator interface and increase the operating voltage. Therefore, a crucial step is to develop a dielectric material (compound) that satisfies all mechanical and electrical properties required in high-performance devices.

2-1-5-Ferroelectricity

The discovery of ferroelectricity in single-crystal materials (Rochelle salt) in 1921 [44] followed by multiple, concurrent work established ferroelectric properties as the source of high dielectric constant in polycrystalline ceramic barium titanate ($BaTiO_3$) [45, 46]. Such work paved the way for a continuous series of new materials, technology developments and significant industrial applications exploiting ferroelectric phenomena [47].

When the polarisation of a dielectric can be altered by an external electric field, it is called a ferroelectric. Since all ferroelectrics are a subset of the polar crystal classes, they are also pyroelectric and piezoelectric and can be used for applications in which corresponding behaviours are desired [48]. As illustrated in Fig. 2.6, ferroelectrics are encircled by spontaneously polarised pyroelectrics.

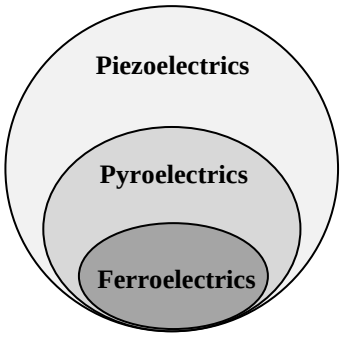


Fig. 2.6: Subcategorical schematic of piezoelectric, pyroelectric and ferroelectric materials.

In contrast with piezoelectrics which produce a polarisation under stress, pyroelectrics develop a spontaneous polarization (formation of permanent dipoles) following a change in temperature. Similarly, ferroelectrics possess spontaneous dipoles. Nonetheless, unlike pyroelectrics, dipoles in a ferroelectric material are reversible by an electric field of some

magnitude less than the dielectric breakdown field of the material. Therefore, existence of a spontaneous polarisation and ability of reorienting the polarisation are two essential criteria to class a material as a ferroelectric [47].

The variation of polarisation with applied electric field is not linear in a ferroelectric material. The key property of ferroelectrics is spontaneous polarisation (giving a dipole moment), the direction of which can be reversed by application of an external electric field. This property is specifically characterised by a hysteresis loop in a plot of 'polarisation vs. electric field' as illustrated in Fig. 2.7 [49].

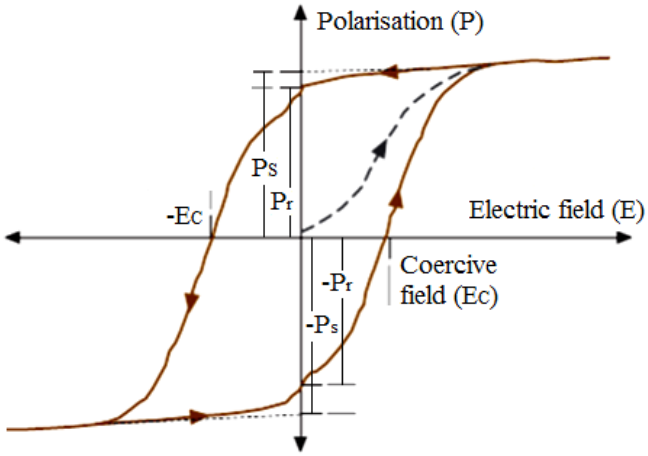


Fig. 2.7: Illustration of the ferroelectric hysteresis loop [49].

As the electric field is increased from zero, the dipolar regions (domains) start to align which correspondingly gives rise to increased overall polarisation (P) in the crystal. At certain field strength, polarisation reaches a saturation point at which the only further increase in P occurs due to relative permittivity of the material. Extrapolation of this line back to the abscissa gives the saturation value of the spontaneous polarisation (P_s). Removing the electric field does not bring polarisation back to zero but leaves a remanent polarisation (P_r), which is usually slightly less than P_s. The crystal cannot be completely depolarised unless a negative field is applied to reduce the polarisation until it reaches zero at the coercive field ($-E_c$). In order words, E_c is the critical electric field for reversing the polarisation. If the field is more negatively increased, it eventually causes a reverse saturation polarisation ($-P_s$) to develop.

When the field returns to zero the crystal is left with a negative remanent polarisation ($-P_r$). Increasing the field once more, increases polarisation from $-P_r$ to zero at E_c, and then up to $+P_s$, resulting in completion of the ferroelectric hysteresis loop. This hysteresis loop is also drawn to present the electric displacement (D) in crystals due to polarisation as a function of electric field (E), and hence often referred to as D-E loop [50].

The ability to switch the polarisation between two states (and presence of the hysteresis loop) makes ferroelectrics highly regarded as emergent materials for new technology applications such as memory-storage elements, piezoelectric transducers and sensors [49]. Moreover, due to the potential to maintain high concentrations of electrical charge as a result of high polarisation, ferroelectric materials are attractive in supercapacitors and low voltage transistors. An overview of ferroelectric and paraelectric ceramic materials, their properties and their application as high-k fillers in high capacitance nanocomposites, is given in the following section 2-2.

2-2- Overview of Alternative High-*k* Dielectric Materials

Dielectric materials can be classified into different categories depending on type of behaviour or property interested to be studied. Based on their polarity, two broad classes of dielectrics can be realised as polar and non-polar. Polar dielectrics possess permanent electric dipole moments with or without the presence of an electric field. The orientation of polar molecules is random in the absence of an external field exhibiting zero net dipole moment. Once an external electric field is applied, a torque is set up that causes the dipole moments to align with the direction of the applied electric field and polarises the dielectric. The aligned molecules then generate an internal electric field that is opposite to the overall applied field but smaller in magnitude (Fig. 2.3). On the contrary, non-polar dielectrics do not have permanent electric dipole moment, but electric dipole moments can be temporarily induced once the material is placed in an externally applied electric field. In normal dielectric materials, removing the electric field would result in loss of polarisation.

With regards to polarisation vs. electric field behaviour, dielectric materials are inclusively categorised into linear and nonlinear. In linear dielectric materials (such as diamond), polarisation increase linearly with the applied electric field. Hence, the slope of the polarisation curve (as an indication of dielectric permittivity) is constant.

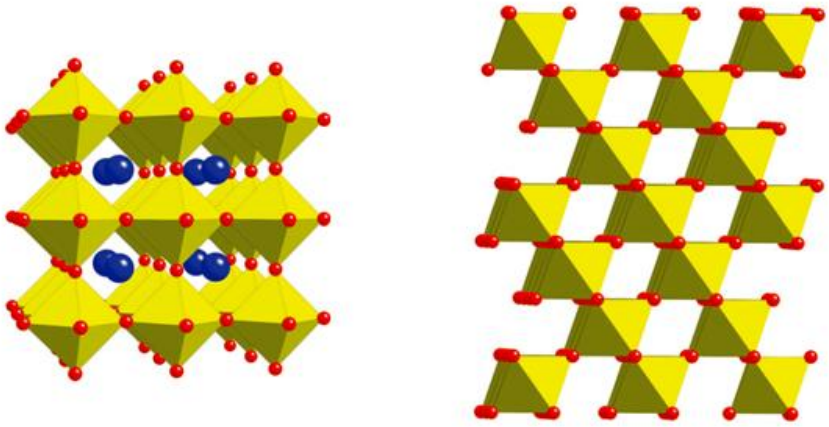
On the other hand, nonlinear dielectric materials such as paraelectrics (Al_2O_3, polypropylene polymer), ferroelectric ($BaTiO_3$, polyvinylidene fluoride (PVDF) polymer) and antiferroelectric ($PbZrO_3$) materials, exhibit enhanced polarisation (and polarisation saturation). In these materials, dielectric permittivity is no longer constant as in linear dielectric but is a function of the externally applied electric field. Further study on ferroelectric and paraelectric materials is given in the following section 2-2-1.

2-2-1-Inorganic Dielectrics: Ferroelectric Ceramic Materials

Ferroelectrics and paraelectrics are the two major classes of dielectric materials. The distinctive difference between ferroelectric and paraelectric materials is the existence of a residual polarisation after the field is removed in the former [51, 52]. Ferroelectric materials are widely used in bulk capacitors and transducers, and are promising dielectrics for integration in the micro- and nano-electronic industry [48]. Ferroelectric materials usually have a transition temperature, so-called Curie temperature (T_c), at which a ferroelectric-to-paraelectric phase transition occurs [50].

In the paraelectric state, as the temperature approaches T_c, the dielectric constant, obeying the Curie–Weiss law, is amplified to largest values attainable. Hence, they are highly suitable for applications in which transient charge storage is required, such as ferroelectric random access memories (FeRAMs) and as decoupling capacitors in power distribution systems [48]. In the ferroelectric state, below the ferroelectric transition temperature (T_c), the ability to reorient the spontaneous polarisation makes them attractive candidates in non-volatile memory elements.

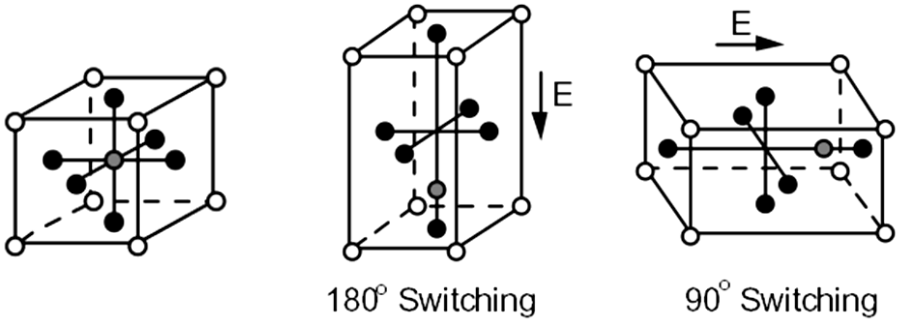
Single crystal or crystalline ceramic metal oxides with ABO_3 perovskite structure are by far the most important, widely used category of ferroelectric materials. They exhibit excellent dielectric properties (such as high-*k*, low dielectric loss and large tunability) and are ideal candidates for fabricating high capacitance non-volatile memory devices and transistors capable of low-voltage operation [53]. Since the discovery of ferroelectric $BaTiO_3$ ($k \sim 3{,}000$), dielectric materials based on such ceramics have been extensively used [54]. The structural chemistry of ABO_3 perovskites can be visualised in terms of close packing of AO_3 layers, where the B cations occupy all the resultant BO_6 oxygen octahedra.



(a) **(b)**

Fig. 2.8: (a) Ideal cubic ABO_3 perovskite structure viewed along (110) to highlight close packing of AO_3 layers and resultant corner sharing of the BO_6 (yellow) octahedra, (b) perspective view featuring corner sharing of the octahedra. Blue and red spheres are A and O respectively [55].

As demonstrated in Fig. 2.8, the structure is called a cubic perovskite when the AO_3 layers are arranged in cubic close packing and the BO_6 octahedra (coloured in yellow) are connected exclusively through corner sharing. In an ideal cubic perovskite, the A and B cations realise their equilibrium bond distances to oxygen (O) without imposing any distortion of the unit cell, and $d_{A-O} = \sqrt{2(d_{B-O})}$ [55].



(a) **(b)** **(c)**

Fig. 2.9: Crystalline structure of a ABO_3 perovskite in (a) Cubic non-ferroelectric phase and (b) and (c) tetragonal ferroelectric phases under an applied electric field (*E*) where the centre atom is displace along the crystalline axis depending on the direction of *E* [56].

As illustrated in Fig. 2.9, upon the application of an external field, the ferroelectric material perovskite crystal undergoes a transition from cubic to tetragonal phase. This transition is brought about due to the displacement of the centre atom (B) in the direction of applied electric field and is maintained even after removing the external field [53].

Examples of ferroelectric perovskite ceramic materials are barium titanate ($BaTiO_3$), strontium titanate ($SrTiO_3$), lead titanate ($PbTiO_3$) and barium strontium titanate ($BaSrTiO_3$) whose dielectric constants are on the order of thousands, significantly higher than those of paraelectric materials such as SiO_2, Al_2O_3 and Ta_2O_5. However, since dielectric properties of ferroelectrics are typically a strong function of temperature, frequency, film thickness and bias, significant nonlinearities are expected in their performance [52]. Moreover, ferroelectric perovskite metal oxides impose various limitations, such as expensive deposition equipments and high temperatures required for sintering these materials, as well as high density, brittleness and challenging processing conditions, all of which make them incompatible with low-cost, (flexible) plastic electronics. In addition, large leakage current under relatively small applied bias and low dielectric strength restricts operating voltages [36].

2-2-2-Organic Dielectrics: Polymer Materials

Polymers such as epoxies, benzocyclobutenes (BCB) and polyimides (PI) have been largely used as dielectrics in microelectronic industry by various coating methods followed by moderate temperature cure [57]. The first successful attempt to utilise polymeric organic materials as gate dielectrics in OTFTs was reported by Peng *et al.* in 1990 [58]. They fabricated devices with a variety of organic polymer insulators using evaporated R-sexithienyl (R6T) films to serve as the semiconductor.

Similar to ceramic materials discussed in the preceding section, polymers have some advantage and disadvantages. Most polymers are paraelectric resulting in capacitance stable with regard to temperature and frequency. In addition, they possess good mechanical property, easy processing, low dissipation factor and high dielectric break down strength. However, most conventional polymers, examples of which are presented in Fig. 2.10, suffer from low dielectric constants. Therefore, a relatively thin layer of such polymers is required to obtain reasonably high values of capacitance; not generally practical and hence

not suitable for application which require super high-capacitance and/or low operating voltages.

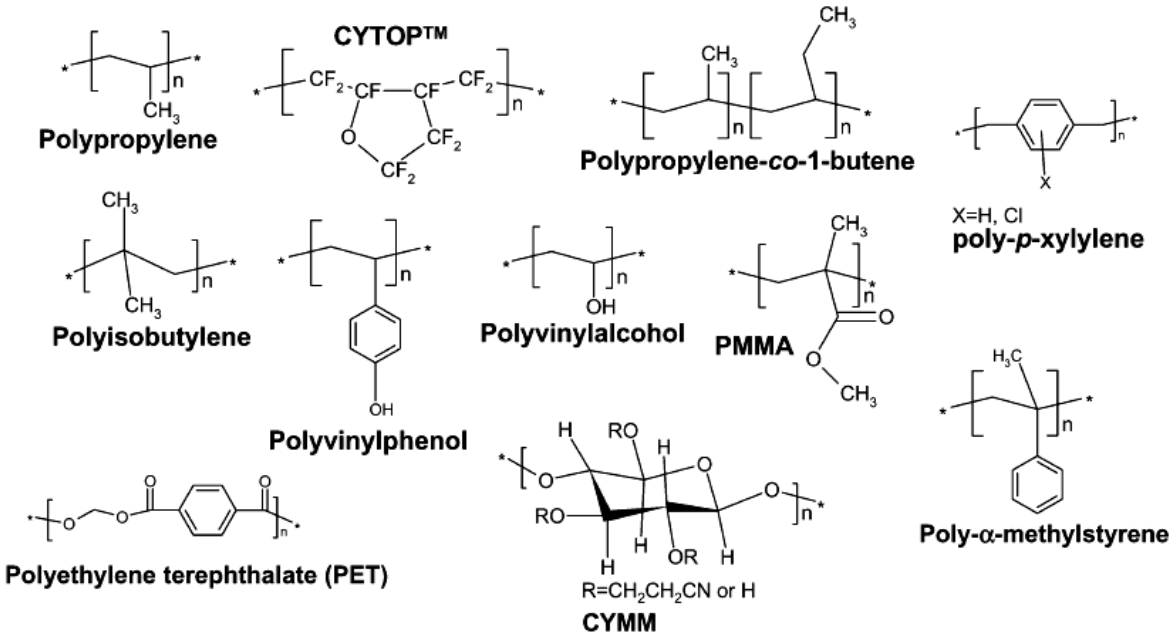


Fig. 2.10: Most common gate dielectric materials [59].

On the contrary, a group of polymers with a polar backbone, so-called ferroelectric polymers (which have been utilised in this work) possess higher values of dielectric constant (~ >10) due to their polar backbone. More details on examples and properties of such polymers can be found in section 3-1-2-2.

2-2-3- Hybrid Dielectrics: Ferroelectric Ceramic/Polymer Nanocomposite Compounds

Basically, a composite material is a mixture of two or more component materials behaving like one system with combined properties of multiple constituents. As already outlined, individual classes of dielectric materials, i.e. ferroelectric ceramics and polymers, have a number of drawbacks restricting their integration as high-*k* materials in certain applications. For instance, high-*k* ceramics frequently lack stability while allowing very low voltage operation, whereas low-*k* polymers offer low leakage currents and high stability but require higher operating voltages [21].

Taking into account and benefiting from advantages both classes of material offer, a new approach that incorporates inorganic ceramics (fillers) into organic polymeric materials (host/matrix) to form a high-*k* dielectric is launched. These hybrid dielectric materials, so-called nanocomposites, combine high dielectric constant of ceramic materials with high breakdown strength, mechanical flexibility, and easy processability of the organic polymers [21]. Moreover, mechanical flexibility and tunable properties of ceramic/polymer nanocomposites (NCs) make them promising choices to achieve high capacitance in energy storage devices and in high performance, low-voltage electronic devices [41].

Nanocomposites are different from conventional composites, since they comprise (high-*k*) ceramic nanoparticle fillers (so-called nanofillers) instead of bulk or sub-micron sized (ferroelectric) ceramics. It is well understood that nanoparticles behave differently from that of the bulk. As previously mentioned, perovskite metal oxides exhibit ferroelectric phase in the bulk which arises due to displacement of A and B atoms from their centrosymmetric position in the unit cell. Nonetheless, at the nanoscale, the ferroelectricity cannot be sustained and such ceramic metal oxides only behave like a dielectric material with a relatively high *k* value [48]. This is generally the case for ferroelectric materials at nano dimensions since the regular domain structure in ferroelectric nanocrystallines becomes energetically unfavourable due to the energy penalty for forming domain walls. Moreover, as a result of large depolarisation field, single domain structures would be unstable and hence deviations from ferroelectric bulk properties are expected as the size of the grain/crystal reduces [60].

The lower *k* of polymer matrix inevitably counteracts the higher *k* of nanoparticles to some extent. Consequently, nanocomposites have a dielectric constant *k* higher than that of the polymer host, but lower than that of the nanoparticle fillers. Considering a simple rule of mixture, *k* of a nanocomposite can be modulated by incorporating constituent fillers (and/or polymer matrix) of different dielectric constants. Various theoretical models have been reported across the literature to predict dielectric constant of nanocomposite materials. The Lichtenecker logarithmic law of mixing is generally used to calculate effective dielectric constant, ε_{eff}, of a composite material consisting of two components as given by:

$$log\ \varepsilon_{eff} = (1-\varphi)\ log\ \varepsilon_m + \varphi\ log\frac{\varepsilon_f}{\varepsilon_m}, \qquad \text{(Eq. 2.18)}$$

where ε_m and ε_f represent the dielectric constants of each component, i.e. polymer matrix and nanoparticle filler respectively, while φ is the volume fraction of fillers (so-called inclusions). It is worth mentioning that *k* and *ε* are interchangeably used. The mixing law is the intermediate form of series and parallel combination laws for dielectric mixture. Lichtenecker's model is supported by experimental studies on heterogeneous dielectric systems, even for anisotropic media. Nonetheless, it neither takes into account the shape of the fillers nor the interactions between them [61].

Assuming filler nanoparticles to be spherical and randomly distributed in a 3D polymer matrix, ε_{eff}, can be theoretically estimated using the Bruggeman model as given by [62]:

$$v_f\left[\frac{\left(\varepsilon_f-\varepsilon_{eff}\right)}{\left(\varepsilon_f+2\varepsilon_{eff}\right)}\right]+v_m\left[\frac{\left(\varepsilon_m-\varepsilon_{eff}\right)}{\varepsilon_m+2\varepsilon_{eff}}\right]=0, \qquad \text{(Eq. 2.19)}$$

where v_f, v_m, ε_f and ε_m are the volume fractions and dielectric constants of the filler and the matrix respectively. Accordingly, a high-*k* nanocomposite can be obtained by increasing volume fraction of the constituent nanoparticles. Bruggeman model takes into account volume fraction of filler and polymer matrix and interactions between the fillers.

Another theoretical model widely employed to estimate dielectric constant of nanocomposites is the Maxwell model, applying the following equation [63]:

$$\varepsilon_{eff}=\varepsilon_m\frac{2\varepsilon_m+\varepsilon_f+2\varphi(\varepsilon_f-\varepsilon_m)}{2\varepsilon_m+\varepsilon_f-\varphi(\varepsilon_f-\varepsilon_m)}. \qquad \text{(Eq. 2.20)}$$

In general, the enhanced dielectric constant of a ceramic/polymer nanocomposite is predominantly attributed to the relatively higher *k* of ceramic nanoparticles compared to that of polymers. Higher filler volume fractions are generally necessary to achieve high-*k* nanocomposites, although there exists an upper limit above which quality and dielectric properties of nanocomposites worsen. According to Bai *et al.* [64], when the volume fraction of the ceramic powder was up to 60 %, the measured dielectric constant of the composite became much lower than that predicted. They attributed this effect to increased porosity of the nanocomposite film on one hand and non-uniform distribution of the (powder) filler due to agglomeration on the other hand.

Kim *et al.* [65] investigated the role of the volume fraction of high permittivity nanoparticles on the dielectric properties (permittivity, dielectric loss, and breakdown strength) of nanocomposites in order to determine the optimum volume fraction(s).They reported on decreased effective permittivity with increasing nanoparticle volume fraction for nanoparticle volume fractions of greater than 50 %. According to Kim *et al.* [65], the presence of the air voids (in the interface between the fillers and the polymer matrix) significantly lowered the breakdown strength of the nanocomposite at higher volume fractions of fillers due to the low breakdown strength of air (~ 3 V/μm). As shown by Almadhoun *et al.* [67], at high filler loading, percolative pathways are created through the aggregated fillers which lead to increased leakage current density and reduced dielectric breakdown strength [65, 67, 68]. They assigned this effect to an increase in the filler-polymer matrix interfacial area within the nanocomposite structure, where nanoparticle inclusions modify charge transport and result in a leakage pathway [67]. Dang *et al.* [66] also reported on gradual increase in conductivity of the nanocomposites with the volume concentration of nanoparticles. Consequently, dielectric constant can only be enhanced to a certain extent while maintaining leakage currents acceptably low [67].

In comparison with conventional composites, properties of nanocomposites are highly influenced by the interfacial properties between nanoparticle fillers and the polymer matrix. The small size of nanoparticle fillers leads to an exceptionally large interfacial area in the nanocomposites. The interface controls the degree of interaction between the (nano-) filler and the polymer matrix, and thus controls the properties of the nanocomposites. The high surface energy and surface-to-volume ratio intrinsic to nanoparticles usually gives rise to agglomeration and phase separation from the polymer matrix, particularly at higher filler loading. Therefore, by simply mixing nanoparticles in a polymer matrix, an inhomogeneous mixture with poor processability, increased porosity and decreased densification is generated [65, 66]. Hence, one of the key challenges in formation of a high quality nanocomposite layer with excellent dielectric properties is to control the homogeneity and stability of the nanocomposite suspension. Therefore, promoting uniform dispersion and minimising aggregation of nanoparticles when incorporated into the polymer matrix is crucial in nanocomposite preparation. Although the impact of k and volume fraction of nanoparticle filler on overall k value of the nanocomposite prevails, using polymer matrix of higher dielectric constant is highly likely to result in enhanced k value of the nanocomposite.

2-2-3-1- Nanoparticles Dispersion and Surface Modification

As previously referred to, the properties of nanocomposites are significantly influenced by both the dispersing degree of nanoparticles (NPs) in the host polymer matrix and the interfacial interactions between the polymer and the inorganic filler [69]. The interfaces created when dispersing a high surface energy particle into a low surface energy polymer make uniform dispersion of the particles problematic and generate paths that can conduct charge [70]. Thus, one of the biggest challenges in nanocomposite preparation is to control interfacial properties between nanofillers polymer host to obtain high quality, uniform and homogenous nanocomposites, particularly at high nanoparticle volume fraction.

From the theoretical point of view, Brownian motion is one of the most important phenomena when it comes to handling of nanoparticles in suspension/fluid. The 3-dimensional mean transfer distance (Δx) of a nano-sized particle by the Brownian motion can be stated as [71]:

$$\Delta x = \sqrt{6 D_B \Delta t}, \qquad \text{(Eq. 2.21)}$$

where D_B and Δt are Brownian diffusion coefficient and time during which diffusion occurs respectively. The Brownian coefficient is defined as:

$$D_B = \frac{kT}{3\pi\mu d_p}, \qquad \text{(Eq. 2.22)}$$

where k is Boltzmann constant, T is the absolute temperature, μ is the viscosity of the media and d_p is the particle diameter.

From these two equations, one can ascertain that the Brownian motion increases as the particle size decreases. Consequently, nanoparticles have strong tendency to attract and collide with other nanoparticles in close proximity regardless of the media. Moreover, the strong van der Waals force working among nanoparticles induces further agglomeration, if no potential barrier is present amongst nanoparticles [71]. Therefore, when preparing nanocomposites, it is important to develop techniques to avoid aggregation and control dispersion of nanoparticles when incorporated into the polymer matrix.

Surface modification (so-called passivation or functionalisation) of nanoparticle fillers with appropriate coupling agents is one of the most widely used methods to enhance nanoparticle-polymer compatibility. It also serves to prevent agglomeration of nanoparticles, promote interfacial interactions between nanoparticles and polymer matrix and improve the uniformity and stability of the nanoparticles dispersion. As a result, a more stable, homogenous nanocomposite is obtained which ultimately enhances the dielectric constant of the nanocomposite. Better nanoparticle-polymer compatibility may also minimise defects/voids in the nanocomposite that can degrade the breakdown strength and overall energy density of electronic devices [65, 67, 72, 73].

Self-assembled monolayers (SAMs) are coupling agents (referred to as surfactants) that have been reportedly employed in surface modification of nanoparticles [74, 75]. Kim *et al.* [74] modified the surfaces of $BaTiO_3$ nanoparticles (BT) with 2-2-2-methoxyethoxyethoxyethyl-phosphonic acid (PEGPA). Their aim was to formulate high volume fractions of PEGPA-BT:cross-linked poly (vinyl phenol) (PVP) nanocomposites (Fig. 2.11). Pentacene devices fabricated with such nanocomposite dielectrics, as shown in Fig. 2.11, exhibited significantly reduced leakage current density and increased dielectric constant compared to those with non-modified nanoparticles. Kim *et al.* attributed the improved device performance to better dispersion of BT nanoparticles inside the PVP and the corresponding high quality, more uniform nanocomposite dielectric films [74].

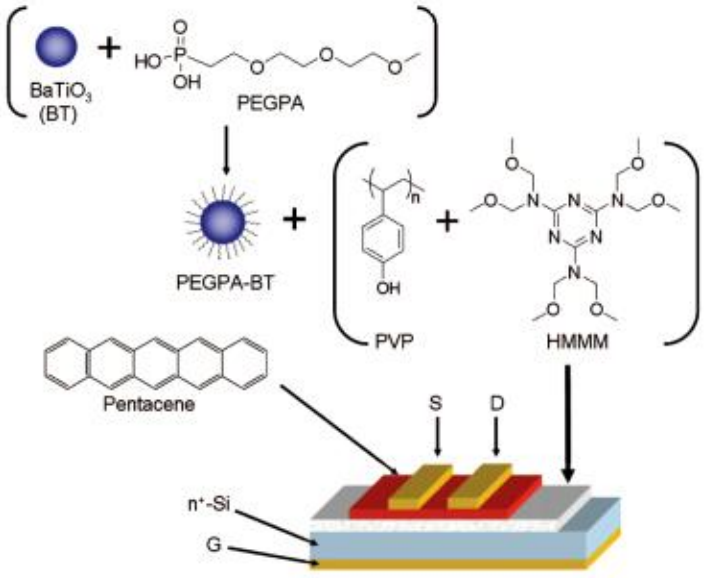


Fig. 2.11: PEGPA-BT:PVP nanocomposite preparation and structure of OTFT devices [74].

Noh *et al.* [68] also treated surfaces of Al_2O_3 particles with a *c*-glycidoxypropyl-trimethoxysilane coupling agent prior to inclusion into a PVP matrix, in an attempt to improve the dispersion of nanoparticles in various polymers. They reported an increased dielectric constant from 4.9 for pure PVP to 7.2 for the nanocomposite with 24 vol % Al_2O_3. However, the mobilities measured for pentacene were decreased as compared to the pure PVP dielectric due to greater surface roughness. More recently, Huang *et al.* [71] studied surface treatment of Al nanoparticles with octyl-trimethoxysilane coupling agent dispersed in a linear low density polyethylene (LLDPE) matrix. They concluded that improvements, such as better nanoparticles dispersion, easier control of dielectric constant and reduced dielectric loss, could be achieved with nanocomposites prepared using surface-modified nanoparticles.

Arita *et al.* [76] reported that the solution-state property of three-dimensional (3D) SAMs (3D SAMs) on CeO_2 nanoparticles seriously affected the dispersion of NPs. The chain length and solvent-dependent changes in the properties of SAMs were investigated by using various n-alkanoic acid SAMs on CeO_2 NPs and various non-polar organic solvents. Mallakpour *et al.* [73] modified the surfaces of zirconium oxide (ZnO) nanoparticles with *γ*-aminopropyltriethoxysilane (KH550) coupling agent and prepared nanocomposites in poly(amide–imide) (PAI) in an attempt to evaluate the effect of surface modification on thermal stability and UV absorption property of the resultant nanocomposites.

One of the most recent, notable works on preparation of nanocomposites using surface-modified nanoparticles has been carried out by Zhou *et al.* [77]. As shown in Fig. 2.12, the surfaces of BT nanoparticles were chemically modified by an aqueous solution of H_2O_2, prior to preparing hydroxylated-BT (h-BT) in PVDF nanocomposites.

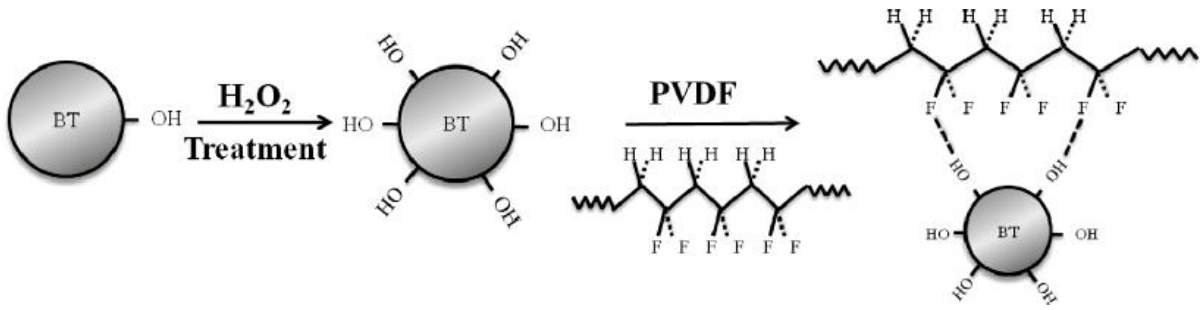


Fig. 2.12: Modification of BT nanoparticles for h-BT/PVDF nanocomposite preparation [77].

Their results manifest lower dielectric loss tangent, higher dielectric strength and higher dielectric constant stability between 20° and 150 °C for h-BT/PVDF nanocomposites. Zhou *et al.* [77] attributed such outstanding properties to the formation of hydroxyl groups (hydroxylation) which led to stronger hydrogen bonds and interfacial interactions between the h-BT fillers and the PVDF matrix in the nanocomposites (i.e. fewer voids were present) and better dispersion of the fillers in the polymer matrix. As described in section 3-1-3, this method (i.e. hydroxylation) was initially applied to nanoparticles prior to subjecting them to surface modification using SAM molecules.

Chemical modification and passivation of nanoparticles surface are critical steps to obtain well-dispersed, uniform nanocomposite suspensions and dielectric thin films subsequently. The advantages of functionalising nanoparticles surface with SAMs prior to dispersion in a polymer matrix can be summarised as [53, 71]:

(i) Suppression of aggregation and better dispersion of nanoparticle fillers in host polymer matrix yielding a homogenous nanocomposite suspension
(ii) Easy control and tuning of the dielectric constant
(iii) Improved dielectric properties such as reduced dielectric loss and enhanced breakdown strength compared to that of non-modified nanoparticles
(iv) Possibility of increasing the nanoparticle concentration (volume fraction)
(v) Enhanced compatibility of the guest nanoparticles in the host polymer matrix
(vi) Stability of the dielectric characteristic with varying frequency

2-3- Thin Film Transistors (TFTs)

At the heart of many inorganic and organic integrated circuits lies the thin-film transistor (TFT) [78]. Liquid crystal displays (LCD) are by far the major application of TFTs, but they also have applications in digital X-ray imaging and radiography, sensing devices, RFID tags, portable e-papers and many other electronic devices. The concept of field-effect controlled current dates back to 1930 when it was first proposed by Lilienfeld [79, 80]. The idea was to replace vacuum lamps by solid-state devices in amplifiers. However, more than thirty years elapsed before that early concept was realised in a practical application as the silicon-based metal-oxide-semiconductor field-effect transistor (MOSFET). In actual fact, the first TFT was made by Weimer *et al.* [81] evaporating all

components on an insulating glass substrate. By early 1970s, demonstration of a LCD based on CdSe TFTs was reported [82]. Nowadays, TFTs are omnipresent in numerous micro- and nano-electronic devices.

The TFT is a special type of field-effect transistor (FET) with an alternative geometry made by depositing thin films of dielectric, semiconductor and contacts onto a substrate in a sequentially layered structure. TFTs differ from MOSFETs in that the conducting channel comprises an accumulation rather than an inversion layer [83]. FETs have not only revolutionised the field of electronics, attracted great technological interests and brought about fantastic breakthroughs, but are also favoured to study charge transport in solid materials. The electric field-induced effect, generally exploited in high performance semiconductor materials, has shown adaptability with low performance materials as well, particularly in the case of hydrogenated amorphous silicon (a-Si:H) [83]. Today, a-Si:H TFTs are largely used in the active matrix of LCD (AM-LCD) displays.

Thin film transistors based on organic semiconductors are referred to as organic thin film transistors (OTFTs). Organic semiconductors have been known since the late 1940s [84]. In 1977, Shirakawa *et al.* [85] reported an increase in conductivity by up to 10^3 S/cm of the semiconducting trans-polyacetylene $(CH)_x$ upon doping the material with iodine. Following this revolutionary discovery, numerous conducting and semiconducting (conjugated) organic materials have been synthesised. Although the first attempt in fabricating OTFTs based on polyacetylene was shown in 1983, it displayed extremely poor performance. The first successfully operational OTFT was reported in 1986 by Tsumura *et al.* [24] who fabricated the device on an electrochemically grown polythiophene film. Since then, the OTFT has turned into a mature device that has tremendously evolved since it was first realised in 1986.

Nonetheless, OTFTs have suffered from limited performance compared to TFTs based on single-crystalline inorganic semiconductors. This has been mainly due to the relatively low field-effect mobility (μ) of the organic semiconductor layers [80]. Thus, OTFTs could not have been visualised for use in applications requiring very high switching speeds. However, the processing characteristics and demonstrated performance of OTFTs suggest they can compete for existing or novel TFT applications, particularly those requiring large-area coverage, structural flexibility and compatibility with plastic substrates. Low-

temperature processing, and especially, low cost are further important factors favouring OTFTs [86].

Today, substantially improved physical understanding of charge transport and of structure-property relationships has supported the development of better organic semiconductor materials for OTFT applications and other devices relying on charge transport, for instance organic solar cells and light-emitting devices.

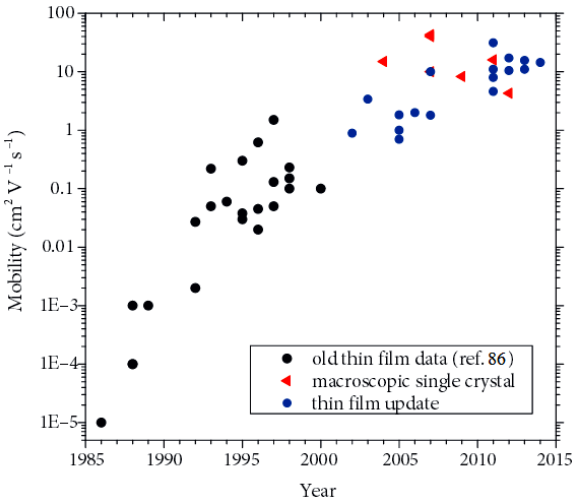


Fig. 2.13: Semilogarithmic plot of each year's highest reported field-effect mobility value from TFTs based on various organic semiconductors [87].

The field-effect mobility (μ), which is the main materials-related figure of merit of an OTFT, has increased from low values $<10^{-3}$ cm^2/Vs (Fig. 2.13) to values >1-10 cm^2/Vs surpassing those of benchmark thin-film amorphous silicon devices (0.5-1 cm^2/Vs) [5].

2-3-1-Organic Semiconductor Materials (OSCs)

The discovery of organic semiconductors has unveiled a new stream of research activities aimed at fabricating inexpensive, easily-processed and large area flexible electronic devices [84]. Organic semiconductors are lightweight materials which can be processed at ambient conditions on a variety of substrates using low-cost deposition techniques, reducing overall production costs. Organic semiconductors are generally referred to as organic conjugated materials. The "conjugation" phenomenon has originated from a structure that comprises alternating single and double/triple bonds between the carbon atoms along the backbone of organic molecules [83].

Considering carbon with the electronic configuration of $1s^2 2s^2 2p^2$, during the process of hybridisation between two atoms of carbon, the atomic orbitals of the second level mix and a combination of the 2s with the $2p^{xyz}$ orbitals occurs. Such a configuration is known as sp^3 and the orbitals are orientated towards the corners of a tetrahedron shape. With sp^3 hybridisation, single bonds are formed as each of the valence electron is bonded with a large orbital overlap with the electrons of other four atoms. Single bonds contain a sigma (σ) bond that is strongly localised to the bonded atoms and do not take part in the charge transport. Double or triple bonds form when only either two (sp) or three (sp^2) second level orbitals are involved in hybridisation. Therefore, the remaining unchanged atomic orbital(s) overlaps laterally with atomic p-orbitals of other carbon atoms and form weak pi (π) bonds. Normally, the electrons that form a π-bond are localised. However, in conductive polymers, π-orbitals of the neighbouring double bonds overlap due to the conjugated structure. As a result of this overlapping, π-electrons are delocalised and can move from one bond to another or move along the entire molecule. Hence, the continuous overlapping π-orbitals of the conjugated backbone and the resultant delocalisation make the conduction of charge carriers along the polymer chain possible [88].

The system of alternating double and single bonds in the conjugated backbone give rise to a separation of bonding and anti-bonding states, resulting in the formation of a forbidden energy gap and a spatially delocalised band-like electronic structure. The highest occupied molecular orbital (HOMO) consists of bonding states the π-orbitals with filled electrons and is analogous to the valence band in inorganic semiconductors. The lowest unoccupied molecular orbital (LUMO) consists of empty higher energy anti-bonding (π^*) orbitals and is analogous to the conduction band [88]. The energy difference between the HOMO and LUMO defines the band-gap energy (E_G). Similarly as in the inorganic materials, organic conjugated molecules, due to the existence of the band gap E_G ~ 1-4 eV, are classified as semiconductors [88]. Common organic semiconductors have band gaps with values in the range of 2-3 eV [89].

There are two broad classes of organic conjugated materials used in organic electronic devices: (1) polymers and (2) small molecules; examples of which are categorised according to their deposition technique (e.g. deposited by vacuum- or solution-processing) and shown in Fig. 2.14 [90].

Conjugated polymers have the advantage of being compatible with specific deposition techniques developed for conventional polymers. Conjugated polymers have a rigid rod backbone, which is made soluble by attaching flexible $(CH_2)_n$ alkyl side chains, and form a polycrystalline film when deposited from solution [91]. However, their performance is relatively inferior to that of small molecules. With regards to small molecules, encouraging performance has been reported, some of which currently offers higher mobility than a-Si:H. Nonetheless, their high performance requires substantial ordering, particularly near the insulator-semiconductor interface, which can be difficult to achieve with certain deposition methods [83].

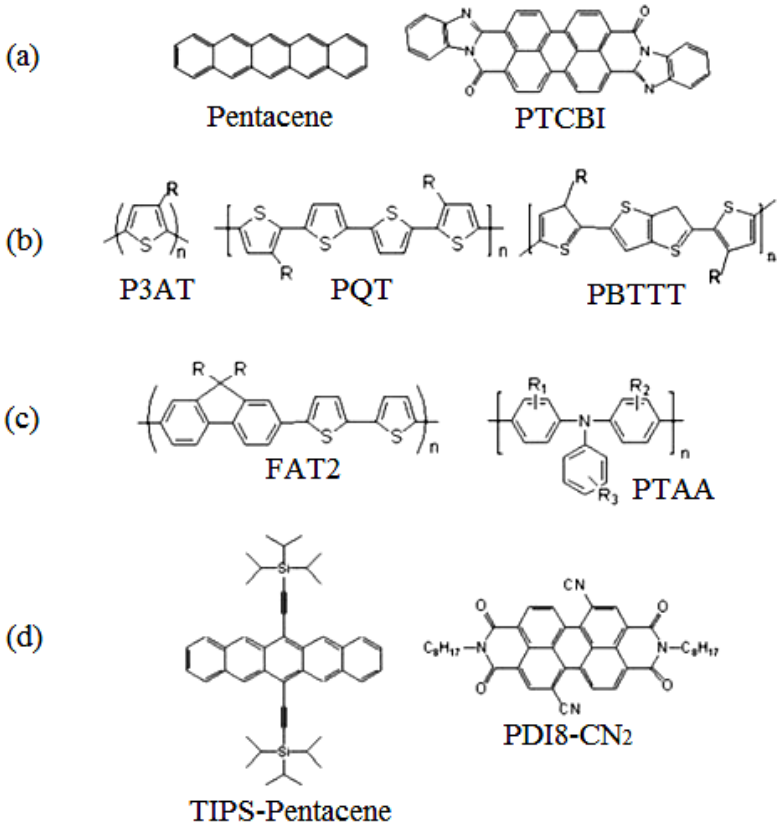


Fig. 2.14: Chemical structure of (a) vacuum-processed, small-molecule semiconductors, (b) semicrystalline polymeric semiconductors, (c) amorphous polymeric semiconductors and (d) solution-processed, small-molecule semiconductors [90].

With the emerging need for low-temperature, large-coverage (roll-to-roll) techniques for deposition of semiconductor layers compatible with flexible substrates, solution-processing has gained considerable attention. Various methods such as spin-coating, screen-printing, spray-coating, ink-jet printing, gravure/flexographic printing and curtain/slot die coating have been developed [92].

Correspondingly, two different approaches to high-performance, solution-processable, polymer semiconductors have emerged. The first approach is based on achieving high carrier mobilities by designing the material to exhibit microcrystalline or liquid-crystalline order through self-organisation, or by making use of specific interactions with a templating substrate. The second approach aims at producing a completely amorphous microstructure to provide a uniform path for charge transport, along which carriers experience a minimum degree of site-energy fluctuations. Although the first approach is likely to yield higher mobilities, impressive device performance and stability has been recently demonstrated using the second approach [5, 93].

The majority of organic semiconductors exhibit p-type (formation of hole accumulation layers upon applying a negative gate bias) rather than n-type (electron transporting for positive gate bias) behaviour. However, recently examples of n-type semiconductors have been developed in OTFTs for use in complementary logic circuits [5]. The mechanism of charge injection and transport in organic semiconductors is reviewed in the section below.

2-3-2- Charge Carrier Injection

In conventional metal-oxide-semiconductor field-effect transistors (MOFETs), the charge transport mechanism is determined by the doping of the semiconductor material. However, the optimal performance of OTFTs critically depends on charge carrier injection from the source electrode into the semiconductor, followed by the effective transport of those injected carriers (current flow) through the channel. In OTFTs, the metal-semiconductor interface is usually regarded as a Mott-Schottky barrier. The characteristics of carrier injection from a metal electrode into a semiconductor are controlled by the barrier height. This is given by the work function (Φ) of the metal relative to ionisation potential (I_p) in the case of p-type, and to electron affinity (E_a) in the case of n-type semiconductors. I_p is the energy slightly less than the HOMO required to remove an electron, while E_a is the energy slightly more than LUMO obtained by adding an electron [36].

A simplified energy level diagram in Fig. 2.15 illustrates carrier injection from the source electrode into the semiconductor in an OTFT. The positions of the HOMO and LUMO of a p- and an n-type organic semiconductor relative to the work function of the source contact are shown in the left and right panels respectively.

According to the schematic, in ideal case, the metal-semiconductor junction is an ohmic contact if the work function of the source contact matches the I_p or E_a of the p- or n-type semiconductor. Therefore, there exists no injection barrier for charge carriers, and upon applying a drain bias, the injected charges can be relatively easily transferred and collected at the drain contact. Nonetheless, in real case, a non-ohmic contact is expected at which a potential barrier is formed, leading to poor charge injection and introducing an extra resistance to the junction (so-called, contact resistance) [89]. Thus, one of the key design considerations for high performance OTFTs is the matching of source/drain (S/D) contacts and semiconductor energy levels.

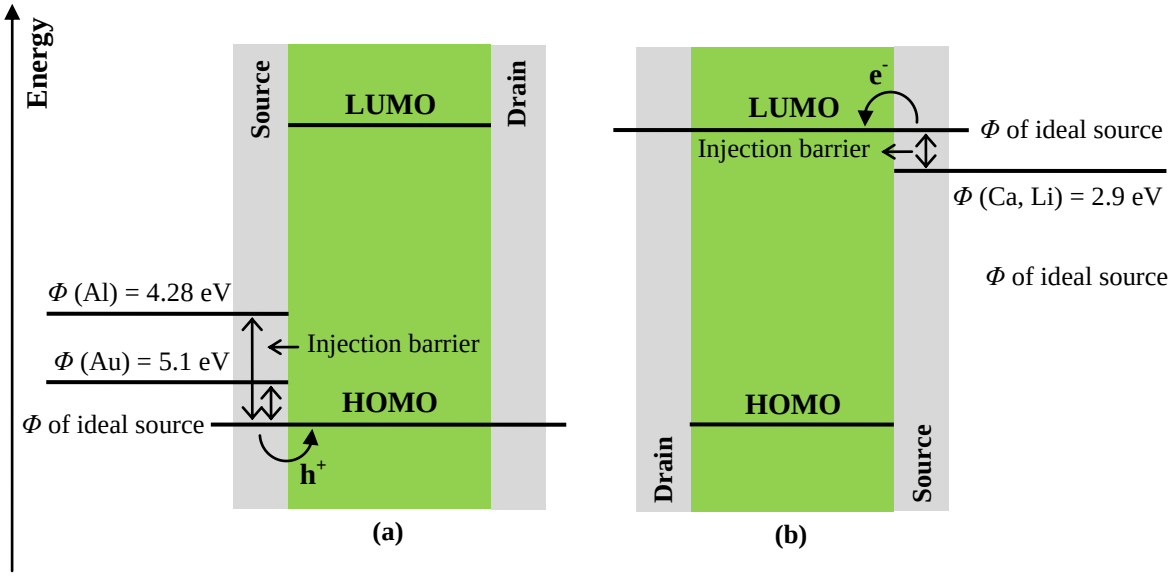


Fig. 2.15: Energy level diagrams of (a) p-type and (b) n-type organic semiconductor and work functions of ideal and real source and drain electrodes, including injection barriers.

As can be observed in Fig 2.15, rather than aluminium (Φ_{Al} = 4.28 eV), gold (Φ_{Au} = 5.1 eV) is typically used in conjunction with p-type semiconductors (e.g. 6,13-bis(triisopropylsilylethynyl)pentacene, TIPS-Pentacene, HOMO level = 5.3 eV), since its charge injection barrier to HOMO (I_p) level is smaller compared to that of aluminium [94].

Moreover, interfaces in OTFTs play a crucial role in obtaining high performance devices. The metal-semiconductor interface influences charge carrier injection, while the dielectric-semiconductor interface contributes to better charge carrier transport. Engineering of the contact-semiconductor interface by chemical modification of the contacts with SAMs has been repeatedly reported in the literature [83]. SAM-modification of electrodes reduces

contact resistance and hence improves charge injection from the source electrode into the semiconductor by tuning the metal work function (Φ) to match the HOMO (I_p) level of the (p-type) semiconductor and reducing the charge injection barrier [95].

2-3-3-Charge Carrier Transport

Organic electronics technology requires a detailed understanding of the electronic properties of the organic semiconductor materials, whose constituent molecules are kept together mainly by van der Waals interactions. In particular, from the engineer's point of view, an understanding of the electronic transport mechanism of majority charge carriers (holes or electrons) is needed. Although charge transport is relatively easy within a molecule, charge transport between molecules is much more difficult due to the disordered molecular structure of most organic semiconductors. The charge transport and emission properties of organic semiconductors have been under intense investigation for many years. It is now well established that charge transport in conjugated semiconductors is favoured in the direction parallel to the deposited layers. Garnier *et al.* [96] proved this preferential charge transport by x-ray diffraction measurements on sexithiophene-based transistors, which indicated that the highest charge mobility was attained when all molecules where standing upright on the surface of the dielectric [83]. Once charge carriers are injected into the semiconductor, they will on average move in the direction of the applied field.

The transport of a charge carrier can be described by the electric field-induced directional drift velocity component, $\langle v \rangle$, a steady velocity up to which the mobile charge carriers accelerate. This velocity is associated with a current density *j*:

$$\boldsymbol{j} = e \cdot n \cdot \langle \boldsymbol{v} \rangle, \qquad \text{(Eq. 2.23)}$$

where *e* is the electronic charge unit and *n* the local charge carrier density. The relation between $\langle v \rangle$ and the applied electric field *E* is usually linear (reflecting Ohm's law), but only if the applied field is not too high:

$$\langle \boldsymbol{v} \rangle = \mu \cdot \boldsymbol{E}. \qquad \text{(Eq. 2.24)}$$

According to equation (2.24), charge carrier mobility μ describes the average drift velocity of the charge carriers under an applied electric field. μ expressed in cm^2/Vs is the fundamental electronic transport quantity specific to a given semiconductor material [97].

An outstanding feature distinguishing organic semiconductors from their inorganic counterparts is a strong tendency of charge carrier localisation in the former. The effects of carrier localisation are reflected by the dominant role of polarons arising from electronic nuclear coupling. Polaron is a collective term used for a charge together with its induced lattice deformation [98]. The inherent tendency for carrier localisation is enhanced by the presence of energetic disorder, which is the result of structural inhomogeneities and chemical impurities, leading to charge carrier trapping in some cases [99]. A trap is defined as a site with an ionisation potential lower than that of the bulk material (hole trap), or with electron affinity higher than that of the bulk material (electron trap). Although transport of only one type of carrier (hole or electron) is believed to be the result of charge-carrier deep traps, even for the carrier type that is transported, traps still exist. In a trap, a carrier is immobilised, contributes to a space charge and consequently screens the externally applied field [100, 101].

In general, there are two main mechanisms of charge carrier transport, namely, coherent (band transport) and incoherent (hopping transport). The band transport explains the extremely high (electron or hole) mobility in inorganic covalently bound semiconductors. On the other hand, the hopping transport describes relatively low mobility in disordered materials with localised excitations, such as organic semiconductors. In the case of the localised states, the tunnelling (hopping) of carriers from one site to the next is assisted by phonons (lattice vibrations) and mobility is thermally activated (increases with rising temperature) [90].

Shortly after the concept of hopping was introduced, Holstein *et al.* [102] developed the concept of polaron motion. Holstein proposed the local electron-phonon interaction model for the small polaron transport in one-dimensional (1D) molecular crystals. Holstein assumed that successive carrier hops to neighbouring sites were uncorrelated, resulting in a simple activated-type variation of carrier mobility with temperature down to some critical temperature, below which band transport dominates.

His model predicts a linear (Arrhenius) relationship of ln(μ) with 1/T. The charge carrier mobility described by the Arrhenius equation is given as [102]:

$$\mu \propto \mu_0 \exp\left[-\frac{E_b}{2k_B T}\right], \qquad \text{(Eq. 2.25)}$$

where T is temperature, k_B is the Boltzmann constant, μ_0 is the mobility for $T \to \infty$ and E_b the polaron binding energy.

An alternative model has been devised by Bässler specifically for disordered organic semiconductors [100, 103]. He assumes that HOMO (LUMO) levels are not equal in energy, but display a Gaussian distribution around the average HOMO (LUMO). This energetic distribution is referred to as diagonal disorder and characterised by variance σ^2, or the dimensionless $\hat{\sigma} = \sigma/k_B T$. The hopping rate is also affected by positional or off-diagonal disorder quantified by another variance, Σ^2. Bässler derived the following equation [103]:

$$\mu(\hat{\sigma}, \Sigma, E) = \mu_0 \exp\left(-\left(\frac{2}{3}\hat{\sigma}\right)^2\right) \begin{cases} \exp C\left(\hat{\sigma}^2 - \Sigma^2\right) E^{1/2}; & \Sigma \geq 1.5, \\ \exp C\left(\hat{\sigma}^2 - 2.25\right) E^{1/2}; & \Sigma < 1.5. \end{cases} \qquad \text{(Eq.2.26)}$$

According to Bässler's model, the mobility μ depends on E. The effect becomes measurable at high fields exceeding 10^4 V/cm. The problem of the field-dependent mobility was resolved numerically assuming a Poole-Frenkel (P-F) type dependency of μ on E [101]:

$$\mu(E) = \mu_0 \exp\left(\beta\sqrt{E}\right), \qquad \text{(Eq. 2.27)}$$

where β is the P-F coefficient. The P-F effect (so-called field-assisted thermal ionisation) is the lowering of a Coulombic potential barrier (lowering of a trap barrier in the bulk of an insulator) by applying an electric field [104]. The P-F equation is equivalent to the Bässler model of $\mu(E)$ if temperature is considered constant β is chosen appropriately.

Fig. 2.16 summarises the various charge (electron) transport models. Fig. 2.16 (a) depicts the hopping mechanism where only trap states exist and charge has a small mobility in the form of infrequent hops. Fig. 2.16 (b) illustrates P-F mechanism in which trap states capture a large part of the charge, fixing it in place, and conduction occurs by temperature-

and field-assisted excitation from the trap to conductive bands [105]. According to equation 2.27, in P-F mechanism, the trap barrier height is reduced due to applied electric field by a magnitude of $\beta\sqrt{E}$.The pure crystal model where there are no impurities and the mobilities reach the upper-limit value of the bands is shown in Fig. 2.16. (c). The hybrid-model which is a combination of hopping and P-F often used in low-conductive inorganic semiconductors, such as nonstoichiometric GaAs, is also illustrated in Fig. 2.16 (d) [105].

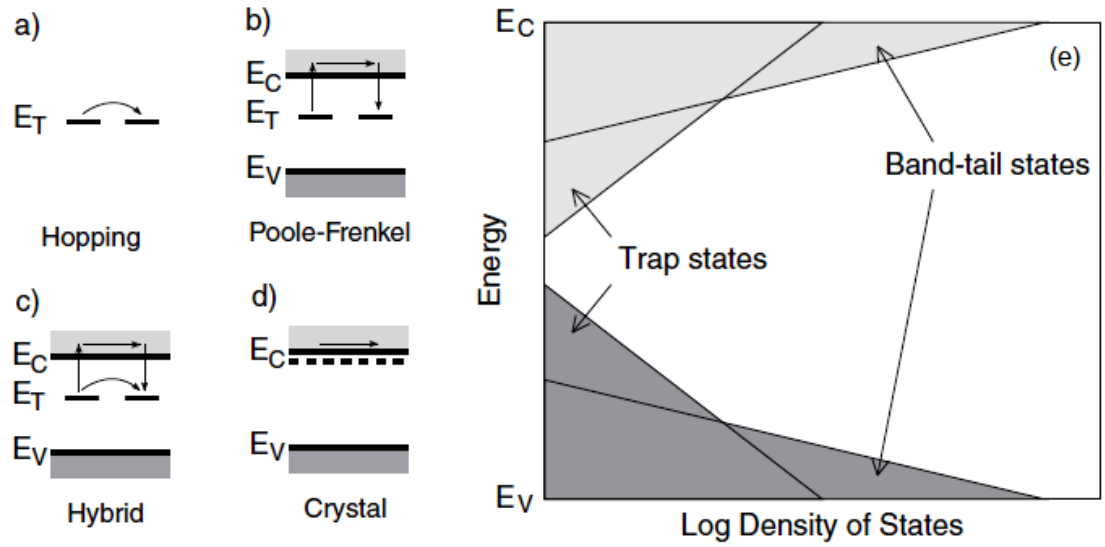


Fig. 2.16: N-type charge carrier transport (conduction) models: (a) hopping, (b) Poole-Frenkel, (c) hybrid and (d) band/crystal theory. (e) Band diagram of amorphous semiconductors with conduction levels ("tail states" of conduction and valence bands, arbitrarily positioned at E_C and E_V, respectively) and trap levels exponentially distributed in energy. The states between E_V and E_C are localised states [105].

The exact nature of charge transport in organic semiconductors is still considered controversial. One may initially think that charge transport occurs at the LUMO level, as electrons are delocalised along the polymer chain. However, in disordered materials, the travel distance (mean free path) of the delocalised electrons is very small due to structural defects and charges do not follow classical band transport in inorganic materials [106]. Nonetheless, there is a clear distinction between the mechanisms of charge transport in disordered semiconductors such as amorphous polymers compared to those in highly ordered organic single crystals [89]. What makes the amorphous materials differ from the crystalline materials is that, apart from the covalent bonds, the material also has unbonded (under-bonded and over-bonded) atoms with unpaired electrons [105].

For many years, OSCs were only produced in the form of highly disordered amorphous materials with very low mobility of carriers (holes). Charge transport in disordered semiconductors is generally described by thermally activated, phonon-assisted hopping of charges through a distribution of deep localised states or shallow traps (Fig. 2.16 (e)) [89]. The more ordered the intermolecular structure, the easier the hopping between molecules. This means that mobility is higher in semiconductors with a well organised molecular structure. As the structural order of the materials improves, leading to polycrystalline films, the band transport (Fig. 2.16 (d)) plays a larger role, the polaron (self-localised states) effects decrease and the extended state wave function becomes more delocalised [91].

2-3-4- Geometry and Operation Principles of TFTs

OTFTs (TFTs in general) can have four configurations, as depicted in Fig. 2.17, depending on the position of the gate electrode (G) and the sequence of the source (S) and drain (D) electrodes deposited relative to the semiconductor layer. These configurations are described as top-gate top-contact (TGTC), top-gate bottom-contact (TGBC), bottom-gate top-contact (BGTC) and bottom-gate bottom-contact (BGBC).

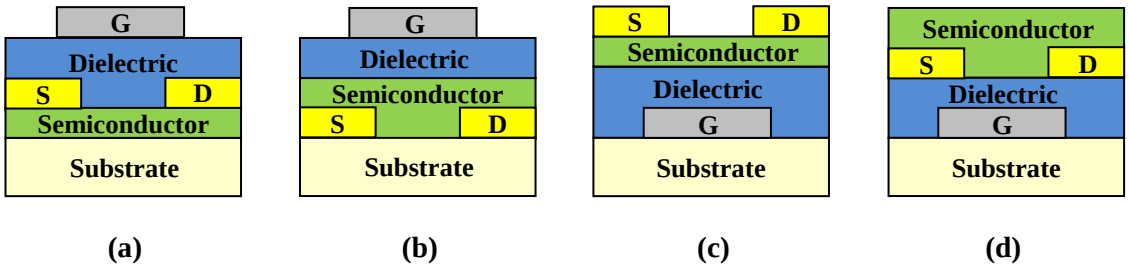


Fig. 2.17: Schematics of (a) TGTC, (b) TGBC, (c) BGTC and (d) BGBC thin film transistors.

In principle, the characteristic that best defines OTFTs is the presence of an electric field that controls and modulates the conductivity of the channel between the source and drain. This electric field is created by the voltage applied between the source and the gate electrodes, i.e. gate voltage (V_G). Application of a negative (or positive) gate voltage will induce holes (or electrons) at the dielectric-semiconductor interface where charge transport takes place. The density of accumulated charge carriers in the channel is modulated by V_G and is dependent on the capacitance C of the dielectric layer.

The performance of an OTFT is typically described by carrying out two common measurements; transfer and output characteristics. Transfer characteristics are acquired by ramping V_G at a constant source-to-drain voltage (V_{SD}), while output characteristics are obtained by sweeping V_{SD} from zero to a given voltage at a number of constant V_G biases. In other words, transfer characteristics provide source-to-drain current (I_{SD} or simply called I_D) *vs.* V_G variation, whereas output characteristics present how I_{SD} vs. V_{SD} varies. Comparing these two characteristics, transfer characteristics provide more information about device performance, while output characteristics are more efficient in presenting injection problems, which are not often noticeable in transfer characteristics. Additionally, $V_G = V_{SD}$ sweeps provide more precise values of threshold voltage (V_T).

When no voltage is applied between the source and gate ($V_G = 0$), the device is "off". Upon applying a negative bias (with respect to the grounded source electrode) to the gate electrode (for a p-type semiconductor), a TFT operates in the accumulation mode and the accumulated charges are holes.

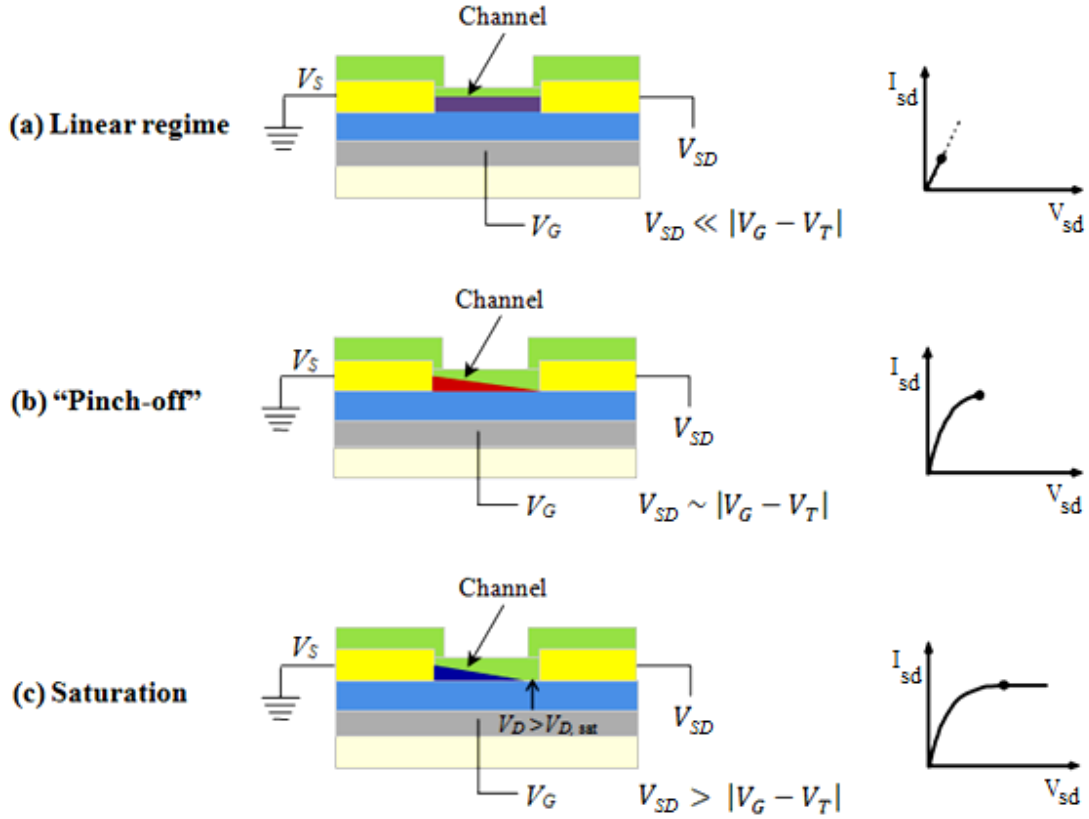


Fig. 2.18: Schematics of principle of operation of an OTFT in (a) linear regime, (b) start of the saturation regime at pinch-off and (c) saturation regime [80].

As illustrated in Fig. 2.18, increasing both V_G and V_{SD}, a linear (drain current vs. drain voltage) regime is initially observed at low $|V_{SD}| \ll |V_G - V_T|$, I_{SD} increases linearly with V_{SD}. Once $|V_{SD}| \sim |V_G - V_T|$, I_{SD} starts to saturate due to "pinch-off" of the accumulation layer. Subsequently, I_{SD} continues to saturate (saturation regime) as V_{SD} increases towards higher values; $|V_{SD}| \gg |V_G - V_T|$ [21, 41].

The current-voltage (*I-V*) characteristic is a key parameter used in evaluating the performance of OTFTs. Derivation of the I_{SD} vs. V_{SD} relationship for OTFTs is described as follows. Consider an infinitesimal portion of the channel of length *dx* at a point x from the source, as depicted in Fig. 2.19, and let the voltage at this point be $V(x)$. The voltage between the gate and this point in the channel, $[V_G - V(x)]$, must obviously be greater than the threshold voltage V_T. The electron charge in this portion of the channel, $dq(x)$, can be expressed as [105]:

$$dq(x) = -C_{ox} W dx\, [V_G - V(x) - V_T], \qquad \text{(Eq. 2.28)}$$

where, C_{ox} is the capacitance per unit area of the parallel plate capacitor formed by the gate electrode and the channel.

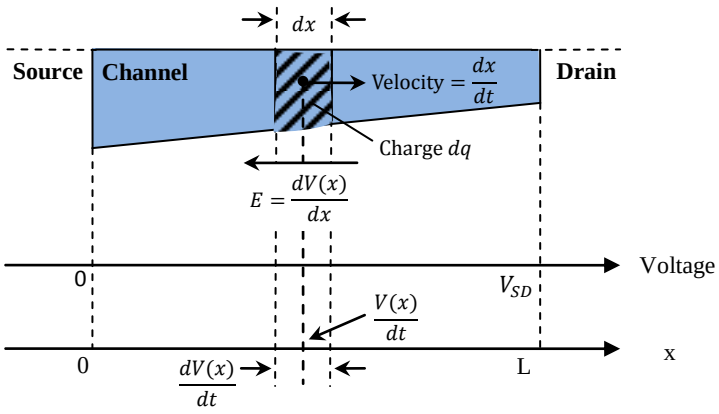


Fig. 2.19: Derivation of the I_{SD} vs. V_{SD} characteristics for an OTFT [107].

Recalling from section 2-1-2, the capacitance of this capacitor with the oxide layer regarded as its dielectric is:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \qquad \text{(Eq. 2.29)}$$

where, ε_{ox} and t_{ox} are the permittivity and thickness of the dielectric layer respectively.

Note that because $dq(x)$ is a negative charge, we have included a negative sign in equation (2.28). As the result of the voltage, V_{SD}, an electric field along the channel in the opposite (negative sign) direction of *x* will be induced. At point *x*, the electric field can be expressed as:

$$E(x) = -\frac{dV(x)}{dx}. \qquad \text{(Eq. 2.30)}$$

The electric field $E(x)$ causes the electron charge $dq(x)$ to drift towards the drain with a velocity $\frac{dx}{dt}$,

$$\frac{dx}{dt} = -\mu_n E(x) \qquad \text{(Eq. 2.31)}$$

$$= \mu_n \frac{dV(x)}{dx}. \qquad \text{(Eq. 2.32)}$$

where μ_n represents the mobility of electrons in the channel.

Taking equation (2.28), the resulting drift current can now be calculated by multiplying the charge per unit length $\frac{dq(x)}{dx}$ by the drift velocity (equation (2.32)):

$$i = -\mu_n C_{ox} W[V_G - V(x) - V_T]\frac{dV(x)}{dx}. \qquad \text{(Eq. 2.33)}$$

Considering the current i (drain-to-source current, I_{DS}) to be constant at all points along the channel, I_{SD} must be opposing I_{DS}, giving

$$I_{SD} = \mu_n C_{ox} W[V_G - V(x) - V_T]\frac{dV(x)}{dx}. \qquad \text{(Eq. 2.34)}$$

By rearranging equation (2.34),

$$I_{SD}\, dx = \mu_n C_{ox} W[V_G - V(x) - V_T]\, dV(x). \qquad \text{(Eq. 2.35)}$$

Integrating both sides of this equation between the limits $x = 0$ and $x = L$, and correspondingly between $V(0) = 0$ and $V(L) = V_{SD}$

$$\int_0^L I_{SD} dx = \int_0^{V_{SD}} \mu_n C_{ox} W \left[V_G - V_T - V(x)\right] dV(x), \qquad \text{(Eq. 2.36)}$$

yields

$$I_{SD} = (\mu_n C_{ox}) \left(\frac{W}{L}\right) \left[(V_G - V_T) V_{SD} - \frac{1}{2} V_{SD}^2\right]. \qquad \text{(Eq. 2.37)}$$

The expression for the I_{SD} vs. V_{SD} the linear region is obtained by setting $V_{SD} \ll V_{GS} - V_t$) in equation (2.37):

$$I_{SD} = (\mu_n C_{ox}) \left(\frac{W}{L}\right) [(V_G - V_T) V_{SD}]. \qquad \text{(Eq. 2.38)}$$

Taking equation (2.37) and setting the derivative of I_{SD} with respect to V_{SD} to zero, I_{SD} becomes maximum when:

$$V_{SD} = V_G - V_T. \qquad \text{(Eq. 2.39)}$$

The expression for the saturation region can be derived by substituting V_{SD} in equation (2.37) with equation (2.39):

$$I_{SD} = \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L}\right) [(V_G - V_T)^2], \qquad \text{(Eq. 2.40)}$$

which gives the value of the constant current for a particular V_G in the saturation region.

Several device figures of merit are used in evaluating the performance of OTFTs, namely the mobility (μ), ON/OFF ratio, threshold voltage and subthreshold swing. Field-effect mobility quantifies the average charge carrier drift velocity per unit electric field and is typically reported in cm^2/Vs, whereas threshold voltage is a minimum gate voltage to induce mobile charges at the insulator/semiconductor interface (i.e. gate voltage at which the conducting channel starts to form). V_T is determined by the amount of traps introduced by interfacial disorder (caused, for example, by fixed charges, surface structural defects and dangling bonds) and the defects in the bulk of the semiconductor. It is also often affected by the quality of source/drain contacts. The ON/OFF ratio is referred to as the source-drain current ratio between the transistor 'On' and 'OFF' states. The value of ON/OFF ratio (10^n) is found by calculating the ratio between the highest and lowest measured drain currents.

For every transistor, the above parameters can be extracted from the transfer characteristics or the $|I_{SD}|^{1/2}$ vs. V_G plot, examples of which for a TIPS-pentacene OTFT are illustrated in Fig. 2.20. The onset voltage (V_0) is marked on the transfer curve. The mobility (in the saturation regime) is calculated by fitting a straight line to the linear region of the square root of the I_{SD} versus V_G plot. The value of slope is found and then substituted into the following equation to obtain the value for mobility:

$$\mu = \frac{2L(Slope)^{\frac{1}{2}}}{WC_{ox}}. \qquad \text{(Eq. 2.41)}$$

The value of threshold voltage can be simply determined from the intersect value of the x-axis by the linear fitted line (as marked in Fig. 2.20).

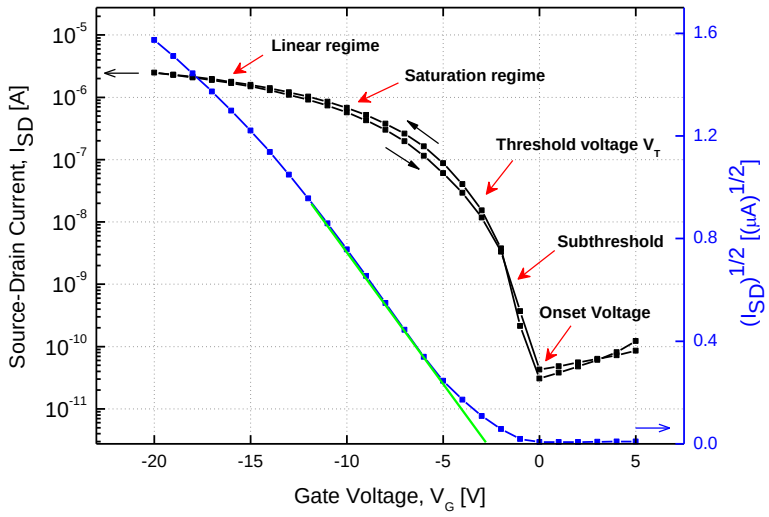


Fig. 2.20: Transfer characteristics of a TIPS-pentacene OTFT, V_{SD} = - 10 V.

The final characteristic parameter of OTFTs is subthreshold swing (SS), which is a measure of how rapidly the device is switched off by the gate voltage. Using the transfer characteristics curve, the slope of the line fitted to the subthreshold linear region of the curve, SS (volt/decade) can be determined.

2-3-5-The role of Interfaces in OTFTs

As mentioned before, interfaces play a crucial role in obtaining high performance devices. As illustrated in Fig. 2.21 below, four different interfaces exist in a (top-contact) OTFT:

(i) Contact-semiconductor layer interface

(ii) Dielectric-semiconductor layer interface

(iii) Semiconductor-semiconductor layer interface

(iv) Semiconductor-atmosphere interface

The first two interfaces can be effectively engineered to achieve high-performance devices by improving charge injection and transport mechanism, enhancing carrier mobility, increasing device stability, reducing operational voltage, etc. The semiconductor-semiconductor interface is present in double layer structures, such as heterojunctions or two semiconductors blended into a single layer. It allows realisation of two types of functionality simultaneously and plays an important role in attaining ambipolar operation and light-emitting OTFTs [108]. Finally, the semiconductor-atmosphere interface (referred to naturally as 'surface') has particular impact on device characteristics post-fabrication. Those of chief concern are stability, sensitivity to certain chemicals and vulnerability to physical damage and corrosion.

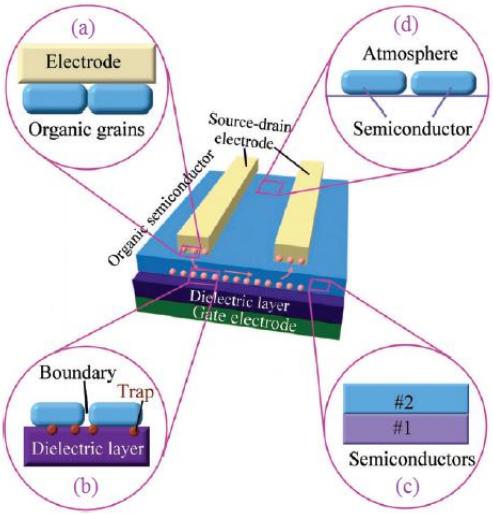


Fig.2.21: Interfaces in top-contact OTFTs: (a) electrode-semiconductor, (b) dielectric-semiconductor, (c) semiconductor-semiconductor and (d) semiconductor-atmosphere [108].

The two major processes of carrier injection and carrier transport occur at the contact-semiconductor layer interface and the dielectric-semiconductor layer interface, respectively. Therefore, the properties of these interfaces dramatically influence the device characteristics. Modification of the electrode-semiconductor or dielectric-semiconductor interfaces remains the most widely investigated approach to improving device performance [108]. The S/D electrode-semiconductor interface has a key impact on carrier injection.

Engineering contact-semiconductor interface by chemical modification of contact with SAMs has been repeatedly reported in the [80]. The energy barrier, carrier injection area and contact condition are three major factors that determine the quality of the contact-semiconductor interface [108]. SAM-modification of electrodes significantly improves device operation through passivation of charge trap states, reducing the energy barrier and improving carrier injection between the S/D electrodes and the semiconductor and influencing the morphology and crystallinity of the semiconductor layer [80, 83]. Once the dielectric and semiconductor layers are deposited, the quality of their interface plays a crucial role in device performance from charge transport and mobility point of view. Thus, particular attention is given to this interface and its impact on device characteristics. Strategies to modify and improve this interface are given in section 2-3-5-2.

2-3-5-1- Dielectric-Semiconductor Interface

The dielectric-semiconductor interface is a vital interface in OTFTs since it dominates the charge carrier transport that occurs in the conductive channel. This is located on the first few semiconductor molecular layers near the dielectric layer (or at interface) [109]. The interface states, including both the dielectric surface and the morphology of the very few semiconductor layers near the interface, are especially important for charge transport. Consequently, modification of the semiconductor-dielectric interface will have a great influence on charge carrier mobility and overall device performance. For an OTFT with a given semiconductor active layer, the dielectric-semiconductor interface is affected by the surface energy, surface roughness, trap density, surface polarity and dielectric constant of the dielectric layer [108, 110]. The surface energy mainly influences the morphology of the top deposited semiconductor layers. If the dielectric layer possesses similar surface energy to that of the semiconductor, the films usually exhibit large grains and low boundary density, which favour effective carrier transport.

It is commonly believed that dielectric surface roughness impedes charge transport by disturbing morphology and microstructure of the organic semiconductor layer from various points of view. These include decreased size of semiconductor grains, increased void and disconnectivity between grains and increased packing defects and enhanced molecular disorder [110-112]. These hindering effects have been observed in semiconductor layers deposited on rough dielectric surfaces by both vacuum evaporation and solution processing

[111, 113]. The trap density at the dielectric-semiconductor interface is another influence on effective field-effect mobility of charge carriers (e.g. decrease output currents). It is well-known that high trap density lowers carrier mobility (number of mobile charge carriers), causes unfavourable increase of all transistor parameters which control the operational voltage of these devices and degrades device performance [108].

Polar groups on the dielectric surface (dielectric surface hydrophobicity) is also proved to greatly affect device performance. It has been reported that surface polarity and polar functional groups led to smaller grain size, a larger number of localised trap states and thus afforded lower mobility and a more negative threshold voltage in OTFTs [114]. Kim *et al.* [115] found the same in addition to considerable hysteresis and degradation of device performances in ambient air. Source-drain current was also found to be more unstable (with respect to time) on polar dielectric surfaces [116].

Last but not least, although high-*k* gate dielectric is essential for low-voltage operation of OTFTs, it can adversely influence the quality of the dielectric-semiconductor interface and OTFTs characteristics. According to Lancaster *et al.* [117], poly (3-hexylthiophene) (P3HT) metal-insulator-semiconductor (MIS) capacitors formed on the high-*k* aluminium titanium oxide (ATO) were highly unstable in accumulation owing to a high concentration of (shallow) hole traps at the insulator-semiconductor interface or in near-interface insulator bulk states. They suggested a means to passivate such states is essential to make ATO suitable for use in MISFETs.

More importantly, it has been demonstrated that an increase in dielectric constant of the gate insulator results in a drop in carrier mobility. This *k*-dependent mobility is quantitatively explained in terms of two effects taking place at dielectric-semiconductor interface. First is the broadening of the density of states (DOS) in the semiconductor layer due to the static dipole disorder in the gate dielectric [59, 118]. Veres *et al.* [59] found that the thermal activation energy required for hopping transport in an amorphous (PTAA) semiconductor increased with *k*. They accordingly suggested that the randomly oriented dipoles present in a high-*k* dielectric increase the disorder in the semiconductor channel resulting in broadening of the DOS and consequently decreased carrier mobility. The mechanism proposed by Veres *et al.* [59, 118] for enhancement of carrier localisation due to polar dielectric surface is illustrated in Fig. 2.22.

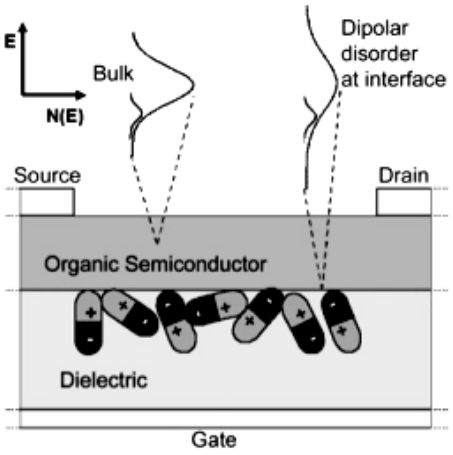


Fig. 2.22: Illustration of the density of states in the bulk of the (amorphous PTAA) semiconductor and at the dielectric-semiconductor interface [59].

The second effect is the formation of Fröhlich polaron in the active layer caused by the interaction between the charge carrier in the semiconductor and induced dipole moments in the dielectric [119]. Since both effects take place within short distance at the interface (<1 nm), modifying the high-*k* dielectric layer with an ultrathin layer of (a low-*k*) dielectric material is critical to improve dielectric-semiconductor interface and hence OTFTs performance [120, 121]. More details on dielectric surface modification are included in the following section.

2-3-5-2- Surface Modification of Dielectric Layers

Substantial work has been devoted to eliminate or weaken the semiconductor-dielectric interfacial effects on the electrical characteristics of OTFTs. As already pointed out, charge trapping at the dielectric-semiconductor interface due to poor semiconductor morphology (crystalline ordering) [80] or dipolar interactions between the semiconductor and polar surface of the dielectric [118] deteriorates device performance. In addition, dielectric surface roughness and hydrophobicity plays a crucial role in formation of dielectric-semiconductor interface and overall device performance.

It is generally well appreciated that the right choice of the dielectric is crucial for achieving optimum field-effect mobility, device stability, and reliability [122]. In addition, thin layers of solution-processed SAMs and polymers have been widely used to treat, control and improve properties of gate dielectric surface at dielectric-semiconductor interface [108].

Amongst various strategies adopted, thiol-based SAMs are mainly used on noble metals (especially gold), while silanes are applied onto oxides surface [123]. SAMs with phosphonic acid head groups are promising alternatives to thiols and silanes since they are relatively robust and can be attached to a wide range of oxide surfaces (Al_2O_3, TiO_2, etc.) [123]. Silane-based SAMs such as (hexamethyldisilazane) HMDS (and octyltrichlorosilane (OTS)) have been widely utilised on thermally grown SiO_2 dielectric layers [124]. Modifying SiO_2 surface in P3HT OTFTs with HMDS have been reported to improve mobility [125, 126].

The phase state of SAMs on dielectric surfaces is considered as an important dielectric-semiconductor interfacial parameter in OTFTs. Lee *et al.* [127] have studied the effects of octadecyltrichlorosilane (ODTS) SAMs in ordered or disordered phase states. They reported on higher crystallinity and a better interconnectivity between pentacene domains of a thermally grown film on relatively highly ordered SAMs which resulted in higher carrier mobility in the corresponding OTFTs. Similarly, Virkar *et al.* [128] measured higher mobilities in pentacene on dense and crystalline octyltrichlorosilane (OTS) surface modification layer compared to those on disordered OTS. Pentacene crystals grown on rougher substrates exhibits finer grain structure, hence higher density of grain boundaries acting as trap states which ultimately lowers charge carrier mobility [80, 111, 129].

A correct choice of SAM molecules can modulate surface energy (or wetting properties) of the dielectric layer to match that of the semiconductor and hence result in a better interface [110]. The presence of interfacial-adsorbed water on the hydrophilic surfaces can be attributed to randomly oriented dipoles acting as electronic trap states [109, 130]. Due to its functional groups, a SAM molecule can tune the dielectric surface energy, prevent adsorption of water molecules and hence can reduce the charge trap density [131, 132].

In addition to SAMs, spin-coated polymer films usually results in a very smooth surface, and show high efficiency in eliminating the interfacial effects on the performance of OTFTs. Cao *et al.* [133] fabricated a solution-processed P3HT device using a double layer dielectric composed of anodized Ta_2O_5 (120 nm) and cross-linked PVP (250 nm). They found increased mobility in OTFTs with a PVP layer covering the metal oxide dielectric, while the same low threshold voltage (1.7 V) of devices with single Ta_2O_5 dielectric layer was maintained. Cheng *et al.* [134] also achieved higher mobility in pentacene devices

with a hybrid PVP-capped magnesium oxide (MgO) dielectric. Reduced leakage current, smoother dielectric surface and optimised pentacene morphology were all accredited to the presence of PVP modifying (buffer) layer.

Investigating the correlation between interface roughness and mobility in solution-processed OTFTs, Chua *et al.* [135] developed an approach to control surface roughness by fabricating self-assembled polymer semiconductor-polymer dielectric bilayers, making use of vertical phase separation by varying the speed of solvent removal. Similarly, Fritz *et al.* [129] found reduced dielectric surface roughness by using a polystyrene (PS) modification layer which induced lager grains, higher crystallinity and higher mobility of pentacene OTFTs. Jang *et al.* [136] also reported on reducing surface roughness of nanoparticle-filled gate dielectric layer and hence optimising device performance by inserting a thin polymer layer between the dielectric and the semiconductor. Mobility of 1.2 cm^2/Vs was obtained for pentacene OTFTs with an 8 wt % barium strontium titanate (BST) nanoparticle-filled PVP nanocomposite dielectric layer capped with a thin (20 nm) layer of PS. Mototani *et al.* [137] studied the effect of surface modification using a SAM of HMDS on cross-linked PVP and investigated the performance of the OTFT. They concluded that not only the orientation and crystallinity of the polymer semiconductor, but also the dielectric properties, surface roughness, and the interface properties between the gate and semiconductor layers are important factors in determining the OTFT performance.

On the other hand, for a high performance OTFT, a low-*k* polymer at the dielectric-semiconductor interface is generally desirable, as low interface polarity has been shown to increase carrier mobility [59]. Thus, to comply with the need for a high-*k* dielectric layer for lowering the driving voltage and a low-*k* dielectric for improved charge carrier transport in the channel, dual-layer dielectrics have been employed in OTFTs **[**110]. Such (bilayer) dielectrics comprise of a low-*k* polymeric film on top of a high-*k* dielectric layer. An overview of examples of organic/inorganic dielectric bilayers, particularly employed in low-voltage devices, is given in the following section.

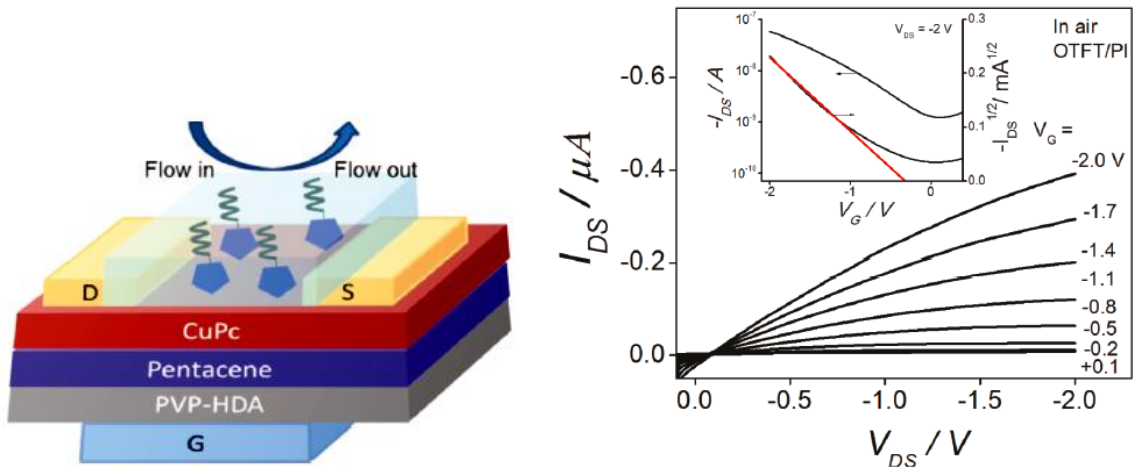
2-3-6-Low-voltage OTFTs

In recent years, OTFTs have particularly attracted substantial interest in inexpensive, single-use chemical or biological sensing applications due to their compatibility with

flexible, large-area substrates, simple processing, highly tunable active layer materials and possibility of operation at low voltage [26, 27]. Low-voltage or battery-driven OTFTs are of particular importance for many emerging applications, including low-power electronics, portable or wearable electronics, disposable and aqueous sensors and RFID tags.

Lowering the operational voltage of OTFTs is achieved by reducing the threshold voltage (V_T) and the subthreshold swing (SS), both of which are basically controlled by the gate dielectric and density of charge traps at dielectric-semiconductor interface. One fundamental approach for lowering V_T and SS is to use high-capacitance dielectric layers which can induce a high charge carrier density at the conducting channel at a lower operational gate voltage. According to equation (2.12), high capacitance can be achieved by either reducing dielectric thickness or using high-*k* dielectric materials [21].

Most common organic dielectrics have relatively low dielectric constants (k ~ 2-4) [29, 138] and hence ultrathin layers (d < 10 nm) [126] are required to obtain low-voltage transistor operation. Examples of solution-processed, ultrathin organic dielectric layers, such as cross-linked polymers [112, 140, 141], and cross-linked polymer blends (CPBs) [142] as well as self-assembled mono- [143] and multi-layer [144] (SAM) (d ~ 2.8 nm) gate dielectrics, have been successfully demonstrated in low-voltage (< 5 V) OTFTs. By using an ultrathin cross-linked PVP dielectric layer (~ 25 nm), Roberts *et al.* [26, 27] and Khan *et al.* [28] demonstrated the fabrication of robust and high performance OTFTs with an operating voltage lower than 1 V (Fig. 2.23).



(a) **(b)**

Fig. 2.23 (a) Schematic and (b) current-voltage output characteristics of a top-contact OTFT with CuPc (35 nm) and pentacene (25 nm) on a PVP-HDA (25 nm) gate insulator [28].

As illustrated in Fig. 2.23, 4,40-(hexafluoroisopropylidene) diphthalic anhydride (HDA) was used as the cross-linking agent, while vacuum-evaporated pentacene and copper phthalocyanine (CuPc) were used as the active semiconducting layer and the passivation layer respectively. This low operating voltage allows a device to detect pH between 3 and 11 and analytes (2,4,6-trinitrotoluene (TNT)) at concentrations on the order of a few parts per billion (ppb) in water [26-28].

Nonetheless, it is difficult to prepare large-area, pinhole-free and uniform organic gate dielectric exhibiting reasonably low leakage current with the thickness less than 100 nm. Furthermore, once a semiconductor was deposited on those ultrathin insulator films, the semiconductor molecules may penetrate into the dielectric layer and result in high gate leakage [31]. Hence, high-*k* dielectrics, including high-*k* polymers, metal oxides and organic-inorganic hybrids, have been attempted instead and enabled OTFTs to be operated at low voltages [21, 59].

For a given thickness, a high-*k* dielectric is more favourable as it allows necessary charges to accumulate at much lower drive voltage. Moreover, applying an ultrathin, low-*k* layer atop high-*k* dielectric layers has been a key element in optimisation of low-voltage OTFTs. Su *et al.* [139] reported a low-temperature, solution-processed ultrathin, high-*k* Al_2O_y/TiO_x dielectric bilayer was effectively used to achieve high-performance, CuPc-based OTFTs under a voltage of only - 2 V. The bilayer dielectric exhibited a very smooth surface (RMS = 0.22 nm) and reduced leakage current by 4 orders magnitude, compared to that of the single TiO_x layer, due to the blocking of electron conduction path by the Al_2O_y layer. They attributed the shift in the dip of the leakage current away from the zero bias and the voltage dependence of the capacitance of Al_2O_y/TiO_x bilayer to the presence of positively charge oxygen vacancies (defects) in the TiO_2 layer (and within the amorphous TiO_x/SiO_2 transition layer).

Excellent examples of high-*k* dielectrics for low-voltage OTFTs have been demonstrated using anodised Al_2O_3 (*k* = 8-10) [145-147] and ultrathin polymer/SAM-coated, anodised TiO_2 (*k* = 20-41) [29, 148] enabling OTFTs to operate at 1 V. Although anodisation is a cheap, well-established technique for making large-area, low-leakage metal oxide gate insulators, producing and handling such delicate, ultrathin dielectric layers (down to few nm) is challenging and laborious [149].

Most recently, Luzio *et al.* [15] fabricated top-gated, low-voltage OTFTs using a double-layered hybrid dielectric composed of an ultra-thin (< 10 nm) organic dielectric (PS) coupled with an ultra-thin (< 30 nm) high-*k* Al_2O_3 (deposited by plasma-based deposition (PLD)). They reported on superior device performance below -2 V using solution-processed, p-type and n-type semiconductors.

High-*k* ferroelectric polymeric dielectrics have been also used in the attempt to operate corresponding TFTs successfully at low voltage [33, 150]. Nonetheless, as discussed earlier, high-*k* dielectrics were shown to degrade the transport properties and carrier mobilities of many organic semiconductors, likely due to ionic impurities, polar functionality and induced dipole disorder causing a broadening of DOS at dielectric-semiconductor interface [15, 59, 151]. As a result, low output current densities, irreversible hysteresis and bias stress behaviour have made reliable operation at low voltages a challenge [152]. Solution-processed high-*k* relaxor ferroelectric polymers, for example poly (vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) (P(VDF-TrFE-CFE)) terpolymer (*k* ~70) has been successfully utilised to fabricate low-voltage (~ 3 V) OTFTs based on solution-processed p-type and n-type semiconductors. Li *et al.* [33] reported that modifying P(VDF-TrFE-CFE) dielectric layer with a polymer layer with lowest dielectric constant (polystyrene (PS), *k* ~ 2.6) and smallest thickness (~ 2.8 nm) resulted in highest mobility (0.62 cm^2/Vs) at low operating voltage (- 4 V) [34].

Hybrid dielectric layers, namely, high-*k* nanocomposites have been unfolding as the most promising alternative class of materials to obtain high-capacitance dielectrics essential to realise low-voltage OTFTs. The ability to form high-*k* dielectric layers of few hundreds of nanometre with excellent dielectric properties make nanocomposites attractive choices in low operational voltage applications. Various examples of high-capacitance dielectrics using nanoparticle-filled low-*k* and high-*k* polymeric dielectric materials have been attempted and successfully utilised in OTFTs. As demonstrated by Schroeder *et al.* [149], pentacene OTFTs using $BaTiO_3$-filled high-*k*, poly(vinyl alcohol)-*co*-poly(vinyl acetate)-*co*-poly(itaconic acid) (PVAIA) nanocomposite dielectric layer (~ 170 nm) successfully operated under -4 V, while maintaining a mobility up to 0.4 cm^2/Vs.

Most recently, Zhou *et al.* [153, 154] reported on aluminium titanate (AT) nanoparticles in PVP-based nanocomposite. The AT nanoparticles were modified using n-

octadecylphosphonic acid (ODPA) prior to addition to the PVP matrix. At 4 vol % concentration, dielectric constant of 8.2 was measured at 1 kHz, about twice that of pristine PVP. While the pentacene TFT with PVP dielectric had carrier mobility (μ) of 0.3 cm^2/Vs and a threshold voltage (V_T) of -14 V, devices using the nanocomposite dielectric exhibited improved μ of 0.4 cm^2/Vs and V_T of -5 V. Making use of inject printing, Liu *et al.* [155] prepared high-*k* PVP-based nanocomposite and fabricated directly printable gate dielectric film for OTFT. They reported on pentacene TFTs using 3 wt % TiO_2 nanocomposite with increased capacitance density (C_i) of 107 pF/mm, improved μ of 0.58 cm^2/Vs and reduced V_T of -5.4 V, compared to those of pristine PVP; C_i of 75 pF/mm, μ of 0.23 cm^2/Vs and V_T of -9.1 V.

Most recently, Beaulieu *et al.* [156] demonstrated low-voltage (< - 6 V) OTFTs using high-*k* cyanoethyl pullulan (CYELP) filled with ZrO_2 as a high-capacitance nanocomposite dielectric. The best device performance (μ=8 cm^2/Vs, V_T = -1 V) was obtained using nanocomposite dielectric containing 50 wt % ZrO_2 and 50 wt% CYELP, followed by dielectric surface modification using ODPA. Zirkl *et al.* [157] reported on low-voltage (-3 V) OTFTs with high-*k* oxide/polymer nanocomposites. The dielectric layer consists of two layers; a 25-30 nm thick ZrO_2 deposited by oxygen reactive sputtering coated with a thin (~ 15 nm) layer of poly (α-methyl styrene) (PαMS) or poly(vinyl cinnamate) (PVCi) to form a smooth and dense gate dielectric.

Despite notable attempts on preparation of high-*k* dielectric nanocomposites using high-*k* polymer matrix and nanoparticle fillers [74, 158], no significant work has been done so far to fabricate low-voltage, OTFTs using solution-processed high-*k* nanocomposite dielectrics (using high-*k* polymer matrix). In this work, we initially aimed at achieving high-*k* (*k* ~ 4 - 20) nanocomposite gate dielectrics by varying nanoparticles concentration in both low- and high-*k* polymer matrices. Substantially higher *k* values were obtained using high-*k* which enabled successful realisation of ultralow-voltage (< 1.5 V) OTFTs using both solution-processed and vacuum-deposited semiconductor active layers. Such low-operational OTFTs were fabricated using novel solution-processed, bilayer gate dielectrics of high-*k* nanocomposites capped with a low-*k* polymer operating at ultralow voltages.

Chapter 3

Methodology

3-1- Nanocomposite Preparation

As previously mentioned, a (nano-) composite material is a mixture of two or more component materials behaving like one system with combined properties of the multiple constituents. However, merely combining the components would not result in an end product with desirable properties. Various parameters play a part in obtaining a homogenous nanocomposite suspension with excellent processability and dielectric and electrical characteristics. Concentration, dissolution and viscosity of the polymeric matrix, loading (wt %) and degree of dispersibility of nanoparticles and solvent choice and compatibility are amongst the parameters to be carefully tailored to acquire a high quality nanocomposite suspension.

The high-*k* nanocomposite suspensions developed and effectively used in this work consist of a polymeric matrix (low-*k* or high-*k*) incorporated with high-*k* nanoparticle fillers. Here, we first discuss the possible choices of polymer matrix and high-*k* nanoparticles tried in this project. This is followed by a description of the surface modification of nanoparticles and an outline of procedures adopted to prepare the nanocomposite using both low- and high-*k* polymer.

3-1-1- Choice of High-*k* Nanoparticle Fillers

As discussed in section 2-2-3, a high-*k* nanocomposite dielectric can be obtained by using either high-*k* nanoparticles or a high-*k* polymer matrix. It has been previously shown that the dielectric constants of films incorporating high-*k* ferroelectric nanoparticles are inherently less than the bulk values due to oxygen defects at the electrode/dielectric interface [75]. In the bulk form, ferroelectric materials have a capacitance sharply peaked at their Curie temperature (T_C). As illustrated in Fig. 3.1, at the peak, the dielectric constant of bulk ferroelectric materials (e.g. BST) can be of the order of tens of thousands [159].

However, in a thin film form, T_C is widely known to drop, the dielectric constant substantially reduces to a few hundreds and in general the temperature dependence of the dielectric constant has only a broad maximum [60, 159]. Accordingly, the dielectric constant becomes even smaller by at least an order of magnitude in nanoparticle form (single crystals).

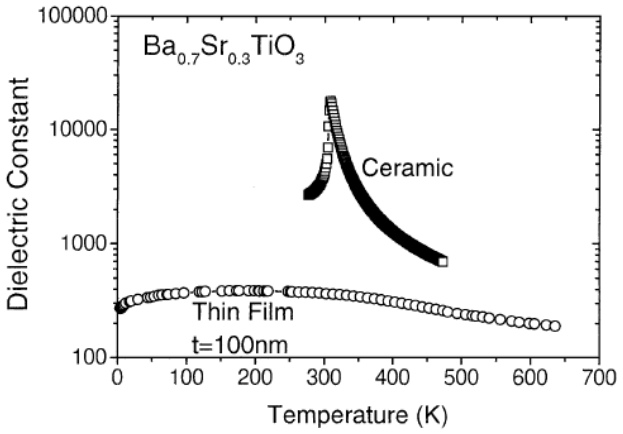


Fig.3.1: Comparison of dielectric constant of ferroelectric BST in bulk and thin film and its temperature dependence [159].

For the purpose of this project, four different ABO_3 nanoparticles with perovskite structures have been investigated and attempted. Table 3.1 contains specifications of these commercially available nanoparticles (nanopowder) as provided by the supplier, Sigma Aldrich. These nanoparticles have been selected based on their outstanding dielectric properties judged suitable for a variety of applications, as reported in the literature.

Nanoparticles	**Linear Formula**	**Size (nm)**	**Density (g/mL)**	**Molecular Weight**
Barium Strontium Titanate (BST)	($BaTiO_3$) ($SrTiO_3$)	<100	4.91	416.68
Barium Zirconate (BZ)	$BaZrO_3$	<50	5.52	276.55
Calcium Titanate (CT)	$CaTiO_3$	<100	4.1	135.94
Calcium Zirconate (CZ)	$CaZrO_3$	<50	5.11	179.30

Table 3.1: Specifications of nanoparticles utilised in this work.

BST is an attractive candidate in applications such as (super) capacitors, memory and transistor devices due to its very high dielectric constant (> 1000), low leakage and high resistance reliability [160]. In bulk, BST has a dielectric constant as high as a few tens of thousands but that greatly reduces to a two-digit value in nanoparticle form [159, 161]. Dimitrakopoulos *et al.* [86] stated a dielectric constant of ~16 for BST nanoparticles. Recently, Huang *et al.* [162] reported a dielectric constant of 47 for synthesised nanocrystals of BST nanoparticles of 25-30 nm, while barium titanate (BT) nanoparticles of the same size exhibited a dielectric constant of 34. The same group also reported a dielectric constant of 18 for a poly(methyl methacrylate) (PMMA)-BST blend with 1:1 ratio.

BZ is one of the most investigated perovskite materials with various unique physical properties such as very high melting point (2,600 °C), small thermal expansion coefficient, poor thermal conductivity, and excellent mechanical properties [163]. BZ is a cubic oxide perovskite that does not undergo phase transitions in the range 4–1600 K [164] and has a reasonably wide band gap of 5.3 eV (compared to other oxides) and high dielectric constant [165]. Stetson *et al.* [166] and Kumar *et al.* [167] reported a room temperature dielectric constant of 32 for BZ nanoparticles, while Roberts *et al.* [168] gave a value of 43.

CT belongs to a class of so-called incipient ferroelectric or quantum paraelectric materials whose dielectric constant increases with decreasing temperature and saturates at low temperatures [169]. Nonetheless, CT is referred to as a ‘higher’ quantum paraelectric since its dielectric constant saturates at a higher temperature than that for other quantum paraelectric materials, e.g. SrTiO and KTaO [170, 171]. Thin films of CT exhibit a high dielectric constant of a few hundred, tunable by an electric field and suitable for use in microwave devices such as filters, phase shifters and antennas [172]. Wise *et al.* [173] reported on a high dielectric constant of 162 (at microwave frequency; 1.49 GHz), while Hao *et al.* [174] demonstrated a dielectric constant of about 150 for thin films of PLD (pulsed-laser deposited) CT at room temperature - very close to that in the bulk of the material. In addition, Hu *et al.* [175] reported a dielectric constant of 13 for a composite of CT (40 vol %) and polytetrafluoroethylene (PTFE).

Finally, various studies have focused on the dielectric properties of CZ nanocrystals and thin films. CZ is a high-temperature perovskite ceramic with excellent dielectric and microwave properties widely used in multilayer ceramic capacitors (MLCC), microwave resonators, filters, solid electrolytes, hydrogen sensors, and thermistors [176]. Nanoparticles of CZ possess a reasonably high *k* value, for instance Prasanth *et al.* [177] demonstrated CZ nanoparticles with dielectric constant of 23.8. Stetson *et al.* [166] also reported dielectric constant values in the range of 24 - 28 for CZ and strontium zirconate (SZ), while Lee *et al.* [176] quoted a dielectric constant of 32 for CZ [162]. CZ (and BZ) has been also used as dopants/additives to shift T_C to higher temperatures, increase dielectric constant and obtain flat capacitance-temperature characteristics (to form a distribution of Curie points) [178].

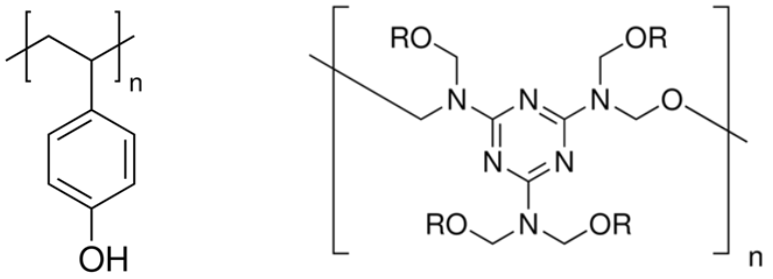
Initially, all four nanoparticles were intended to be used to prepare nanocomposite suspensions, in particular for low-*k* polymer matrices. Nonetheless, following careful consideration and conclusions reached on best nanoparticle type, the decision was made to narrow the scope of the work. The main focus was thus invested in BST and BZ nanoparticles, and especially their use in nanocomposites with high-*k* polymer matrix. The comprehensive results and discussions presented in chapter 4 justify our ultimate choice of nanoparticles suitable in OTFTs.

3-1-2-Choice of Polymer Matrix

3-1-2-1 Low-*k* Polymer

Recalling laws of mixing studied in section 2-2-3, a high-*k* nanocomposite can be obtained by incorporating high-*k* nanoparticles in either a low-*k* or a high-*k* polymer matrix. Nonetheless, one can speculate that for given nanoparticles, a nanocomposite with a lower *k* would be achieved using a low-*k* polymer matrix. This project was initially aimed at preparing and characterising low-*k* polymeric-based nanocomposite dielectrics. PVP [poly (4-vinylphenol)] has been our choice of low-*k* polymer matrix, since it is easily processed from solution and exhibits excellent dielectric properties with a dielectric constant of ~ 4. Halik *et al.* [179, 180] reported a *k*- value of 3.6 for thin films of PVP, while Jang *et al.* [136] and Chen *et al.* [181] measured 4.3 and 3.9 respectively.

In addition, PVP can be thermally cross-linked with the addition of a cross-linking agent, such as poly (melamine-co-formaldehyde) [PMF]. Chemical structures of PVP and the cross-linking agent PMF are shown in Fig. 3.2. The process of cross-linking is particularly crucial since it results in the formation of robustly interconnected dielectric films which remain intact against many organic solvents (e.g. acetone, propylene glycol methyl ether acetate (PGMEA) and 1,2-dichlorobenzene (DCB)), acids and developers.



(a) **(b)**

Fig. 3.2: Structural formula of (a) PVP and (b) PMF.

PVP has been widely used as a promising low-*k* polymeric matrix in nanocomposite dielectrics. Chen *et al.* [181] incorporated TiO_2 nanoparticles (k = 80) in PVP with the hope to increase the dielectric constant. They reported a ~ 30 % increase in *k* for only 7 wt % TiO_2. The corresponding OTFTs exhibited comparable device characteristics to that of pristine PVP at slightly better operating voltage (V_T). The most closely related work has been demonstrated by Jang *et al.* [136] who reported on high mobility TFTs using a solution-processed PVP/BST nanocomposite dielectric layer. By incorporating variable BST loadings (4-11 wt %) into a PMF-added PVP solution, this group achieved an enhanced dielectric constant, from 3.9 for pristine PVP to 6.6 for 11 wt % BST. Jang *et al.* reported on mobilities of 0.96 and 1.2 cm^2/Vs measured on pentacene TFTs using pristine 8 wt% BST nanocomposite dielectric and that coated with a thin layer of polystyrene (PS) respectively [136].

In this work we prepared PVP-based nanocomposite suspensions with 2-11 wt % nanoparticles loading. Nanoparticles were surface-modified in order to promote better dispersion and more uniform nanocomposite suspensions. The procedures for nanoparticle modification and nanocomposite preparation are thoroughly described in sections 3-1-3 and 3-1-4 respectively.

3-1-2-2 High-*k* Polymer

As the project progressed, the goal to further enhance *k* and the capacitance density (C_i) of the nanocomposite dielectric layers and thereby reduce the operating voltages of TFTs, necessitated substituting low-*k* PVP with a high-*k* polymer. PVP-based nanocomposite suspensions suffer from agglomeration and precipitation of nanoparticles (especially at higher nanoparticles loading) which leads to less uniform suspension and film when deposited. Moreover, since PVP has a relatively low dielectric constant, an ultrathin layer dielectric is required to operate such OTFTs at low voltage.

Yang *et al.* [140] reported on low voltage (< 3 V) OTFTs using a 10-nm thick cross-linked PVP layer. Nonetheless, such thin layers are not easy to reproduce and prone to high leakage current. By incorporating high-*k* nanoparticles into a high-*k* polymer matrix, a nanocomposite dielectric layer with improved uniformity and a much larger capacitance density was obtained at smaller nanoparticles loading and thickness. In addition, it has been demonstrated that by carefully identifying the best combination of a high-*k* polymer, solvent and nanoparticles-to-polymer volume ratio, a reproducible, uniform, high-*k* nanocomposite suspension was made without the need for nanoparticles surface modification.

Other high-*k* dielectric polymers of choice reported in low-voltage OTFTs are polyvinylidene fluoride (PVDF) homopolymer [77, 182, 183] and other of its copolymers such as P(VDF-trifluoroethylene) (P(VDF-TrFE)) [67, 182] and P(VDF-TrFE-chlorofluoroethylene) (P(VDF-TrFE-CFE)) [33, 34]. Fluoropolymer PVDF and its well-known copolymers are the most developed and promising ferroelectric polymers because of their high spontaneous polarisation and chemical stability [184]. They are thermoplastics of high thermal stability and technologically important because of their availability in different crystalline forms. The discovery of the piezoelectric properties of PVDF by Kawai in 1969 [185], and the study of its pyroelectric and nonlinear optical properties [186, 187] led to the discovery of its ferroelectric properties in the early 1970s. Since that time, considerable development and progress have been made on both materials and devices based on PVDF [184]. PVDF is a semicrystalline polymer with pyro and piezoelectric properties. The high permittivity and relatively low dissipation factor of PVDF has made it a candidate for many potential applications [183].

In this work, poly (vinylidene fluoride-*co*-hexafluoropropylene), P(VDF-HFP) for short, has been chosen as the high-*k* polymer host to produce high-*k* nanocomposite dielectrics. The crystalline structure of the P(VDF-HFP) is similar to that of PVDF. It is a highly processable, thermoplastic copolymer comprising both a crystalline (vinylidene fluoride) and an amorphous phase (HFP units) (Fig. 3.3). It offers high dielectric constant (k ~11 at 1 kHz) and high dielectric strength due to its ferroelectric domain [188]. However, introducing HFP units to the PVDF backbone generates a copolymer that exhibits certain advantages compared with the homopolymer, such as enhanced piezoelectricity and improved mechanical behaviour.

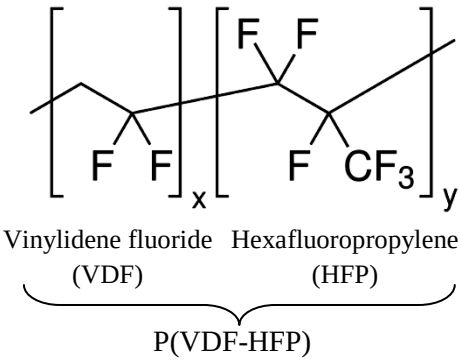


Fig. 3.3: P(VDF-HFP) chemical structure.

The degree of crystallinity of the P(VDF-HFP) is sufficiently reduced in comparison with pure PVDF, whereas the flexibility and chemical resistance are enormously enhanced [189]. In comparison with PVDF polymer, P(VDF-HFP) has a lower glass transition temperature (T_g), so-called Curie temperature, and greater solubility in organic solvents [190].

Kim *et al.* [74, 191] reported on BT-P(VDF-HFP) nanocomposites with high dielectric constant and dielectric strength. They obtained a dielectric constant of ~ 37 for nanocomposites consisting of 50 vol % modified BT with pentafluorobenzyl phosphonic acid (PFBPA) in P(VDF-HFP). They attributed the high breakdown strengths and low leakage currents of such nanocomposites to the surface modification of nanoparticles by phosphonic acid ligands. The modification led to reduced percolative pathways by virtue of improved dispersion and less aggregation of nanoparticles. Most recently, Ehrhardt *et al.* [158] reported on BT-P(VDF-HFP) nanocomposites with a dielectric constant (~ 25), about 5 times higher than that of the pristine polymer. They modified BT nanoparticles with PFBPA to inhibit agglomeration and improve wetting properties of P(VDF-HFP).

However, besides a few studies of the properties of P(VDF-HFP)-based dielectrics in capacitors, no other significant work on application of such gate dielectric layers in OTFTs has been reported. Hence, in this project, we took an original step forward to fabricate OTFTs using P(VDF-HFP)-based nanocomposites and to evaluate whether the gate dielectrics comprising these nanocomposites would be beneficial, particularly in lowering operational voltages in OTFTs.

3-1-3-Surface Modification of Nanoparticles

As mentioned in section 2-2-3-1, surface modification of nanoparticles is a useful approach to suppress nanoparticles' aggregation and facilitate their dispersion in the host polymer matrix. As a result of modification, a well-dispersed, homogenous nanocomposite suspension is formed which subsequently allows uniform thin films to be deposited to serve as high quality dielectric layers in capacitors and transistors.

In this work, surface modification has only been applied to nanoparticles prior to their incorporation into low-*k* PVP polymer. No surface modification was necessary when P(VDF-HFP) copolymer was used. Careful selection of polymer viscosity and nanoparticle loading induced bonding between the fluorine and existing -OH groups on non-modified nanoparticles surface. This resulted in the formation of a relatively homogenous suspension. As depicted in Fig. 3.4, coupling agents capable of forming SAMs, consist of three unique segments:

(i) The head (coupling/binding) group that strongly binds to the surface. The most common head groups are thiols, silanes, phosphonates and sulfonates.

(ii) The terminal functional group that carries specific chemical functions and interacts directly with the surroundings.

(iii) The tail which connects the head to the functional group and controls structural flexibility, solubility and the packing density of the SAMs [38, 74].

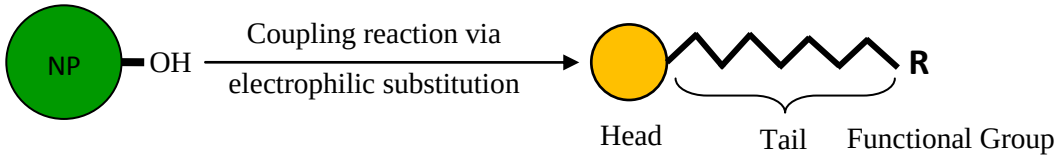


Fig. 3.4: Schematic of the coupling between a nanoparticle and a SAM.

Table 3.2 contains the specifications of those SAMs (purchased from Sigma Aldrich) trialled in this work. This selection allowed study of the effect of chain length (short, medium and long) as well as chemistry of the head group on the functionalised nanoparticles, nanocomposite suspension and dielectric layer.

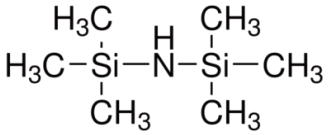
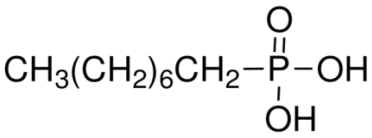
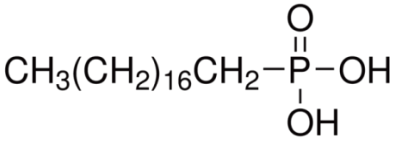
SAM	Molecular weight (g/mol)	Chemical formula
hexamethyldisilazane (HMDS)	161.39	
octylphosphonic acid (OPA)	194.21	
octadecylphosphonic acid (ODPA)	334.47	

Table 3.2: Chemical structure of SAM molecules used in this work as modifiers.

With regards to modification of nanoparticles surface, PA coupling agents have been the SAMs most reported to modify various metal oxides such as TiO_2, ZrO_2, HfO_2, $BaTiO_2$ and Al_2O_3. These agents couple onto the surface of the metal oxides via either heterocondensation with surface hydroxyl groups or coordination to metal ions on the surface [153, 191]. The surfaces of ferroelectric metal oxide (MO) nanoparticles usually have many defective sites, which are typically terminated with a hydroxyl group (-OH) in the form of MO-OH. These hydroxyl groups are generally considered as the linking bridge between the nanoparticle surface and SAMs via organic coupling reactions where an electrophilic substitution occurs replacing the proton in the surface hydroxyl group with the binding group (head) of the SAM (Fig. 3.4). Therefore, the SAM molecule has to have at least one good functional group to receive the hydroxyl proton and form a stable product. The head of the SAM molecule should also have valence of two or greater to provide a bridge between the nanoparticle surface and the terminal functional group. Other desired attributes of SAMs are namely fast binding kinetics, straightforward binding reaction, stability of binding and non-toxicity [74, 192].

The schematic in Fig. 3.5 visualises how surface functionalisation of nanoparticles with SAMs influences their degree of dispersion and free suspension in the polymer matrix, with less likelihood of agglomerates (or lumps in thin films). In addition, this schematic envisages the possibility of achieving high-*k* nanocomposites with lower volume fraction of well-dispersed nanoparticles.

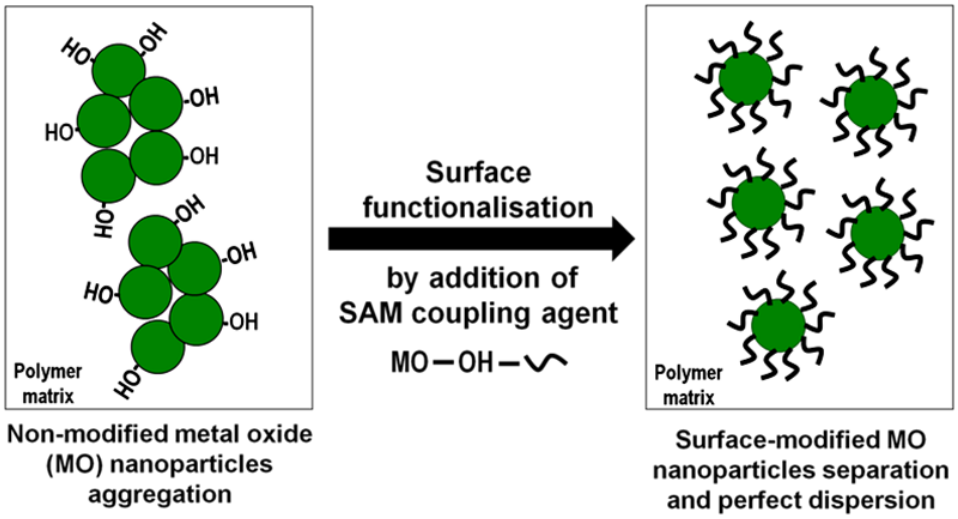


Fig. 3.5: Comparison between modified and non-modified nanoparticles in a polymer matrix.

Although MO nanoparticles are reported to contain hydroxyl groups on their surface and in the crystal lattice, the surface content of -OH is not sufficient to significantly improve the surface reactivity with coupling agents and dispersants. Hydroxylation, or so-called H_2O_2 treatment, as a common approach to introduce denser surface -OH population can be a prerequisite for effective modification of nanoparticles [193]. On the other hand, hydroxylation can standalone be a surface modification technique without the need to introduce additional SAMs.

Throughout the literature, a wide range of methods for surface modification of nanoparticles is covered. In this work, four different surface modification approaches, including hydroxylation and surface modification using silane- and phosphonic acid-based SAMs, have been attempted. An overview of these methods is illustrated in Fig. 3.6. These approaches have been considered suitable from different points of view such as processability, reproducibility, safety and risk assessment, stability and quality of the subsequently prepared nanocomposite and finally characteristics of the end device.

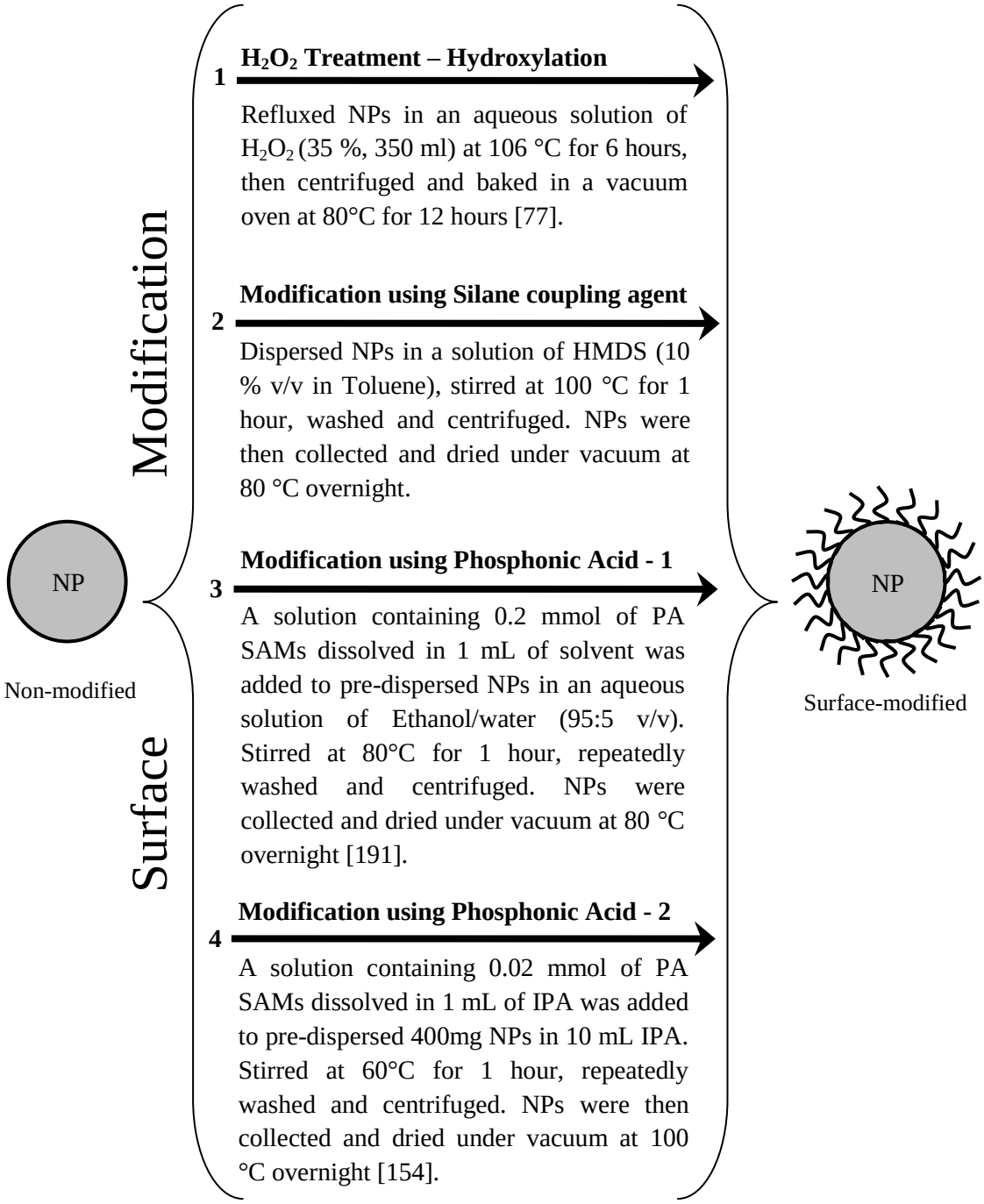


Fig. 3.6: Various approaches adopted in this work towards surface modification of nanoparticles (NPs).

Hydroxylation was the first method tried. It was only applied to BST nanoparticles and nanocomposite suspensions of hydroxylated BST (h-BST) were subsequently processed in PVP. The specific hydroxylation approach adopted here was first proposed by Zhou *et al.* [77] who studied the dielectric properties of PVDF-based nanocomposites filled with surface hydroxylated $BaTiO_3$ (h-BT) nanoparticles.

The second approach (Fig. 3.6.) involved using HMDS - the surface modifier with shortest chain length (a single -H_3C) and smallest molecular weight. No reference to using HMDS to modify nanoparticles for nanocomposites has been found thus far in literature searches. Due to the novelty of this process, a number of different solvents and concentration ratios had to be tried to obtain the most suitable HMDS solution. A 10 % v/v solution of HMDS in toluene was finally chosen and nanoparticle modification was followed up as summarised in Fig. 3.6.

A PVP-based nanocomposite is prepared straightway by dispersing variable wt % loading of HMDS-modified nanoparticles (described in section 3-1-4). The HMDS-based surface modification technique was only applied to BST nanoparticles due to novelty-bound difficulties involved in obtaining a good quality modified-BST-PVP nanocomposite suspension and gate dielectric layer. As a result, the project was directed towards utilising phosphonic acid-based SAMs by adopting modification methods already reported in the literature.

Two slightly different approaches have been dominantly pointed out in the literature with regards to surface modification of nanoparticles using phosphonic acid-based (PA) SAMs. The first approach (Fig. 3.6.) is adopted from Kim *et al.* [191] who reported on modifying surface of BT nanoparticles using PA coupling agents and preparation of nanocomposites using such modified nanoparticles in a P(VDF-HFP) matrix. However, this approach did not result in a satisfactory outcome and a number of complications arose during application of this method. For instance, centrifugation and collection of nanoparticles after being heated in the SAMs solution failed; nanoparticles sank to the bottom only 10 sec into centrifugation at 6000 rpm. Various reasons can be proposed for the failure of this method when adopted in our process of surface modification and nanocomposite preparation. Firstly, the method employed by Kim *et al.* [191] involved ball-milling of modified BT nanoparticles prior to addition to the polymer matrix - a technique which has not been available and accessible in this project. Secondly, BT nanoparticles used by the aforementioned group were 30 - 50 nm in diameter - smaller than our commercially purchased nanoparticles, especially BST and CT (both 100 nm). Therefore, attachment of OPA/ODPA molecules to the surface of larger nanoparticles made them so heavy that they lost their floating/suspending properties and precipitated quickly. Thus, the need for an alternative approach was inevitable.

Following investigation of other possible approaches, the surface modification method finally settled on for this project was an optimisation of the approach demonstrated by Zhou *et al.* [154]. They reported on novel polymer nanocomposite dielectrics based on ODPA-functionalised aluminium titanate (AT) nanoparticles as in a PVP polymer matrix. Here, we have modified their approach accordingly to meet the requirements of our project. This ultimately optimised method is perceived as the finest, easiest processable and repeatable surface modification method. It has been applied to all four types of nanoparticles used in this project together with OPA and OPDA coupling agents. A summary of this surface-modification method using phosphonic acids (PAs) is given Fig. 3.6. After completion of nanoparticle surface-modification, it is preferred that modified nanoparticles are used straightaway to prepare the nanocomposite suspension. However, if prompt use of modified nanoparticles is not possible, they should be stored in a vacuum desiccator to avoid moisture absorbance. The procedure of nanocomposite preparation using surface modified nanoparticles is described in the following section.

3-1-4-Process of Nanocomposite Formulation

Depending on the choice of polymeric matrix (discussed in section 3-1-2), slightly different approaches were pursued in the preparation of nanocomposite suspensions. As mentioned in 3-1-3, in order to obtain a homogenous suspension using a low-*k* polymer matrix, nanoparticle fillers have to be surface modified. Initially, suspensions using non-modified BST and CZ nanoparticles in PVP were made, but non-uniform dispersion and subsequently poor quality films were obtained. The reason identified was lack of sufficient adhesion between the non-modified nanoparticles and the low-*k* polymer which led to fast agglomeration and subsequent precipitation. Although here we report on using non-modified nanoparticles for preparing nanocomposites with high-*k* polymer, surface modification should not be completely ruled out as a dispersion-assisting option. We envisage that incorporating SAM-modified nanoparticles into high-*k* polymer will result in relatively finer nanocomposite suspensions with minimal occurrence of agglomeration. Such nanocomposites might be then processable using printing techniques in which extremely uniform suspensions are required to avoid clogged nozzles. Nonetheless, diameters of nanoparticles play a crucial role in obtaining high quality nanocomposites, as surface-modified nanoparticles with larger diameter are more likely to descend to the bottom during centrifugation or while the suspension is left standing for some time.

3-1-4-1- PVP-based Nanocomposite Preparation

PVP-based nanocomposite suspensions were prepared by addition of SAM-modified nanoparticles to the premade polymer matrix - a PVP solution with added PMF cross-linker formulated as follows:

i. 10 wt % (100 mg ml^{-1}) PVP (M_w ~ 25,000, Sigma-Aldrich 436224) powder dissolved in PGMEA (99.5%, Sigma-Aldrich 484431) and stirred overnight

ii. 5 wt % (50 mg ml^{-1}) cross-linker PMF (84 wt % in 1-butanol, Sigma-Aldrich 418560) is added to the above 10 wt % PVP solution and stirred overnight.

iii. Solution is then filtered through 0.45 μm and 0.25 μm polytetrafluoroethylene (PTFE) syringe filters successively, and stored in a new vial before use. PMF-added PVP solution is stable for months with no degradation observed.

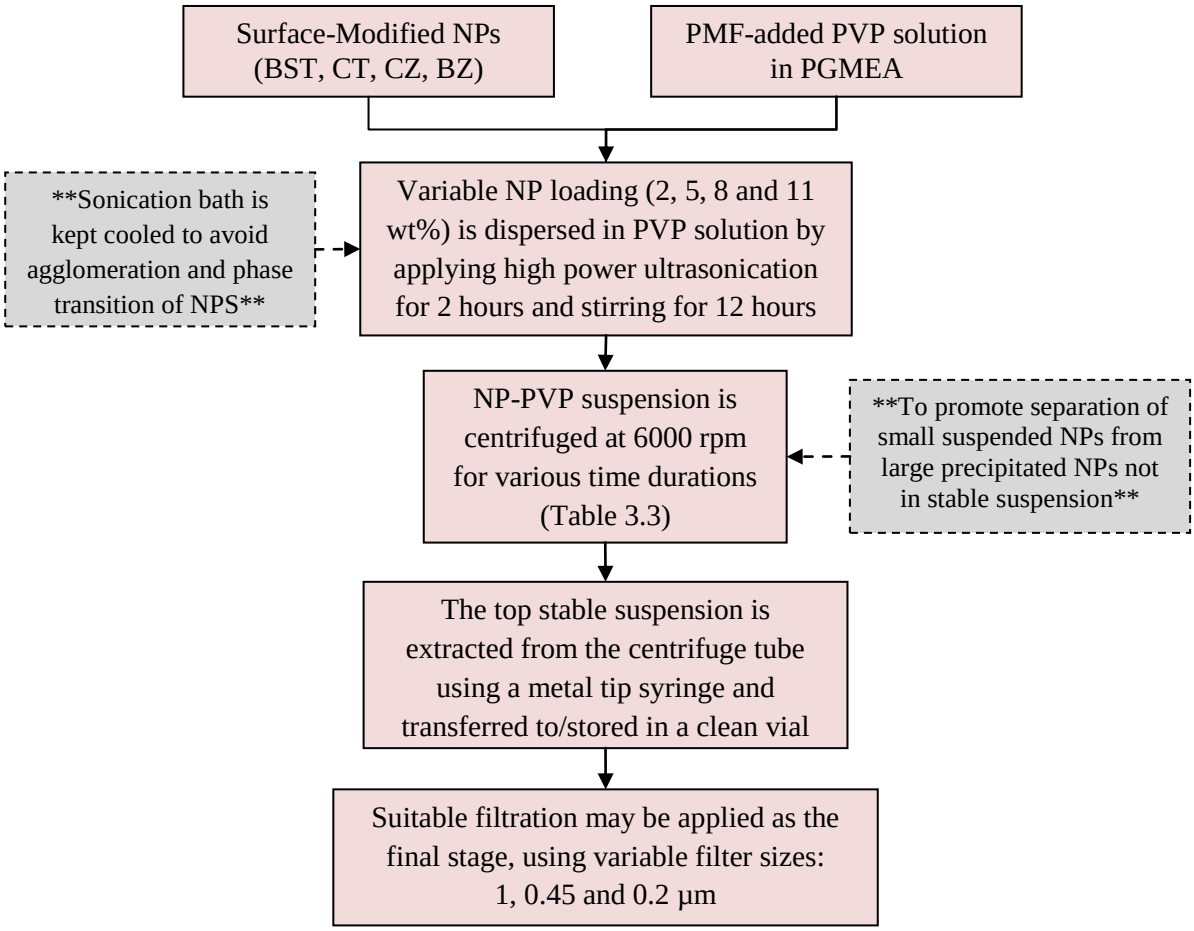


Fig. 3.7: Step-by-step process for preparation of nanocomposite suspensions.

Once cross-linked PVP solutions were ready, the nanocomposite suspensions were prepared by following the step-by-step procedure outlined in Fig. 3.7. Suspensions containing variable (wt %) concentrations of the six different surface-modified nanoparticles, namely OPA-BZ, OPA-CZ, ODPA-CZ, HMDS-BST, OPA-BST and OPA-CT were formulated.

This procedure was implemented for formulating PVP-based nanocomposites using any of the four nanoparticle types modified with any type of SAM molecules. However, the centrifugation duration had to be accordingly adjusted depending on nanoparticle size, SAM chain length and NPs wt % loading.

Table 3.3 records the time durations used until apparent 'precipitation' took place for various combinations of nanoparticles and SAMs.

Nanocomposites filler	**Centrifugation duration**
HMDS-modified BST	3-4 min
OPA-modified BZ	1.5-2 min
OPA-modified CZ	1.5 -2 min
ODPA-modified CZ	40-60 sec
OPA-modified BST	1-1.5 min
OPA-modified CT	1-1.5 min

Table 3.3: Centrifugation duration for each nanocomposite filler

As can be perceived from the above data, the longer the SAM chain is the faster precipitation of nanoparticles occurs. For instance, ODPA-modified CZ nanoparticles required less centrifugation duration to exhibit apparent phase separation than OPA-modified CZ, since ODPA has an 18-carbon chain compared to the 8-carbon of OPA. In addition, the bigger the nanoparticles' diameters are, the quicker they settle during centrifugation, e.g. OPA-modified BST nanoparticles precipitate almost four times faster than OPA-modified CZ (and BZ) nanoparticles.

After experiencing fast precipitations and large aggregations, speculation arose regarding accuracy of the information provided by Sigma Aldrich on nanoparticles' size. Thus, Malvern Zetasizer equipment with dynamic light scattering (DLS) implemented as its measurement method has been utilised to verify nanoparticles' diameter. The Zetasizer is capable of detecting particles as small as 10 nm, sufficient for the expected size of purchased nanoparticles. As presented in Fig. 3.8, plotting mean particle density versus particle size (i.e. size distribution), the mean particle size of BST nanoparticles was detected to be 342 nm; substantially in contradiction to that quoted (< 100 nm) by the supplier. Thus it appeared that information given by the supplier could not always be relied upon.

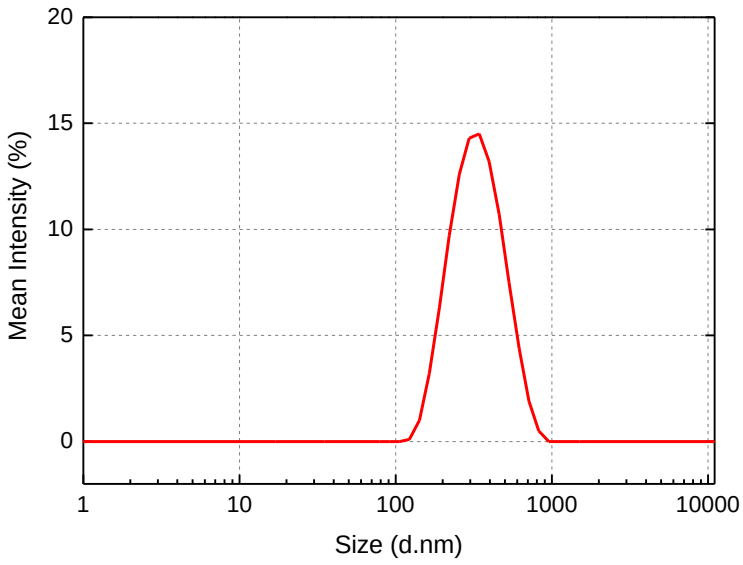


Fig. 3.8: Size distribution of BST nanoparticles determined by DLS, peak = 342 nm.

Pinpointing the average particle size offered a possible explanation for certain oddities observed in the behaviour of the corresponding nanocomposite suspensions. These affected dispersibility and precipitation of the nanoparticles, the stability and uniformity of the nanocomposite, and subsequently the dielectric properties of the deposited nanocomposite films.

The formulated nanocomposite suspensions were stable for up to a month and reasonably repeatable results could be obtained from devices made using the same suspension. However, as clearly illustrated in Fig. 3.9, nanocomposite suspensions started to settle when left standing for more than a week.

Therefore it was necessary to ultrasonicate the suspensions for at least 30 minutes prior to forming a thin film. This would scatter any possible agglomerates, circulate nanoparticles inside the polymer matrix, induce a homogenous suspension and eventually result in the formation of a uniform thin layer when deposited. In rare cases, subsequent centrifugation and filtration was suggested to ensure no lumps of nanoparticles were present. However, this might have attenuated the initial concentration used in each nanocomposite, so the idea was dropped.

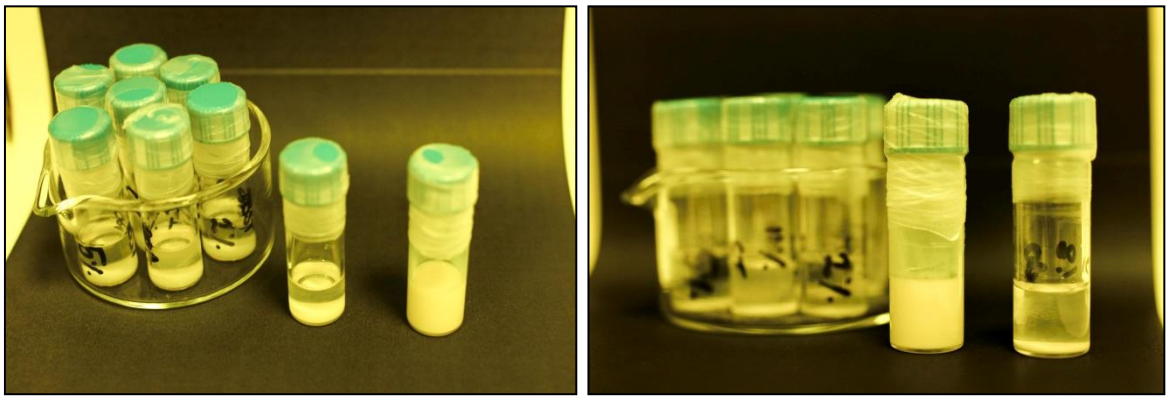


Fig. 3.9: Demonstration of nanocomposite suspensions when made fresh (milky) and left aside for more than a week (clear top portion with precipitants at the bottom).

Once the suspension was sonicated for sufficient amount of time, as can be observed from the above figure, it recovered its original milky form, regained all chemical and dielectric properties possessed by a freshly made suspension and remained stable for a week from then. Nonetheless, it was recommended that, where possible, one-month old nanocomposite suspensions were disposed of and fresh ones prepared and used.

3-1-4-2- P(VDF-HFP)-based Nanocomposite Preparation

Switching from low-*k* PVP to high-*k* P(VDF-HFP) in the nanocomposite preparations required extensive experimental work to identify a suitable solvent (Appendix A), polymer concentration and spin-coat speed (revolution per minute, rpm) for depositing a dielectric layer. The process of formulating nanocomposites using P(VDF-HFP) polymer matrix differs from that using PVP from various aspects. Firstly, P(VDF-HFP) comes in the form of pellets (Sigma-Aldrich 427187) with a molecular weight (M_w ~ 400,000) 16 times higher than that of PVP powder. As a result, a reduced percentage solution of P(VDF-HFP) compared to that of PVP has to be prepared to compensate for higher molecular weight.

A 10 wt % solution of P(VDF-HFP) resulted in a highly viscous solution hardly practicable for processing. Secondly, no cross-linking agent was introduced, since most fluoropolymers are stable due to their strong, polar covalent carbon-fluorine bonds. In addition, unlike the PVP film which was cross-linked at 200 °C, the P(VDF-HFP) layer has to be annealed at a relatively lower temperature below its melting temperature (T_m ~135-140 °C). Finally, with regards to nanocomposite preparation, the higher viscosity of P(VDF-HFP) and electronegativity of fluorine atoms in HFP enabled better dispersion of the nanoparticles without the need for surface modification.

The following schematic in Fig. 3.10 summarises the procedure taken up in this work to prepare nanocomposites using P(VDF-HFP) polymer matrix. Initially, all four available nanoparticle types were used in preparation of nanocomposite suspensions using P(VDF-HFP) polymer matrix. Based on the outcomes of trial experiments, it was decided to use only BST and BZ nanoparticles, since their incorporation into P(VDF-HFP) resulted in high quality, high-*k* nanocomposites without inclusion of surface modification. In addition, this selection of nanoparticles has allowed systematic analysis of nanoparticle size effect on properties of the nanocomposite suspension and electrical characteristics of the corresponding thin films. However, the possibility of obtaining good quality, P(VDF-HFP)-based nanocomposites by incorporating surface-modified CZ and CT nanoparticles should not be ruled out. Due to time constraints, surface modification had to be disregarded but suggested as possible future work.

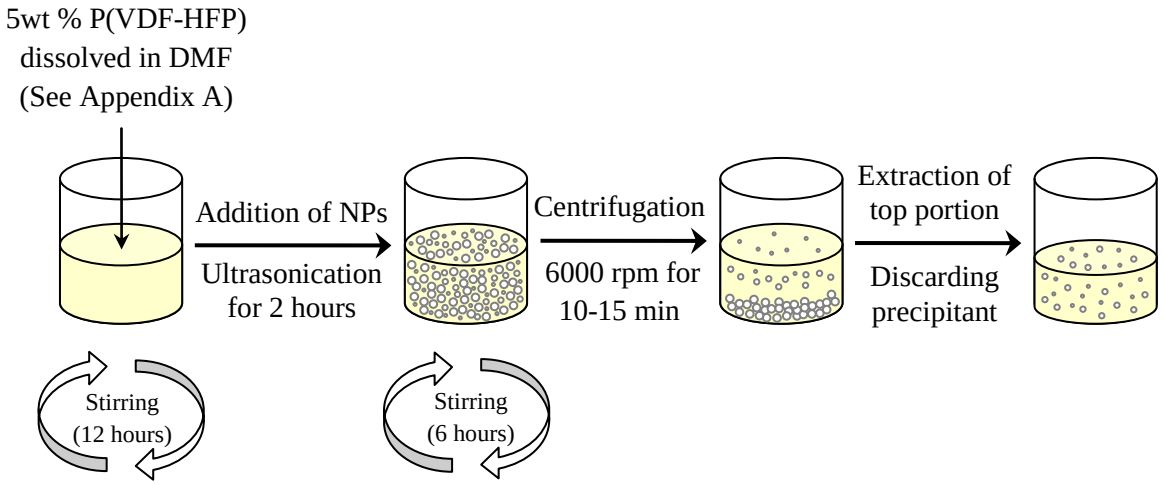


Fig. 3.10: Schematic of step-by-step process of P(VDF-HFP)-based nanocomposite preparation.

As one can perceive, procedures of nanocomposite preparation using PVP and P(VDF-HFP) are almost analogous, apart from elimination of a filtering step in the latter. Due to the relatively high viscosity of the P(VDF-HFP) polymer solution (in dimethylformamide (DMF)), the resultant nanocomposite suspension would clog the filter and not pass through. Therefore, filtering had to be discarded because of impracticality and emerging health and safety risks. In addition, as speculated, centrifugation duration for P(VDF-HFP)-based nanocomposites differed from that for nanocomposites using PVP matrix (Table 3.4).

Nanocomposites filler	Centrifugation duration
BST	10-12 min
BZ	12-15 min

Table 3.4: Centrifugation duration of P(VDF-HFP)-based nanocomposite suspensions. Centrifugation speed was set to 6000 rpm.

Higher viscosity of P(VDF-HFP) and its strong chemical affinity to hydroxyl groups present on the surfaces of nanoparticles provided a better matrix to keep the nanoparticles suspended. As a result, longer centrifugation was needed to observe precipitant in P(VDF-HFP)-based nanocomposite suspensions.

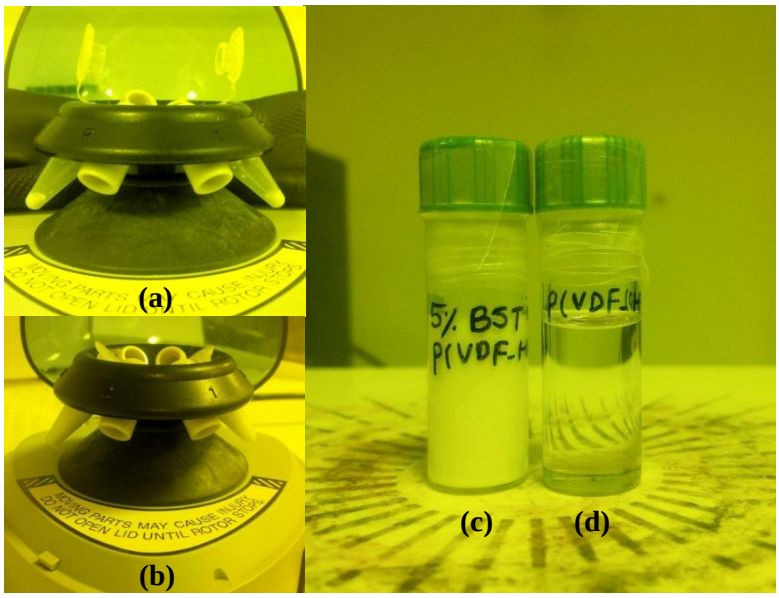


Fig. 3.11: Illustration of centrifuged suspension of 5 wt % BST in (a) PVP where clear precipitation can be observed and (b) in P(VDF-HFP) in which no precipitation is visible. Ready to use (c) 5 wt % BST in P(VDF-HFP) suspension and (d) P(VDF-HFP) solution.

As shown in Fig. 3.11 (a) and (b), centrifuging 5 wt % non-modified BST in PVP for 2 minutes resulted in a considerable amount of precipitant, while on the other hand, no noticeable precipitation was observed following centrifugation of an equivalent loading of BST in P(VDF-HFP). The final solution of P(VDF-HFP) and its corresponding nanocomposite suspension using 5 wt % BST nanoparticles are shown in Fig.3.11 (c). As in the case of PVP-based nanocomposites, short-run stirring or ultrasonication is suggested, unless a freshly made suspension is used, to induce homogenous dispersion and uniform deposition of the associated thin film. The process of thin film deposition is described in the following section.

3-1-5-Nanocomposite Thin-film Deposition

Once the nanocomposite is formulated, thin-film dielectrics can be deposited. The main advantage of using such polymer-based nanocomposites is their inexpensive, easy solution-processability. Various solution processing techniques can be adopted; herein we used a simple spin-coating approach.

Using a Laurell spin-coater, thin films were formed by spin-coating a few drops of pristine polymer or nanocomposite suspension. Thickness of thin films could be monitored by adjusting the spin speed, so-called revolutions per minute (rpm). In this project, both pristine PVP and P(VDF-HFP) and their corresponding high-*k* nanocomposites, when serving as the main dielectric layer, were spin-coated at 3000 rpm for 2 min to form the dielectric thin films. This particular spin speed was chosen following numerous experiments carried out to identify the most suitable dielectric thickness to yield a low leakage current and enable low-voltage device operation.

Polymer matrix	**Annealing temperature (°C)**	**Annealing duration (min)**
10 wt % PVP with added PMF	100	1
	200	60
5 wt % P(VDF-HFP)	135	90

Table 3.5: Annealing time and duration for different polymer matrix

Following spin-coating, thin films are annealed under N_2 to remove remaining solvent and solidifying the dielectric layer. As aforesaid, the annealing temperature varies with the type of polymer matrix; pristine or a nanocomposite. Taking into account transition temperatures and melting points of the polymers, annealing temperatures and durations in Table 3.5 were applied. Regarding PVP, a two-stage annealing was adopted to initially remove PGMEA solvent and thereafter promote cross-linking.

In contrast to pristine polymer thin films, the surface of the nanocomposite layers suffered from a considerable degree of roughness (as confirmed by surface analysis) which scaled up as the nanoparticle loading increased. Although higher concentrations of nanoparticles contribute towards increased dielectric constant (*k*) of the overall thin film, increased roughness gives rise to film thickness which on the contrary reduces capacitance. Therefore, one had to find a balance between amount of nanoparticles incorporated into the nanocomposite and overall thin-film thickness in order to obtain a high capacitance dielectric. Nonetheless, topographic features in a rough surface serve as a single point of contact and hence contribute to high capacitance per unit area. Moreover, as already mentioned in section 2, added roughness enhances surface properties such as surface energy and wettability. In the following section, the need for surface modification of high-*k* nanocomposites, in particular those with fluorinated polymer matrix, is described.

3-1-6-Surface Modification of High-*k* Nanocomposite Thin Films

As previously referred to in section 2-2-3, a high-capacitance nanocomposite dielectric was envisaged by incorporation of high-*k* nanoparticles into a low- or high-*k* polymer matrix. The nanocomposite dielectrics exhibited an increase in *k* and capacitance, relatively higher than that of the pristine polymer, as the nanoparticle loading increased. However, higher nanoparticle concentration led to increased surface roughness and degraded device performance consequently. This effect was more prominent when low-*k* polymer matrix (e.g. PVP) was used, since considerably higher concentrations of high-*k* nanoparticles were required to obtain a high-capacitance dielectric. As will be presented in chapter 4, despite achieving relatively high-capacitance dielectrics using a low-*k* based nanocomposite dielectric, the corresponding OTFTs could only operate at higher voltages ($\geq$ 20 V). Moreover, it had been found that the field-effect mobility of OTFTs was adversely affected by roughness of the gate dielectric layer [74].

One primary approach to resolve the surface roughness of nanocomposite thin films is to replace low-*k* polymer matrix with a high-*k* one. As a result, an equivalent high-*k* nanocomposite dielectric layer can be achieved with lower nanoparticle filler fraction. However, surface roughness would still be present to an extent noticeably larger than that of pristine high-*k* polymer. As depicted in Fig. 3.12 (a), the topographic 'hills' and 'valleys' comprising a rough nanocomposite surface act as charge trapping sites. The higher the root mean square (RMS) roughness is, the harder it becomes for a charge trapped in a valley to come out to the surface of the dielectric. RMS roughness is given by

$$RMS = \sqrt{\sum_{n=1}^{N} \frac{R_{h(n)}^2 + R_{v(n)}^2}{2N}}, \qquad \text{(Eq. 3.1)}$$

where R_h and R_v are the height of a hill and depth of a valley relative to the mean value respectively.

It is known that various surface properties intrinsic to high-*k* fluorinated polymers (e.g. P(VDF-HFP)), in particular low surface tension and low wettability, are magnified as surface roughness increases [194]. This makes subsequent deposition and adhesion of semiconductor layers atop such nanocomposite dielectrics troublesome, in some cases impracticable. Moreover, it has been reported that surface polarity and polar functional groups present in fluorinated polymer matrices lead to a smaller semiconducting grain size, a larger number of localised trap states and thus lower mobility and more negative threshold voltage in OTFTs [65].

The problem of the high surface roughness of the nanocomposite layer can be resolved by inserting an ultrathin planarising layer of a low-*k* polymer between the dielectric and the semiconductor layer [136]. This combination of high-*k* nanocomposite layer and thin polymeric capping layer is simply referred to as a bilayer gate dielectric. Nonetheless, the high-*k* nanocomposite layer still serves as the main gate dielectric layer. Implementation of such bilayer dielectrics plays a crucial role in fabrication and performance of OTFTs by modifying underlying nanocomposite surface properties (e.g. roughness, surface polarity, surface energy, and wettability) and improving the dielectric-semiconductor interface.

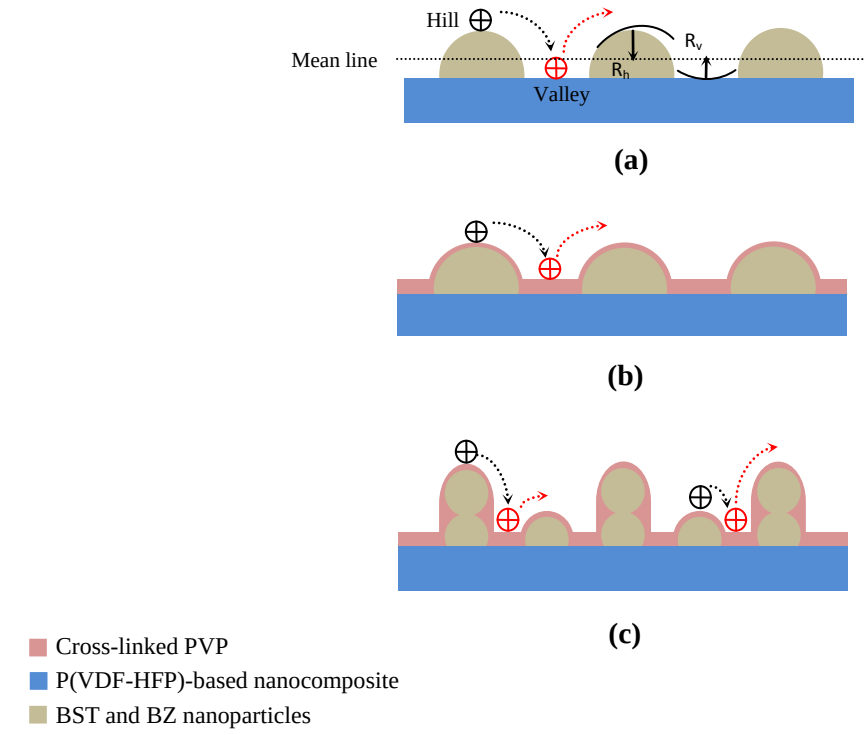


Fig. 3.12: Simplified schematics of (a) uncapped BST-P(VDF-HFP), (b) PVP-capped BST-P(VDF-HFP) and (c) PVP-capped BZ-P(VDF-HFP).

Despite an inevitable reduction in overall capacitance of the bilayer dielectric due to the presence of two layers in series, various compensating approaches can be implemented to preserve device performance at a reasonably high level. The main strategies for maintaining a high-capacitance bilayer dielectric are as follows:

(i) Increasing filler volume fraction,

(ii) Using a polymer host with a high enough *k*,

(iii) Choosing a low enough *k* capping polymer,

(iv) Monitoring thickness of the capping layer so that it does not counteract the effect of the main nanocomposite dielectric layer.

Cross-linked PVP is considered as an effective material to cap high-*k* nanocomposite dielectric layers, since it is already proven as a reliable gate dielectric layer with relatively low *k* and smooth interface. The thickness however of the PVP layer is critical; it has to only partially cover the nanocomposite's extremely rough features to reduce pinholes and provide a comparatively smooth and less hydrophobic interface.

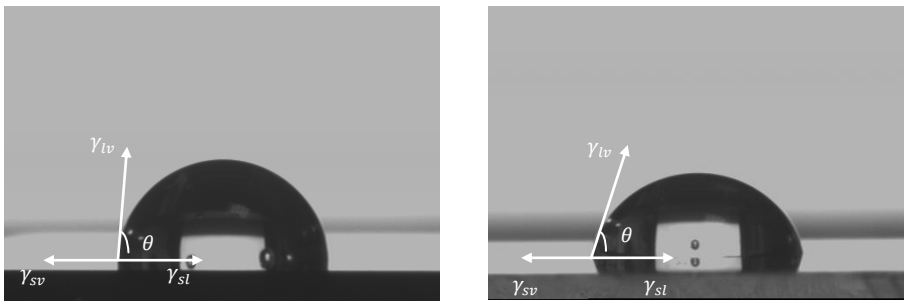
As will be presented in chapter 4, partial capping of a high-*k* nanocomposite dielectric with an ultrathin PVP layer allows advantageous use of surface roughness to obtain a high-capacitance dielectric while improving the dielectric-semiconductor interface to give an exceptionally low operating voltage OTFT with reasonably high carrier mobility.

Simplified schematics of BST-P(VDF-HFP) and BZ-P(VDF-HFP) nanocomposites capped with an ultrathin PVP layer are shown in Fig.3.12 (b) and (c) respectively. As depicted, ideally the PVP layer does not fully cover the rough topographic features on the nanocomposite surface, but only fills in the majority of the valleys where P(VDF-HFP) and a few smaller nanoparticles are present, while forming an ultrathin layer (so-called skin) over the rougher features. Hence, delicate tailoring of the PVP concentration and thickness was essential in this project to achieve such selective coverage. Results on how full and partial coverage of PVP affected device performance are included in chapter 4.

Furthermore, depending on size of nanoparticles, different scenarios were expected to take place. As pictured in Figs. 3.12 (b) and (c), it was envisaged that unlike BST-P(VDF-HFP) nanocomposites, using BZ nanoparticles (~50 nm) in place of BST would result in possible stacking of nanoparticles and hence a thicker film and rougher surface. Hence, capping would not be as effective as in the case of the BST nanocomposite film, but roughness would be reasonably reduced compared to that of uncapped BZ-P(VDF-HFP) layer.

To comply with the required thickness of the capping layer, a 2 wt % PVP in PGMEA with 1 wt % added PMF was prepared based on the procedure mentioned in section 3-1-4-1. It was then spin-coated atop a P(VDF-HFP) nanocomposite layer at 5000 rpm for 2 min, followed by annealing under N_2 at 130 °C for 90 min. Unlike the case where PVP was used as the main dielectric layer, this thin capping layer of PVP could not be annealed at 200 °C, since the underlying nanocomposite layer should not be strictly heated above the melting temperature (135-140 °C) of P(VDF-HFP). Nevertheless, further investigation manifested cross-linking of PVP taking place at this lower temperature. The thickness of the PVP layer was determined at ~ 30 nm using atomic force microscopy (AFM) and confirmed by transmission electron microscopy (TEM). Additionally, the presence of PVP was probed by measuring the contact angle of water on both uncapped and capped nanocomposite dielectric layers.

As shown in the Fig. 3.13, a 14 % reduction in contact angle was measured on the PVP-capped nanocomposite surface compared to the un-capped surface. In other words, the PVP-capped nanocomposite dielectric had become less hydrophobic than the uncapped one which provided a desirable base for deposition of semiconductor and a promising interface for charge transport.



(a) **(b)**

Fig. 3.13: Contact angle of a water drop on (a) an uncapped: 89° ± 0.7° and (b) PVP-capped: 77° ± 0.5°, BST-P(VDF-HFP) nanocomposite; γ_{lv} , γ_{sv}, and γ_{sl} represent the liquid-vapour, solid-vapour, and solid-liquid interfacial tensions, respectively. θ is the contact angle.

It is worth emphasising that although the concept of the capping layer can also be applied to PVP-based nanocomposites, it would only contribute towards a trivial reduction of the surface roughness of such layers and not improve the surface properties (including surface energy and adhesion) any further. Substantial surface roughness of PVP-based nanocomposites requires a much thicker capping layer which would result in unnecessary increased thickness of the overall (bilayer) dielectric. A more detailed study of physical and electrical characteristics of different P(VDF-HFP)-based nanocomposites capped with cross-linked PVP supporting the aforementioned speculation is presented in chapter 4.

3-2- Device Structure and Fabrication

Following the overview on formulation of various nanocomposite suspensions, and consideration given to the many issues concerning deposition of nanocomposite dielectric layers (and bilayers), the procedures for device fabrication and characterisation can now be described in this section. In order to allow consistent characterisation, every time an OTFT was fabricated (using various combinations of dielectric and semiconductor layers), a capacitor using the same (pristine/nanocomposite) dielectric layer was simultaneously made. This ensured precise monitoring of thickness and surface roughness of the gate

dielectric film, as well as giving capacitance and the corresponding dielectric constants of the pristine polymer or the nanocomposite. Finally, information on mobility and other characteristics of OTFTs may be derived. Appendix B and C provide an overview of quantity and performance of devices fabricated in this project using PVP- and P(VDF-HFP)-based gate dielectrics respectively.

3-2-1-Parallel-plate Capacitors

In order to evaluate dielectric properties of our in-house formulated nanocomposites, parallel-plate capacitors (also called metal-insulator-metal (MIM) capacitors) were fabricated and characterised. Depending on whether nanocomposites with a low- or high-*k* polymer matrix were used, capacitors (and TFTs thereafter) with single or bilayer dielectric layers were fabricated.

The start-to-end process adopted and optimised in the work for fabricating capacitors is described as follows:

i. Pre-cut, square-shaped, corning glass samples (A = 1.2 cm^2), purchased from Apex Optical Services, were used as substrates.
ii. Samples were initially sonicated in a Decon 75 and water mixture (1:5 ratio), and cleaned thereafter in three subsequent 10-minute sonication stages using acetone, methanol and 2-Propanol (IPA).
iii. Samples were then dried at 60 °C for 20 minutes to remove excess solvent and ensure bubble-free surface and allowed to cool down before placing them inside evaporation chamber ready for deposition of aluminium (Al) bottom plate (electrode).
iv. A thick layer of Al (~ 1 μm) was evaporated onto glass substrates to serve as the bottom electrode. In order to obtain consistent Al film thickness, evaporation was steadily carried out in a turbo pumped evaporator. The settings could vary within an acceptable range 50-60 W for 2-3 minutes. Once evaporation is completed, it was important to allow samples to cool down for 15-20 minutes, while inside the chamber and under vacuum, before bringing the evaporator to atmosphere to unload samples. This minimised any potential contamination.

v. For further cleanliness, samples were briefly treated by UV ozone before spin-coating the gate dielectric layer.

vi. Single or bilayer dielectric layer was deposited atop bottom Al electrode by adhering to the procedures outlined in 3-1-5 and 3-1-6. If the nanocomposite suspension was not prepared on the same day as the device fabrication, it had to be sonicated for at least 30 minutes prior to spin-coating to induce homogenous dispersion of nanoparticles and avoid any possible precipitation of nanoparticles in the polymeric matrix.

vii. Samples were then allowed to cool down to room temperature before depositing the top electrode. As the final stage, a 50 nm layer of Al was evaporated at 50 W for ~ 1 min through a shadow mask with 1.2 mm^2 rectangular patterns (Fig. 3.14 (a)) to form the top electrode.

Schematic of a parallel-plate capacitor fabricated with a bilayer gate dielectric is illustrated in the following Fig. 3.14 (b). Parallel-plate capacitors were fabricated to determine properties of the nanocomposite dielectric layer.

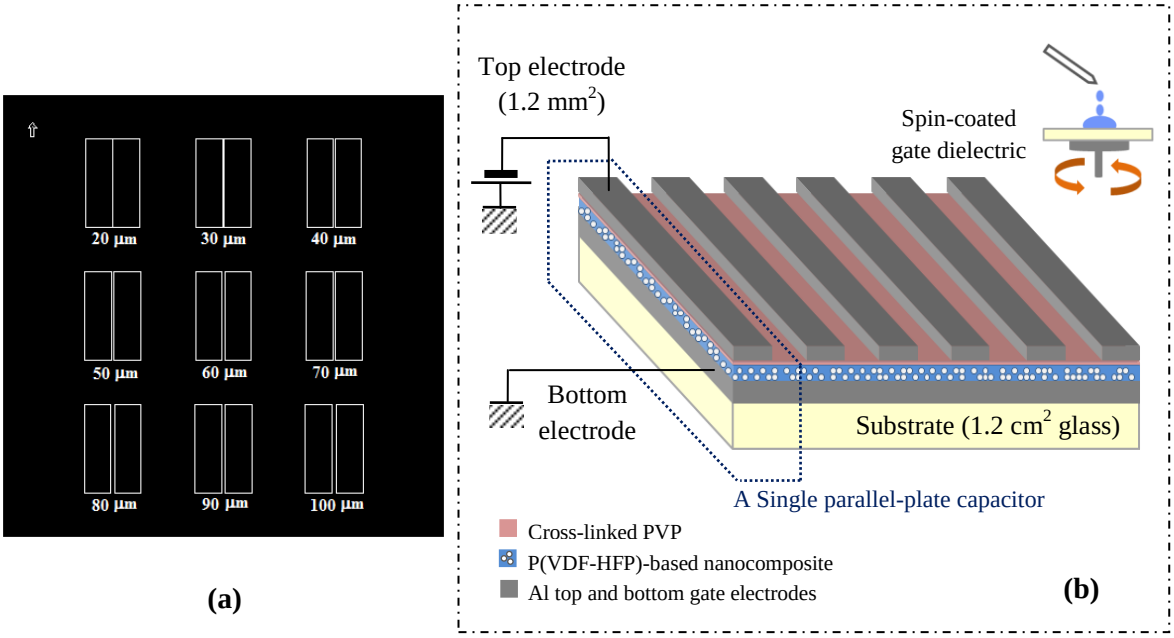
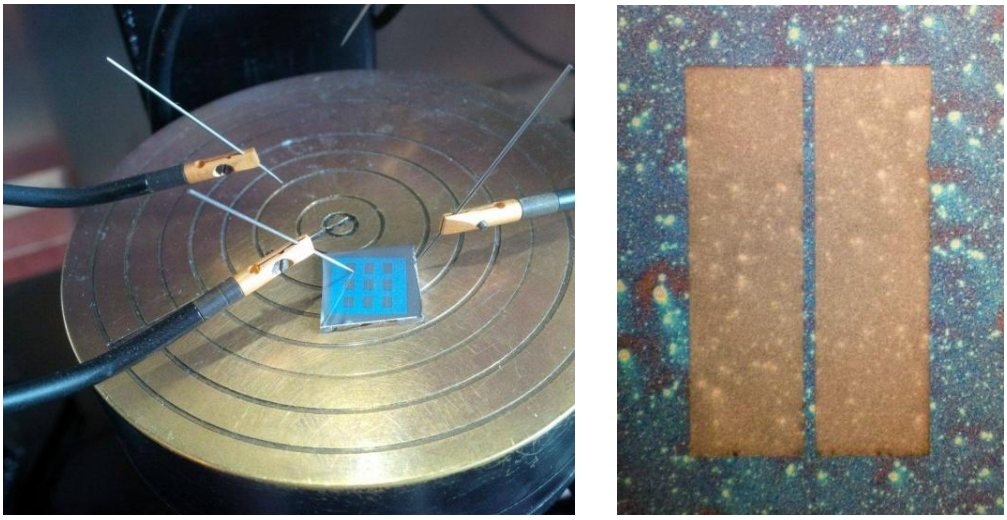


Fig. 3.14: (a) Shadow mask pattern consisting of nine TFTs. Numbers indicate channel length for each device (paired rectangles) and (b) Schematic of parallel-plate capacitors.

Leakage current density as a function of applied voltage and capacitance (at various frequencies) were measured on each capacitor via a two-probe method as shown in Fig. 3.15 (a).

Subsequently, applying the equation (2.12), the dielectric constant of each type of nanocomposite dielectric was calculated using the average value of dielectric thickness and compared on the basis of nanoparticle type and loading as well as choice of polymer matrix. In-depth discussions on capacitor results are provided in section 4-1-2.



(a) **(b)**

Fig. 3.15: Illustration of (a) measurement set-up on a typical sample with 18 capacitors and (b) two parallel-plate capacitors, also serving as a single TFT with addition of a semiconductor atop, with 11 wt % BST-P(VDF-HFP) nanocomposite dielectric (blue colour).

An example of two parallel-plate capacitors made with a gate dielectric of 11 wt % BST nanocomposite in P(VDF-HFP) is illustrated in Fig.3.15 (b). Extreme rough surface of the dielectric layer is evident even at areas underneath the electrodes. Such topographic features not only affect formation of the top electrode, but also lead to high leakage current and possibility of short-circuit.

3-2-2-Thin-film Transistors

For the purpose of this project, mainly OTFTs with bottom-gate, top- and bottom-contact (BGTC and BGBC) configuration were fabricated. Since BGBC TFTs can be visualised as a metal-insulator-metal-semiconductor (MIMS) structure, a simplified process of fabricating (BGBC) TFTs involves fabrication of parallel-plate capacitors followed by deposition of the active layer on the top electrodes (contacts) as the final layer.

The procedure of OTFT fabrication executed in this project is summarised below:

(i) Follow steps (i) to (vi) previously described in section 3-2-1.

(ii) A 50 nm layer of gold (Au) was evaporated atop single/bilayer gate dielectric through a shadow mask which resulted in nine variable-channel TFTs with 1.2 mm^2 source and drain electrodes (Fig. 3.14 (a)).

(iii) To modify source and drain contacts, samples were immersed in 80 µl of pentafluorobenzenethiol (PFBT) SAM in 40 ml IPA and soaked for 2 hours. As reported by Conrad *et al.* [195], the work function (Φ) of untreated (bare) gold (5.1 eV) reduces when modified with PFBT (4.77 eV). Moreover, cross-linked PVP is chemically stable against IPA and no delamination of Au source/drain electrodes was observed during immersion. Samples were then thoroughly washed with IPA to remove excess, unreacted PFBT and fully dried.

(iv) As the final stage of TFT fabrication, the semiconductor layer was deposited from solution at variable rpm and subsequently annealed to remove excess solvent. A more specific deposition process for each semiconductor type is given in Table 3.6.

(v) Prior to characterisation, to further reduce leakage current, the semiconductor layer was patterned by scratching the film using a wooden toothpick to segregate adjacent transistors (dotted lines in Fig. 3.16 represent a single TFT). To minimise the parasitic effect outside the S/D electrodes, for each TFT, the semiconductor was additionally patterned as close to the electrodes as possible. Nonetheless, no evident difference was observed in transfer and output characteristics of TFTs with and without the latter patterning step.

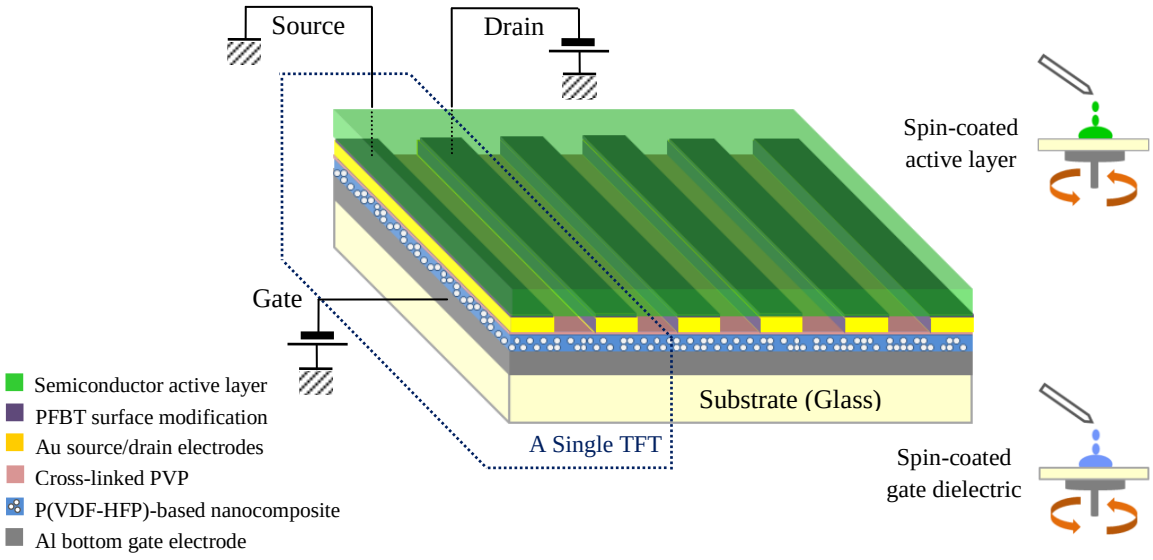


Fig. 3.16: Schematic of a bottom-gate, bottom-contact thin-film transistor.

Solution deposition of semiconducting materials atop a solution-processed dielectric layer can lead to interfacial mixing, increased interface roughness and charge trapping due to possible dissolution or swelling effects [83]. By choosing compatible materials, using orthogonal solvents for deposition of the multilayer structure and cross-linking the capping layer, any device structure can be realised with no interfacial mixing observed. Defined, trap-free interfaces are obtained and desired phase separation is promoted [93, 122]. Different classes of semiconductors, e.g. small molecules, amorphous and polycrystalline polymers and small-molecule/polymer blends were attempted in this work (Fig. 3.17) to ascertain compatibility of the developed nanocomposite dielectric when integrated in OTFTs.

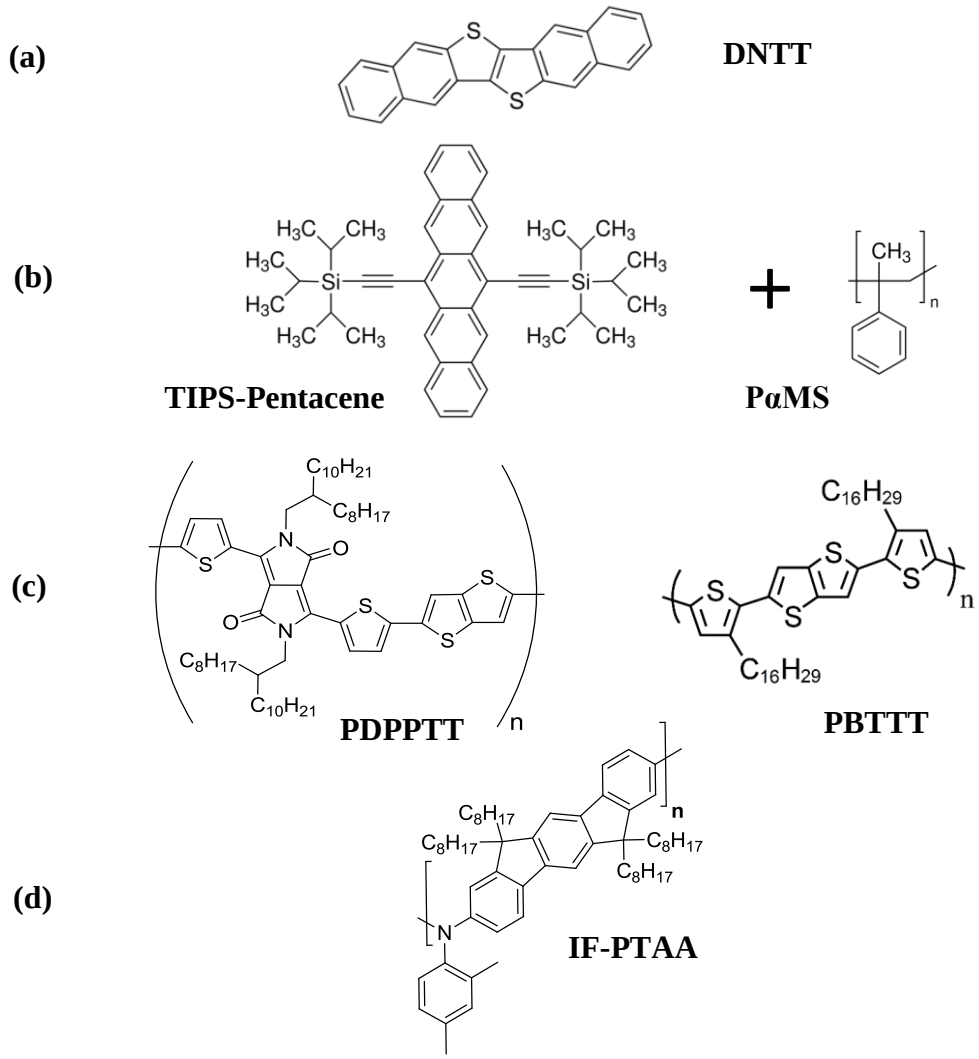


Fig. 3.17: Chemical structure of (a) small molecule/polymer blend (TIPS-Pentacene/PαMS), (b) small molecule dinaphtho-thieno-thiophene (DNTT), (c) polycrystalline (poly(3,6-di(2-thien-5-yl)-2,5-di(2-octyldodecyl)-pyrrolo[3,4-c]pyrrole-1,4-dione)thieno[3,2-b]thiophene) (PDPPTT) and poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTTT) and amorphous polymer (indium fluoride-poly(triarylamine) (IF-PTAA)) semiconductors.

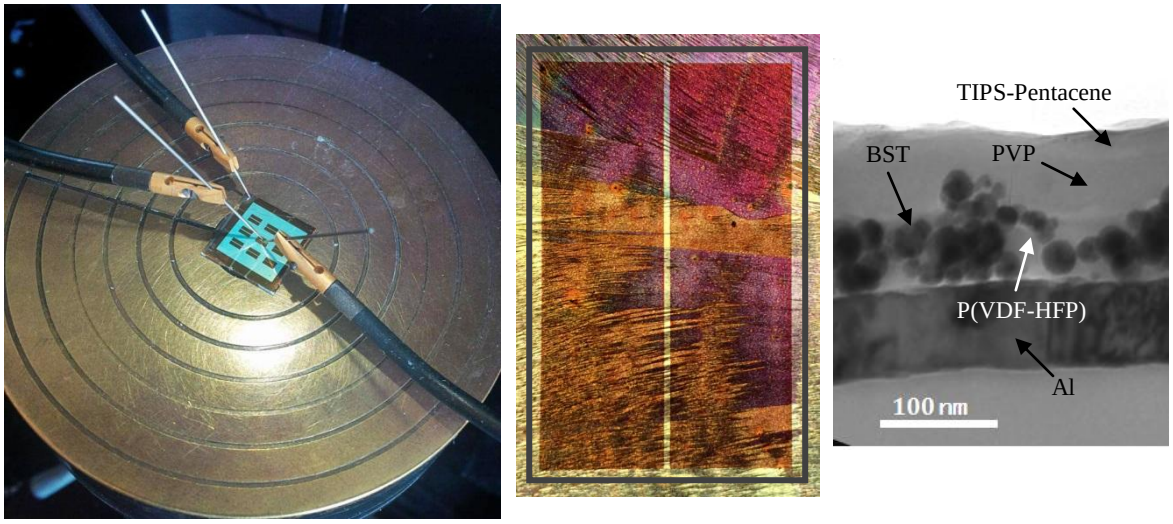
Fig. 3.17 illustrates chemical structure of specific examples from each class of semiconductors which were successfully utilised to fabricate vacuum-deposited and solution-processed devices. To encompass major methods of semiconductor deposition, solution-processing and vacuum-deposition have been both tried. Nonetheless, solution-based deposition is the most appealing technique with the move towards cheap, large-area and flexible electronics.

It should be noted that due to time constraints and growing interest in low-voltage operation, a full set of semiconducting materials has only been attempted on OTFTs using P(VDF-HFP)-based bilayer nanocomposites (see Appendix C). Following deposition and modification of Au source/drain contacts (recalling aforementioned step (iii)), individually optimised steps, as summarised in Table 3.6 below, were subsequently taken for each specific type of semiconducting material:

Semiconductor	**Type**	**Deposition process**
DNTT	Small molecule	10 mg of DNTT crystals were evaporated under high vacuum at rate of 1 nm/min. DNTT crystals are very fragile, hence extra care had to be taken during sublimation in vacuum evaporator.
TIPS-Pentacene/ PαMS	Blend	A 7:3 by weight (10 mg ml^{-1}) of TIPS-pentacene: PαMS solution (in various solvents; See Appendix D) was spin-coated at 500 rpm for 2 min, followed by heating the sample at 60 °C for 20 min under N_2 to remove solvent.
PDPPTT	Polycrystalline	A 5 mg ml^{-1} solution in 1, 2-dicholorobenzene was spin-coated at 1000 rpm for 2 min and then annealed at 110°C for 40 min under N_2.
PBTTT, PBTTT/PαMS	Polycrystalline Blend (7:3)	A hot solution (105°C) of 7 mg ml^{-1} PBTTT in 1,2-dicholorobenzene was spin-coated onto a pre-heated sample (105°C). Sample was subsequently annealed at 110°C for 40 min under N_2.
IF-PTAA	Amorphous	IF-PTAA: A 10 mg ml^{-1} solution in toluene was spin-coated at 3000 rpm for 1 min followed by annealing at 85°C for 2 hours.

Table 3.6: Semiconductor layer deposition procedure for each type of material.

Once the devices were fabricated, characterisation was performed using an Agilent Technologies' E5270B measurement mainframe fitted with four E5287A source measure units. Each source measure unit was connected with a Karl Suss PH100 micromanipulator probe. Each sample consisting of nine TFTs with variable channel lengths (20 - 100 μm) was placed on the probe station's sample holder and electrical contacts were made between the probes and device electrodes. As shown in Fig. 3.18 (a), for TFTs, three electrical contacts were made, i.e. gate, source and drain, while for capacitors, only two connections were made, i.e. top and bottom electrodes (bottom electrode is usually grounded).



(a) **(b)** **(c)**

Fig. 3.18: (a) A patterned sample comprising nine OTFTs with BST-P(VDF-HFP) nanocomposite dielectric and PDPPTT active layer, (b) optical microscopic image of a single (patterned) OTFT manifesting crystal formation of TIPS-Pentacene/PαMS; channel length of 20 μm; crystals have an average size of 1 μm and (c) TEM image of a stacked structure of PVP-capped BST-P(VDF-HFP) nanocomposite layer spin-coated on an Al-coated substrate.

Prior to commencing device characterisation, the semiconductor layer was patterned by segregating the devices from one another using a wooden toothpick (Fig. 3.18). This was to reduce gate leakage current down to an acceptable level, not to compensate device performance. An example of a finalised OTFT ready for characterisation is shown in Fig. 3.18 (a). An example of enlarged single OTFTs exhibiting crystal formation of TIPS-Pentacene/PαMS perpendicular to the corresponding channel of 20 μm is demonstrated in Fig. 3.18 (b). A TEM image of PVP-capped BST-P(VDF-HFP) nanocomposite presented in Fig. 3.18 (c) confirms the presence of the nanocomposite, PVP (partial) coverage and TIPS-Pentacene/PαMS semiconductor layer.

Chapter 4

Results and Discussions

In this chapter, properties of various nanocomposite dielectric layers using various combinations of polymer matrix and nanoparticle filler are initially studied from physical and electrical by means of AFM analysis and capacitance characterisation. Thereafter, characteristics of the corresponding OTFTs are presented and extensive analysis is carried out accordingly. Finally results on low-voltage TFTs are presented and in-depth study is provided. Comparative analyses are consistently performed throughout this chapter to determine individual and collective effects of various key elements in nanocomposite formulation, including type of polymer matrix and type, size and surface modification of nanoparticles, on device characteristics and performance. It is worth mentioning that the best results obtained after implementing numerous device optimisations are presented here.

4-1- Characterisation of Nanocomposite Gate Dielectrics

Dielectric layer plays a critical role in device overall performance and hence detailed study of its surface properties, thickness, capacitance and leakage current provides a clear indication of its suitability when implemented as part of the device structure. In this section, characteristics of nanocomposite dielectric layers formulated using different combinations of polymer matrix and nanoparticle filler is studied. Furthermore, the crucial role of an ultrathin PVP capping layer introduced atop P(VDF-HFP)-based nanocomposite layer is comprehensively explored using AFM analysis and capacitor characterisation.

Classifying nanocomposite dielectrics based on their polymer matrix, i.e. low- and high-*k*, properties of each category is systematically studied. Once nanocomposite surface analysis (and thickness measurement) had been carried out, parallel-plate capacitors were fabricated (see section 3-2-1) and relevant characteristics, including capacitance and dielectric constant, were determined. Results presentation in each subsection is followed by comparative studies on how dielectric properties of nanocomposites surpassed those of pristine polymer, in addition to the impact of incorporation of different nanoparticles and inclusion of nanoparticle's surface modification (when low-*k* polymer is used).

4-1-1-PVP-based Nanocomposite Dielectric Layers

In this work, as outlined in section 3-1-4-1, six different types of PVP-based nanocomposites comprising surface-modified, perovskite nanoparticles, namely OPA-BZ, OPA-CZ, ODPA-CZ, HMDS-BST, OPA-BST and OPA-CT, were formulated to serve as gate dielectric layers in capacitors and TFTs. As previously mentioned, using low-*k* polymer matrix necessitates surface modification of nanoparticle fillers prior to incorporation and formulation of the nanocomposites. Therefore, major portion of results included here are on PVP-based nanocomposites with surface-modified nanoparticles. To enable broad comparison, four different concentrations (2, 5, 8 and 11 wt %) of each nanocomposite suspension were prepared and utilised.

According to equation (2.12), capacitance is directly proportional to the area of the capacitor's plates and inversely proportional to the distance between them (i.e. thickness of the dielectric layer). On the other hand, the thickness of thin films deposited by spin-coating from solution is inversely proportional to the speed at which the film is spun and directly proportional to the viscosity of the nanocomposite suspension. In other words, the higher the spin-coating speed is the thinner the deposited film becomes. In addition, it is expected that, keeping the spin speed constant, thicker and rougher dielectric films are resulted as the NP loading % in the nanocomposite suspension increases. Thus, it is crucial to find an effective trade-off between the film thickness and roughness. One might easily misjudge by increasing the spin speed to obtain a thinner film (to supposedly get higher capacitance), but at the same time lose most of the nanoparticle fillers or end up with a film of immensely rough surface, which adversely affects device characteristics. Numerous trial experiments were carried out to identify the most effective speed (i.e. 3000 rpm) at which a decent, uniform film of nanocomposite dielectric is formed.

In order to characterise nanocomposite gate dielectrics, the dielectric film thickness, as a determinant factor, has to be measured. As a result, along with every paired capacitor and TFT fabricated using a specific type of nanocomposite (single or bilayer) dielectric, a clean glass substrate (from the same batch) was spared on which the same nanocomposite (or pristine polymer) layer was formed to subsequently undergo thickness measurement. This ensured that characteristics of each device using particular nanocomposite dielectric layer were determined by taking into account their exact, matching dielectric properties.

Thickness measurement is carried out by measuring the height of a step/trench created into the dielectric layer; the distance between the glass surface at the bottom and surface of the dielectric film on the top, as illustrated in Fig. 4.1.

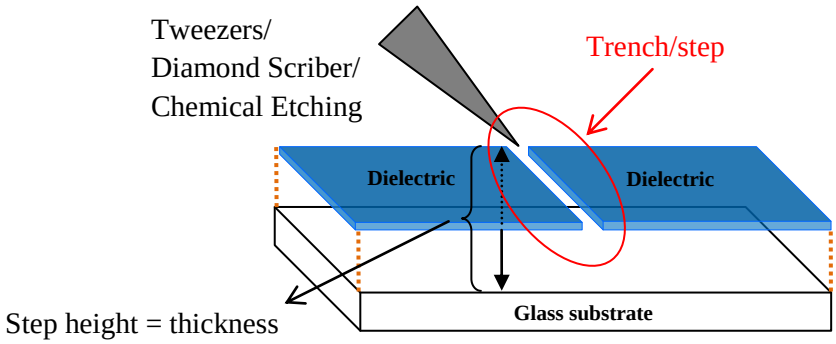
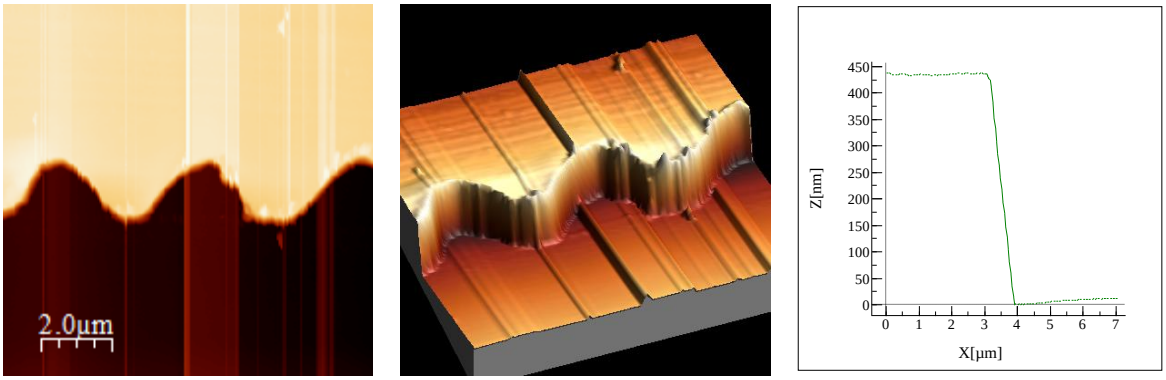


Fig. 4.1: Demonstration of creating a trench/scribe line for thickness measurement.

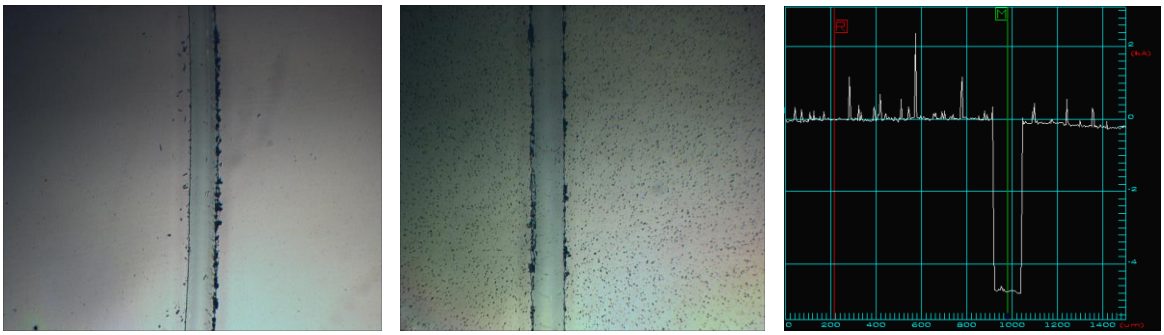
Different methods were applied to create the trench, such as manually creating a scribe line by using a diamond scriber (or tip of a pair of tweezers) or by chemical etching. Extra care was taken during applying the former method to avoid scoring the glass slide underneath. It has been previously reported that once the PVP polymer matrix is cross-linked it cannot be etched. However, adopting a particular bilayer lift-off process using two resists, LOR-3A (PMGI) and S1805, developed by Microchem, PVP-based nanocomposite layer was successfully etched and thickness measurement pursued. Nonetheless, since outcome of this technique was almost comparable to that of simply scratching the film manually, the lift-off process was dropped out due to its complexity and time consumption.



(a) **(b)** **(c)**

Fig. 4.2: (a) AFM Top view and (b) 3D image of a trench made in pristine PVP film and (c) step profile representing height of the trench as a measure of PVP film thickness.

Once the trench is created, AFM or 3ST Profilometer can be employed to determine the thickness of the dielectric film. Both techniques have been attempted and examples of each are demonstrated in Fig. 4.2 and 4.3 respectively. Nevertheless, AFM was the mainly used technique, since it reveals more information on dielectric layer properties such as roughness, adhesion, phase, and also thickness.



(a) **(b)** **(c)**

Fig. 4.3: Scribe line on (a) pristine PVP and (b) 5wt % BST-PVP nanocomposite and (c) screenshot of film thickness measured using DEKTAK 3ST.

The complete set of data, including average thickness, capacitance and dielectric constant, acquired on PVP-based nanocomposite dielectric layers using various surface-modified nanoparticle fillers are presented and comparatively studied in the subsequent section.

4-1-1-1 Results on Parallel-plate Capacitors

Following performing surface analysis and thickness measurement, capacitors with dielectric layers made from various concentrations (wt %) of the six different types of nanocomposites in PVP (as outlined in section 3-1-4-1) were fabricated. Capacitance per unit area (So-called capacitance density, *Ci*) of each capacitor was measured as a function of frequency using an Agilent LCR meter adopting a two-probe method (Fig. 3.15). The 500 Hz - 1 MHz frequency range was chosen to investigate variation of measured capacitance of the nanocomposites at different frequencies. Capacitance measurement at frequencies outside this range could not be carried out due to limitations of the available LCR meter. Once capacitance (or C_i) is measured, the value of dielectric constant (k) can be calculated.

According to equation (2.12), thickness of dielectric layer along with its capacitance is the necessary variable to determine *k*. Despite spin-coating pristine PVP and all different nanocomposites dielectric films at same speed rpm (3000 rpm for 2 min), different thicknesses – lowest value belongs to PVP layer - were measured using both AFM and DEKTAK profilometer. This can be attributed to nanocomposites different viscosities resulted from variable NP loading % and/or modification using SAMs of different chain length. Unfortunately, it was outside the span of this project to calibrate the spin-coater to identify exact speed (rpm) at which each type of nanocomposite suspensions had to be spun to obtain same film thickness across the whole set.

Thickness values of pristine PVP (0 wt %) and all six nanocomposite dielectric layers of various NP loading % measured with DEKTAK Profilometer are collected in Table 4.1. As expected, thicker dielectric films are formed as the NP loading % increases; the lowest and highest thicknesses belong to pristine PVP and nanocomposites with 11 wt % nanoparticles. Disregarding the thickness data for OPA-CT nanocomposites, the thickness vs. NP wt % relation is relevant regardless of the nanoparticles' and SAMs' type and size.

NP wt %	OPA-BZ	OPA-CZ	ODPA-CZ	HMDS-BST	OPA-BST	OPA-CT
0	484.0 ± 1.3	484.0 ± 1.3	484.0 ± 1.3	484.0 ± 1.3	484.0 ± 1.3	484.0 ± 1.3
2	491.0 ± 0.7	541.0 ± 1.2	514.0 ± 1.7	485.0 ± 0.9	459.0 ± 1	459.0 ± 1.4
5	525.0 ± 0.9	585.0 ± 1.6	564.0 ± 1.7	495.0 ± 0.8	470.0 ± 1.5	460.0 ± 1.8
8	557.0 ± 1.6	617.0 ± 1.9	614.0 ± 2.5	510.0 ± 1.2	478.0 ± 1.5	468.0 ± 2
11	585.0 ± 1.5	660.0 ± 2.1	675.0 ± 3.1	525.0 ± 1.2	489.0 ± 2.3	482.0 ± 2.7

Table 4.1: Thickness values (mean ± standard deviation) for nanocomposite dielectric films measured by DEKTAK. Values are in nm.

However, taking to the account the effect of nanoparticles and SAMs on dielectric thickness, ODPA-CZ and OPA-CZ nanocomposite dielectric films (with 11 wt % nanoparticle content) exhibited the highest values of thickness (675 nm and 660 nm respectively). The lowest thickness (482 nm; lower than that of the pristine PVP) was measured on OPA-CT films. This trend can be accredited to the possible correlation between type and chain length of SAM molecules and the chemical structure and size of nanoparticles and nanocomposite film thickness.

Following demonstrating the thickness data, the capacitance of the corresponding dielectric layers measured on parallel-plate capacitor is presented. As earlier pointed out, the capacitance (pF) is measured at a 500 Hz - 1 MHz frequency range. However, insignificant variations were observed in values of capacitance across the selected frequency range. To exemplify, values of capacitance per unit area (C_i, nF/cm^2) measured on nanocomposite dielectrics of various wt % of OPA-BZ are displayed as a function of frequency in Fig. 4.4. As clearly depicted, the highest values of C_i are measured for nanocomposites with 11 wt % OPA-BZ content. Otherwise, a consistent trend of capacitance invariance against frequency is apparent for all four NP wt % loading across the frequency range.

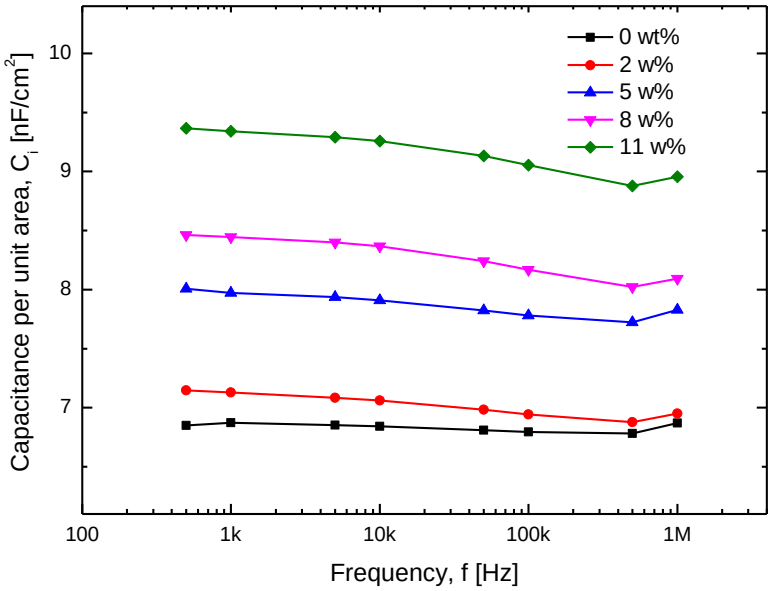


Fig. 4.4: Capacitance density vs. frequency measured on OPA-BZ nanocomposite dielectrics with variable NP loading. The 0 wt % refers to pristine PVP.

Full set of values of capacitance density (C_i) measured on capacitors with pristine PVP and the six types of PVP-based nanocomposite dielectric layers of different NP concentrations are recorded in Table 4.2. Although capacitance was measured at a frequency range, data presented in the Table 4.2 are C_i values measured at 1 kHz, at which the most stable, high capacitance was recorded. Comparing C_i data collected in Table 4.2, HMDS-BST and OPA-CT nanocomposite dielectric layers exhibit highest (10.2 nF/cm^2) and lowest (7.72 nF/cm^2) values of capacitance. Similar to the trend perceived in thickness data (Table 4.1), highest values of C_i are measured on PVP-based nanocomposites with 11 wt % nanoparticle content.

NP wt %	OPA BZ	OPA CZ	ODPA CZ	HMDS BST	OPA BST	OPA CT
0	6.87 ± 0.30	6.87 ± 0.30	6.87 ± 0.30	6.87 ± 0.30	6.87 ± 0.30	6.87 ± 0.30
2	7.13 ± 0.10	6.78 ± 0.30	7.04 ± 0.40	7.94 ± 0.20	7.93 ± 0.40	7.24 ± 0.30
5	7.97 ± 0.20	7.27 ± 0.20	7.28 ± 0.70	8.41 ± 0.30	8.16 ± 0.40	7.41 ± 0.60
8	8.44 ± 0.30	7.71 ± 0.30	7.64 ± 0.70	8.75 ± 0.20	8.53 ± 0.40	7.51 ± 0.60
11	9.34 ± 0.50	8.15 ± 0.50	7.99 ± 0.80	10.2 ± 0.50	9.15 ± 0.70	7.72 ± 0.40

Table 4.2: Values (mean ± standard deviation) of C_i (nF/cm^2) measured on different types of nanocomposite dielectrics.

Although capacitance is inversely proportional to dielectric layer thickness (Equation (2.12)), correlative rise in both thickness and capacitance of PVP-based nanocomposites is observed as NP concentration increases. This anomaly is simply attributed to the enhanced packing of high-*k* nanoparticles inside PVP matrix in nanocomposites with high nanoparticle concentration. Thus, not only thicker films are obtained, but also C_i increases due to a rise in number of dipoles aligned with applied electric field (a characteristic of high-*k* nanoparticle). In order to find a better indicator to evaluate effect of nanoparticles and SAMs on properties of the nanocomposite dielectric layer, dielectric constant (*k*) has to be calculated and evaluated.

Technically, as previously referred to in section 2-2-3, dielectric constant of a nanocomposite would be less than that of high-*k* constituent nanoparticles, since comparably lower *k* of the polymer host impedes *k* value of the nanoparticles and eventually that of the nanocomposite. Applying equation (2.12), values of dielectric constant are calculated using thickness and capacitance data collected in Table 4.1 and 4.2. The dielectric constant data for pristine PVP and all six choices of nanocomposite dielectric layers are recorded in the Table 4.3. According to these data, the value of *k* has improved from 3.76 for pristine PVP to ~ 6 for nanocomposites with 11 wt % NP content. The increasing trend in the of value of *k* is apparent for all six choices of nanocomposite dielectric layers as the nanoparticle content has increased from 0 wt % (pristine PVP) to 11 wt %. Regardless of the choice of nanocomposite, the highest dielectric constant is consistently obtained for nanocomposites with 11 wt % NP content.

With regards to the choice of nanoparticles and SAMs, nanocomposites consisting of OPA-BZ, ODPA- and OPA-CZ and HMDS-BST demonstrate the highest *k* at 11 wt % NP content with OPA-BZ strived to yield a slightly greater average value.

NP wt %	OPA-BZ	OPA-CZ	ODPA-CZ	HMDS-BST	OPA-BST	OPA-CT
0	3.76 ± 0.20	3.76 ± 0.20	3.76 ± 0.20	3.76 ± 0.20	3.76 ± 0.20	3.76 ± 0.20
2	3.95 ± 0.10	4.14 ± 0.30	4.09 ± 0.10	4.35 ± 0.20	4.11 ± 0.10	3.75 ± 0.30
5	4.73 ± 0.20	4.80 ± 0.30	4.64 ± 0.40	4.70 ± 0.20	4.33 ± 0.20	3.85 ± 0.30
8	5.31 ± 0.30	5.37 ± 0.20	5.30 ± 0.30	5.04 ± 0.30	4.61 ± 0.20	3.97 ± 0.20
11	6.17 ± 0.20	6.08 ± 0.20	6.09 ± 0.30	6.05 ± 0.20	5.05 ± 0.40	4.20 ± 0.30

Table 4.3: Values (mean ± standard deviation) of dielectric constant *k* for all six choices of PVP-based nanocomposite dielectrics.

The following conclusive remarks have been made with regards to the effect of various parameters, such as type, size and concentration of nanoparticles, the chain length of SAMs and compatibility between nanoparticles and SAMs, on dielectric properties of end PVP-based nanocomposites:

i. Modifying identical sets of nanoparticles with SAMs of same composition but different chain lengths may not impose a huge difference on properties of the dielectric layer, particularly when nanoparticles of small diameter (e.g. CZ) are used. However, it is speculated that as the NP content increases, those modified with SAMs of longer chain might result in slightly thicker film and higher dielectric constant.

ii. The effect of intrinsic properties of different nanoparticles when modified with the same SAM, as well as (chemical) compatibility between the two constituents has been identified. In addition, different nanoparticles of same diameter might have their surface properties affected differently with addition of same SAM. For example, nanocomposites using OPA-BST nanoparticles exhibit better dielectric properties than those with OPA-CT nanoparticles.

iii. The size of nanoparticles modified with the same SAM molecule exhibited significant impact on dielectric properties of the nanocomposites. OPA-BZ (and OPA-CZ) nanocomposites demonstrated superior dielectric properties, i.e. higher k (and C_i) than their OPA-CT (and OPA-BST) counterparts. Although BST has a greater intrinsic k value than BZ, modification of smaller nanoparticles with SAMs might result in more uniform, thicker layers with better dielectric properties.

iv. Finally, modifying same nanoparticles with SAMs of different composition and chain length results in nanocomposite dielectric layers with correspondingly different properties. For example, HMDS-BST nanocomposites yielded higher values of C_i and k compared to those with OPA-BST nanoparticles. This effect may be attributed to better surface adhesion and compatibility between BST and HMDS than OPA, resulting in higher quality nanocomposite dielectrics.

In conclusion, solid observations have been made on the impact of various parameters, namely nanoparticle size, type and compatibility with SAM molecules, on dielectric properties of PVP-based nanocomposite layers. Assuming a constant thickness, dielectric layers of nanocomposites with (11 wt %) BZ and CZ nanoparticles exhibited the largest values of C_i and k. Nonetheless, integration of such dielectric layers into OTFTs has yet to be examined to justify suitability of PVP-based nanocomposites for both supercapacitors and high performance electronic devices.

4-1-2-P(VDF-HFP)-based Nanocomposite Bilayer Dielectrics

As discussed in section 3-1-6, nanocomposite dielectric layers using high-k, P(VDF-HFP) polymer matrix have to be (partially) capped with an ultrathin planarising (PVP) layer to improve its surface properties and enable implementing it into TFTs. Although speculations have been made (Fig. 3.12) with regards to presence, extent and role of PVP coverage, it is crucial to demonstrate how effectively PVP capping layer has modified underlying nanocomposite and influenced properties of bilayer dielectric and overall device performance. It is worth mentioning that terms ‘coating’ and ‘capping’ have been interchangeably used throughout this document.

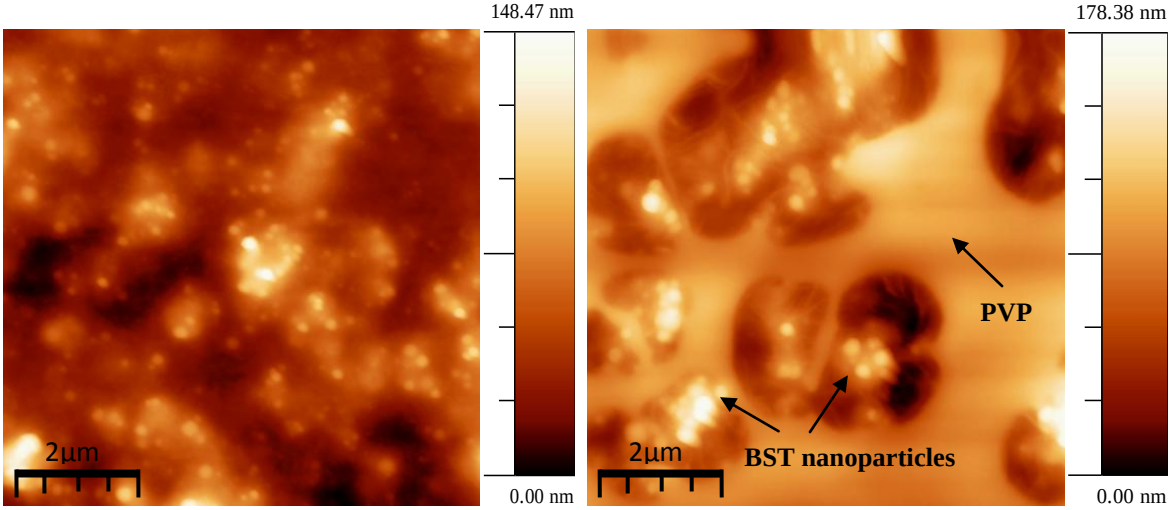
4-1-2-1- AFM Analysis

Although water contact angle measurements (Fig. 3.13) revealed a drop in θ and hydrophobicity following introducing cross-linked PVP capping layer, further verification was necessary to understand how PVP has modified the surface of P(VDF-HFP) nanocomposites and contributed to improved device characteristics. In this section, a series of AFM images of P(VDF-HFP)-based nanocomposites using non-modified BST and BZ nanoparticles are presented. With the aid of these pictorial representations, numerical derivations and follow-up discussions, the impact of nanoparticle type and size on the formation of PVP capping layer and overall properties of their corresponding bilayer nanocomposite dielectrics is systematically pinpointed.

Here, comparative analysis is planned out in such a way to probe the role of the planarising PVP layer on one hand and that of the incorporated nanoparticle filler on the other hand. To avoid convolution and keep analysis concise, only AFM profiles mapped on P(VDF-HFP)-based nanocomposites with 5 wt % nanoparticle loading is presented. Similarly, the best low-voltage operating devices have been reported using nanocomposite dielectrics of such filler concentration; characteristics of which can be found in section 4-2-3. Nonetheless, since relatively similar AFM images were obtained using other concentrations of nanoparticles, any conclusive remarks made here are inclusively applicable to their corresponding nanocomposite layers.

AFM images were recorded by Dr Ian Ingram - School of Chemistry, University of Manchester - on a Bruker Multimode 8 in Peak Force tapping mode at a resolution of 512 × 512 pixels. Cantilevers had a spring constant of approximately 0.350 Nm^{-1}, with a resonant frequency of approximately 50-80 kHz. A modulation frequency of 2 kHz was used. AFM has been adopted not only to determine thickness of uncoated and PVP-coated nanocomposite layer, but also to quantitatively ascertain surface properties, in particular roughness, adhesion and stiffness. On each sample, thickness and roughness are measured from AFM height profile, while adhesion and stiffness are determined using adhesion and Derjaguin-Muller-Toporov (DMT) modulus profiles respectively. In addition to quantitative data, each profile explicitly sheds light on effect of varying parameters, e.g. PVP capping layer and different nanoparticles, and enables comparative analysis accordingly.

Height profiles of uncapped and PVP-capped BST-P(VDF-HFP) nanocomposite films are shown in Fig. 4.5 (a) and (b) respectively. Points with the highest intensity relative to the entire image represent BST nanoparticles. Although technically the only difference between two samples is the presence of PVP layer in Fig. 4.5 (b), the two profiles are profoundly different from one another. While the profile in Fig. 4.5 (a) resembles a galaxy with BST nanoparticles acting as the stars, the profile in Fig. 4.5 (b) looks like an ocean, being PVP, with islands of various sizes and shapes scattered around.



(a) **(b)**

Fig. 4.5: Height profiles mapped by tapping mode AFM on surface of (a) uncapped and (b) PVP-capped BST-P(VDF-HFP) nanocomposite dielectric layer.

Fig. 4.5 (b) justifies the hypothesis made earlier on (Fig. 3.12) about partial coverage of nanocomposite using ultrathin PVP. As can be perceived by comparing Fig. 4.5 (a) and 4.5 (b), ultrathin PVP has covered almost half of nanocomposite topographies fully, while only formed skin on larger individual or collection of nanoparticles. The image contrast has reasonably reduced in Fig. 4.5 (b) which can be interpreted as a drop in surface roughness. Although ultrathin layer of cross-linked PVP has created areas of smooth, pinhole-free interface serving as suitable pathways for charge transport, rough areas of BST nanoparticles responsible for high capacitance are beneficially preserved. Therefore, development and implementation of such bilayers of nanocomposites (Fig. 4.5 (b)) into device structures not only lowers density of traps and improves dielectric-semiconductor interface, but also offers high-capacitance dielectric which collectively results in reduced operational voltage. Moreover, PVP coverage is believed to have somehow neutralised surface of the nanocomposite and enabled deposition of the semiconducting materials.

Although height profiles have demonstrated differences in surface morphology, thickness and roughness with and without PVP coating, additional surface parameters were mapped to conclusively validate the presence and impact of PVP capping layer onto surface of nanocomposites.

In Fig. 4.6 (a), (b) and Fig. 4.6 (c), (d), DMT modulus and adhesion profiles of uncapped and PVP-capped surface of BST-P(VDF-HFP) nanocomposites are respectively illustrated. DMT modulus is the Young's modulus (a measure of stiffness and rigidity) calculated by bringing into account van der Waals interaction between AFM tip and surface (outside the elastic contact regime) giving rise to the load force, and adhesion.

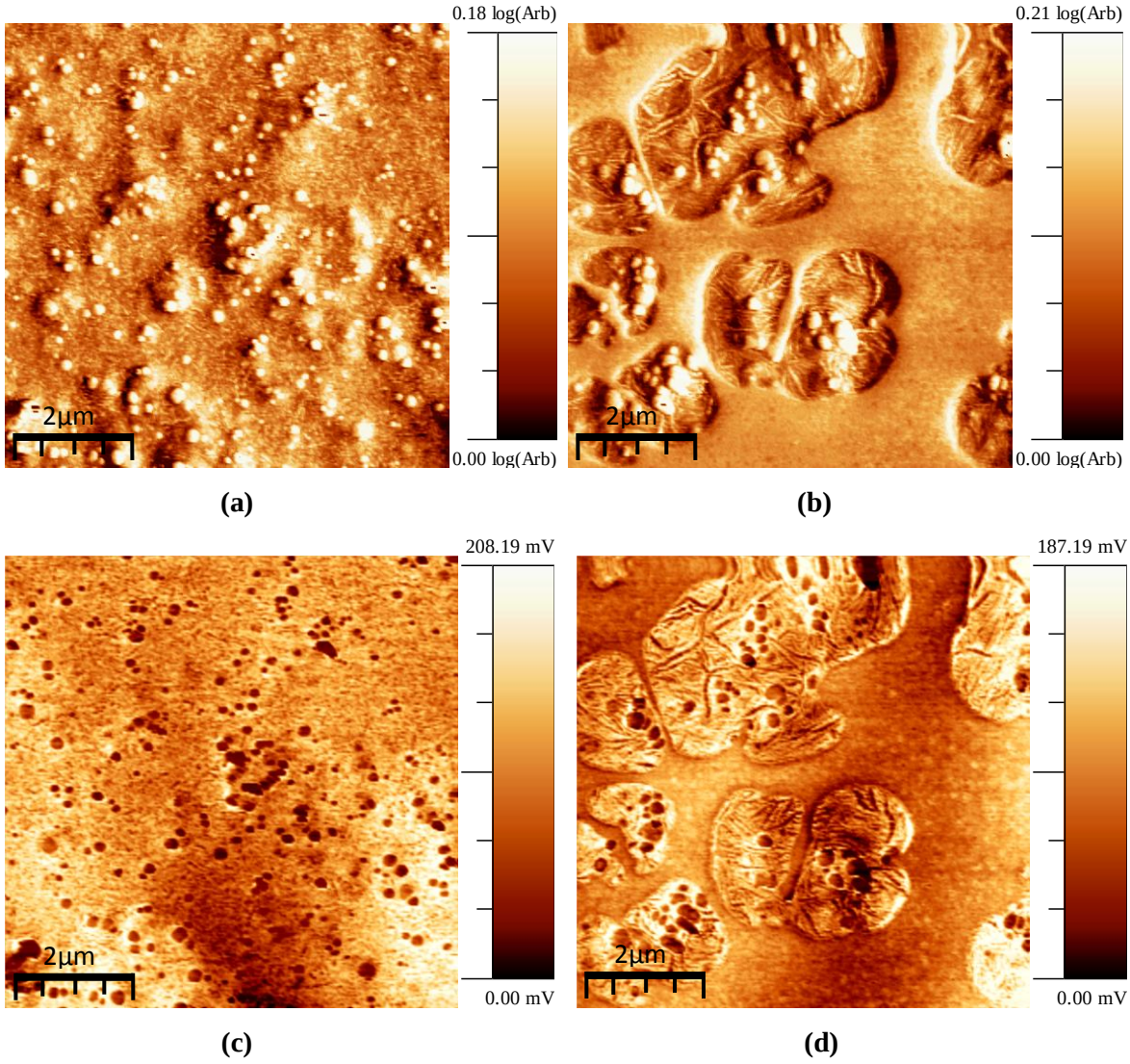


Fig. 4.6: Tapping mode AFM images of (a) and (b) DMT modulus and (c) and (d) adhesion profiles of uncapped and PVP-capped BST-P(VDF-HFP) films respectively.

The qualitative interpretation of DMT modulus profile is that darker regions are softer than the brighter regions. Therefore as shown in Fig. 4.6 (a) and (b), areas of brightest intensity represent BST nanoparticles, the population of which is considerably higher in the case of uncapped nanocomposite (Fig. 4.6 (a)) leading to rougher surface. Fig. 4.6 (a) illustrates intensive topographic features as a result of BST nanoparticles packing into P(VDF-HFP). In comparison, Fig. 4.6 (b) comprises smooth (soft) areas indicating full PVP coverage over rough surface, and clusters/islands of BST nanoparticles (bright dots) partially covered or surrounded by ultrathin PVP. As one can perceive from Fig. 4.6 (b), the term 'island' is correctly used for areas where PVP partially capped surface nanocomposite, since they are visibly greater in height relative to areas of PVP full coverage.

Besides DMT modulus, adhesion profiles mapping the adhesion (pull-off) force, i.e. any attractive force, between the AFM tip and surface of the sample, hold valuable information. In air, van der Waals, electrostatics, and forces due to the formation of a capillary meniscus contribute to adhesion depending on parameters such as surface charges and hydrophobicity. If either the surface of the sample or the tip is hydrophilic, a capillary meniscus will typically form, leading to higher adhesion that extends nanometres beyond the surface. In adhesion profiles, darker areas correspond to lower adhesion and hence more hydrophobic (low surface energy) surface [196]. Accordingly, as can be perceived from Fig. 4.6 (c) and (d), darker areas in Fig. 4.6 (c) represent BST nanoparticles and P(VDF-HFP) both of which contribute to hydrophobicity of nanocomposite surface. In contrast, bright scattered islands in Fig. 4.6 (d) indicate ultrathin PVP partially coating dark areas of BST nanoparticles, while areas in between them present full coverage of PVP over the nanocomposite (no dark dots of BST is visible). As a result, adhesion profile manifests increased surface energy and reduced hydrophobicity across PVP-capped nanocomposite (since colour contrast is relatively reduced) compared to that of uncapped surface. Hence, partial capping of nanocomposite surface with an ultrathin PVP layer is a prerequisite when deposition and adhesion of subsequent layers atop the nanocomposite is a key element in device fabrication and performance.

Similarly, to justify favourable effects of applying an ultrathin PVP layer on the surface of 5 wt% BZ-P(VDF-HFP) nanocomposites, relevant tapping mode AFM profiles and quantitative data were obtained.

While Fig. 4.7 (a), (c) and (e) represent height, DMT modulus and adhesion profiles of uncapped BZ-P(VDF-HFP) nanocomposite films, Fig. 4.7 (b), (d) and (f) are those of the PVP-coated films.

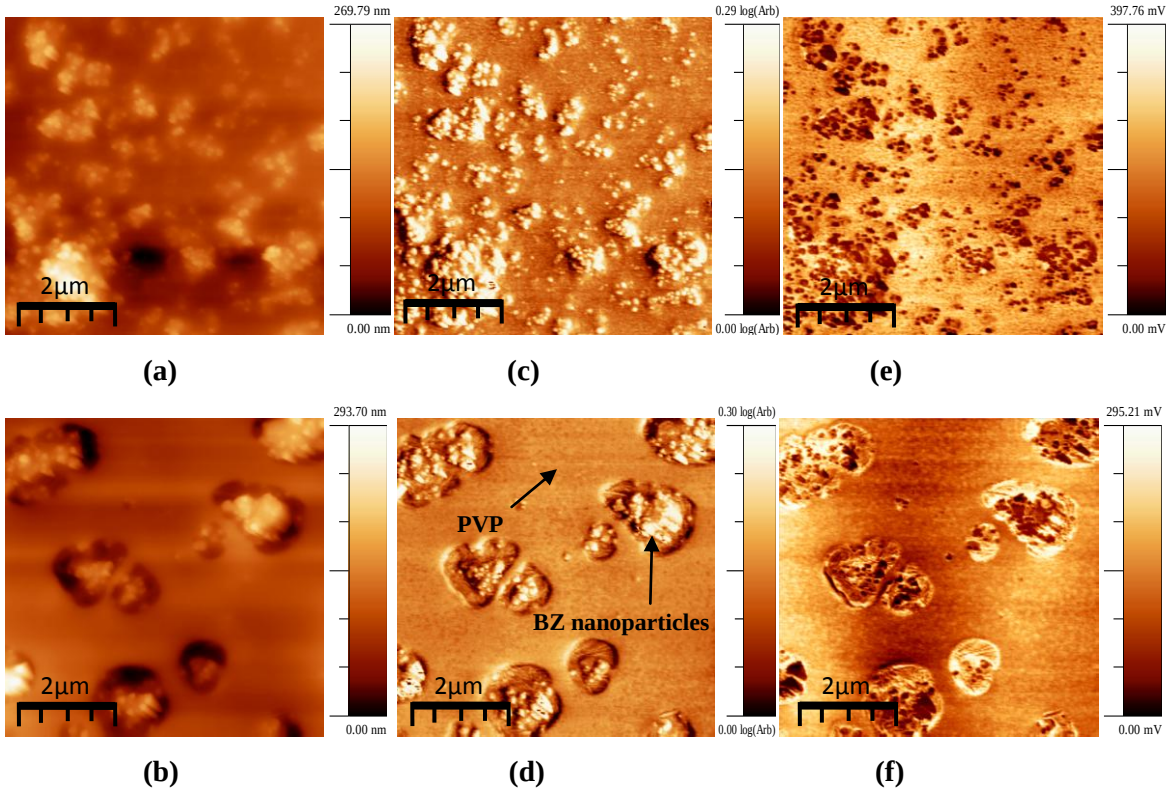


Fig. 4.7: Tapping mode AFM images of (a) and (b) height, (c) and (d) DMT modulus and (e) and (f) adhesion profiles of uncapped and PVP-capped BZ-P(VDF-HFP).

In conformity with profiles presented in Fig. 4.6, PVP partial capping along with reduced surface roughness and hydrophobicity of BZ-P(VDF-HFP) have been verified. Fig. 4.7 (b), (d) and (f) comprise smooth areas of full PVP coverage over the nanocomposite surface and scattered islands of (clustered) BZ nanoparticles partially covered or surrounded with ultrathin PVP layer. Nevertheless, fundamental differences between BST- and BZ-P(VDF-HFP) nanocomposites with or without PVP can be clearly pinpointed. Comparing DMT modulus profiles in figure (BZ-c) and (BST-a) verifies higher packing of BZ nanoparticles inside P(VDF-HFP) matrix and enhanced degree of agglomeration between them compared to that in BST-P(VDF-HFP) nanocomposites. This effect is attributed to smaller dimensions (Table 3.1) and larger surface-to-volume ratio of BZ nanoparticles which results in higher packing, greater tendency to aggregate and hence formation of thicker, rougher and less uniform films.

As a result of comparing Fig. 4.6 (b) and Fig. 4.7 (d), despite observing larger areas of PVP full coverage (possibly) only over P(VDF-HFP) or smaller BZ nanoparticles, BZ nanocomposite films considerably comprise more rough features. These features (highly agglomerated clusters of BZ) are clearly visible due to their colour contrast (BZ represented as the brightest points) and super fine coating of PVP. The presence of larger areas of PVP full coverage has resulted in better surface adhesion of BZ-incorporated bilayer dielectric (Fig. 4.7 (f)) in comparison to that of uncapped and also BST-incorporated bilayer (Fig. 4.6 (d)). However, as will be discussed in section 4-2-3-2, relatively higher ratio of PVP compared to areas of uncapped BZ-P(VDF-HFP) nanocomposite has rather counteracted desired characteristics of using high-*k* gate dielectric resulting in smaller high-capacitance and correspondingly larger operating voltage. Full set of data on film thickness, surface roughness and capacitance characteristics of uncoated and coated BST- and BZ-P(VDF-HFP) nanocomposites are gathered and exhibited in the following section 4-1-2-2.

4-1-2-2- Results on Parallel-plate Capacitors

Following specifying surface properties of P(VDF-HFP) nanocomposite films with respect to impact of PVP capping layer, here dielectric properties of such nanocomposites are studied. Recalling from section 3-1-4-2, (non-modified) BST and BZ nanoparticles were identified as the most suitable fillers in P(VDF-HFP)-based nanocomposites. The most extensive work has been done on formulation, integration and evaluation of BST-P(VDF-HFP) nanocomposite dielectrics with different filler wt % content. Once establishing a benchmark in acquiring the best dielectric characteristics using BST-P(VDF-HFP) nanocomposites, BZ-P(VDF-HFP) dielectric nanocomposites were accordingly formulated and utilised. Since best performing devices were obtained by implementing P(VDF-HFP) nanocomposite dielectrics with 5 wt % BST content, results on BZ-P(VDF-HFP) nanocomposites using similar nanoparticle loading are exclusively included here.

In order to systematically evaluate the impact of replacing low-*k* with high-*k* polymer matrix, prior to fabrication and characterisation of capacitors with P(VDF-HFP)-based nanocomposite dielectric layers, those using 5 wt % pristine P(VDF-HFP) were made and analysed. Results obtained from pristine P(VDF-HFP) were then compared to those from its corresponding nanocomposites of variable NP loading %.

Plenty of experiments have been executed with the aim to find the most suitable nanoparticle type and wt % content inside P(VDF-HFP) polymer matrix. To maintain consistency and allow comparison based on similar grounds, nanocomposite dielectrics with matching nanoparticle content (i.e. 2, 5, 8 and 11 wt %) to that of PVP-based were deposited and their dielectric properties analysed.

Despite being spin-coated at identical speed, pristine P(VDF-HFP) and its nanocomposite suspensions resulted in formation of considerably thinner (uncapped) dielectric films compared to those deposited from pristine PVP and PVP-based nanocomposites. This effect can be assigned to higher viscosity of P(VDF-HFP) solution than that of PVP. It has been reported that thickness of spin-coated films depends on initial solution viscosity, spin speed and rate of solvent evaporation. Starting with a less viscous (dilute) solution, as spin-coating progresses and solvent evaporates, the solute concentration becomes large, solution becomes thicker and much more viscous than the starting solution and hence thicker films are expected [197]. Esmlie *et al.* [198] determined the total fluid thinning rate as a function of time:

$$\frac{dh}{dt} = -2\frac{\rho\omega^2}{3\eta}h^3, \qquad \text{(Eq. 4.1)}$$

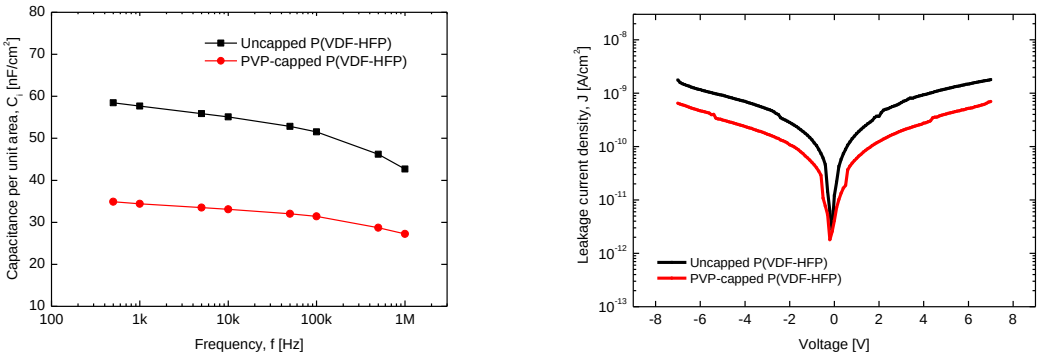
where h is the thickness, η is the viscosity, ρ is the density and ω is the rotation rate. Accordingly, they proved that an initially thicker layer thins out much faster than a thin one [198, 199].

Favourably increased viscosity of P(VDF-HFP) solution provides a more stable medium for better packing, dispersion and uniformity of nanoparticles in nanocomposite suspensions. Hence, dielectric layers formed from such suspensions manifest improved roughness and reduced thickness as less lumps or aggregates of nanoparticles are present. In addition to the role of solution viscosity, inclusion of a cross-linking agent and subsequent densification has resulted in increased film thickness in PVP-based dielectric layers. On the whole, unlike the case for PVP-based dielectrics, a more reasonably moderate, linear thickness growth is observed as nanoparticles content increases. Furthermore, capacitance and dielectric constant of P(VDF-HFP) nanocomposite dielectrics are expected to increase dramatically. This effect is not only accredited to

reduced dielectric thickness, but also to higher *k* value of P(VDF-HFP) compared to that of PVP and better dispersion and more effective impact of (non-modified) nanoparticles.

As explained in section 3-1-6, P(VDF-HFP)-based dielectric layers have to be coated with an ultrathin layer of a low-*k* polymer (e.g. PVP) to adjust its surface energy and enable deposition of subsequent layers atop. Although introduction of a capping layer is only necessary when fabricating TFTs, not capacitors, dielectric properties of both uncoated and coated P(VDF-HFP)-based films are presented and evaluated here. This will enable better understanding of TFTs characteristics demonstrated in the following section 4.2.

In Fig. 4.8, capacitance per unit area (C_i) and leakage current density (J) of capacitors with 5 wt % pristine P(VDF-HFP) dielectric layers and those capped with 2 wt % PVP are illustrated. At 1 kHz, a ~ 32 % drop in C_i of capacitor with PVP-capped P(VDF-HFP) dielectric layer (39.4 ± 0.2 nF/cm^2) compared to that of uncapped P(VDF-HFP) (57.7 ± 0.4 nF/cm^2) is reported. As expected, replacing low-*k* PVP with high-*k* P(VDF-HFP) in parallel-plate capacitors noticeably reduces dielectric breakdown voltage. While capacitors with PVP dielectric layer withstand operating voltages up to ± 20 V, those with P(VDF-HFP) dielectric exhibit similarly low leakage current density (~ 10^{-9} A/cm^2) at relatively lower breakdown voltage of ± 8 V. Such characteristics are favoured in applications requiring high performance at low operational voltages.



(a) **(b)**

Fig. 4.8: Comparison of (a) capacitance per unit area and (b) leakage current density between pristine, uncapped P(VDF-HFP) dielectric layer with that of PVP-capped.

To perform a more comprehensive analysis on the effect of (BST) nanoparticle content and that of cross-linked PVP capping layer on dielectric properties of pristine P(VDF-HFP) and its nanocomposites, values of d and C_i and accordingly calculated k, for capped and uncapped nanocomposite dielectric layers are included in Table 4.4. Values of C_i were measured at frequency of 1 kHz. The 0 wt % notation refers to pristine P(VDF-HFP) dielectric layer.

NP wt %	Uncapped			PVP-capped		
	d **nm**	C_i **nF/cm^2**	***k***	***d*** **nm**	C_i **nF/cm^2**	***k***
0	132.0 ± 0.8	57.7 ± 0.4	8.61 ± 0.2	144.0 ± 0.5	39.4 ± 0.2	6.42 ± 0.10
2	141.0 ± 1.1	75.1 ± 0.7	12.0 ± 0.2	152.0 ± 0.5	56.7 ± 0.5	9.75 ± 0.20
5	148.0 ± 0.7	93.7 ± 0.2	15.7 ± 0.4	178.0 ± 0.2	64.4 ± 0.2	13.2 ± 0.2
8	152.0 ± 1.3	99.4 ± 0.4	17.1 ± 0.5	184.0 ± 0.9	69.0 ± 0.3	14.3 ± 0.5
11	172.0 ± 2.1	102.0 ± 0.6	20.0 ± 0.5	201.0 ± 1.4	72.4 ± 0.3	16.4 ± 0.3

Table 4.4: Full set of data (Mean ± standard deviation) measured on capacitors with BST-P(VDF-HFP) nanocomposite dielectric layers of different nanoparticle wt % content.

A number of important observations can be made from data collected in this table:

i. In both uncapped and capped scenarios, a proportional rise in values of d, C_i and k is perceived as nanoparticle wt % content increases, with highest values reported on nanocomposites with 11 wt % BST.

ii. As already justified, for each BST nanoparticle content, a reduced (~ 70 %) thickness is measured on P(VDF-HFP)-based nanocomposite layers in comparison to their PVP-based counterparts.

iii. Due to combined effects of lower thickness and higher intrinsic k of P(VDF-HFP) matrix, for each BST nanoparticle content, higher C_i and k is obtained for such nanocomposites, in contrast with those of with PVP polymer matrix.

iv. The value of k for (5 wt %) pristine P(VDF-HFP) is determined to be 8.61 ± 0.20 at 1 kHz. The value provided by Sigma Aldrich is 11 measured at 100 Hz.

v. Capping the nanocomposite layer resulted in expectedly, increased thickness of the bilayer. Values of C_i and k are accordingly reduced due to the presence of PVP capping and nanocomposite layers acting as two capacitors in series.

vi. One key observation is the notable ~ 25 % drop in k for pristine P(VDF-HFP) once capped with PVP. In contrast, a relatively lower reduction in k (~ 16 %) is recorded comparing uncapped and PVP-capped nanocomposite layers of various nanoparticle content (wt %).

These findings confirm speculations made earlier in section 3-1-6 and observations from the AFM images illustrated in section 4-1-2-1 with regards to partial capping of nanocomposite layers. Surface of pristine P(VDF-HFP) is significantly smoother than that of the nanocomposites, therefore, ultrathin PVP layer would fully cover surface of pristine polymer hindering its contribution to overall high-k bilayer dielectric. On the contrary, as demonstrated in Fig. 4.5 and 4.6, surface of nanocomposites are only partially capped with PVP, leaving a portion of nanoparticles out on the surface to serve as high-k elements in such bilayer dielectric films. As a result, a relatively smaller difference is identified between k values of uncapped and PVP-capped nanocomposites. Although these justifications in combination with AFM images presented in section 4-1-2-1, establish the beneficial role of ultrathin PVP capping layer, further evaluation is required in terms of implementing such bilayers in TFTs.

In Fig. 4.9, C_i values measured on PVP-capped, P(VDF-HFP) nanocomposite dielectrics with variable BST nanoparticle content are plotted as a function of frequency. In agreement with observations made in Fig. 4.4, a consistent trend of trivial capacitance variation against frequency is evident for all different wt % of BST nanoparticles (including that of P(VDF-HFP)) across the 500 Hz - 1 MHz frequency range. As expected, a continuous rise in C_i can be observed as the nanoparticle content increases, with the highest value measured on nanocomposites with 11 wt % BST. A significant rise (by ~ 50 %) in C_i has occurred from pristine P(VDF-HFP) to 2 wt % BST nanocomposite dielectric layers. However, at higher nanoparticle content, the rate at which C_i increases gradually decreases, such that an only 9 % rise in C_i is measured by increasing BST content from 8 wt % to 11 wt %. These observations indicate possible saturation of nanoparticles inside P(VDF-HFP) polymer matrix at high wt % loading, above which no significant improvement in dielectric properties can be achieved.

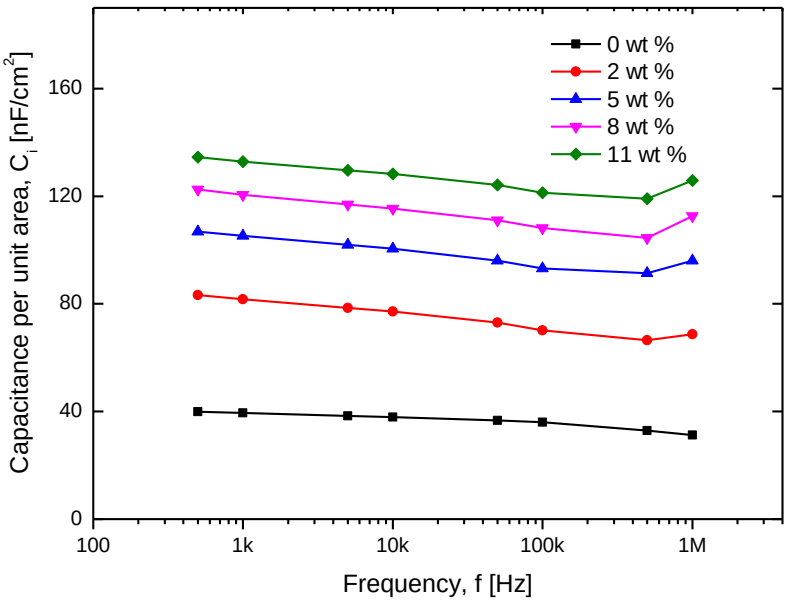


Fig. 4.9: Capacitance density vs. frequency measured on PVP-capped, P(VDF-HFP)-based nanocomposite bilayer dielectrics with variable BST nanoparticle content.

In addition to dielectric parameters recorded in Table 4.4, leakage current density is an important characteristic of a dielectric layer in capacitors and TFTs. Incorporating nanoparticles into P(VDF-HFP) enhances capacitance and dielectric constant of the end nanocomposite dielectric layer. However, leakage current density considerably deteriorates with increasing nanoparticle concentration. This effect is attributed to the rise in leakage conduction path as a result of increased surface roughness and defect states [142]. Therefore, the most effective nanoparticle wt % content should not only result in (uncapped or capped) nanocomposite dielectric layers with high C_i and k values, but also with reasonably low leakage current density.

In Fig. 4.10 and 4.11, leakage current densities measured on both uncapped and PVP-capped, BST-P(VDF-HFP) nanocomposite dielectrics with various nanoparticle concentration are plotted as a function of applied voltage. As it can be clearly perceived from Fig. 4.10, leakage current through uncapped dielectric layer escalates proportionally as the nanoparticle content increases, with highest current measured on nanocomposites with 11 wt % BST content. Therefore, despite yielding highest values of C_i and k, nanocomposites with 11 wt % nanoparticle concentration cannot serve as an excellent dielectric layer when integrated into an OTFT.

One key observation in both figures is the substantially reduced voltage differential range down to ± 2 V, ± 1.5 V and ± 1 V for nanocomposites compared to ± 8 V for pristine P(VDF-HFP) as demonstrated in Fig. 4.8 (b). As already clarified, based on equation (2.4), by utilising high-capacitance gate dielectrics, same amount of charge can be stored at lower applied voltage.

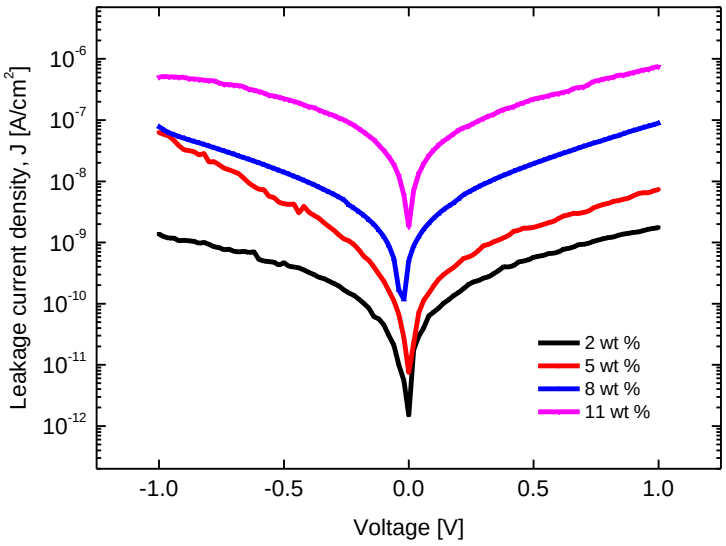


Fig. 4.10: Leakage current densities measured on uncapped, P(VDF-HFP)-based nanocomposites with various BST nanoparticle concentrations.

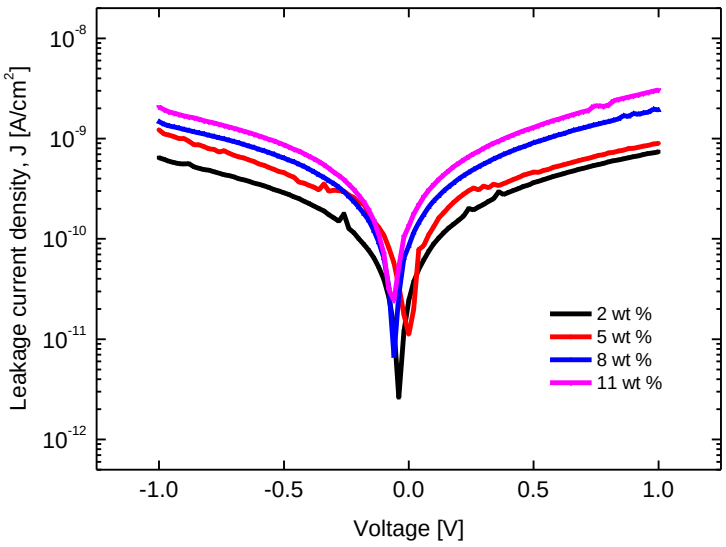
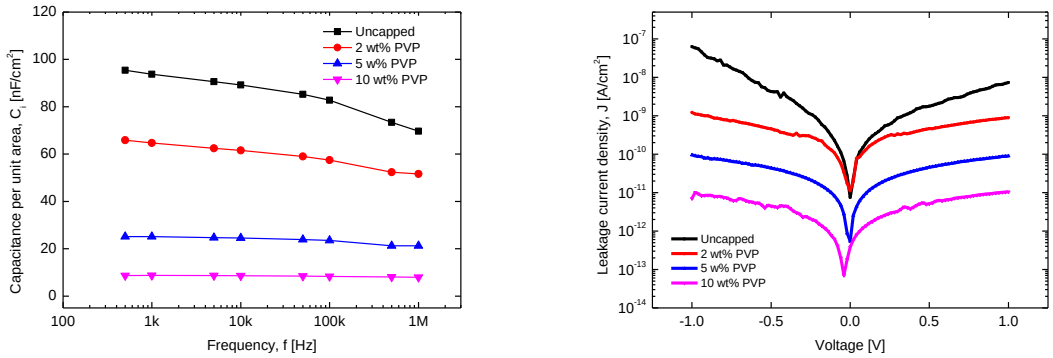


Fig. 4.11: Leakage current densities measured on PVP-capped, P(VDF-HFP)-based nanocomposites with various BST nanoparticle concentrations.

In contrast with Fig. 4.10, leakage current densities measured through PVP-capped, P(VDFHFP)-based nanocomposite dielectric, plotted in Fig. 4.11, are relatively lower by at least one and almost three orders of magnitude for 2 wt % and 11 wt % BST content respectively. In other words, following coating surface of nanocomposites of various nanoparticle loadings, less differentiation is spotted amongst leakage current densities of the corresponding gate dielectrics. Hence, one can conclude that the higher the surface roughness of a nanocomposite is the more effective is the presence of a capping layer. Nevertheless, as is obvious from Fig. 4.11, the direct relationship between leakage current through a nanocomposite layer and its nanoparticle content would hold regardless of a capping layer inclusion.

Based on data collected in Table 4.6 and leakage current densities shown in Fig. 4.11 for PVP-capped, BST-P(VDF-HFP) nanocomposites, 5 wt % is established as the most satisfactory nanoparticle concentration. Nanocomposites consisting of 5 wt % BST have demonstrated higher capacitance and dielectric constant than 2 wt % ones, while exhibiting lower leakage current density than those of 8 wt % and 11 wt %; all at a reasonable film thickness. Further investigations included in section 4-2 also justifies choosing 5 wt % as the best choice of nanoparticle concentration in formulation of P(VDF-HFP)-based nanocomposites with superior dielectric and device characteristics.

As discussed in section 3-1-6, a 2 wt % PVP is spin-coated onto every P(VDF-HFP)-based nanocomposite dielectric layer. AFM images presented in section 4-1-2-1, in addition to dielectric properties obtained on uncoated and coated nanocomposite gate dielectrics confirm the existence and influence of such ultrathin PVP layer. This specific concentration of PVP (leading to its suitable coverage thickness, ~ 20 - 30 nm) was chosen following attempting a number of trial experiments involving spin-coating various wt % of PVP over BST-P(VDF-HFP) nanocomposite layers. Capacitance and leakage current densities measured on 5 wt % BST-P(VDF-HFP) nanocomposite films without and with PVP capping of various concentrations (2, 5 and 10 wt %) are plotted in Fig. 4.12 (a) and (b) respectively. Capacitance density of pristine nanocomposite has dropped by 30 % for 2 wt % PVP capping and by 60 % when capped with 5 wt % and 10 wt % PVP. Similarly, leakage current densities exhibit drop of about one order of magnitude following capping pristine nanocomposite dielectric layer with PVP of 2, 5 and 10 wt % concentration.



(a) **(b)**

Fig. 4.12: (a) Capacitance and (b) leakage current densities of uncapped 5 wt % BST-P(VDF-HFP) nanocomposites and that of capped with PVP of different concentrations.

Using a 10 wt % PVP capping layer has almost completely counteracted the (beneficial) effects of the underlying nanocomposite material and the bilayer dielectric behaves nearly as mediocre as a single dielectric layer of pristine PVP.

4-2- TFTs' Device Characteristics

In this last section of results and discussions chapter, characteristics of OTFTs fabricated using the two different classes of nanocomposite dielectric materials developed in this work are presented and evaluated. Similar to trend taken up in the previous section, in order to perform methodical comparisons, OTFTs were initially analysed based on their dielectric layers, i.e. PVP- and P(VDF-HFP)-based nanocomposites. Then, in each category, device characteristics using different semiconducting materials were included and extensively studied. Finally, a large chunk of this section is allocated to demonstration of novel, ultra-low TFTs with P(VDF-HFP)-based nanocomposite dielectric layer and using a variety of semiconducting materials as the active layer.

4-2-1-PVP-based Nanocomposite Gate Dielectrics

Following characterisation of PVP-based nanocomposite dielectric layers with different surface-modified nanoparticle fillers, OTFTs performance using such dielectric layers are studied here.

Recalling from section 4-1-1-1, nanocomposite dielectric layers consisting of OPA-BZ, ODPA- and OPA-CZ and HMDS-BST nanoparticles consecutively yielded improved dielectric properties (such as C_i and k) compared to that of the pristine PVP. Nevertheless, performance of such dielectric layers when implemented into OTFTs has to be examined and compared in order to identify the best choice of nanocomposite dielectric layer for use in high performance OTFTs.

OTFTs (with BGBC configuration) have been fabricated using PVP-based nanocomposite dielectrics comprising different concentration of all six choices of surface-modified nanoparticles. TIPS-Pentacene and its blend with PαMS have been applied as the semiconducting material following steps described in Table 3.6 (section 3-2-2). OTFTs using the TIPS-pentacene/PαMS blend exhibited better figures of merit compared to those with pristine TIPS-pentacene (See Table Apx.B2). This is attributed to a vertical phase separation occurring upon the semiconductor blend deposition. As a result, a TIPS-pentacene layer is sandwiched in between two layers of PαMS which leads to formation of a smoother semiconductor-dielectric interface with less defects, reduced charge trapping and improved charge transport. Therefore, only limited number of devices was initially fabricated using the pristine TIPS-Pentacene (solely for comparison purposes) and TIPS-pentacene/PαMS blend was ultimately applied as the semiconducting material in PVP-based OTFTs (See Appendix B).

In agreement with findings reported in section 4-1-1-1, dielectric nanocomposites with 11 wt % nanoparticle content have yielded the best device characteristics, such as carrier mobility, threshold voltage and on/off ratio. Apart from unsatisfactory attempts to make operational transistors with ODPA-CZ nanocomposite dielectrics, all the other PVP-based nanocomposites were successfully applied as dielectric layers in TIPS-Pentacene and TIPS-Pentacene/PαMS OTFTs. Transfer characteristics of TIPS-Pentacene/PαMS OTFTs using the pristine PVP and other five choices of surface-modified nanoparticles (11 wt %) in PVP gate dielectrics are collectively plotted in Fig. 4.13. As can be perceived, OTFTs using nanocomposite dielectrics with 11 wt % OPA-BZ and HMDS-BST have resulted in relatively better device performance, whereas device using OPA-CZ nanocomposite dielectrics exhibited poor performance with extreme hysteresis in their transfer characteristics.

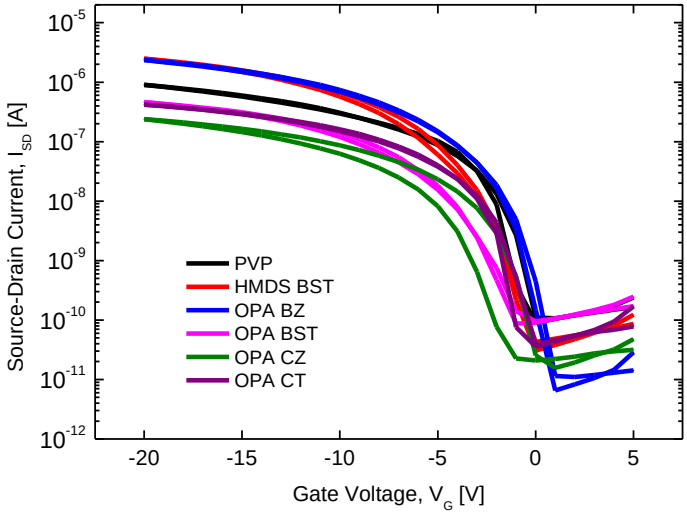
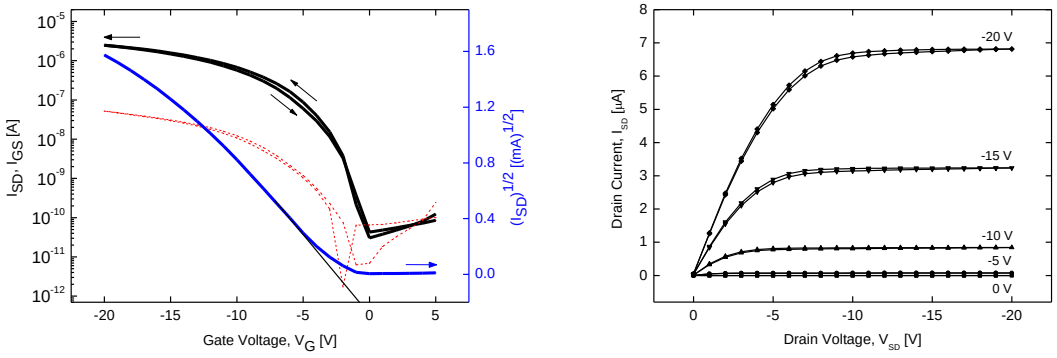


Fig. 4.13: Comparison of transfer characteristic of TIPS-Pentacene/PαMS blend TFTs using pristine PVP and its nanocomposites with 11 wt % of various surface-modified NPs, V_{SD} = -20 V, channel width (W) = 2000 µm and channel length (L) = 30 µm.

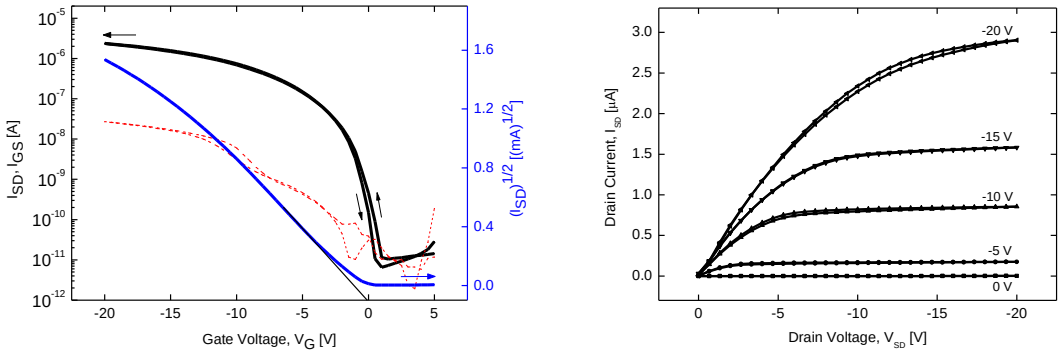
To carry out more detailed analyses, transfer, leakage and output characteristics of OTFTs with OPA-BZ and HMDS-BST in PVP nanocomposite gate dielectrics are illustrated in Fig. 4.14 and 4.15. For both devices, the characteristics show negligible hysteresis, clear, well-behaved linear (ohmic) regime and well-saturated, relatively high I_{SD} in $|V_{SD}| = |V_G - V_T|$ regime.



(a) **(b)**

Fig. 4.14: (a) Transfer and (b) output characteristic of a TIPS-Pentacene/ PαMS TFTs using PVP-based nanocomposites with 11 wt % HMDS-BST nanoparticle concentration, V_{SD} = -20 V, channel width (W) = 2000 µm and channel length (L) = 30 µm.

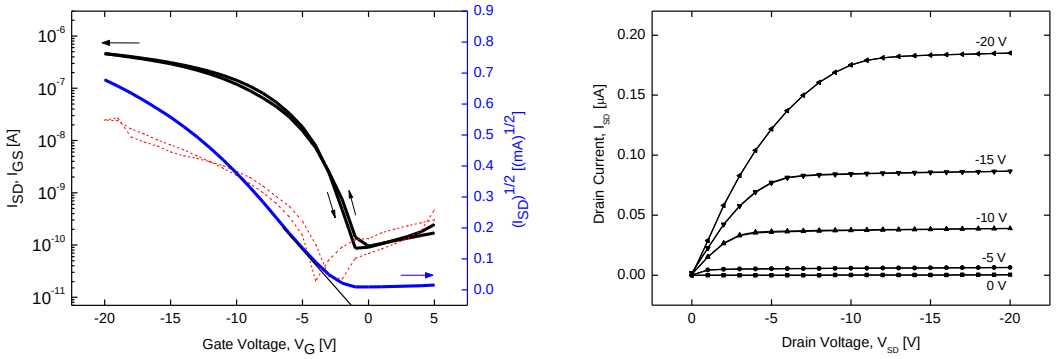
Gate leakage current is in both devices is at least one order of magnitude lower than "on" current. Nonetheless, better output characteristics, i.e. steeper, more saturated with lower pinch-off voltage and (about twice) higher output current, is observed in devices with HMDS-BST nanocomposites.



(a) **(b)**

Fig. 4.15: (a) Transfer and (b) output characteristic of a TIPS-Pentacene/ PαMS TFT using PVP-based nanocomposites with 11 wt % OPA-BZ nanoparticle concentration, V_{SD} = -20 V, channel width (W) = 2000 µm and channel length (L) = 50 µm.

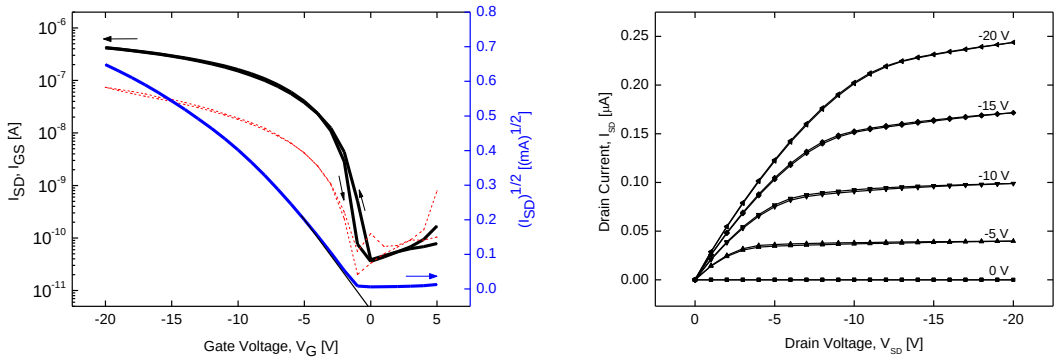
In addition, transfer and output characteristics of OTFTs using OPA-BST and OPA-CT nanocomposites in PVP as the gate dielectric are demonstrated in Fig. 4.16 and 4.17 respectively. These devices operate successfully at -20 V with negligible hysteresis, although the on/off ratios on both devices are noticeably lower than those of HMDS-BST and OPA-BZ nanocomposite dielectrics shown in Fig. 4.14 and 4.15.



(a) **(b)**

Fig. 4.16: (a) Transfer and (b) output characteristic of a TIPS-Pentacene/ PαMS TFT using PVP-based nanocomposites with 11 wt % OPA-BST nanoparticle concentration, V_{SD} = -20 V, channel width (W) = 2000 µm and channel length (L) = 20 µm.

Comparing the output characteristics in Fig. 4.14, 4.15, 4.16 and 4.17, smaller output currents are measured on transistors using OPA-BST and OPA-CT nanocomposites (Fig. 4.16 (b) and 4.17 (b)) compared to those with HMDS-BST and OPA-BZ (Fig. 4.14 (b) and 4.15 (b)). Moreover, evidence of contact resistance, poor saturation behaviour and slight hysteresis can be observed in OTFTs with OPA-BZ (Fig. 4.15 (b)) and OPA-CT (Fig. 4.17 (b)) nanocomposite dielectrics.



(a) **(b)**

Fig. 4.17: (a) Transfer and (b) output characteristic of a TIPS-Pentacene/ PαMS TFT using PVP-based nanocomposites with 11 wt % OPA-CT nanoparticle concentration, V_{SD}= -20 V, channel width (W) = 2000 µm and channel length (L) = 50 µm.

The figures of merit for TIPS-Pentacene/PαMS OTFTs using pristine PVP and four choices of nanocomposite gate dielectrics are collected in Table 4.5. In comparison with pristine PVP, devices with nanocomposite dielectric layer exhibit improved device performance. The figure-of-merit 'μC_i' is highest for OTFTs with HMDS-BST and OPA-BZ nanocomposite dielectrics (only slightly higher for HMDS-BST nanocomposites), while the lowest value belongs to OPA-CT nanocomposites. Overall, better threshold voltage and subthreshold swing are reported on OTFTs with OPA-BZ nanocomposites.

Gate dielectric		**C_i** **nF/cm^2**	**µ** **cm^2 /Vs**	**V_T** **V**	**SS** **mV/dec**	**ON/OFF** **ratio**
PVP		6.87	7.73×10^{-3}	0.74	734	10^4
Nanocomposite	OPA-BZ	9.34	3.87×10^{-2}	- 0.24	530	10^5
	HMDS-BST	10.24	4.1×10^{-2}	- 1.4	804	10^5
	OPA-BST	9.15	1×10^{-2}	-1.75	970	5×10^3
	OPA-CT	7.72	1×10^{-2}	-0.42	875	10^4

Table 4.5: Device characteristics of TIPS-Pentacene/PαMS OTFTs with different dielectrics.

The low values of carrier mobility, particularly in the case of pristine PVP, can be attributed to the thickness of the dielectric layer and quality of the semiconductor-dielectric interface. Nonetheless, the cleanroom's unsatisfactory conditions should not be overlooked. In conclusion, nanocomposites with BST and BZ nanoparticles are considered as better choices of high-*k* dielectrics for OTFT applications.

4-2-2-P(VDF-HFP)-based Nanocomposite Bilayer Dielectrics

In this section, results and discussions on OTFTs with P(VDF-HFP)-based nanocomposite bilayer dielectrics are presented. All devices reported here were fabricated using PVP-capped nanocomposite dielectric layers. Apart from some comparative data presented in the first part of this section, a significant portion of this section is predominantly allocated to demonstration and evaluation of ultralow-voltage OTFTs. Unlike the case for TFTs with PVP-based nanocomposite dielectric layers in which 11 wt % nanoparticle content yielded best operating devices, in P(VDF-HFP)-based TFTs, excellent device characteristics at ultralow operating voltage are obtained using 5 wt % nanoparticle loading (in agreement with conclusion made in section 4-1-2-2). For this reason only TFTs using P(VDF-HFP)-based nanocomposites with 5 wt % nanoparticle content are included and results on nanocomposites of higher NP concentrations are omitted to avoid complication.

As, explained in chapter 2 and empirically verified in section 4-1-2-1 and 4-1-2-2, the presence of an ultrathin (PVP) capping layer plays a critical role in improving the nanocomposite surface properties and fabrication and operation of OTFTs. Despite their excellent leakage current density and high *k*, when integrated into an OTFTs, BST- and BZ-P(VDF-HFP) dielectric layers exhibit increased leakage current, minimised surface wettability and poor dielectric-semiconductor interface, leading to unsatisfactory formation of the semiconductor layer and reduced carrier mobility. Enhanced surface roughness of nanocomposites gives rise to a higher density of traps at the dielectric-semiconductor interface, acts as conduction paths and results in increased leakage current and poor device performance. Partial coating of rough nanocomposite surface not only fills in the pinholes and improves the interface, but also enables subsequent solution-processing of the semiconducting materials by adjusting surface energy of the underlying layer. Finally, cross-linked PVP layer minimises likelihood of interfacial mixing and charge trapping due to possible dissolution or swelling effects following deposition of the semiconductor.

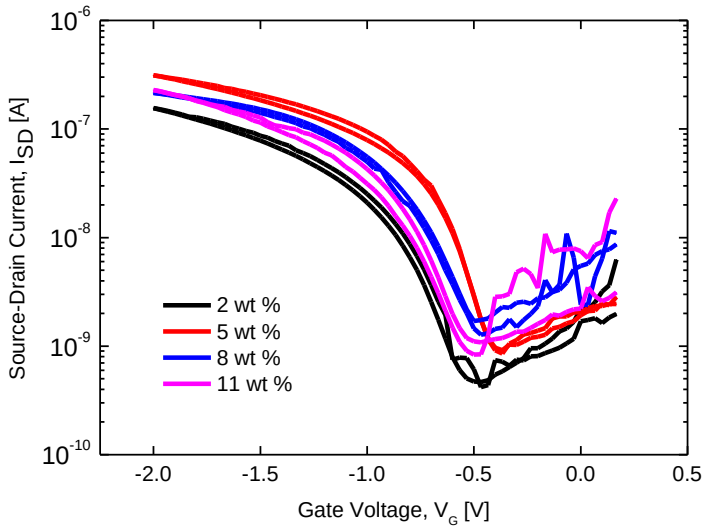


Fig. 4.18: Transfer characteristics of TIPS-pentacene/PαMS OTFTs with bilayer dielectric of various wt % BST, V_{SD} = -2 V, channel width (W) = 2000 µm and channel length (L) = 30 µm.

In Fig. 4.18, transfer characteristics of TIPS-pentacene/PαMS TFTs with PVP-capped, P(VDF-HFP)-based nanocomposite dielectric with various BST content are demonstrated. As can be perceived, all four different BST loadings result in operational TFTs below -2 V with distinct transition from "off" to "on" state and minimal hysteresis. Based on visual evaluations, transfer characteristics measured on TFTs using nanocomposite dielectric with 5 wt % BST exhibit better device performance. Nevertheless, in order to make a conclusive decision on which NP wt % concentration to ultimately choose, figures of merit for each TFT is calculated and collected in the Table 4.6. According to these data, TFTs using a 5 wt % BST-P(VDF-HFP) nanocomposite bilayer dielectric layer demonstrate higher carrier mobility and lower threshold voltage (-0.5 V); characteristics which make such TFTs promising candidates for operation at/below -1 V.

BST concentration wt %	**µ cm^2/Vs**	**V_T V**	**ON/OFF ratio**
2	2×10^{-2}	-0.7	6×10^{2}
5	4.1×10^{-2}	-0.5	4×10^{2}
8	2.6×10^{-2}	-0.6	2×10^{2}
11	2.3×10^{-2}	-0.7	3×10^{2}

Table 4.6: Device quantitative characteristics of TIPS-pentacene/PαMS TFTs using PVP-capped, P(VDF-HFP)-based nanocomposite dielectric with various wt % BST content.

4-2-3- Ultralow-voltage OTFTs

Once P(VDF-HFP)-based nanocomposites with 5 wt % nanoparticle concentration had been established as the most suitable gate dielectric for low-voltage operational TFTs, various modifications and improvements were attempted to identify a benchmark to fabricate and realise ultralow-voltage, solution-processed OTFTs. To perform solid, methodical analyses on impact of using high-*k* nanocomposite bilayers in TFTs, (recalled) dielectric properties and device characteristics of P(VDF-HFP)-based nanocomposite dielectrics using BST and BZ nanoparticles are separately investigated. The influence of different nanoparticle type (and size) on characteristics of the end-use devices are accordingly evaluated. Nevertheless, as will be disclosed, the most emphasis is paid to BST-P(VDF-HFP) nanocomposite gate dielectrics as their distinctive attributes to realise one volt-operating TFTs using a variety of semiconducting materials prevailed. In order to avoid using convoluted terminologies, in each of the following two subsections, the shortened term 'nanocomposite' is mainly used to refers to PVP-capped, P(VDF-HFP)-based nanocomposites with 5 wt % BST or BZ nanoparticle content correspondingly.

4-2-3-1- BST-P(VDF-HFP) Nanocomposite Dielectrics

Prior to studying TFTs characteristics, impact of PVP-capping layer on dielectric properties of the related nanocomposites is recollected. Fig. 4.19 illustrates leakage current densities measured through uncoated and coated BST nanocomposite dielectric layers.

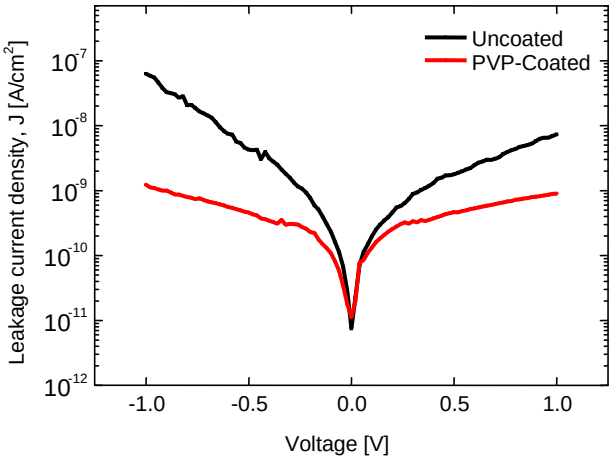


Fig. 4.19: Leakage current density of BST-P(VDF-HFP) nanocomposite dielectric films.

As can be clearly perceived, inclusion of PVP (partial) capping has reduced leakage current through the nanocomposite bilayer by at least one order of magnitude. Other key dielectric parameters measured on single and bilayer BST nanocomposite dielectric layers are gathered in Table 4.7. Firstly, based on these data, thickness of the PVP layer is ~ 30 nm. Secondly, reduced surface roughness (by 28 %) is one of the crucial observations in PVP-capped nanocomposites. To reiterate, reduction in *Ci* and *k* within such reasonable margins range is inevitable to compensate for improved surface properties.

BST-P(VDF-HFP) nanocomposite	**RMS Roughness [nm]**	**Mean Thickness [nm]**	**C_i* [nF/cm^2]**	**Dielectric Constant (k)**
Uncapped	28.4 ± 0.7	148.0 ± 0.7	93.7 ± 0.2	15.7 ± 0.4
PVP-Capped	20.32 ± 0.4	178.0 ± 0.4	64.4 ± 0.2	13.2 ± 0.2

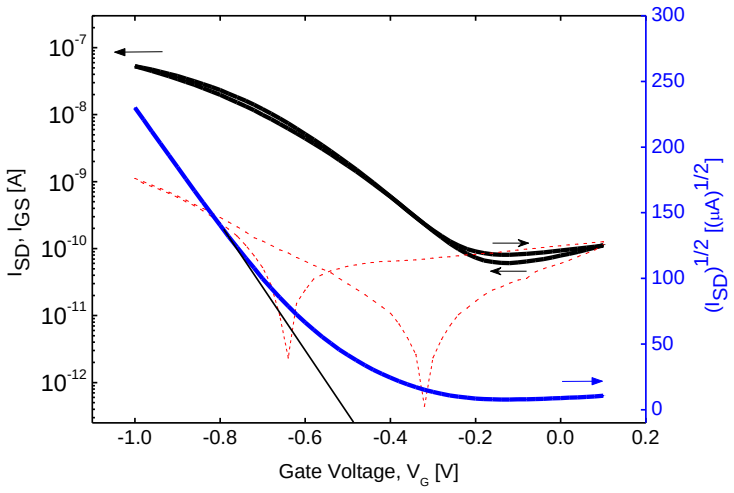
***Capacitance was measured at 1 kHz**

Table 4.7: Surface and dielectric properties of BST-P(VDF-HFP) nanocomposite layers.

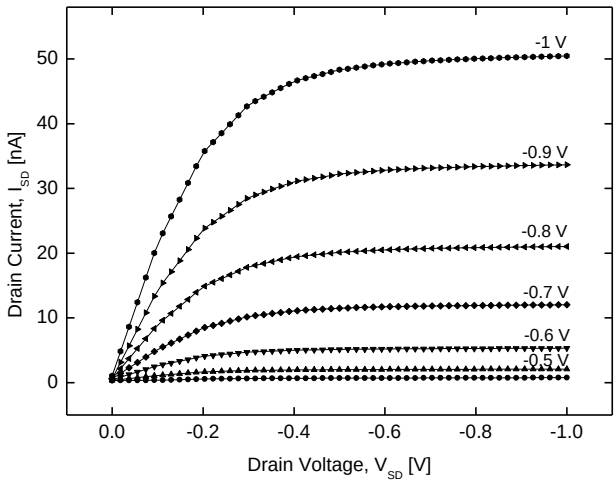
Once nanocomposite dielectric layers are characterised, TFTs are fabricated by following specific procedures carefully tailored to suit each semiconducting material type as pointed out in Table 3.6 (section 3-2-2). Transfer (in combination with gate leakage current) and output characteristics of TFTs using different semiconductors are illustrated below.

As was mentioned before, to verify versatility of P(VDF-HFP)-based nanocomposite dielectric bilayers, OTFTs using both solution-processed and vacuum-deposited semiconductors have been attempted. In addition, semiconducting blends of amorphous polymer with small molecule (TIPS-pentacene) and polycrystalline polymer (PBTTT) have been attempted in this work. As already discussed in section 4-2-1, using a semiconductor blend improves dielectric-semiconductor interface and charge transport. Hence, generally, better operating devices are expected when a blend rather than the corresponding pristine semiconductor is used. Apart from IF-PTAA OTFTs exhibiting very poor device characteristics or being completely non-operational (See Table Apx.C1 and C2), all other TFTs with high-*k* nanocomposite bilayer dielectrics demonstrate desirable characteristics at or near -1 V. Therefore, results on IF-PTAA OTFTs have been omitted from this document.

In Fig. 4.20, transfer and leakage, and output characteristics of solution-processed PDPPTT OTFTs are illustrated. Clean, almost hysteresis-free transfer characteristics, sufficiently low leakage current (at least one order of magnitude below "on" current) and clear "off" and "on" operating states are demonstrated at -1 V. Steep and well-saturated output characteristics with relatively high I_{SD} in $|V_{SD}| > |V_G - V_T|$ regime is satisfactorily achieved. Such ultralow-voltage operational devices are particularly promising candidates for low power electronics, portable/wearable electronics and aqueous sensing applications.



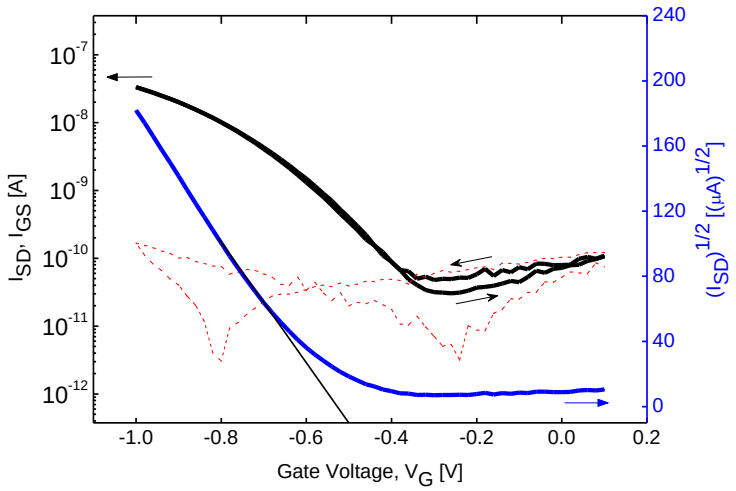
(a)



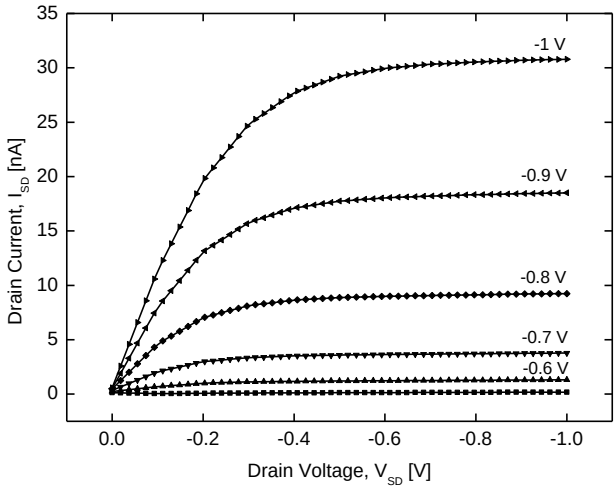
(b)

Fig. 4.20: (a) Transfer characteristics including leakage current (dotted line) and (b) output characteristic of a PDPPTT OTFT using PVP-capped BST-P(VDF-HFP) gate dielectric layer, V_{SD} = -1 V, channel width (W) = 2000 µm and channel length (L) = 40 µm.

Next, transfer and output characteristics of solution-processed, TIPS-pentacene/PαMS TFTs are presented in the following Fig. 4.21. Well-defined transition between "on" and "off" states and almost no hysteresis is evident below -1 V. In comparison with PDPPTT devices, lower subthreshold swing (169 mV/dec) and reduced leakage current density (an order of magnitude) is observed in TIPS-pentacene/PαMS TFTs due to improved dielectric-semiconductor interface.



(a)



(b)

Fig. 4.21: (a) Transfer and leakage current (dotted line) and (b) output characteristics of a TIPS-pentacene/PαMS blend TFT with BST-P(VDF-HFP) bilayer dielectric, V_{SD} = -1 V, channel width (W) = 2000 µm and channel length (L) = 50 µm.

As a result of a vertical phase separation occurring upon the semiconductor blend deposition, a TIPS-pentacene layer is sandwiched in between two layers of PαMS. The PαMS layer at the bottom (collectively with PVP capping layer) contributes to a smoother and more robust and trap-free interface at the dielectric. Nevertheless, (twice) lower drain current is collected in TIPS-Pentacene/PαMS devices compared to that in PDPPTT ones.

PBTTT polymer has been similarly blended with PαMS prior to depositing as semiconductor layer. This approach came to existence following unsatisfactory attempts in realising low-voltage operational TFTs using pristine PBTTT (See Appendix E). It has been speculated that polycrystallinity of PBTTT polymer in addition to surface roughness of the underlying nanocomposite bilayer resulted in poor dielectric-semiconductor interface, increased leakage current and ill-behaved OTFTs. Therefore, as already shown in TIPS-pentacene/PαMS blend devices, one possible solution was to improve dielectric-semiconductor interface by blending PBTTT with amorphous PαMS and reducing its polycrystallinity.

Fig. 4.22 illustrates transfer and leakage characteristics of PBTTT/PαMS blend TFTs. As can be perceived, leakage current is reasonably lower than that of "on" current. However, "on" current (and on/off ratio) is relatively lower than that reported in previous two devices. It is believed that PBTTT gets doped quickly (in air) and device performance is deteriorated accordingly due to the presence of oxygen vacancies (acting as charge traps).

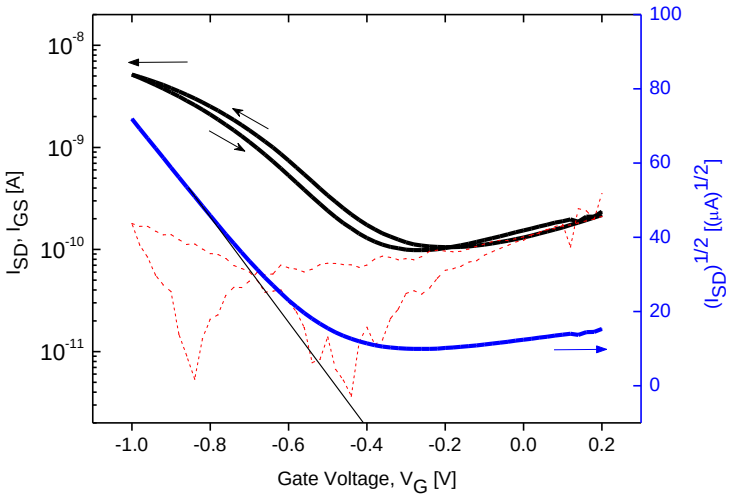
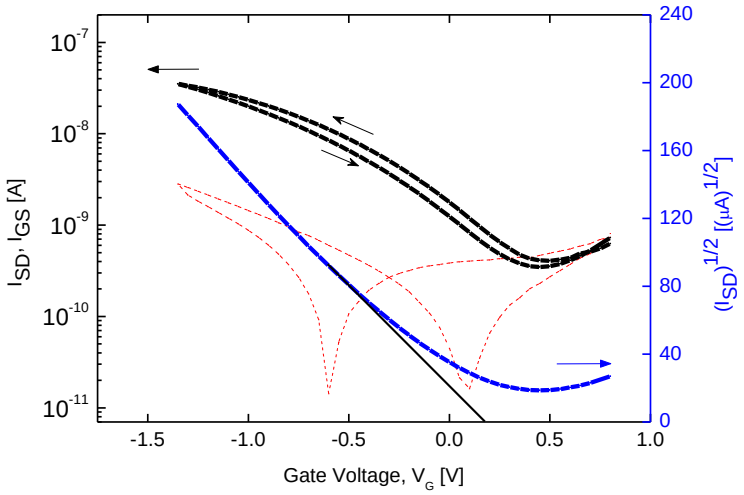


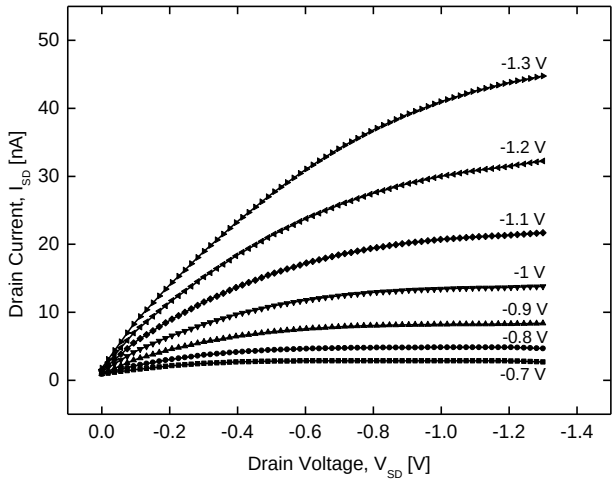
Fig. 4.22: Transfer characteristics of a PBTTT/PαMS blend TFT with BST-P(VDF-HFP) bilayer dielectric, V_{SD} = -1 V, channel width (W) = 2000 µm and channel length (L) = 40 µm.

Following demonstrating TFTs using solution-processed semiconductors, transfer and output characteristics of vacuum-deposited DNTT devices are presented in Fig. 4.23. The procedure of depositing DNTT adopted in this work has been described in section 3-2-2. DNTT crystals are very delicate which necessitates taking extra care during deposition.

Several attempts had to be made to successfully obtain a DNTT layer atop PVP-capped nanocomposite dielectric layer under mediocre lab and evaporator conditions. As can be observed, TFTs exhibited reasonable performance, such as low leakage current and clear transition from "off" to "on" state, below -1.2 V.



(a)



(b)

Fig. 4.23: (a) Transfer and (b) output characteristic of a DNTT TFT with BST-P(VDF-HFP) bilayer dielectric, V_{SD} = -1 V, channel width (W) = 2000 µm and channel length (L) = 40 µm.

Nonetheless, on/off ratio and subthreshold swing are noticeably worse than those illustrated in previous devices. Such poor behaviour is ascribed to the formation of smaller grains and more disordered domains in DNTT thin films (atop rough nanocomposite dielectric) which act as charge traps at the dielectric-semiconductor interface.

Similarly, the output characteristics illustrates higher pinch-off point ($|V_{SD}| = |V_G - V_T|$) for DNTT TFTs compared to those with PDPPTT and blend active layers leading to higher operating voltage in the former. It has been reported that solution-processed alkylated-DNTT semiconductor layers have much larger grain size than those of vacuum-deposited resulting in less interface trap density and OTFTs with smaller threshold voltage and subthreshold swing [200]. The positive shift in threshold voltage of vacuum deposited DNTT (Fig. 4. 23 (b)) is speculated to be due to interfacial trap density and the possible increase in trapped charges into localised states; an effect which is time dependent and referred to as bias stress effect [201].

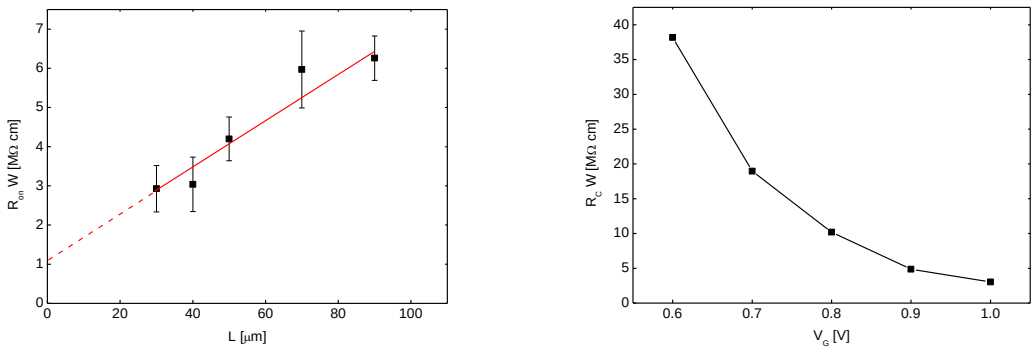
To allow quantitative evaluation of devices performance and draw a decisive conclusion on what class of semiconducting materials to utilise, figures of merit derived from transfer characteristics of each of the corresponding devices are gathered in Table 4.8. According to this table, the highest carrier mobility is obtained on PDPPTT TFTs, while the lowest value is measured on PBTTT/PαMS devices which also exhibit the lowest on/off ratio. TFTs using TIPS-Pentacene/PαMS are considered as the second best devices in terms of charge carrier mobility, but are the best with regards to subthreshold swing.

Semiconductor	**μ** cm^2/Vs	**V_T** **V**	**SS** **mV/dec**	**On/Off ratio**
PDPPTT	1.4×10^{-1}	-0.5	221	10^3
TIPS-Pentacene/PαMS	6×10^{-2}	-0.55	169	10^3
PBTTT/PαMS	1.2×10^{-2}	-0.4	560	5×10^1
DNTT	2×10^{-2}	0.1	640	10^2

Table 4.8: Figures of merit calculated for TFTs with PVP-capped, BST-P(VDF-HFP) nanocomposite bilayer gate dielectric using different semiconducting materials.

The highest subthreshold swing is reported on TFTs with vacuum-deposited DNTT, indicating that the transition between "off" and "on" states is hampered in the latter due to higher interface charge trap density. All in all, we can conclude that by utilising our in-house developed dielectric BST-P(VDF-HFP) nanocomposite formulation, ultralow-voltage TFTs can be realised with a variety of semiconducting materials, processed from solution or by vacuum-deposition.

To complete device characterisation, total on-resistance (R_{on}) as a function of channel length (L) and contact resistance (R_C) as a function of gate voltage (V_G) for TIPS-Pentacene/PαMS OTFTs are plotted in Fig. 4. 24.



(a) **(b)**

Fig. 4.24: Estimation of contact resistance of TIPS-Pentacene/PαMS OTFTs with PFBT-treated S/D contact by using the transfer-line method. (a) Channel width-normalised R_{on} as a function of channel length, (b) Width-normalized R_c as a function of V_G.

As expected, R_{on} increases linearly as channel length (same as the shadow mask) increases. While the contact resistance is independent of channel length, the channel resistance is proportional to the channel length [162]. Consequently, the relative influence of the contact resistance decreases as the channel length is increased. Reduction in R_C with increasing gate-source voltage (V_G) is likely to be due to an increase in carrier density in the channel and near the contacts as a result of better charge injection from the source [163]. R_C can be also estimated using a 4-probe measurement setup in which the voltage between source and drain is monitored, while passing current during V_{SD}or V_G sweeps. The value of R_C determined from the Y intercepts of a linear fit to the data in Fig. 4.24 (a) is 1.1 MΩ cm. Although this value is relatively large, it is still acceptable for such low operational voltages resulting in device performance comparable to those operating at higher voltages.

Further device optimisation to enhance the quality of S/D contacts and improve the semiconductor morphology is likely to reduce the contact resistance in (bottom-gate, bottom-contact) TFTs.

4-2-3-2- BZ-P(VDF-HFP) Nanocomposite Dielectrics

In this very last section of chapter 4, characteristics of TFTs fabricated on PVP-capped, P(VDF-HFP)-based nanocomposite dielectric layers with 5 wt % BZ nanoparticles are reviewed. As was mentioned before, due to time constraints, attempting extensive experiments and analyses similar to that demonstrated in section 4-2-3-1 (OTFT with BST-based nanocomposite dielectric) to examine the versatility of BZ-based nanocomposite dielectrics was almost impractical. Hence, only TFTs using TIPS-Pentacene/PαMS blend semiconductor has been attempted. Results presented here not only allow evaluation of BZ-nanocomposite bilayer dielectrics when implemented in TFTs for ultralow-voltage operation, but also comparison between such TFTs and those with a BST-nanocomposite dielectric layer. Similar to section 4-2-3-1, impact of PVP-capping layer on dielectric properties of BZ-P(VDF-HFP)-based nanocomposite bilayers is recalled, prior to characterisation of the corresponding TFTs. Leakage current densities measured through uncapped and capped nanocomposite dielectric layers are presented in Fig. 4.25. BZ-nanocomposite bilayer dielectrics exhibit reduced leakage current density by at least one order of magnitude compared to uncapped, single layers. This is attributed to less rough, denser and thicker bilayer dielectrics.

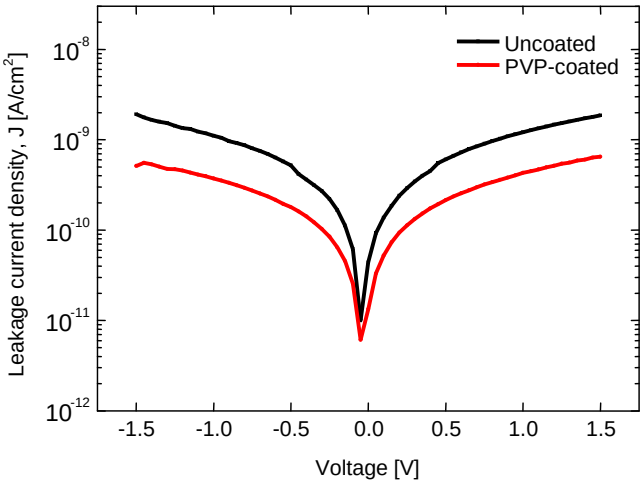


Fig. 4.25: Leakage current density of uncoated and coated, BZ-P(VDF-HFP) nanocomposite dielectric films.

Additional key dielectric parameters measured on the corresponding dielectric layers are collected in Table 4.9. Firstly, PVP thickness is ~ 24 nm.

BZ-P(VDF-HFP) nanocomposite	**RMS Roughness [nm]**	**Thickness [nm]**	**C_i* [nF/cm^2]**	**Dielectric Constant (*k*)**
Uncapped	33.8 ± 0.5	269.0 ± 0.6	72.3 ± 0.8	21.9 ± 0.4
PVP-Capped	29.3 ± 0.2	293.0 ± 0.1	27.5 ± 0.3	8.9 ± 0.4

***Capacitance was measured at 1 kHz**

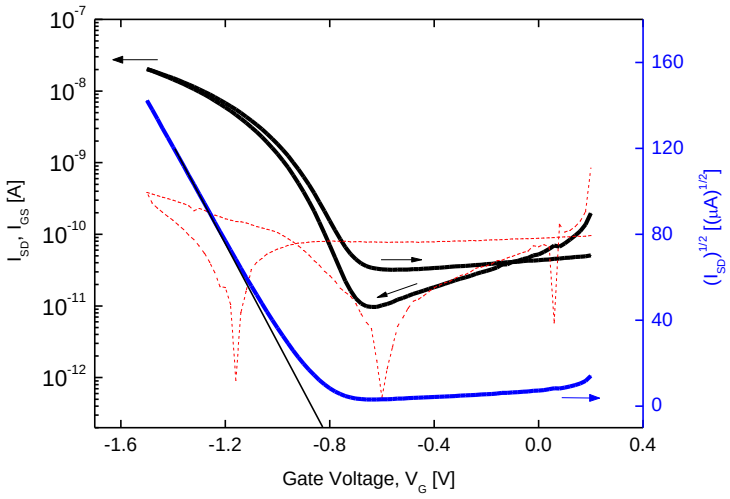
Table 4.9: Surface and dielectric properties of BZ-P(VDF-HFP) nanocomposite layers.

Secondly, in accordance with speculations made in section 3-1-6 and observations on AFM images in Fig. 4.7, uncapped and capped BZ nanocomposite films exhibit greater surface roughness than their BST counterparts. This effect is accredited to smaller dimensions (and higher surface-to-volume ratio) of BZ nanoparticles and their higher degree of packing, greater tendency to aggregate and formation of thicker and rougher films. In comparison with data in Table 4.7, uncoated, BZ nanocomposites exhibit higher dielectric constant than BST nanocomposites. However, since surface roughness and film thickness of BZ nanocomposite film are greater, their C_i is smaller than that of BST nanocomposites.

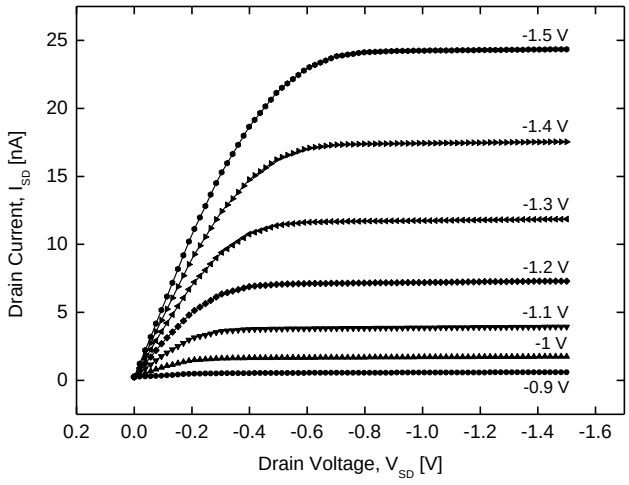
One other key observation is a 60 % drop in *k* for BZ nanocomposite dielectric layers once capped with PVP compared to only a 16 % reduction in the case of BST nanocomposites. Ultrathin PVP layer is believed to have mostly coated smaller BZ nanoparticles, while larger aggregates scattered randomly on the surface has only contributed to higher RMS roughness rather than higher *k*. Once nanocomposite dielectric layers were characterised, TFTs using solution-processed, TIPS-pentacene/PαMS semiconductor blend were fabricated.

Transfer and output characteristics of such TFTs are demonstrated in Fig. 4. 26. Standard transfer characteristics with clear “on” and “off” states and sharp linear and well-saturated regime in output characteristics are demonstrated. Leakage current density is also reasonably low (by at least one order of magnitude than “on” current). However, in comparison with characteristics presented in Fig. 4.21, OTFTs with BZ nanocomposite

bilayer dielectrics switched on at higher threshold voltages (V_T = -0.85 V) and thus could not be successfully operational below -1 V. Moreover, transfer characteristics of such TFTs manifest higher hysteresis (as a result of higher dielectric surface roughness and increased traps density at the interface) and lower "on" current, while relatively lower drain current (almost twice) and higher pinch-off point (output characteristics), in contrast to TFTs with BST nanocomposite dielectric.



(a)



(b)

Fig. 4.26: (a) Transfer and leakage current and (b) output characteristic of TIPS-pentacene/PαMS OTFTs using BZ-P(VDF-HFP) nanocomposite bilayer gate dielectric, V_{SD} = -1.5 V, channel width (W) = 2000 µm and channel length (L) = 50 µm.

Figures of merit measured on such TFTs derived from transfer characteristics (Fig. 4.26) are recorded in the Table 4.10. Although a higher V_T is measured (and higher operational voltages), almost comparable carrier mobility, subthreshold swing and on/off ratio is obtained on TFTs using BZ- and BST-nanocomposite bilayer gate dielectrics.

Semiconductor	**μ** **cm^2/Vs**	**V_T** **V**	**SS** **mV/dec**	**On/Off ratio**
TIPS-Pentacene/PαMS	8×10^{-2}	-0.85	153	10^3

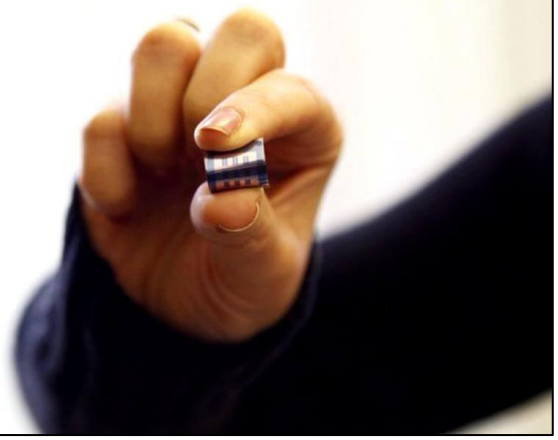
Table 4.10: Figures of merit calculated on TFTs with BZ-P(VDF-HFP) nanocomposite bilayer gate dielectric using TIPS-pentacene/PαMS blend

Nevertheless, although further investigations are required, BST-P(VDF-HFP) nanocomposite bilayers are provisionally considered as a better choice of gate dielectric in high performance, low-voltage OTFTs (particularly at or below -1 V) compared to their BZ counterparts.

4-2-3-3- Ultralow-Voltage OTFTs on Plastic Substrates

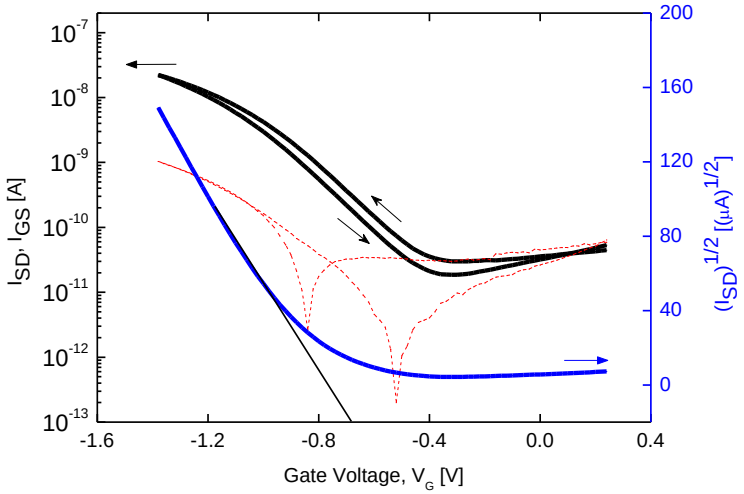
In addition to rigid substrates (e.g. glass), a few trials on ultralow-voltage OTFTs on flexible polyethylene terephthalate (PET) substrates using high-*k* nanocomposite bilayer gate dielectrics were successfully attempted in this work (Fig. 4.27). Mechanical flexibility is a key advantage that organic electronic devices have over their conventional inorganic counterparts. Organic materials intrinsically have mechanical flexibility due to van der Waals bonding between organic molecules, making ultra-flexible organic devices feasible [203]. In particular, low-voltage, solution-processed OTFTs on flexible substrate are promising candidates for low-cost, disposable electronics.

Fig. 4.27: Demonstration of an OTFT on PET flexible substrate.

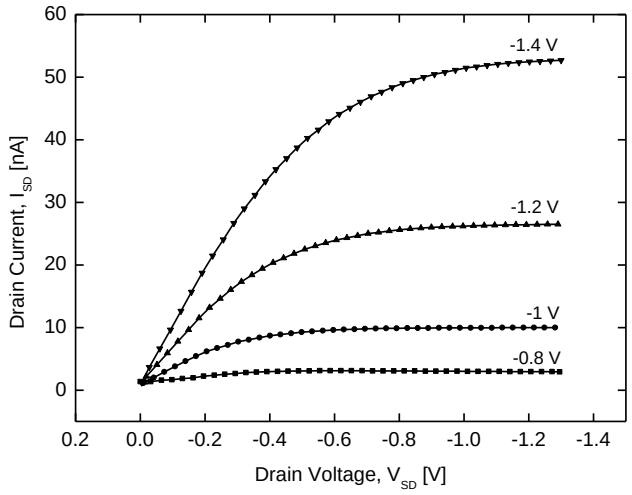


To evaluate the impact of using PET substrates on device performance, OTFTs using both BST- and BZ-P(VDF-HFP) nanocomposite gate dielectrics have been fabricated and evaluated. The procedure of fabricating such devices is identical to that already described in section 3-2-2. In addition, PET substrates had to be secured on a glass substrate to avoid curling up during evaporation of electrodes.

Due to inevitable time constraints and material shortage, for each OTFT (using either of the nanocomposite bilayer dielectric), only one type of semiconductor has been attempted.



(a)



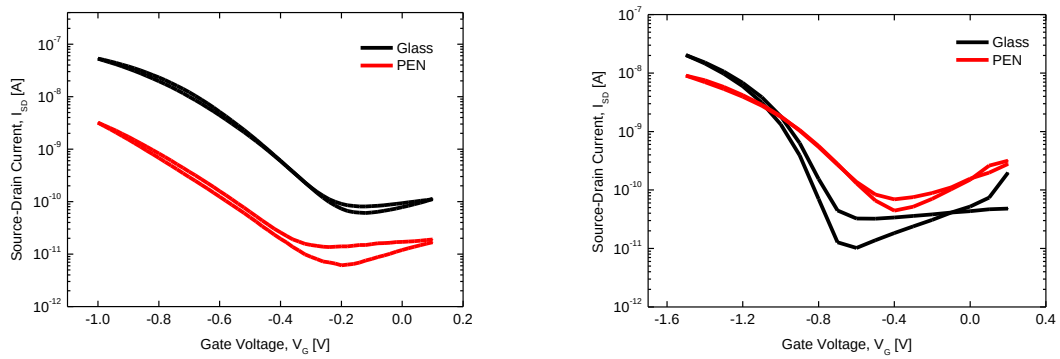
(b)

Fig. 4.28: (a) Transfer characteristics including leakage current and (b) output characteristic of a PDPPTT OTFT fabricated on PET using PVP-capped BST-P(VDF-HFP) gate dielectric layer, V_{SD} = -1.4 V, channel width (W) = 2000 µm and channel length (L) = 80 µm.

Strictly speaking, solution-processed PDPPTT and TIPS-pentacene/PαMS semiconductors have been used on OTFTs with BST- and BZ-P(VSF-HFP) nanocomposite gate dielectrics respectively. Nevertheless, the outcome of the experiments was sufficient enough to allow effective comparison between corresponding devices made on glass and PET.

Transfer and output characteristics of PDPPTT OTFTs using BST-P(VDF-HFP) gate dielectrics fabricated on PET substrate are presented in Fig. 4.28. Clear "on" and "off" states and relatively high drain current at -1.4 V are evident. Steep and saturated output characteristics with relatively high I_{SD} in $|V_{SD}| > |V_G - V_T|$ regime are satisfactorily achieved. Moreover, marginally higher leakage current and increased hysteresis compared to that for OTFTs on glass (Fig. 4.20) were measured, due to likelihood of damage incurred during sample handling and/or measurement.

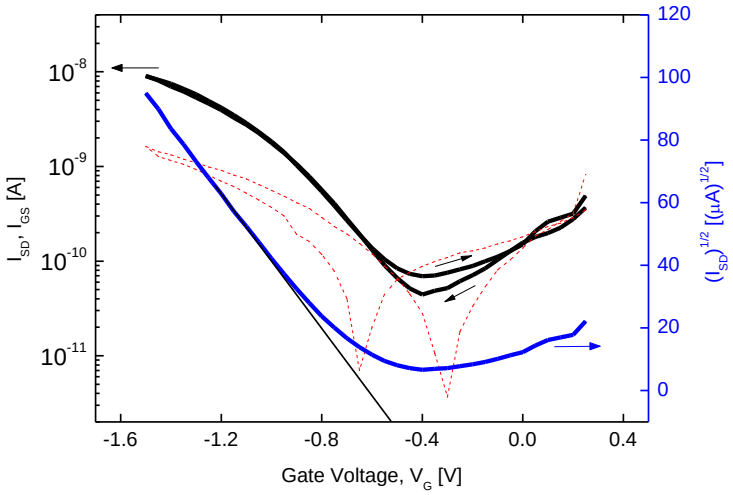
As can be observed in Fig. 4.26, such OTFTs had to be operated at slightly higher voltage (due to higher V_T) to obtain figures of merit nearly comparable to those fabricated on glass. Nonetheless, to allow comparison on similar basis, transfer characteristics of PDPPTT OTFTs fabricated on glass and PET measured at V_{SD} = -1 V are collectively depicted in Fig. 4.29 (a). Lower I_{SD} (about one order of magnitude) is measured on OTFTs made on PET compared to those on glass. A slight shift in V_T is also observable.



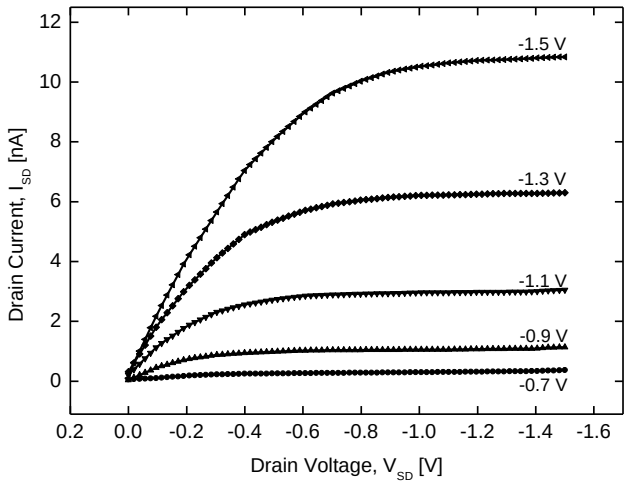
(a) (b)

Fig. 4.29: Comparison between transfer characteristics of (a) PDPPTT OTFTs with BST-P(VDF-HFP) gate dielectric and (b) TIPS-pentacene/PαMS OTFTs using BZ-P(VDF-HFP) gate dielectric fabricated on glass and PET substrates.

Device characteristics measured on TIPS-pentacene/PαMS OTFTs using BZ-P(VDF-HFP) nanocomposite gate dielectric are demonstrated in Fig. 4.30. Promising device performance at low operating voltages (-1.5 V), almost analogous to that measured on the corresponding devices on glass, is recorded here. Clear transition from "off" to "on" state with nearly no hysteresis and relatively low leakage current is achieved on such devices. However, in comparison with Fig. 4.26 (a), larger leakage current is measured on OTFTs made on PET (Fig. 4.30).



(a)



(b)

Fig. 4.30: (a) Transfer characteristics and (b) output characteristic of a TIPS-Pentacene/PαMS OTFT fabricated on PET using PVP-capped BZ-P(VDF-HFP) dielectric layer, V_{SD} = -1.5 V, channel width (W) = 2000 µm and channel length (L) = 60 µm.

As already mentioned, OTFTs with BZ-P(VDF-HFP) dielectric were not capable of being successfully operated at/below -1 V. Similar behaviour is also observed on devices made on flexible substrates. Satisfactory output characteristics have been measured on these devices, although the output drain current was lower (almost twice) than that shown in Fig. 4.26 (b) for those fabricated on glass.

The comparative figure illustrating transfer characteristics measured on BZ-P(VDF-HFP)-based OTFTs on glass and PET substrates is shown in Fig. 4.29 (b). Unlike Fig. 4.29 (a), a completely different behaviour is observed between these devices compared to their BST-P(VDF-HFP)-based counterparts. To allow quantitative analysis, figures of merit measured on each device are recorded in Table 4.11. As expected, better device performance is measured on OTFTs using BST-based nanocomposite dielectric layers, although PDPPTT used in these devices is a higher-mobility semiconductor compared to TIPS-pentacene/PαMS.

Semiconductor	**Gate dielectric**	**V_{SD} V**	**μ cm^2/Vs**	**V_T V**	**SS mV/dec**	**On/Off ratio**
PDPPTT	BST-P(VDF-HFP)	-1.4	9.5×10^{-2}	-0.8	287	10^3
		-1	5×10^{-2}	-0.7	277	6×10^2
TIPS-pentacene/PαMS	BZ-P(VDF-HFP)	-1.5	1.6×10^{-2}	-0.6	385	2×10^2

Table 4.11: Figures of merit calculated on OTFTs fabricated on PET substrates.

Comparing data in Table 4.11 and Table 4.8 and 4.10, relatively better characteristics, including lower V_T and subthreshold swing in particular, are achieved on OTFTs fabricated on glass due to firmer substrate and easier fabrication and measurement. Nonetheless, these results cannot be considered conclusive until more comprehensive experiments are carried out using PET substrates (see chapter 5 on conclusions and future work).

Chapter 5

Conclusions

This work has addressed the emerging need for alternative high-*k* dielectric materials for low-voltage OTFTs. The low-voltage operation is critical to performance of various organic electronic devices, including disposable, aqueous sensors and wearable and portable electronics. As discussed, nanocomposite materials are considered the most promising choice of dielectrics as they combine the high dielectric constant of ceramic metal oxide nanoparticles with high breakdown strength, mechanical flexibility, and easy processability of the organic polymers. Moreover, mechanical flexibility and tunable properties of ceramic/polymer nanocomposites make them unrivalled in high performance, low-voltage organic electronic devices.

Herein, formulation of two different types of nanocomposite materials by incorporation of high-*k* perovskite nanoparticles in low- and high-*k* polymer matrices is reported. The primary objective was to prepare high-quality, well-dispersed nanocomposite suspensions from which uniform thin layers with excellent dielectric properties can be deposited and subsequently integrated into OTFTs. PVP with added cross-linker and P(VDF-HFP) were utilised in this work as the choices of low- and high-*k* polymer host respectively. Surface modification techniques were adopted to assist better dispersion and stability of nanoparticles inside the PVP-based nanocomposite suspension.

Numerous experiments were conducted to find the best polymer concentration, nanoparticle wt % loading, SAM coupling agent and surface modification and nanocomposite preparation approach. Homogeneous suspensions of PVP-based nanocomposites with surface-modified nanoparticles were prepared and spin-coated to serve as dielectric layers in parallel-plate capacitors and OTFTs. The dielectric constant was improved from 3.76 ± 0.20 for pristine PVP to 6.17 ± 0.20 for nanocomposites with 11 wt % OPA-modified BZ nanoparticles. The best nanoparticle concentration was determined to be 11 wt %. TIPS-pentacene/PαMS OTFTs with satisfactory device characteristics (operational below 20 V) were demonstrated using 11 wt % OPA-BZ and HMDS-BST nanocomposites.

In hopes of envisaging dielectric materials with notably higher *k* which would enable a lowering of the operation voltage down to a few volts, novel, nanocomposites using a high-*k* fluorinated P(VDF-HFP) copolymer host were prepared. Since such nanocomposites were the first of their kind, a large number of experiments were undertaken not only to formulate the suspensions but also to form thin dielectric layers compatible with the OTFTs' structure and choice of materials. Since PVP-based nanocomposites using BST and BZ nanoparticles exhibited relatively better device performance, only these two nanoparticles were used as fillers in P(VDF-HFP)-based nanocomposites. It was found that using the correct combination of fluorinated copolymers, solvents and nanoparticles-to-polymer volume ratio, a reproducible, uniform nanocomposite suspension could be made without the need for nanoparticles surface modification. A high dielectric constant of 20.0 ± 0.5 was measured on 11 wt % BST loading. This corresponded to an increase of more than twice that of the pristine P(VDF-HFP).

Increased surface roughness and low surface energy of P(VDF-HFP)-based nanocomposites, both of which factors scale up as nanoparticle wt % loading increases, necessitated a capping layer to improve the dielectric-semiconductor interface in OTFTs. Surfaces of all the nanocomposite dielectric layers were (partially) capped with an ultrathin, cross-linked PVP layer. Despite an inevitable reduction in capacitance and dielectric constant, improved surface roughness, leakage current, device processability and OTFTs characteristics were achieved using (PVDF-HFP)-based nanocomposite dielectric capped with PVP. Hence, we concluded that a capping layer is essential when using nanocomposite dielectrics based on high-*k* fluorinated polymers. The key to superior device performance is the partial rather than full coverage of the nanocomposite surface with an ultrathin PVP. Otherwise the capping layer would act as the main dielectric layer by counteracting the effect of high-*k* nanocomposites. Implementing these high-capacitance bilayer dielectric layers in OTFTs resulted in substantially lowered operating voltages down to - 1.5 V and -1 V for BZ- and BST-based gate dielectrics respectively. The compatibility and versatility of the novel, high-*k* bilayer dielectric layer with a variety of vacuum-deposited and solution-processed p-type semiconducting materials were verified. It appears that using the developed nanocomposite bilayer dielectric, both high-capacitance and low-operational voltage objectives can be achieved. It is hypothesised that such partial coverage provides areas of smooth, pinhole-free PVP-semiconductor interface facilitating the charge carrier transport, while enables realisation of high-capacitance

regions where rough areas of the (uncapped) nanocomposite across the dielectric surface exist. Nonetheless, investigation into the exact mechanism of charge transport in OTFTs using such bilayer nanocomposite dielectric layers was out of the scope of this project. In the following subsection, potential future work with particular outlook on low-voltage OTFTs is discussed.

5-1- Future Work

Investigation into the possibility of employing top- or bottom-contact OTFTs using the developed high-*k* nanocomposite dielectric layer in aqueous sensing applications is considered as one of the most immediate future work. Moreover, attempt to fabricate low-voltage (< 3 V), top-gate OTFTs using nanocomposite gate dielectrics is highly recommendable. Throughout this work, bottom-gated OTFTs with top- and bottom-contact configuration have been fabricated. However, it is vital to demonstrate compatibility of the developed nanocomposite gate dielectric with all possible device structures, in particular from the commercial point of view. Nonetheless, the main challenge in realisation of solution-processed, top-gate transistors is avoiding the potential mixing of the active layer at the bottom and the nanocomposite dielectric on the top. One possible solution would be to introduce an intermediate layer in between or use orthogonal solvents for deposition of the layers. As aforementioned, further work to shed light on and justify the impact of partially-capped nanocomposite dielectric layer on device performance is also required.

5-1-1-Low-voltage OTFTs using N-type Semiconductors

In order to draw a final conclusion on the versatility of our high-*k* nanocomposite (bilayer) dielectric, OTFTs using n-type semiconductor have to be also fabricated and characterised at low voltages. More importantly, complementary circuits, such as complementary metal-oxide-semiconductor (CMOS) inverters, could be realised using p-type and n-type OTFTs. As the final stage of this work, the n-type poly{[*N*,*N*′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)} (P(NDI2OD-T2), Polyera ActivInk™ N2200) was purchased and attempted in bottom-gate, bottom-contact OTFTs using a bilayer nanocomposite as the gate dielectric. P(NDI2OD-T2) is reported as a high mobility (> 0.1 cm^2/Vs) electron transporting polymer which has also been used in low-

voltage OTFTs [33, 202]. As speculated, substituting an n-type for a p-type semiconductor is not a straightforward task. During our trial experiments, we experienced great difficulty in spin-coating P(NDI2OD-T2) onto the nanocomposite bilayer dielectric and thus no successfully operational devices were obtained. In addition, devices exhibited characteristics indicating possible doping of the semiconductor during deposition and/or measurement. Unfortunately, due to time constraints, fabrication of OTFTs using n-type semiconductors had to be dropped.

5-1-2- High-*k* Nanocomposites Using Surface Modified Nanoparticles in P(VDF-HFP)

As justified in this work, no surface modification of nanoparticles is necessary to formulate homogenous, well-dispersed P(VDF-HFP)-based nanocomposite suspensions. However, it is worth investigating how incorporation of surface-modified nanoparticles into P(VDF-HFP) would affect dielectric properties of the nanocomposite layer and device characteristics of the corresponding OTFTs. In addition, it is worth attempting to make P(VDF-HFP)-based nanocomposites using the other remaining nanoparticles (i.e. CT and CZ) with and without surface modification and compare the devices' performance to those using BST and BZ. Moreover, other choices of high-*k* polymer matrices, such as other PVDF copolymers, CYELP, etc., can be tried.

5-1-3- Printed and Bendable OTFTs

Fabrication of low-voltage OTFTs on flexible substrates (PEN) has been briefly attempted in this work. Despite achieving device performance nearly as good as those made on rigid (glass) substrates, devices were measured in the flat (normal) status, without imposing any bending to the sample. In order to investigate the extent of device flexibility and reliability, its figures of merit in deformed status have to be measured for various radiuses of (inward/outward) curvature. Finally, as printing is the emerging technology to fabricate large-scale, roll-to-roll electronic components, it would be greatly advantageous to explore the possibility of mass producing low-voltage OTFTs using printed high-*k* nanocomposite gate dielectric. Moreover, by employing inkjet-printing, the need to pattern the dielectric layer is dismissed.

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Appendix A: Solution-processing of P(VDF-HFP) from different solvents

The rate of P(VDF-HFP) polymer dissolution in various solvents attempted in this work are summarised in Table Apx.A1. Difficulty in solution-processing of the semiconductor layer atop highly polar dielectric layers (in BGBC and BGTC configurations) necessitated striving to dissolve P(VDF-HFP) in a number of different solvents to improve compatibility between the dielectric and semiconductor layers. PGMEA solvent would have been preferred, since it was already approved as a suitable solvent to process PVP layers from and compatible with the subsequent semiconductor layer. Nonetheless, based on Table Apx.A1, DMF was chosen as the best solvent to process P(VDF-HFP) from. 5 wt % P(VDF-HFP) was completely dissolved in DMF following a 60-minute stirring at room temperature. Layers of P(VDF-HFP) in DMF were successfully spin-coated, annealed and subsequently coated with an ultrathin layer of PVP in PGMEA.

	PGMEA	**MEK***	**DMF**	**DMF:PGMEA 70:30**	**DMF:PGMEA 90:10**
Dissolution rate (%)	10	80	100	60	70

*** methyl ethyl ketone**

Table Apx.A1: Dissolution rate of P(VDF-HFP) polymer in various solvents.

Appendix B: A Summary of Attempted Devices using PVP-based Gate Dielectrics

In this appendix, all capacitors and TFTs attempted in this project using PVP-based dielectric layers are quantitatively and qualitatively classified. Table Apx.B1 is a colour-coded overview of quantity and performance of devices fabricated (and tested) using pristine PVP and its nanocomposites as the gate dielectrics. Nanocomposite dielectrics with both non-modified and modified nanoparticles were attempted, although majority of OTFTs using the former operated poorly. All the OTFTs made with ODPA-CZ nanocomposite dielectric are highlighted as unsuccessful indicating highly leaky or short-circuited characteristics. Since these sets of experiments were carried out during the second year of this project when only TIPS-Pentacene and its blend with PαMS were readily available, only the corresponding OTFTs were inevitably fabricated. Better device performance was obtained using the semiconductor blend (see Table 4.5); hence, not many OTFTs were attempted using the pristine TIPS-Pentacene.

Dielectric layer	**PVP**			**BST***			**CZ***			**OPA-BZ**			**OPA-CZ**			**ODPA-CZ**			**OPA-BST**			**OPA-CT**			**HMDS-BST**		
Parallel-plate Capacitors	8	6	2	2	5	3	3	4	3	10		2	10		2	10		2	6	8		6	8		10		2
OTFTs (TIPS-Pentacene)	5	5	2	1		1	1		1	3	2	1	1	3		4			2	2		2	2		3	1	2
OTFTs (TIPS-Pentacene/ PαMS)	9	8	1	4		2	4		2	7	5	2	3	3	2	6			5	4	3	2	5	3	7	4	1

*Non-modified

Very good Good Average Poor Unsuccessful

Table Apx.B1: Total number and extent of device performance of PVP-based capacitors and OTFTs attempted in this work.

The figures of merit for TIPS-Pentacene OTFTs are presented in Table Apx.B2. In conformity with data collected in Table 4.5, OTFTs using OPA-BZ and HMDS-BST nanocomposite dielectrics exhibited the best device characteristics (e.g. high mobility and On/OFF ratio), while those with pristine PVP and OPA-CZ nanocomposite as their gate dielectrics suffered from poor performance. Nonetheless, devices with TIPS-Pentacene active layer have demonstrated relatively inferior performance compared to those using the semiconductor blend. The presence of the (Top and bottom) PαMS buffer layers sandwiching the TIPS-Pentacene layer in between, in the case of using the semiconductor blend, would improve the morphology of the semiconductor layer (crystals), the semiconductor-insulator interface and the charge transport occurring along that interface.

Gate dielectric		**C_i** **nF/cm^2**	**μ** **cm^2 /Vs**	**V_T** **V**	**SS** **mV/dec**	**ON/OFF ratio**
PVP		6.87	5.11×10^{-3}	0.84	717	10^4
Nanocomposite	OPA-BZ	9.34	3.52×10^{-2}	0.61	575	10^5
	HMDS-BST	10.24	3.72×10^{-2}	1.49	822	10^4
	OPA-BST	9.15	6.28×10^{-3}	1.88	1004	10^3
	OPA-CT	7.72	5.35×10^{-3}	1.22	900	10^4

Table Apx.B2: Summarised device characteristics of TIPS-Pentacene OTFTs with different types of gate dielectrics.

Appendix C: A Comparative Overview of OTFTs Fabricated Using P(VDF-HFP)-based Gate Dielectrics

The scope of operational devices (OTFTs) fabricated (and tested) throughout this project using P(VDF-HFP)-based gate dielectrics is summarised in this appendix. Colour coding system (similar to Appendix B) is adopted to allow differentiation of device performance based on various scenarios (e.g. device configuration, semiconducting material, etc.). Table Apx.C1 illustrates the overall performance outcome of OTFTs fabricated throughout the course of this project with respect to the choice of the semiconductor and the deposition technique. A detailed breakdown of the number of OTFTs attempted and tested in this work, in particular those with BST- and BZ-P(VDF-HFP) nanocomposite dielectric bilayers, are included in Table Apx.C2 and Apx.C3 respectively.

			TIPS-Pentacene		**TIPS-Pentacene/ PαMS**		**PBTTT (Spin-cast)**		**PDPPTT (Spin-cast)**			**DNTT**		**IF-PTAA**
			Spin-cast	Drop-cast	Spin-cast	Drop-cast	Pristine	PBTTT/ PαMS	1 wt %	0.7 wt %	0.5 wt %	Spin-cast	Evaporated	Spin-cast
Glass	BGBC	Non-modified contacts												
		Modified contacts												
	BGTC		N/A	N/A										
	TGBC		N/A	N/A		N/A	N/A	N/A				N/A	N/A	N/A
PET	BGBC	Non-modified contacts	N/A	N/A		N/A	N/A	N/A	N/A	N/A		N/A	N/A	N/A
		Modified contacts	N/A	N/A		N/A	N/A	N/A				N/A	N/A	N/A
	BGTC		N/A	N/A		N/A	N/A	N/A	N/A	N/A		N/A	N/A	N/A

Table Apx.C1: Colour-coded performance presentation of all OTFTs attempted in this work using P(VDF-HFP)-based gate dielectrics.

	TIPS-Pentacene		TIPS-Pentacene/ PαMS		PBTTT (Spin-cast)		PDPPTT (Spin-cast)				DNTT		IF-PTAA
	Spin-cast	Drop-cast	Spin-cast	Drop-cast	Pristine	PBTTT/ PαMS	1 wt %	0.7 wt %	0.5 wt %		Spin-cast	Evaporated	Spin-cast
									Glass	PET			
Very good	2	4	25	8	-	-	4	7	15	3	-	2	-
Good	22	25	11	6	-	2	3	4	8	7	-	2	-
Average	6	7	2	-	-	4	2	2	2	4	-	1	-
Poor	-	-	-	-	3	2	-	-	1	-	-	3	3
Unsuccessful	-	-	2*	-	1	-	1*	1*	-	-	6	-	3
Total	30	36	40	14	4	8	10	14	26	14	6	8	6

***TGBC configuration**

Table Apx.C2: Quantitative and qualitative representation of all BST-P(VDF-HFP)-based OTFTs fabricated in this project.

	TIPS-Pentacene/ PαMS (Spin-cast)	
	Glass	PET
Very good	12	2
Good	9	6
Average	1	2
Poor	-	-
Total	22	10

Table Apx.C3: Quantitative representation of BZ-P(VDF-HFP)-based OTFTs fabricated in this project.

Appendix D: Effect of solvent on performance of TIPS-Pentacene/PαMS OTFTs

This appendix illustrates the effect of various solvents from which the semiconductor is processed from on the overall performance of the end device. Device characteristics of TIPS-Pentacene/PαMS OTFTs (using cross-linked PVP as the dielectric layer) with respect to the choice of solvents are presented in Table Apx.D1. The best performing OTFT was achieved by solution-processing the semiconductor from DCB. The boiling point of DCB in comparison to the other solvents played a key role in formation (i.e. packing) of the crystals in the semiconductor films. These results were applicable to some other semiconductors tried in this work, such as PDPPTT.

Solvent	Chlorobenzene (CB)	1,2-dichlorobenzene (DCB)	Trichlorobenzene (TCB)	Toluene
Boiling point (°C)	131	180	214.4	110.6
μ (cm^2/Vs)	9.5×10^{-3}	2.1×10^{-2}	1.9×10^{-3}	2.5×10^{-3}
On/Off ratio	10^3	10^4	10^3	10^4
V_T (V)	-4.23	-3.11	0.22	-0.94

Table Apx.D1: TIPS-Pentacene/PαMS OTFTs' characteristics.

Appendix E: Optimisation of PBTTT OTFTs with BST-P(VDF-HFP) Nanocomposite Bilayer Gate Dielectric

In an attempt to fabricate OTFTs using PBTTT semiconductor, unsatisfactory results were obtained. As shown in Fig. Apx.E1, devices suffer from extreme leakage and the poor transfer characteristic implies possible doping of the semiconductor. PBTTT is a highly polycrystalline semiconductor which should be deposited from hot solution and handled and measured under N_2 condition, otherwise it easily get doped in air.

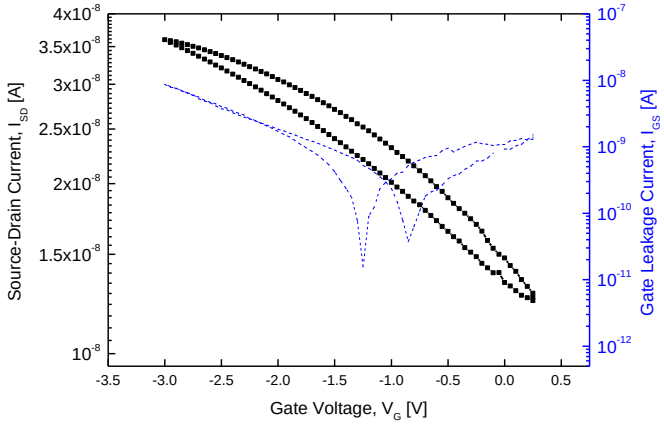

Fig. Apx.E1: Transfer characteristic of PBTTT OTFTs, V_{SD} = -3 V.

In order to tackle this problem, using a blend of PBTTT with a polymer such as PMMA or PαMS was suggested. It was speculated that possible phase separation of the blend would minimise the effect of polycrystallinity at the dielectric-semiconductor interface, reduce leakage current and enable the device to successfully operate.

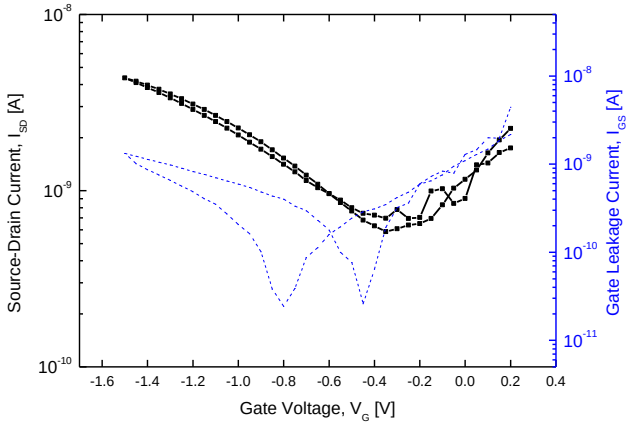

Fig. Apx.E2: Transfer characteristic of PBTTT OTFTs, V_{SD}= -1.5 V.

As it is demonstrated in Fig. Apx.E2, using a 7:3 PBTTT/PMMA blend resulted in slightly reduced leakage current and noticeably better device performance, i.e. clear 'on' and 'off' state at V_{SD}= -1.5 V. Since using a semiconductor blend led to improved device characteristics, one stop forward was taken to replace PMMA with PαMS. PαMS is a lower molecular weight polymer and hence it was expected to form a thinner layer at the interface upon phase separation of the blend. As a result, not only a better interface would be formed and leakage current would be reduced, but also OTFTs would be operated at slightly lower voltages. Fig. 4.22 illustrates characteristics of a PBTTT/PαMS OTFT successfully operated at -1 V yielding reasonable figures of merits.

Despite achieving an operational device with fairly reasonable characteristics, PBTTT might not be considered as a suitable semiconducting material for these specific OTFTs with high-*k* nanocomposite dielectrics. However, various factors might have affected the device performance such as fabrication and measurement of device in air rather than under N_2 condition (due to lack of appropriate laboratory facilities), and speculation of the likelihood of poor quality material obtained from the supplier. Hence a definite conclusion cannot be drawn, unless further investigations are carried out.