

This paper is a post print of a paper submitted to and accepted for publication in Electronics Letters and is subject to Institution of Engineering and Technology Copyright. The copy of record is available at IET Digital Library

<http://dx.doi.org/10.1049/el.2013.2838>

DOI 10.1049/el.2013.2838

# A NanoWatt multi-scale Continuous Wavelet Transform chip

Alexander J. Casson and Esther Rodriguez-Villegas

This letter presents a four scale Continuous Wavelet Transform filter bank implemented in a 0.18  $\mu\text{m}$  CMOS process. Experimental results demonstrate the real-time multi-scale analysis of ECG signals with a power consumption of 1.3 nW, the lowest reported power consumption for a complete wavelet filter bank. In addition the results demonstrate for the first time the use of pico-Amp scale currents in a 0.18  $\mu\text{m}$  CMOS process for providing advanced signal processing functions.

**Introduction:** The Continuous Wavelet Transform (CWT) is a hugely important signal processing basis and is widely used for bio-signal analysis [1]. As a result multiple on-chip implementations have been reported for applications in power constrained sensor nodes that include local intelligence algorithms [2]–[5]. The CWT is well suited for these low-power, low-voltage, low-frequency applications as it can be readily mapped to analogue domain filters.

The CWT transform is defined as

$$C(a, b) = \frac{1}{\sqrt{a}} \int_{-\infty}^{\infty} x(t) \psi^* \left( \frac{t-b}{a} \right) dt. \quad (1)$$

where  $x(t)$  is the input signal,  $a$  is the analysis scale and  $b$  is the time at which the transform is taken. (1) can be re-written as the convolution of the signal  $x(t)$  with the impulse response

$$h(t) = \frac{1}{\sqrt{a}} \psi \left( \frac{-t}{a} \right) \quad (2)$$

and hence the CWT at a single scale is carried out by using a filter with impulse response  $h(t)$ . It is found that this corresponds to a bandpass filtering operation where  $\psi(t)$  defines the shape of the frequency response.

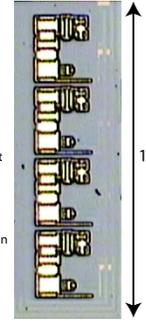
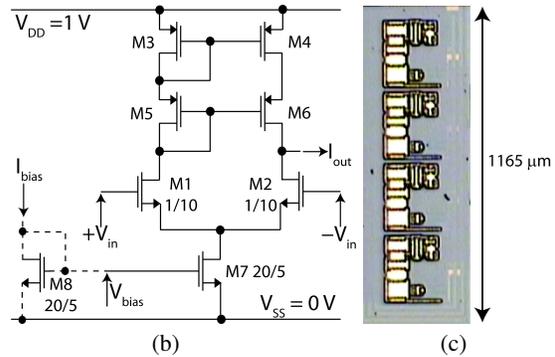
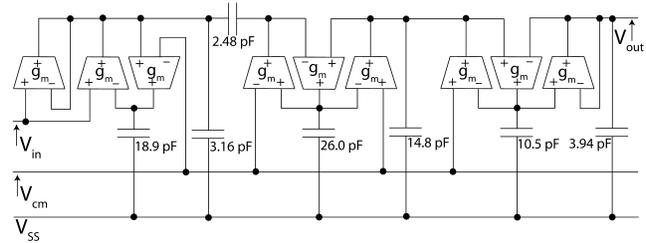
For the low power analysis of bio-signals analogue  $g_m C$  filters are of significant interest as  $g_m C$  filter centre frequencies are proportional to  $g_m/C$  and the power consumption of the transconductors generally proportional to the bias current. Bio-signals, such as the ECG (electrocardiogram) and EEG (electroencephalogram), are commonly in the 0–100 Hz range and thus the use of very low on-chip currents (typically in the single pico-Amp range) simultaneously provides: the low centre-frequencies required for the applications; small capacitance values, minimising the circuit area; and small current values, minimising the power consumption. Using this ultra-low current approach power consumptions for a single scale down to 60 pW have been reported [4].

However, most reported CWT circuits (with the exception of [3]) have only presented experimental results for a single scale at a time, not complete filter banks. In addition, while the use of very low on-chip currents—down to single pico-Amps—for on-chip signal processing has been established at the 0.35  $\mu\text{m}$  process node [4], [6] there are very few reported experimental results using pico-Amp currents in high order systems for signal processing in smaller process nodes. The viability of such small currents in other nodes is therefore not clear and it is not apparent *a priori* whether the ultra-low current approach can be re-applied.

This letter presents experimental results from a four scale CWT circuit designed for the real-time processing of ECG signals. This realises 7<sup>th</sup> order CWT transfer functions (as compared to 2<sup>nd</sup> order in the other reported filter bank implementation [3]) and has a lower power consumption. The circuit is implemented in a 0.18  $\mu\text{m}$  CMOS process and demonstrates that pico-Amp scale processing is feasible in what is currently the most commonly used Europractice process node [7].

**Circuit design:** The CWT filter bank implements four scales of the LPCWT mother wavelet defined in [4]. This is realised using four versions of the  $g_m C$  filter topology shown in Fig. 1(a) and the transconductor in Fig. 1(b) with dyadically scaled bias currents.

To achieve simultaneous low power and low capacitance operation the transconductance in Fig. 1(b) is nominally 190 pS–1.5 nS and based upon using bias currents in the 8–64 pA range. This ultra-low current approach was proposed in [4] and uses simple on-chip transconductors biased at very low currents to provide a superior power trade-off compared to approaches that use higher current values combined with techniques to lower the effective transconductance (see [8] for an introduction to such techniques).



**Fig. 1**  $g_m C$  filter realising the LPCWT mother wavelet. (a) Topology; (b) Transconductor; (c) Micro-photograph of the fabricated circuit.

The transconductor used here incorporates a cascaded load to maintain suitable bandwidth and d.c. operating points as the current is scaled down in the 0.18  $\mu\text{m}$  process.

The main limiting factor in the use of ultra-low on-chip currents is the limited bandwidth of the resulting transconductors. In order to maintain the spread of CWT centre frequencies the transconductor is pre-distorted to optimize the bandwidth available at each analysis scale. Transistors M3–M6 are sized (in microns) as: 1/8.4; 1/4; 1/1.8; 1/0.75 respectively for filter centre frequencies of 2 Hz; 4 Hz; 8 Hz; 16 Hz. Transistor M8 is shared between all of the transconductors in a single filter and the four scale filter bank is formed by repeating the structure of Fig. 1(a) with the appropriate pre-distorted transconductor and an on-chip bias current scaler such that only one external current source is required to set up the entire filter bank.

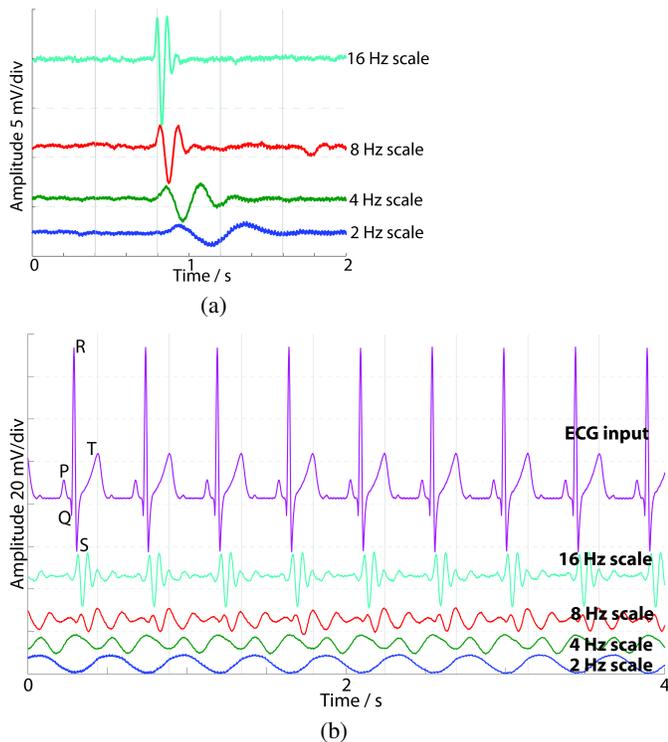
**Experimental results:** The CWT filter bank has been fabricated in a 0.18  $\mu\text{m}$ , triple well, MIM-cap, 6 metal CMOS process, and a micro-photograph of the chip is shown in Fig. 1(c). The CWT filter bank has an area of 0.4 mm<sup>2</sup>.

At nominal operation with a 64 pA bias current four wavelet bandpass filters are provided with centre frequencies at 2, 4, 8 and 16 Hz. The measured impulse responses from these, giving the shapes of the wavelet functions, are shown in Fig. 2(a). These clearly show the LPCWT mother wavelet shape, which resembles the well known Mexican hat with a 180° phase shift. The responses are seen to be scaled in both duration and amplitude to reflect the correct CWT operation at different analysis scales.

The real-time multi-scale analysis of an 100 mV<sub>pp</sub> ECG (electrocardiogram) signal is then shown in Fig. 2(b). The 16 Hz scale has a clear output in response to each QRS complex which can be used to identify the time of each heart beat. Alternatively the 2 Hz scale output is a sinusoid directly at the heart rate frequency. Although less distinct, there are peaks in the 8 Hz scale output (marked with vertical lines) which highlight the times of the T peak in the ECG waveform. The utility of the four scale CWT for bio-signal processing is thus clear.

In the CWT chip the smallest quiescent current present is 4 pA (in one branch of the 2 Hz filter transconductors) and the experimental results demonstrate the ability to use low pico-Amp currents for useful signal processing in the 0.18  $\mu\text{m}$  CMOS process. The use of these low currents allows the entire filter bank to consume only 1.3 nW of power from a 1 V supply.

**Conclusions:** For power constrained sensor nodes that include local intelligence algorithms it is critical to realise advanced signal processing functions with the minimum amount of power. This letter has presented experimental results of a four scale Continuous Wavelet Transform filter



**Fig. 2** Measured operation of the filter bank. (a) Impulse responses showing the LPCWT mother wavelet at multiple scales. (b) Real-time four scale CWT analysis of an ECG signal.

bank for use with ECG processing in such sensor nodes. The filter bank has been implemented in a  $0.18 \mu\text{m}$  CMOS process and demonstrates the practical use of pico-Amp currents for signal processing. The result is a multi-scale CWT chip with a power consumption of only 1.3 nW.

*Acknowledgment:* The research leading to these results has received funding from the European Research Council under the European Community's 7<sup>th</sup> Framework Programme (FP7/2007-2013) / ERC grant agreement no. 239749 and supported in part by the Junior Research Fellowship of Imperial College London.

A. J. Casson and E. Rodriguez-Villegas (*Department of Electrical and Electronic Engineering, Imperial College London, London, UK*)

E-mail: acasson@imperial.ac.uk

## References

- 1 Addison, P.S., Walker, J., and Guido, R. C.: 'Time-frequency analysis of biosignals', *IEEE Eng. Med. Biol. Mag.*, 2009, **28**, (5), pp. 14–29
- 2 Zhao, W., Sun, Y., and He, Y.: 'Minimum component high frequency Gm-C wavelet filters based on maclaurin series and multiple loop feedback', *Electron. Lett.*, 2010, **46**, (1), pp. 34–36
- 3 Gurrola-Navarro, M.A., and Espinosa-Flores-Verdad, G.: 'Analogue wavelet transform with single biquad stage per scale', *Electron. Lett.*, 2010, **46**, (9), pp. 616–618
- 4 Casson, A.J., and Rodriguez-Villegas, E.: 'A 60 pW  $g_m C$  Continuous Wavelet Transform circuit for portable EEG systems', *IEEE J. Solid-State Circuits*, 2011, **46**, (6), pp. 1406–1415
- 5 Karel, J.M.H., Haddad, S.A.P., Hiseni, S., Westra, R.L., Serdijn, W.A., and Peeters, R.L.M.: 'Implementing wavelets in continuous-time analog circuits with dynamic range optimization', *IEEE Trans. Circuits Syst. I*, 2012, **59**, (2), pp. 229–242
- 6 Linares-Barranco, B., and Serrano-Gotarredona, T.: 'On the design and characterization of femtoampere current-mode circuits', *IEEE J. Solid-State Circuits*, 2003, **38**, (8), pp. 1353–1363
- 7 Europractice IC service, 'Activity report 2012', 2012, <http://www.europractice-ic.com/>.
- 8 Veeravalli, A., Sanchez-Sinencio, E., and Silva-Martinez, J.: 'Transconductance amplifier structures with very small transconductances: a comparative design approach', *IEEE J. Solid-State Circuits*, 2002, **37**, (6), pp. 770–775