NONLINEAR NANOELECTRONIC DEVICES OPERATING AT ROOM TEMPERATURE

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List of abbreviations

2DEG	Two-dimensional electron gas
3D	Three-dimensional
AC	Alternating current
ADC	Analog-to-digital convertor
AFM	Atomic-force microscopy
AlAs	Aluminium arsenide
AlGaAs	Aluminium gallium arsenide
BN	Boron nitride
CMOS	Complementary MOSFET
CNT	Carbon nanotube
CPW	Coplanar waveguide
CVD	Chemical vapor deposition
CW	Continuous wave
DC	Direct current
DFT	Discrete Fourier transform
E-beam	Electron-beam
EBL	Electron-beam lithography
FET	Field-effect transistor
GaAs	Gallium arsenide
GFET	Graphene field-effect transistor
GNR	Graphene nanoribbon
G-R	Generation-recombination
G-S-G	Ground-source-ground
hBN	Hexagonal boron nitrite
HBT	Heterojunction bipolar transistor
HEMT	High-electron-mobility transistor
HMDS	Hexamethyledisilzane
IC	Integrated circuit
InAs	Indium arsenide
InGaAs	Indium gallium arsenide

InP	Indium phosphide
IPA	Isopropyl alcohol
ISM	Industrial scientific and medical
ITRS	International technology roadmap for semiconductors
JFET	Junction field-effect transistor
MBE	Molecular-beam epitaxy
MC	Monte Carlo
mHEMT	Metamorphic-high-electron-mobility transistor
MIBK	Methyl isobutyl ketone
MOCVD	Metal organic chemical vapour deposition
MODFET	Modulation-doped field-effect transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
MOST	Metal-oxide semiconductor transistor
MtM	More-than-Moore
NEP	Noise equivalent power
NIL	Nanoimprint lithography
NTRS	National technology roadmap for semiconductors
pHEMT	Pseudomorphic-high-electron-mobility transistor
PMMA	Polymethyl methacrylate
PSD	Power spectral density
QCL	Quantum cascaded laser
QED	Quantum electrodynamics
R&D	Research and development
RF	Radio frequency
RFID	Radio frequency identification
RMS	Root-mean-square
RTD	Resonant tunnelling diode
SBD	Schottky barrier diode
SEM	Scanning electron microscope
SET	Single electron transistor
SGT	Side gate transistor
SIA	Semiconductor industry association
Si	Silicon

SiC	Silicon carbide
SiO_2	Silicon dioxide
SiP	System-in-package
SOC	System-on-chip
SOI	Silicon-on-insulator
SSD	Self-switching device
TBJ	Three terminal junction
THz	Terahertz
UHF	Ultra high frequency
UTC-PD	Uni-travelling-carrier photodiode

Abstract

Innovative nanoelectronic device concepts that are beyond the scaling limits of silicon technology can have applications in future generation computations and communications, medical and security imaging, radio astronomy, etc. In particular, these devices may achieve a very high speed well beyond those of the conventional semiconductor devices. A variety of novel devices have recently been proposed including the ballistic rectifier and self-switching device (SSD). Compared with conventional rectifying diodes, both devices are based on entirely new working principles since they do not require any *p-n* junction or barrier structures. As a result, zero threshold voltage can be achieved, eliminating the need for a bias circuit. The planar nature of these devices means that the electrodes are placed side by side rather than on top of each other, which greatly reduces the parasitic capacitance and enables THz (1 THz = 1,000 GHz) speeds at room temperature. Despite previous work on the novel device working principles and high-speed operation, the devices have only been fabricated using conventional semiconductors. Furthermore, the research on their noise properties is so far very limited even though the device noise figures are almost as important as the speed when used as THz detectors.

Manchester is the birthplace of graphene and both novel nanodevices have single-layered architecture, which is ideally-suited to use graphene as the active layer. Since the device speed generally scales with the carrier mobility, graphene based ballistic rectifiers and SSDs are expected to operate at THz frequencies. In this work, both mechanically exfoliated graphene flakes and chemical-vapour deposited graphene films have been used to fabricate the nanodevices for the first time. Their DC and radio-frequency performance have been characterised.

Properties of graphene are strongly influenced by its immediate surroundings including any adsorbed molecules, interaction with the supporting substrate due to its large surface to volume ratio. Here, back-gate voltage induced hysteresis of electrical transport under normal atmospheric conditions is systematically investigated. Time-domain DC measurement and short pulse characterisation technique were employed to develop the understanding of such mechanisms, which will help to improve the stability and the reliability of graphene device properties.

Finally, the noise properties of the ballistic rectifier were studied. Both thermal noise and flicker noise have been characterised. The findings have been discussed in the context of the mobility fluctuation based Hooge's empirical relation. A physical model was also constructed on the noise of a narrow constriction, and the obtained analytical expression may be applicable to a wide range of nanodevices that consist of point-contact-like structures.

University: The University of Manchester Degree: Doctor of Philosophy (PhD)
Candidate's name: Arun Kumar Singh Date: 11 November 2013
Thesis title: Nonlinear nanoelectronic devices operating at room temperature

Declaration

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List of publications

Journals

1. **A. K. Singh**, S.R. Kasjoo, and A. M. Song, "Low-frequency noise of a ballistic rectifier," *IEEE Trans. Nanotechnol.* (Accepted).
2. **A. K. Singh**, G. Auton, E. Hill, and A. M. Song, "Graphene based ballistic rectifiers," *IEEE Electron Device Lett.* (Submitted).
3. **A. K. Singh**, G. Auton, E. Hill, and A. M. Song, "Graphene based self-switching nanodiodes," (Manuscript in preparation).
4. **A. K. Singh,** *et al.*, "Hysteresis of electrical transport in CVD graphene devices," (Manuscript in preparation).
5. **A. K. Singh**, G. Auton, and A. M. Song, "Ballistic rectifier for radio frequency applications," (Manuscript in preparation).

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2. **A. K. Singh**, S. R. Kasjoo, L. Q. Zhang, Y. Alimi, C. Balocco, and A. M. Song, "Novel nanodiodes for terahertz operation," The 2nd IET Annual Active RF Devices, Circuits and Systems meeting, Rutherford Appleton Laboratory, Oxford, UK, September 3, 2012.
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4. S. R. Kasjoo, C. Balocco, X. F. Lu, **A. K. Singh**, L. Q. Zhang, Y. Alimi, and A. M. Song "Low-frequency noise properties in nanodiodes" American Physical Society March Meeting 2012, Boston Massachusetts, USA, February 27 - March 2, 2012.
5. **A. K. Singh**, S. R. Kasjoo, L.Q. Zhang, C. Balocco, and A. M. Song, "Unipolar nanodiodes for ISM band applications," International conference on Nanomaterials and Nanotechnology (ICNANO), Delhi, India, December 18-21, 2011.

Chapter 1

Introduction

1.1 Overview

The invention of the solid-state transistor in 1947 [1] and the integrated circuit (IC) in 1959 [2], has led the astounding developments in semiconductor electronics. The consequences are so profound in our modern lifestyle that the requirement of electronic products is increasing exponentially. Recently, the Semiconductor Industry Association (SIA) announced the largest growth in global sales of semiconductors since March 2011; reaching $25.87 billion in August 2013 with an increase of 6.4% compared to August 2012 [3]. This does not only contribute significantly to the world economy, but also has become an enabler for even more sophisticated, powerful, energy-efficient, and cost-effective electronic products [3]-[5].

The revolution in information technology has also seen unprecedented economic growth over the past half-century largely due to the exponential increase in the performance of semiconductor ICs that are at the heart of all the modern electronic products [6]. The productivity of IC technology has increased by a factor of one billion times since 1960 [7]. Concurrently, the performance has increased one million times since the early 1970s. The productivity of IC technology N, the number of transistors per chip, can be written as [8]:

$$N = \left(\frac{1}{F^2}\right) D^2 P_E \tag{1.1}$$

where F is the minimum feature size, D^2 is the area of an IC and P_E is the transistor packing efficiency, i.e., the number of transistors per F^2. F has been the most potent factor since 1960. As a result, an increase in N has been observed primarily due to scaling down the minimum feature size of the transistors and interconnects. The scaling rules, as indicated by Eq. (1.1), were first outlined by Dennard *et al.* in the early 1970s [9]. Figure 1.1 shows the progress in the evaluation of metal-oxide-semiconductor field-effect transistor (MOSFET) gate length and the number of transistors per processor chip since 1970 [10]. The number of components in an IC has been doubled every 24 months which has improved the performance significantly and reduced the price per transistor. This was first predicted by Gorden E. Moore of Intel Corporation in 1965, which later came to known as Moore's law [11].

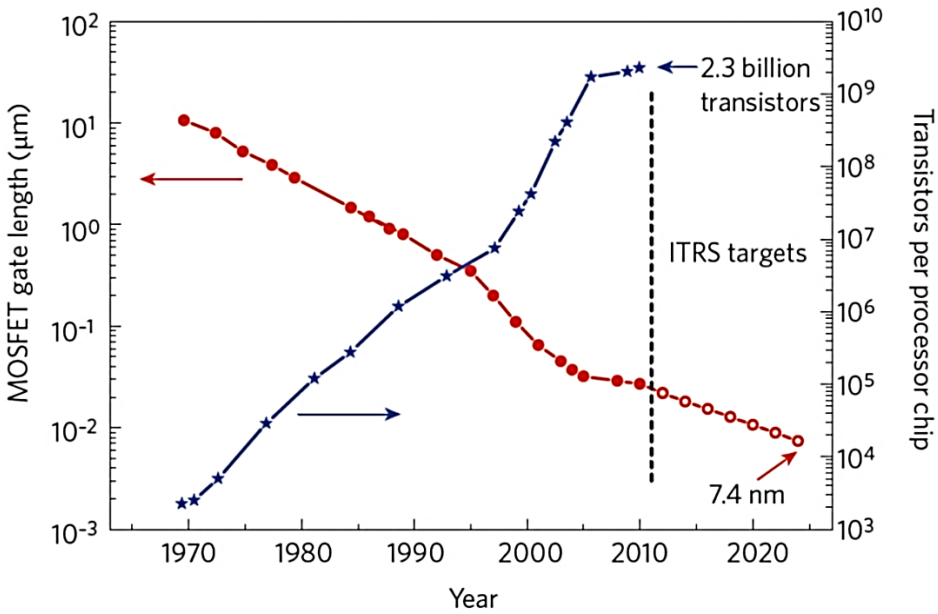

Figure 1.1 The MOSFET gate length with respect to the year since 1970 (filled red circles). The size scaling of MOSFET gate length has significantly increased the complexity of ICs over the years and hence the number of transistors per processor chip (blue stars). It also shows that the targets (open red circles) set by the International Technology Roadmap for Semiconductors (ITRS) [10].

These improved scaling trends have been advanced by large research and development (R&D) investments, which have motivated industry collaborations, R&D partnerships and other cooperative ventures. In 1992, the SIA started the

National Technology Roadmap for Semiconductors (NTRS) to guide these programs, which was later joined by the corresponding industry associations in Europe, Japan, Korea, and Taiwan in 1998 [12]. The roadmap was later renamed the International Technology Roadmap for Semiconductors (ITRS) in 1999 and since then, the ITRS has been updated and fully revised in even-numbered and odd-numbered years, respectively. The objective of the ITRS is to present an industry-wide consensus, extended out to a 15-year horizon depending on the current estimate of research and development needs. This has improved the quality of research significantly and led to many research efforts into areas where research breakthroughs are most needed.

Geometrical scaling of conventional transistors has followed Moore's law for many years in order to enhance signal processing and data storage of an IC [12]. The miniaturization has already reached below 20 nm, consequently it is difficult to imagine the further developments of Si based complementary MOSFET (CMOS) technology based on Moore's law [13]. Therefore, the equivalent scaling targets such as performance improvement by using innovative designs, software solutions and other new materials/structures, which were not covered by Moore's law have been incorporated by ITRS in 1995 to their roadmap and are known as "More Moore" and "More-than-Moore" (MtM) [12], [14].

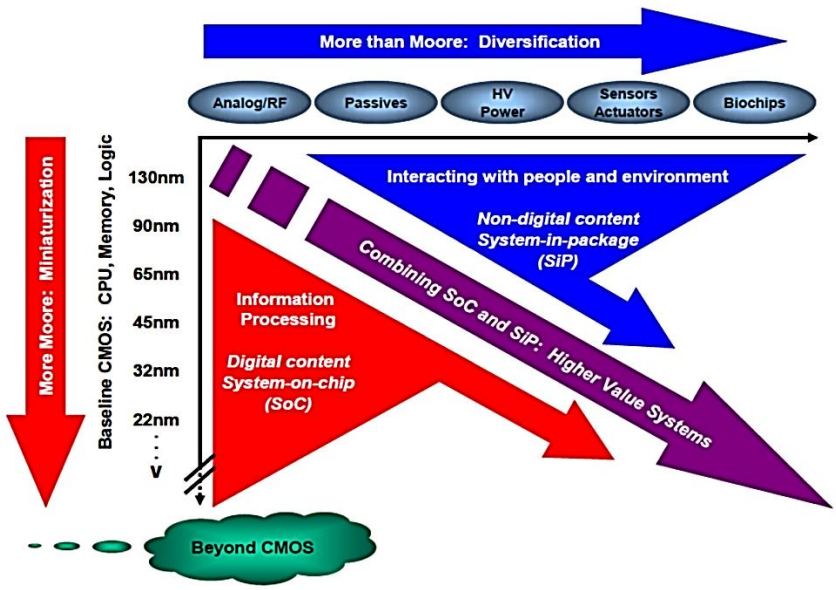

Figure 1.2 A graphical illustration of the Moore's law, "More Moore", and "More-than-Moore" set by the ITRS. It explains the main development trends of the miniaturization in integrated systems for various applications in electronics [14].

Figure 1.2 shows a graphical representation of the roadmap and illustrates the miniaturization and diversification trends of the semiconductor industry. The "More Moore" is aimed for the developments of further miniaturization of circuit elements beyond 100 nm down to the physical limits of the CMOS technology. The performance trade-off against the power requirement of "More Moore" technology can be significantly improved by the incorporation of novel device concepts and material in the "Beyond CMOS" domain. The second trend MtM refers to a set of technologies beyond the boundaries of conventional semiconductor technology. Non-digital applications such as radio frequency (RF) communications, sensors, and bio-chips which interact with the outside world for powering the products are included in the functional diversification of MtM and can be regarded as a complement of digital signal and data processing. These functionalities do not necessarily scale down with Moore's law. The integration of digital and non-digital devices into a miniaturized compact system-in-package (*SiP*) level is within the scope of this domain. Further, cross-disciplinary areas e.g. nanoelectronics, nanothermomechanics, and nanobiology will also contribute as shown in Fig. 1.2 [12], [14], [15].

Initially, the ITRS roadmap was focused on semiconductor logic and memory products. However, due to the increased importance of wireless and RF products, an extensive chapter on RF devices entitled "RF and analog/mixed-signal technologies for communications" has been added since 2003 [16]. This chapter describes the performance targets and the requirements of Si based CMOS, bipolar MOS, heterojunction bipolar transistors (HBTs), III-V compound semiconductor devices, high-voltage MOS, and passive device technologies. Based upon the different technology requirements, the frequency band has been categorised from 0 to 0.4 GHz, 0.4 to 30 GHz, 30 to 300 GHz, and beyond 300 GHz [17].

Most of the frequency bands of the electromagnetic spectrum shown in Fig. 1.3 have been progressively explored by physicists and engineers. The successive regions of the spectrum have been colonised and technologies have been fully developed in order to fully exploit the radiation: e.g. microwaves are used for mainly for communications, near infrared radiation is commonly being used in fibre optic communication, and X-rays are routinely employed for imaging purposes etc.

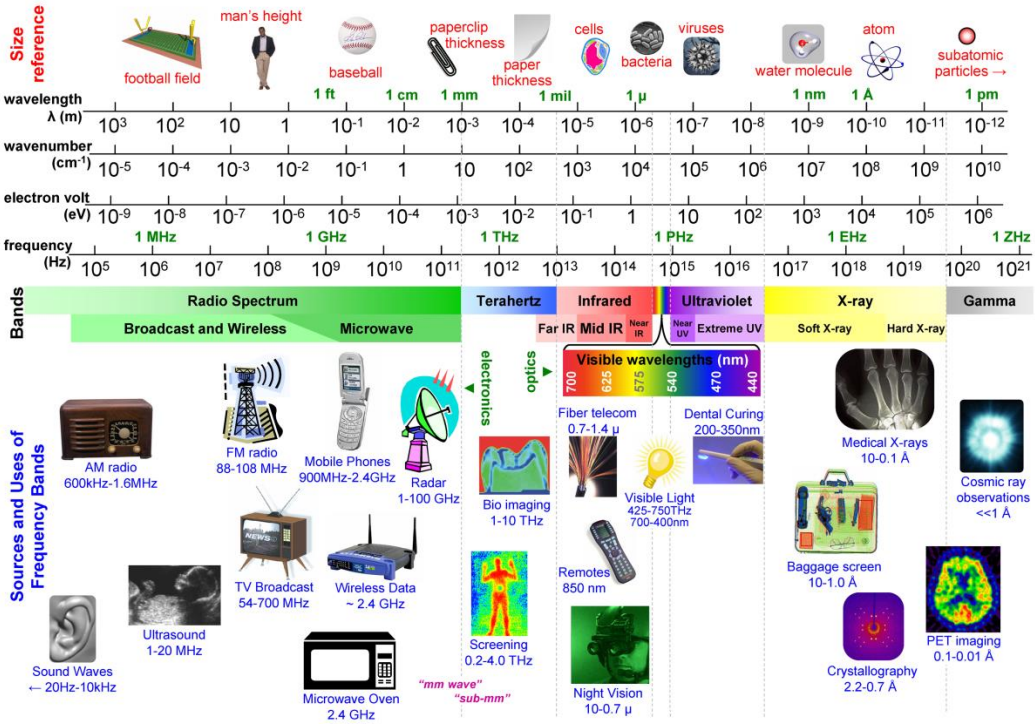

Figure 1.3 The electromagnetic spectrum showing the various frequency bands and their applications. The corresponding wavelength, wavenumber, and photon energy are also shown with the size references at the top [18].

The frequencies ranging from 0.1 to 30 THz are referred as the terahertz (THz) region [19] and lies between the microwave and infrared regions of the spectrum as shown in Fig. 1.3. THz radiation is able to penetrate a wide variety of dielectric materials such as plastics, papers, fabrics, and organic compounds including human tissues without the damage associated with ionising radiation such as X-rays. In addition, THz radiation cannot go through the metallic objects and liquid, hence can be employed for the imaging of wide variety of objects including explosives, chemicals, biological materials, and cancerous tissues [20]. Recent technological innovations have enabled the use of THz technology in wide variety of sectors e.g. biology and medical sciences, information and communication technology, non-destructive evaluation, quality control of food, agricultural products, global environmental monitoring, and ultra-fast computing etc. [19].

The THz technology has been benefitted by the advancements in the performance of high frequency electronics operating at frequencies higher than 100 GHz (0.1 THz). However, despite continual research there is a scarcity of solid-state, compact, and

low-cost THz sources and detectors that can operate at room temperature. Therefore, sometimes these frequencies are known as “THz gap” [19].

One of the leading market research firms (BCC) has forecasted that the THz market will rise to $570 million by 2021 from $83.7 million in 2011 [21]. The recent developments and realisations of many THz devices including quantum cascaded laser (QCL) [22], uni-travelling-carrier photodiode (UTC-PD) [23], resonant tunnelling diode (RTD) [24], Schottky barrier diode (SBD) [25], bolometer [26], and THz single-photon detector [27] have accelerated the pace of the advancement of THz technologies to cover the so-called “THz gap” [19]. Further breakthroughs in THz technologies are expected through novel devices either from existing technology or entirely from new innovative concepts.

1.2 Emerging electronic devices

In order to fully exploit the effects of small dimensions, the development of advanced device designs, materials, and architectures are required. The ITRS has already included a chapter entitled as “Emerging research devices” [28] with a perspective on the emerging technologies as addressed in the MtM, which can serve as a bridge between CMOS and nanoelectronics beyond the end of CMOS. This can

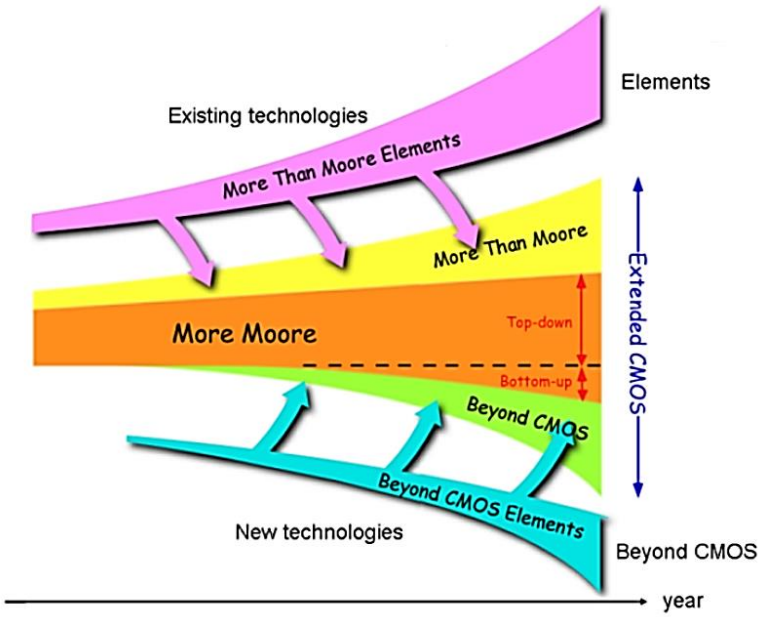

Figure 1.4 Relationship between More Moore, More-than-Moore, and Beyond CMOS [28].

be accomplished by integrating "Beyond CMOS" technologies as well as MtM technologies into the "More Moore" to form a heterogeneous platform called the "Extended CMOS" as illustrated in Fig. 1.4.

Based on the novel concepts, a multitude of devices including high-electron-mobility transistor (HEMT) [29]-[31], nanowire FETs [32], *n*-type III-V [33], [34], and Ge channel replacement devices [35], tunnel FETs [36], [37], spin FETs [38], carbon nanotube FETs [39], graphene nanoribbon FETs [13], impact ionization MOS [40], [41], negative gate capacitance FET [42], bilayer pseudo-spin FET [43], excitonic FETs [44], RTD [24], HBT [45], single electron transistor (SET) [46], nanoscale cross junctions [47], three terminal junctions (TBJs) [48], ballistic rectifiers [49], and self-switching devices (SSDs) [50] have emerged. Some of these devices have already been included in the ITRS 2011 edition. They not only work at nanoscale dimensions but also have a great potential to operate at very high frequencies possibly up to THz.

In contrast, silicon (Si), which is one of the abundant materials on the Earth, is still being used as a principal semiconductor by the electronic industry to produce economical products. For example, Si MOSFET based CMOS technology is one of the important components in the modern ICs with much improved RF properties for analog and digital applications. Recently, the highest cut-off frequency of 485 GHz has been reported for a Si MOSFET with the gate length of 29 nm [51].

Innovations and continuous improvements in fabrication techniques have allowed Intel to shrink device technology to 45 nm in 2007, 32 nm in 2009 and 22 nm in 2011 [52]. Some of the recent milestones are a result of strained silicon in 2003, high-κ/metal gate in 2007, and three-dimension (3D) transistor or tri-gate transistor in 2011 [53]. The tri-gate transistor allows the current to be controlled in 3 sides of the channel (top, left and right) rather than just from the top when compared to the conventional planar transistors. As a result, the best performance is assured by maximizing and minimizing the current flow when transistor is on and off, respectively. Recently, Intel has invested $ 5 billion to start a new chip manufacturing facility to fabricate transistors with 14 nm tri-gate technology [54].

High-performance transistors can also be fabricated from III-V semiconductors such as GaAs and InP because of their excellent electronic properties. These structures are

commonly known as HEMT or modulation-doped FET (MODFET) or heterostructure FET [30], [31]. Due to the heterojunction in HEMT there is almost no impurity scattering in the channel unlike MOSFET which utilises a doped region. Two different semiconductor materials with the same lattice constants are commonly used to form a heterojunction for the HEMT. However, sometimes materials with slightly different lattice constants e.g. AlGaAs and GaAs are also being used which in turn results in crystal defects and degrades device performance significantly. To overcome this problem, HEMTs has been modified to metamorphic HEMTs (mHEMT) by introducing a buffer layer in-between the heterojunction. Another approach is the use of a very thin layer of the material in which the lattice constant is stretched to match the lattice constant of the other material. This type of device is known as a pseudomorphic HEMT(pHEMT). The GaAs pHEMT with a gate length of 100 nm, InP HEMT with a gate length of 30 nm, and GaAs mHEMT with a gate length of 40 nm have demonstrated cut-off frequencies of 152, 644, and 688 GHz respectively as shown in Fig. 1.5 [13].

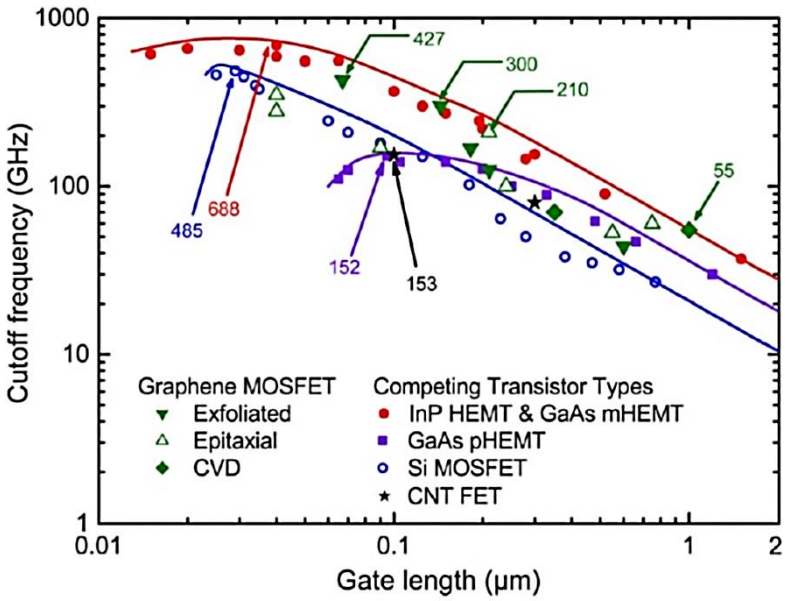

Figure 1.5 Comparison of the cut-off frequency of various types of RF FETs as a function of gate length [13].

Graphene based devices

Recently, graphene has emerged as a potentially well-suited semiconductor material for RF applications because of its excellent electronic transport properties and purely two dimensional structure [55]-[57]. Graphene is a single layer of carbon atoms

arranged in a honeycomb structure and it demonstrates the highest mobility (up to 200, 000 $cm^2/V.s$) when compared to other semiconductor materials [58], [59]. Such high mobility and possibility of having a one atom thick channel are perhaps the most appealing features of graphene for use in a transistor.

The first graphene field-effect transistor (GFET) was demonstrated by Novoslev *et al.* in 2004 [60] by employing a one-atom thick graphene fabricated by the mechanical exfoliation technique. In 2008, Meric *et al.* fabricated a GFET with a gate length of 500 nm operating up to 14.7 GHz [61]. The cut-off frequency was increased to 50 GHz in 2009 [62] and 100 GHz in early 2010 [63] with the GFETs having a gate length of 350 and 240 nm respectively, followed by a 300 GHz with 144 nm gate GFET. Finally in 2012, the GFET has been demonstrated to work at 350 GHz with a gate length of 40 nm [57] and 427 GHz with a gate length of 67 nm [64], though the projected intrinsic cut-off frequency is higher than 1 THz [57], [65].

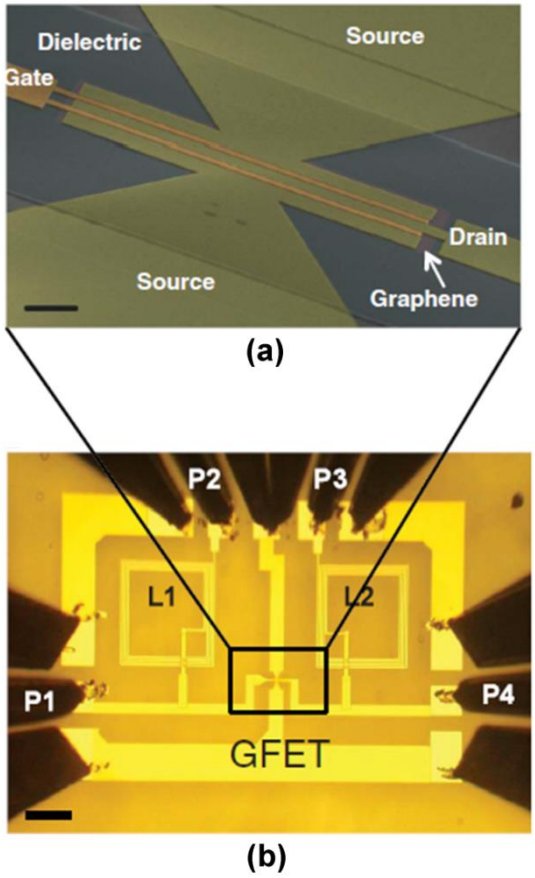

Figure 1.6 Integrated circuit of GFET mixer with inductors (a) scanning electron images of top-gated dual channel mixer IC, the gate length was 550 nm.(b) The optical image of the complete IC. Scale bar is equal to 100 μm [66].

Figure 1.5 shows the cut-off frequencies of the best GFETs reported so far with a comparison to other established and competing technologies. It can be seen that the cut-off frequency for all the transistor types is inversely proportional to the gate length. It is interesting to note that the GFETs with 100 nm gate length are much superior to the carbon nanotube FETs and are comparable with the well-known fastest RF transistors, i.e., InP HEMT and GaAs mHEMT.

IBM scientists have demonstrated an integrated GFET based RF mixer with other components such as inductors on a single chip fabricated from a silicon carbide (SiC) wafer as shown in Figs 1.6 (a) and (b) [66]. In addition, a GFET has been configured as a frequency doubler at the Ku band (12-18 GHz) without any filtering element [56]. In 2009, Chen *et.al*. demonstrated a single layer graphene based 50-80 MHz nanomechanical resonator having a quality factor of 1×10^4 at low temperatures (5 K) [67]. Chemical vapor deposition (CVD) graphene based electromechanical RF switchs have also been reported [68]. Nevertheless, a few graphene based devices including the TBJ [69] and the geometric diode [70] have been demonstrated for the rectification of RF signals.

1.3 Motivation and aims

It is quite clear from the above comprehensive review of ITRS and the emerging technologies that there is still a scarcity of compact, ultra-fast, cost-effective electronic devices which can work at room temperature with very high cut-off frequencies possibly up to THz. Numerous novel devices and materials have emerged as a result of intense research to meet this demand. In response to this call, two nonlinear nanoelectronic devices namely the ballistic rectifier [49] and the self-switching device [50] have been conceived to include in the family of emerging research devices, with an objective to serve a number of sectors and to bridge the "THz gap". The planar geometry of both the devices is a promising solution to offer the best possibilities of integration with other existing solid-state electronic and photonic technologies within a single IC.

The ballistic rectifier was conceptualised by Song *et al.*, by inserting an artificial scatterer at the centre of a nanoscale cross junction to rectify RF signal. The ballistic rectifier does the same operation of a bridge rectifier which requires four

conventional diodes [71]. This device differs from all the conventional diode structures because it does not contain any doping junctions or barrier structures. The ballistic-electron transport regime and the planar structure of the ballistic rectifier has enabled room temperature RF operation up to 50 GHz [72], however Monte Carlo (MC) simulations have predicted the cut-off frequencies in THz region [73].

The self-switching device was proposed and realised by the researchers at University of Manchester, United Kingdom. The device exhibits a nonlinear current-voltage (*I-V*) characteristic due to the geometrically induced asymmetry in the channel. This behaviour resembles to that of a conventional diode but without any doping junction [74]. The key feature of SSD includes the ability to construct an array of several devices connected in parallel without any interconnection layer using single step nanolithography; as a result, the whole fabrication process is simpler, faster and inexpensive. Due to a small parasitic capacitance, SSD enables the ultra-fast rectification at 1.5 THz even at room temperature with excellent noise equivalent power (NEP) [75]. In addition, SSDs may also be used as a THz source due to Gunn oscillations as envisaged by MC simulations [76].

Despite of aforementioned studies on the novel working principles, and high-speed room temperature operations, there has never been any report on the noise properties of ballistic rectifier. As a potential THz detector, they are as important as their speed. Since the device speed generally scales up with the carrier mobility, novel semiconducting materials, in particular, graphene has not been utilised yet for the fabrication of ballistic rectifier and SSD. Graphene demonstrates a very large mean-free path length even at room temperatures due to its ultra-high mobility, which is the fundamental requirement to realise a ballistic rectifier. On the other hand, high carrier concentrations of graphene are favourably befitting to SSDs. Importantly, due to such mobility these devices are expected to work at THz frequencies, which is normally sought from novel concept based devices. Moreover, both devices have single-layered architecture that is ideally-suited to use graphene as an active layer.

This research was centred on the design and development of the ballistic rectifier and the SSD with the aim of working at room temperature and/or at RF frequencies. Both devices were explored and characterised in order to streamline the requirements for more practical applications. This thesis is structured in seven chapters, the first being

this introduction, which has included the detailed review of market requirements, efforts being made by researchers, and the motivation behind this research.

Chapter 2 deals with the general physics concepts related to this research. The semiconductor heterostructure and two-dimensional electron gas (2DEG) are first presented, followed by a brief description of novel semiconductor or "miracle material" known as graphene [77]. The basic concepts of various types of noises observed in semiconductor devices are then discussed. The last section presents a brief review of novel underlying concepts, properties of the ballistic rectifier and the SSD.

In Chapter 3, a ballistic rectifier fabricated from lattice matched InGaAs/InAlAs heterostructure material was utilised for RF characterisation. Details about the fabrication process using electron-beam lithography (EBL) and wet chemical etching have been presented. A standard coplanar measurement was utilised to demonstrate the RF rectification capability of the ballistic rectifier up to 3 GHz, which was the highest frequency of the instrument used in these experiments.

Chapter 3 then presents the experimental characterisation of low-frequency noise properties of the ballistic rectifier at room temperature. A brief introduction to the urgent need to explore the noise properties has been discussed. It has been shown that flicker noise can be utilized as a reliability tool to ensure the flawless design of the device for high frequency applications [78].

The latter sections of Chapter 3 elaborate on the techniques used to measure low-frequency noise of the device from a theoretical point of view through the measurement. The analysis of the measured noise findings using different theories of flicker noise has also been included. Furthermore, a quantitative model of the observed noise at finite biases in a device with variable width along the channel has also been proposed.

In Chapter 4, graphene was utilized to fabricate two different geometries of ballistic rectifier, i.e., with and without a scatterer at the centre. Graphene demonstrates a large electron mean-free path length due to its high carrier mobility [79], which is a desirable feature of merit for ballistic rectifiers. Monolayer graphene fabricated by mechanical exfoliation and CVD technique were used for the fabrication. The measured voltage-current characteristics have been analysed by using a scattering approach of multi-terminal ballistic transport. In the last section of the Chapter, a CVD-grown graphene

based ballistic rectifier has been employed to detect the RF signals to demonstrate its ability to be an ultra-fast rectifier.

Chapter 5 highlights the first experimental realisation of an SSD using monolayer graphene fabricated by mechanical exfoliation onto a SiO_2 substrate. This chapter starts with the introduction of microwave rectification theory based on the analysis of the nonlinear *I-V* characteristic of a device. A graphene SSD can be realised by short-circuiting the both gates with the drain in a graphene based side-gated transistor [80]. This device has benefited with the intriguing property of graphene in which the charge carrier type can be tuned from electrons to holes or vice-versa.

The planar nature of the device architecture has allowed the fabrication of 22 SSDs connected in parallel as an array structure. CVD-grown monolayer was utilised for the fabrication of these devices. DC characterisation was then performed in ambient conditions. The graphene based SSD array has demonstrated exceptional RF properties in contrast to graphene *p-n* junctions [81]. The responsivity and NEP have been estimated from the measured results.

Being a potential semiconductor, it is important to analyse the electronic properties of graphene in detail. It has been observed that the graphene devices demonstrate a hysteresis in DC measurements at ambient conditions due to the interaction of graphene with the surroundings which traps free charge carriers [82]. As a result, the estimated field-effect mobility may not be as high as desired which is an anticipated figure of merit for the ballistic rectifier and the SSD. Therefore, Chapter 6 is dedicated to the detailed investigation of the charge trapping and/or de-trapping behaviour of these devices in air. CVD-grown monolayer graphene has been utilized for these studies.

The estimated characteristic time constants of the charge trapping and de-trapping at different back-gate voltages have been analysed quantitatively. The devices were further exposed to nitrogen gas for chemical induced doping in order to achieve *n*-type carrier transport to the right of neutrality point. Short pulse characterisation was also employed, which significantly reduced the time constants of charge trapping and de-trapping.

The summary and outlook are then presented in Chapter 7.

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Chapter 2

Physics background

2.1 Introduction

This chapter builds the theoretical framework required for the subjects discussed in this research. The first section covers semiconductor heterostructures and two-dimensional electron gases (2DEGs) followed by the brief overview about the structural and electronic properties of graphene. The physical origin of various types of noises in semiconductor devices is then described. The last section covers the novel underlying concepts and unique properties of ballistic rectifiers and self-switching devices (SSDs).

2.2 III-V semiconductors

In the last decade, III-V semiconductors have become very important in fundamental research on condensed matter. Developments in growth and processing techniques have allowed excellent control on material composition and doping which provides high quality samples for the fabrication of modern electronic and optoelectronic devices [1]. They provide very high operating speeds when compared to conventional Silicon (Si) based structures. Further, in compound semiconductors such as InGaAs, GaAs, InAs etc., the electron mobility is about 10 times higher than that of Si at a comparable sheet density [2]. In particular, InGaAs based high-

electron-mobility transistors (HEMTs) have been demonstrated to have cut-off frequency higher than 1 THz [3].

2.2.1 Semiconductor heterostructures

Semiconductors made from more than one material are known as heterostructures, in which band engineering is used to control the movement of electrons and holes by varying the composition of the materials [4]. A large range of III-V semiconductors have been investigated so far, however only a few of them are commonly used to realise the heterostructures. Alloys between different compounds such as $Al_xGa_{1-x}As$ and $In_xGa_{1-x}As$ (usually known as AlGaAs and InGaAs, respectively, where the value of x ranges from 0 to 1 and reflects the composition of alloys) are very often used to enlarge the range of possible electronic and optoelectronic properties. The energy bandgaps and lattice constants of semiconductors are the most important parameters in determining the intrinsic properties of a heterostructure. Figure 2.1 shows the energy bandgap and crystal lattice constant for some common compounds of semiconductors [5].

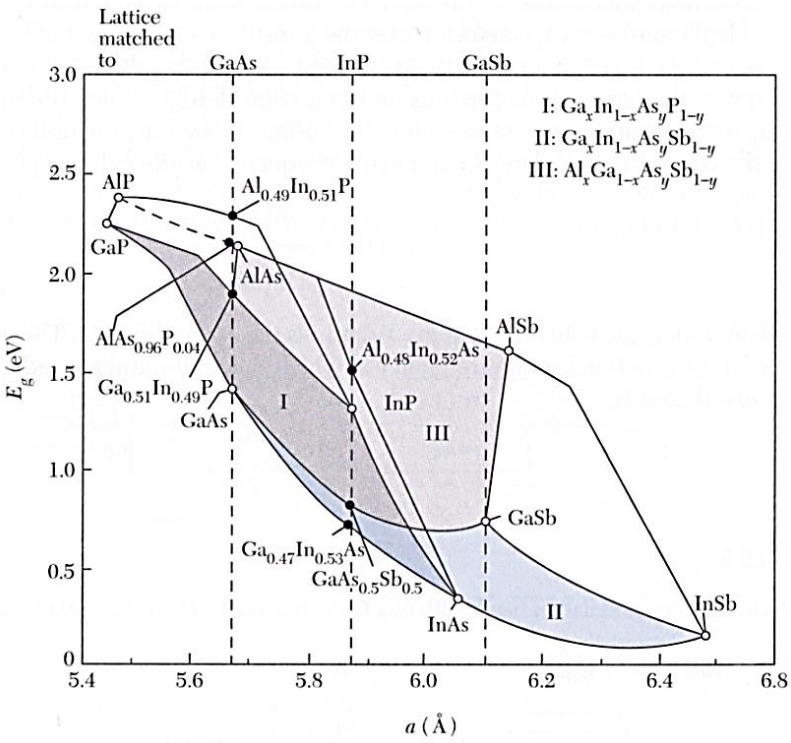

Figure 2.1 Energy bandgap E_g with respect to the lattice constant a for III-V alloys [5].

Semiconductors with different bandgaps are used for the fabrication of 2DEG (to be introduced later), which can be utilised to fabricate fast transistors [6], [7]. In order to fully exploit the capabilities of heterostructures, dedicated fabrication techniques which can grow superlattices with the control of thickness down to the monolayer atomic scale are required. The most common methods to grow semiconductor heterostructures are molecular-beam epitaxy (MBE) and metal organic chemical vapour deposition (MOCVD) [8]-[10].

Lattice matching between two semiconductor materials in heterostructures is essential to avoid electrical defects such as interface traps caused by undesired dislocation or broken bands. To achieve a good quality heterostructures, two materials with different bandgaps and similar lattice constants must be matched e.g GaAs/AlAs or InGaAs/InP or GaAs/AlGaAs in Fig. 2.1. An epitaxial growth technique can grow a good-quality heterostructure despite severe lattice constant mismatch between two semiconductors, provided that the thickness of grown epitaxial layer is smaller than the critical thickness t_c. The maximum thickness allowed for an epitaxial layer is directly related to the lattice mismatch Δ between two materials and can be defined as [9]:

$$\Delta = \frac{|a_e - a_s|}{a_e}, \tag{2.1}$$

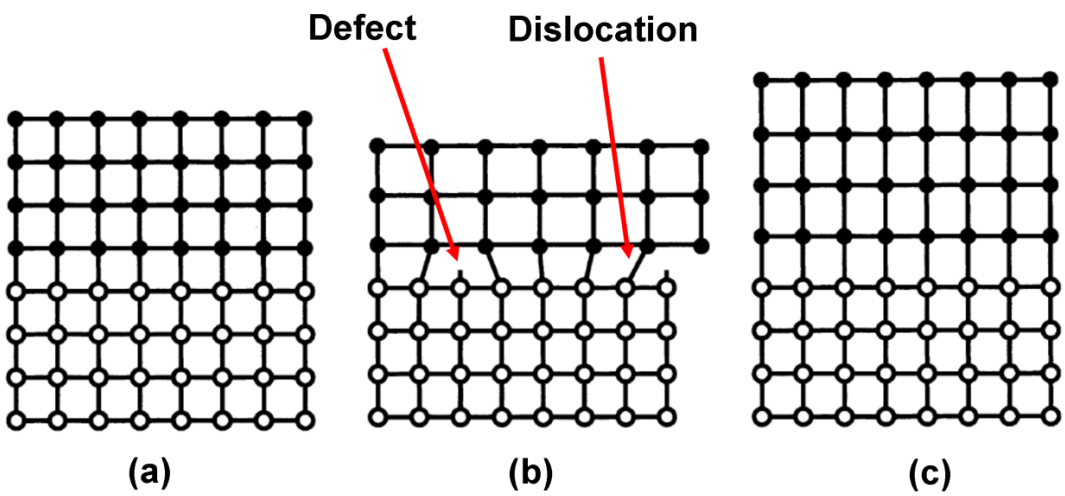

Figure 2.2 Schematic illustration of an atomic arrangement in the various modes of epitaxial growth: (a) lattice-matched, (b) lattice-mismatched, and c) strained lattice-mismatched [10].

where a_e and a_s are the lattice constant of the epitaxial layer and the substrate, respectively. If the epitaxial layer is thin enough, the dislocations at the interface can be eliminated by physical straining the epitaxial layer to the extent that the lattice constant of this layer becomes similar to the substrate as shown in Fig 2.2. The critical thickness and lattice mismatch follow the following empirical relation [9]:

$$t_c \approx \frac{a_e}{2\Delta} \approx \frac{a_e^{\,2}}{2|a_e - a_s|}. \tag{2.2}$$

Considering a mismatch of 2%, the critical thickness of an epitaxial layer is approximately 10 nm from an a_e of 5 Å. Hence, this technique provides an extra degree of freedom and allows the use of a broader range of materials such as InGaAs epitaxial layer on an InP substrate, for realising novel devices with improved performances. Furthermore, Vegard's law can be used to predict the lattice constant of an alloy as a linear interpolation between its constituents [11]. For example, the lattice constant of $Al_xGa_{1-x}As$ is given by $xa_{AlAs} + (1-x)a_{GaAs}$, where a_{AlAs} and a_{GaAs} are the lattice constant of AlAs and GaAs, respectively [12],[13].

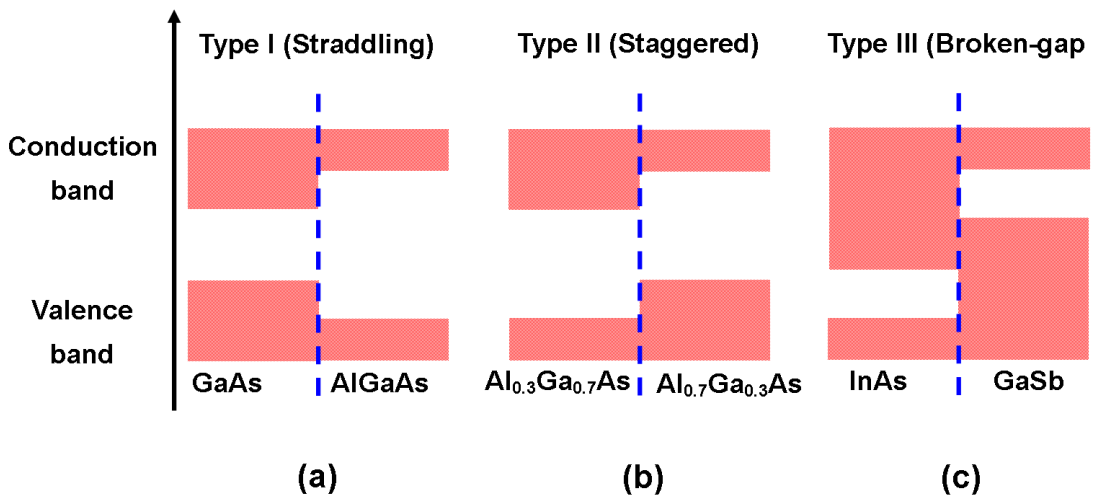

Figure 2.3 Three possible conduction band and valence band alignments in a heterostructure (a) Type I or straddling alignment of GaAs/AlGaAs, (b) Type II or staggered alignment of AlGaAs/AlGaAs, and (c) Type III or broken-gap alignment in InAS/GaSb system. The dashed line represents the interface of two semiconductors.

The conduction and valence bands of two different semiconductors can be aligned in three different ways while forming a heterostructure as shown in Fig. 2.3:

i) *Type I or straddling alignment*, in which the bandgap of one semiconductor is sandwiched between the conduction and valence bands of the other, hence it naturally has a smaller energy gap like in InGaAs/InAlAs and GaAs/AlGaAs.

ii) *Type II or staggered alignment*, where the discontinuities between the conduction and valence bands of two semiconductors have the same sign so electrons and holes are being collected at lower conduction and higher valence band, respectively e.g. InAlAs/InP or AlGaAs/AlGaAs junction.

iii) *Type III or broken-gap alignment* exists when the energy levels of the conduction and valence bands of one semiconductor are both above the conduction band of the other. Thus the conduction band overlaps the valence band at the interface such as GaSb/InAs.

2.2.2 Two-dimensional electron gas

In a 2DEG, normally confined at a doped hetrojunction, the electrons occupy the same state level for the motion in one plane but remain free in other two dimensions [4],[5],[9],[14],[15]. A typical method to establish a 2DEG is remote or modulation doping, where the doping is grown in one semiconductor such that the carriers subsequently migrate to another undoped semiconductor. Figure 2.4 illustrates Type I (straddling) heterojunction between a large bandgap semiconductor (AlGaAs) grown onto a narrower bandgap semiconductor (GaAs). The electrons are introduced by *n*-type dopants (e.g. Si) in a wide bandgap semiconductor at some distance from the interface with the GaAs substrate. The undoped AlGaAs layer is known as spacer, which remains free from the intentional doping. The electrons in *n*-AlGaAs are free to move around and some of them cross into the GaAs. These electrons lose their energy and become trapped because the barrier ΔE_c at the junction between the *n*-AlGaAs and GaAs stops them returning into the *n*-AlGaAs. As a result, an electric field across the interface develops separating negatively charged electrons from their positively charged donors.

The built-in electric field tends to drive the electrons in GaAs back to the donors into *n*-AlGaAs, but the barrier stops them from doing that which in turn results in a discontinuity in the conduction band as shown in Fig. 2.4. Hence, the electron can only be squeezed against the interface, where they are trapped in a triangular

potential well. This well is typically 10 nm wide and is known as so-called two-dimensional electron gas [4]. The energy levels of the electrons motion perpendicular to the interface are discrete however electrons can move freely along the plane of interface.

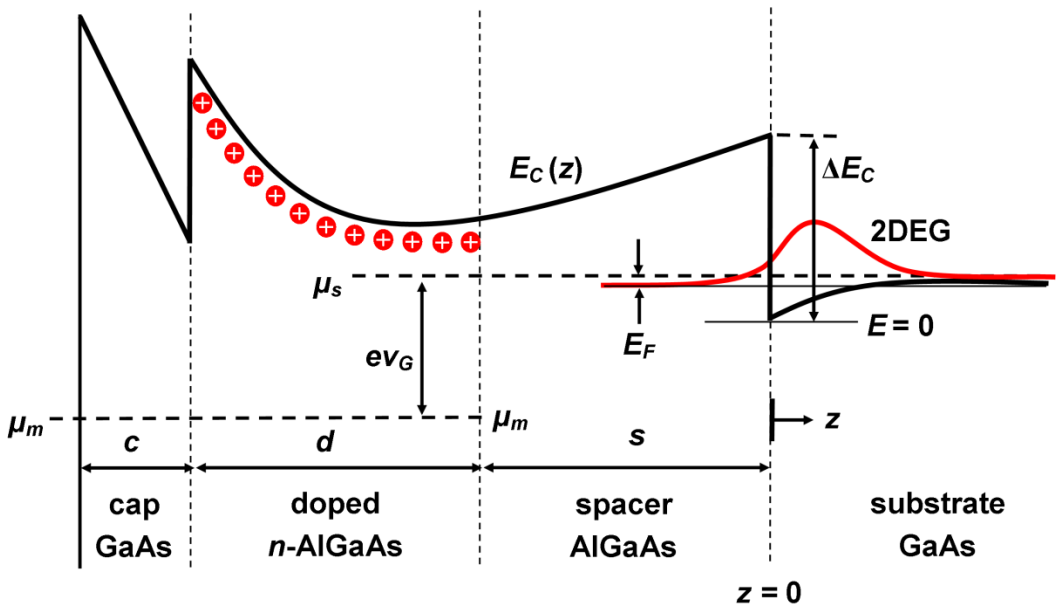

Figure 2.4 Schematic illustration of a modulation doped heterostructure based on AlGaAs/GaAs system. The electrons from *n*-AlGaAs are trapped at the interface forming a 2DEG layer. This can be achieved by the built-in electric field across the interface which introduces a discontinuity ΔE_c in the conduction band. The density of 2DEG can be modulated by applying a bias V_G to the gate, which changes the alignment of the Fermi level E_F between the metal (μ_m) and semiconductor (μ_s) [4].

Modulation doping and the spacer layer separate the mobile carriers and the parent impurity dopants. This results in a significant decrease in the Coulomb scattering and thus increases the mobility. The electron mobility of 1000 m^2/Vs can be achieved in heterostructures such as InGaAs/InP at low-temperatures, while the low-temperature electron mobility in metal-oxide-semiconductor field-effect transistors (MOSFETs) is only approximately 4 m^2/Vs [16]. The typical electron density of 2DEGs ranges from $2\times10^{11}/cm^2$ to $2\times10^{12}/cm^2$ [17].

By inserting a monolayer of δ-doping (e.g. Si) into the AlGaAs region instead of using uniform doping, the performance of a 2DEG system can be significantly improved [18],[19]. Furthermore, a top-gate electrode can be introduced to achieve further modulation. This system is effectively equivalent to a parallel two plate capacitor, i.e., the gate and the 2DEG. A bias is applied to the gate electrode to

modulate the 2DEG density which changes the alignment of the Fermi level between metal (μ_m) and semiconductor (μ_s) as illustrated in Fig. 2.4. The most common gate consists of a reversely biased Schottky contact, which is used for the fabrication of a HEMT. In addition, the 2DEG systems are not only used widely in the development of high performance telecommunication systems [20] but are also very important in solid-state physics to study integer and fractional quantum Hall effects [21],[22].

In this work, wafers with embedded 2DEGs in the lattice matched InGaAs/InGaAs heterostructure have been used for the fabrication of ballistic rectifier in Chapter 3.

2.2.3 Electronic transport in mesoscopic structures

The advancements in lithography techniques in combination with the availability of high quality semiconducting materials has allowed the fabrication of semiconductor nanostructures with dimensions smaller than or comparable to the electron mean-free path length λ, as illustrated in Fig. 2.5 [23]. Device structures fabricated at this scale are often referred to as mesoscopic structures, in which the current conduction deviates significantly from that predicted by Ohm's law. This regime of conduction is known as ballistic transport, where scattering caused by intrinsic impurities can be neglected and more importantly the transport properties can be defined by tailoring the geometry of a structure.

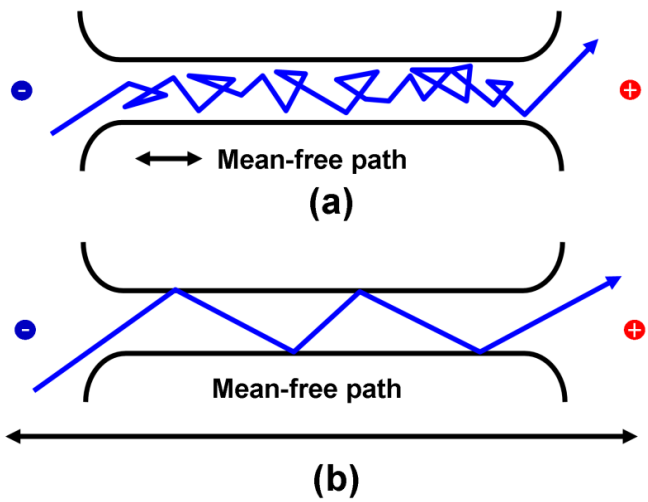

Figure 2.5 Schematic electron trajectories for the diffusive and ballistic wire structures. (a) In the diffusive regime, the electrons are randomly scattered due to the intrinsic impurities of a conductor. (b) The device dimensions are much smaller than the mean-free path length in ballistic conductors, as a result the electrons behave like billiard balls and their trajectories are defined by the wire geometry rather than impurities [23].

In the ballistic transport regime, where the device dimensions are scaled below the length of elastic mean-free path, the conductance is limited by the scattering of electrons at the device boundary rather than impurity scattering. This conductance is better understood by considering the wavelike nature of carriers as explained in Landauer approach [24]. It expresses the conductance in terms of transmission probabilities of propagating modes at the Fermi level and can be used to determine the conductance of conducting wires whose transmission probabilities are close to unity. The conductance of such wire is found to be a multiple of a quantity known as quantised conductance G_0 which can be written as [23]:

$$G_0 = \frac{2e^2}{h} \approx \frac{1}{12.9}\,\mathrm{k\Omega}. \tag{2.3}$$

where e is the electron charge and h is the Plank's constant. It is interesting to note that the above quantised conductance is independent of the wire length, hence does not decrease inversely with the length as it would classically.

2.3 Graphene

Carbon is the most common element in the Universe and is the basis of organic chemistry. Due to the flexibility in bonding, there is an extensive list of carbon allotropes with a large variety of physical properties. The most commonly used carbon allotropes, such as diamond and graphite, have great importance in our daily lives. Diamond has sp^3 bonding meaning that all the *p*-orbitals of the carbons are used for the bond formation [25]. As a result there are no free electrons left for the electrical conduction. The graphite was first discovered in England and became widely known after the invention of pencil in 1564. Graphite is a three-dimensional carbon allotrope, which comprises of many two-dimensional layers of carbon atoms arranged in the hexagonal lattice. The bonding in the two-dimensional plane is strong, while in the perpendicular plane is very weak. Therefore, graphite has only 2 of the 3 *p*-orbitals tied up in bonds unlike a diamond. This unpaired *p*-orbital is the basis of electron transport; hence graphite is better than the diamond in terms of electrical conductance [26].

The two-dimensional allotrope of carbon is graphene, in which carbon atoms are densely packed in a honeycomb structure made out of hexagons. Being a two-

dimensional system, graphene plays an important role in understating the electrical properties among all other allotropes. The zero- and one-dimensional carbon allotropes are fullerenes [27] and carbon nanotubes (CNTs) [26],[28], respectively. The carbon atoms are spherically arranged in fullerenes while carbon nanotubes can be obtained by rolling graphene along a direction and reconnecting the carbon atoms [25],[29]. Figure 2.6 shows the various types of carbon allotropes such as graphene, fullerenes, carbon nanotubes, and graphite.

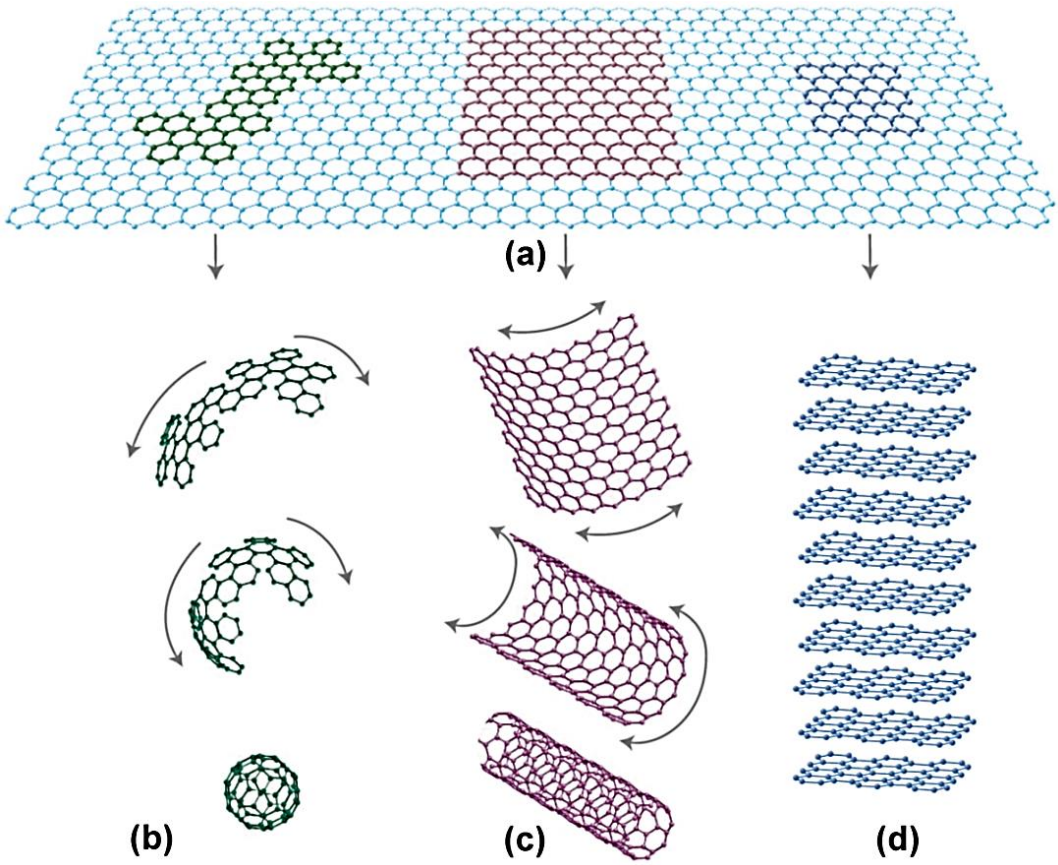

Figure 2.6 (a) Carbon atoms arranged in a honeycomb lattice in graphene. A graphene sheet can be used to obtain various types of allotropes such as (b) fullerenes (wrapped graphene in zero-dimension), (c) carbon nanotubes (rolled-up cylinders of graphene in one-dimension), and (d) three-dimensional graphite (stack of graphene layers) [29].

2.3.1 Structure of graphene

Graphene consists of sp^2 hybridized carbon atoms. The sp^2 orbitals form three strong covalent bonds with the neighbouring atoms [25]. This strong bonding results in extraordinary mechanical strength making it stable while only being one atom thick [30]. The remaining *p*-orbitals are located over the surface of graphene and are responsible for current conduction. Figure 2.7 (a) gives a closer look at the lattice

structure of graphene. The graphene atoms are arranged in a triangular lattice with two atoms (A and B, as depicted in Fig. 2.7) per unit cell. The lattice vectors a_1 and a_2 can be written as [25]:

$$a_1 = \frac{a}{2}(3, \sqrt{3}), a_2 = \frac{a}{2}(3, -\sqrt{3}), \tag{2.4}$$

where a = 1.42 Å is the distance between two adjacent carbon atoms. The reciprocal lattice vectors b_1 and b_2 can be written as:

$$b_1 = \frac{2\pi}{3a}(1, \sqrt{3}), b_2 = \frac{2\pi}{3a}(1, -\sqrt{3}). \tag{2.5}$$

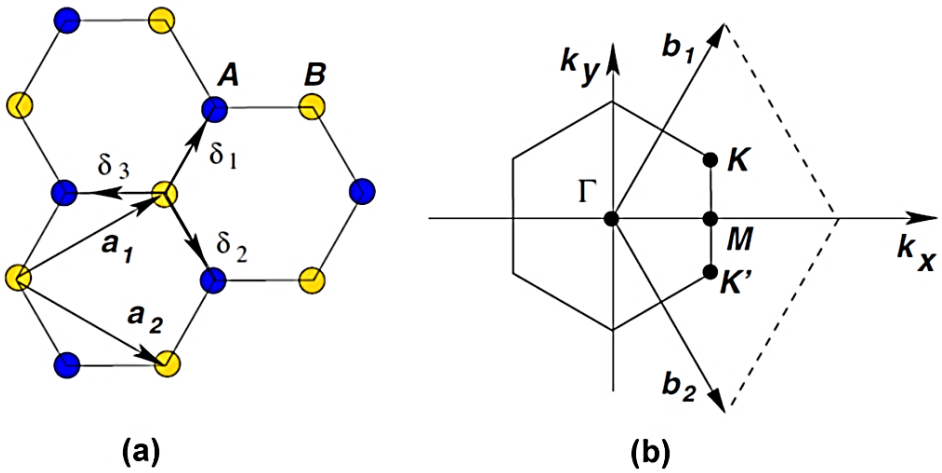

Figure 2.7 (a) Honeycomb structure of graphene is made out of two triangular lattices (where a_1 and a_2 are the lattice unit vectors). (b) Brillouin zone of the corresponding lattices showing the points K and K' where Dirac cones are located [25].

As shown in Fig. 2.7 (b), two points K and K' at the corner of Brillouin Zone are known as the Dirac points. The position of these points in space can be given as [25]:

$$K = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right), K' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right) \tag{2.6}$$

The free electrons of graphene are responsible for forming π bonds. The presence of two atoms, gives rise to two bands known as the valence band from the π bonding states and the conduction band from the π* anti bonding states. These valence and conduction bands are cone shaped and degenerate only at K and K' of the Brillouin

zone. Hence, graphene is a semimetal or a semiconductor with zero bandgap. At low energies, the energy bands can be derived based on tight binding calculations:

$$E_{\pm} = \pm t\sqrt{3 + f(k)} - t' f(k), \tag{2.7}$$

where t and t' are the nearest neighbour hopping energy (hopping between different sublattices) and next nearest neighbour hopping energy (hopping in the same sublattice), respectively and $f(k)$ can be given as [25]:

$$f(k) = 2\cos\left(\sqrt{3}k_y a\right) + 4\cos\left(\frac{\sqrt{3}}{2}k_y a\right)\cos\left(\frac{3}{2}k_x a\right). \tag{2.8}$$

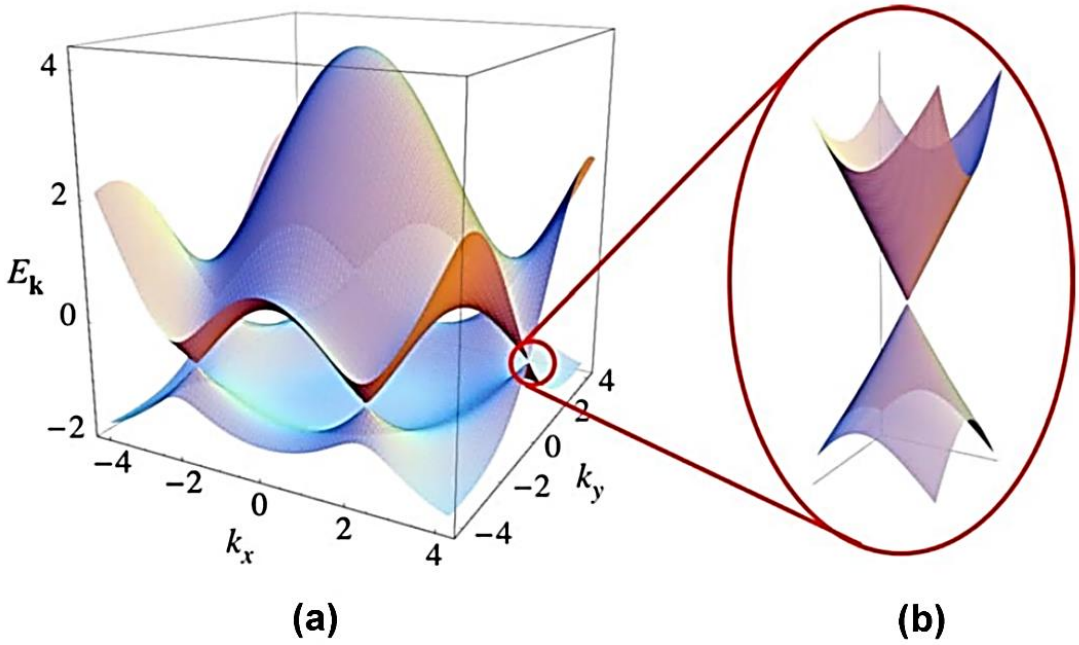

Figure 2.8 (a) Energy spectrum of Brillouin zone showing the Dirac points. (b) Zoom of dispersion relation close to one of the Dirac point [25].

The plus sign in Eq. 2.7 represents the π* band and minus sign is for lower energy band π. The π and π* bands touch each other exactly at the Dirac points K and K' at the corners of the Brillouin zone. Figure 2.8 (a) shows the results of Eq. 2.7 using t' = -0.2t. For $t' \neq 0$, the electron-hole symmetry is broken and the π and π* bands become asymmetric.

A linear dispersion can be obtained by expanding full band structure close to the K points as shown in Fig. 2.8 (b). For $k = K + q$, $|q| << |K|$, and t'= 0, linear dispersion can be written as:

$$E_{\pm}(q) \approx \hbar v_F |q| + O\left[(|q|/|K|)^2\right], \tag{2.9}$$

where q is the momentum measured with respect to the Dirac point , $\hbar$ is the reduced Plank's constant, and $v_F \approx 1\times10^6$ m/s. These results were first obtained by Wallace in 1947 [31]. In undoped graphene, the Fermi energy lies exactly at the Dirac point, i.e., the π and π^* bands are completely filled and empty, respectively. Detailed calculation of band structure can be found elsewhere in refs. [25],[31].

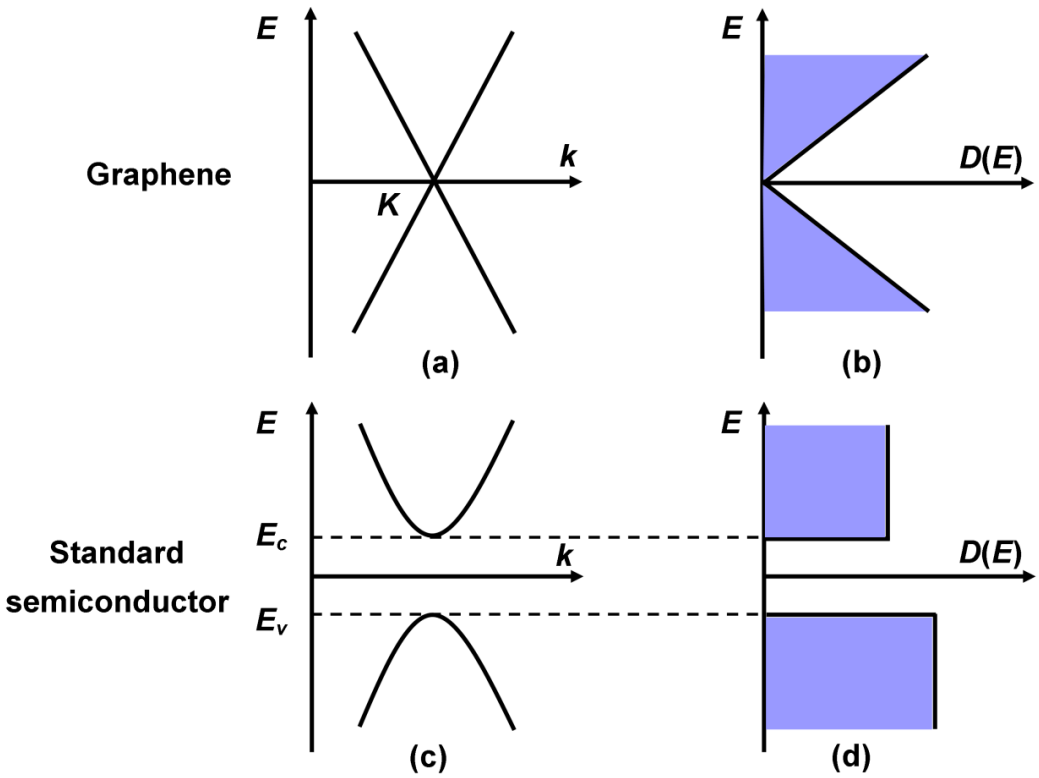

Figure 2.9 Comparison between graphene and standard semiconductor. Schematic illustration of (a) the band structure of graphene around the Dirac Point, (b) density of states of graphene, (c) the band structure of a standard semiconductor with direct bandgap, and (d) two-dimensional density of states for a semiconductor.

The linear dispersion relation around the Dirac points, the absence of a bandgap and the electron-hole symmetry differentiates graphene from standard semiconductors as shown in Fig. 2.9. The conduction and valence bands of graphene degenerate only at the Dirac points with a linear dispersion $E_{\pm}(q) \approx \hbar v_F |q|$ as illustrated in Fig. 2.9 (a).

Considering four-fold degeneracy due to the spin and valley degeneracy, this dispersion leads to a two-dimensional density of states $D(E) = 2|E| / \pi\hbar^2 v_F{}^2$. However, the density of states vanishes at the Dirac point for ideal graphene as shown in Fig. 2.9 (b). The dispersion of typical direct band gap semiconductor is depicted in Fig. 2.9 (c). It is a parabolic with a bandgap between the conduction and valence bands. The conductance band dispersion is similar to valence band and can be given as $E = E_c + (\hbar^2 k^2 / 2m^*)$, where m^* is the effective electron mass. The density of the function is zero for the region where the bandgap exists and is constant in the valence and conduction band region ($D(E) = m^* / \pi\hbar^2$).

Bilayer graphene, i.e., a stacking of two monolayers of graphene, also exhibits a zero bandgap, making it metallic at the neutrality point similar to that of a monolayer graphene. However, an applied back-gate voltage to the bilayer device not only changes the carrier concentration of bilayer graphene but also induces an asymmetry between two monolayers of graphene, resulting in a bandgap between the conduction and valence band [25],[29].

The low-energy of graphene can also be described by two-dimensional Dirac equation [25]:

$$-iv_F \sigma.\nabla \psi(r) = E\psi(r), \tag{2.10}$$

where $\sigma = (\sigma_x, \sigma_y)$ are the Pauli matrices. The band structure resulting from the honeycomb lattice means the electrons can be described as massless Dirac Fermions. The resulting quasiparticles can be described by two-component wavefunctions with an index to indicate sublattices A and B. This is similar to the spin in quantum electrodynamics (QED) and is referred as (pseudo)spin. In graphene, Pauli matrices relate to the (pseudo)spin rather than the electron spin. In addition, one can define the chirality as the projection of the (pseudo)spin on the wavevector *q*. The chirality for electrons and holes are positive and negative, respectively. Due to analogy between the charge carriers in graphene and QED, it is possible to exhibit QED-specific phenomena in graphene. These QED-related phenomena are inversely proportional to the speed of light and are expected to be enhanced by a factor of c/v_F = 300 [29].

2.3.2 Graphene synthesis

Since its discovery in 2004, several fabrication processes have been developed including micromechanical cleavage exfoliation of thick graphite [32], epitaxial growth by thermal decomposition of silicon carbide (SiC) [33]-[35], chemical vapor deposition (CVD) growth on a metal substrate [36]-[38], chemical reduction of graphene oxide films [39],[40], liquid-phase exfoliation [41], chemical exfoliation [42], and unzipping carbon nanotubes [43].

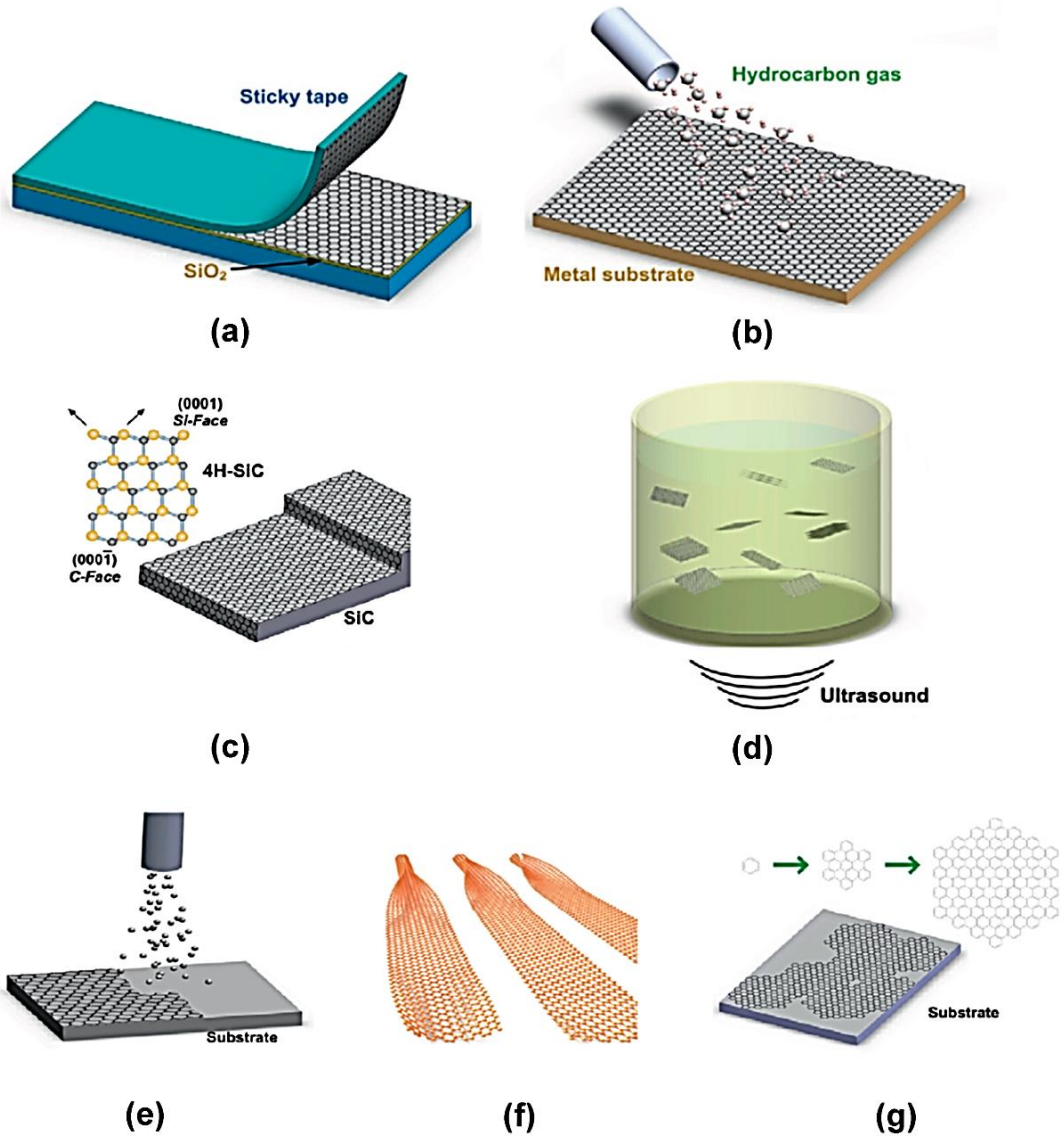

Figure 2.10 Schematic illustration of graphene fabrication techniques (a) micromechanical cleavage, (b) chemical vapor deposition, (c) growth on SiC, (d) liquid phase exfoliation, (e) molecular beam epitaxy, (f) unzipping carbon nanotubes, and (g) chemical synthesis using benzene as building block [44].

Figure 2.10 is the schematic illustration of a few of the graphene fabrication techniques. Among all of these methods, the mechanical exfoliation technique is used to produce the best quality graphene with ultra-high mobility μ, resulting in a large mean-free path length, i.e., $\lambda = (h/2e)\mu(n/\pi)^{1/2}$, at room temperature [45]. However, CVD growth on SiC or metals is most commonly used for large area and high throughput applications. Despite having slightly impaired electrical properties when compared to some other methods of graphene production, it is worth exploring CVD-grown graphene for future applications because it can be produced economically on a large scale [46].

In this research, the mechanical exfoliation and CVD techniques were used for producing monolayer graphene films onto a SiO_2 substrate. Heavily *p*-type doped Si was used as a back-gate substrate in all the samples. These samples were utilised for the fabrication of nanodevices in Chapters 4-6. The details about the synthesis process for the exfoliation and CVD techniques of graphene are given in Chapters 4 and 6, respectively.

2.4 Noise in semiconductor devices

In all semiconductor devices and systems, the current or voltage at their terminals is deviated from their steady state response due to the interference of spontaneous random fluctuations, which are usually referred as noise [47]-[50]. These fluctuations originate from external sources like AC power lines, adjacent circuits, electromagnetic transmission etc. or can arise from random and microscopic behaviour of electron transport, lattice defects, phonon scattering, and other physical processes within the device or system itself. Extrinsic noise can be eliminated by employing a better technology but the latter types of noise cannot be completely eliminated as it is inherent to the device. Therefore, intrinsic noise limits the accuracy of the measurements and sets a lower limit of detectable signals. Thus, the study of noise becomes very significant for the quality assessment of the semiconductor devices as well as can help in designing better quality devices [51]-[53].

This section briefly describes the various types of noises such as thermal noise [54]-[56], shot noise [57], recombination-generation (G-R) noise [58],[59], and 1/*f* noise

[60]-[65]. In chapter 3, low-frequency noise measurement of a ballistic rectifier is presented. A quantitative modelling of the observed noise properties have also been included in the same chapter.

2.4.1 Thermal noise

Thermal noise, also known as Johnson noise or Nyquist noise arises due to a very large number of independent random electron movements analogous to Brownian movement in a semiconductor device at non-zero temperature. This noise was first experimentally discovered in 1927 by Johnson [54],[55] and later explained by Nyquist in 1928 [56].

The free electrons in a device collide with other electrons resulting in a fluctuating current (or voltage) on the terminals. The power spectral density (PSD) of the thermal noise follows a Gaussian distribution and is also constant with frequencies typically in the microwave region and above. Thus, it is flat across the entire spectrum and is also known as white noise. The root-mean-square (rms) voltage v_{th} due to thermal noise over a frequency bandwidth Δf can be defined by the Nyquist equation as below [56]:

$$v_{th} = \sqrt{4k_B TR\Delta f} \tag{2.11}$$

where k_B is the Boltzmann's constant, T is the absolute temperature, and R is the resistance of the device. Thermal noise can also be defined in terms of the rms current i_{th} as:

$$i_{th} = \sqrt{\frac{4k_B T\Delta f}{R}} \tag{2.12}$$

The thermal noise is inherent to any semiconductor device due to non-zero resistance, hence is unavoidable. However, it can be reduced by employing a better design.

2.4.2 Shot noise

In 1918, W. Schottky first discovered the shot noise in vacuum tubes and presented the theory about its origin [57]. Unlike thermal noise, shot noise can be observed in a device when the current is flowing at non-equilibrium state. Several independent events, which occur randomly, can be considered to contribute to this type of noise

phenomena. The current flowing across a potential barrier, like a *p-n* junction, is of discrete nature due to the charge quantization. These moving charge carriers constitute the current across the barrier during a period of the time, and cross the barrier independently and randomly. The emission current is assumed to exhibit a shot noise. Based on the Schottky formula, the noise current i_{th} in the white spectrum can be given by [57]:

$$i_{th} = \sqrt{2eI\Delta f} \tag{2.13}$$

where I represents the current flowing across the device. The shot noise is a Poisson process and is mostly associated with photodiodes, Zener diodes, avalanche diodes, and Schottky diodes.

2.4.3 Generation-recombination noise

Generation-recombination noise in a semiconductor device is generated by the fluctuation of free charge carriers available for current transport due to the existence of traps or defects which randomly capture and emits these carriers [58],[59]. The traps in the semiconductor materials are formed due to the various defects or impurities available. A trapped charge carrier can also induce a secondary fluctuation in the mobility, electric field, barrier height, space charge region width etc. Consequently, a fluctuation in the resistance of the device occurs which can be easily detected by passing a DC current through the device.

The G-R noise was first observed in 1951, since then several experiments have been performed in order to develop the underlying theories. The PSD of G-R noise can be described as [58]:

$$\frac{S_R(\omega)}{R^2} \equiv \frac{S_G(\omega)}{G^2} \equiv \frac{S_N(\omega)}{N^2} = \frac{\overline{\Delta N^2}\tau_N}{N^2\left[1+(\omega\tau_N)^2\right]} \tag{2.14}$$

where $S_R(\omega)$, $S_G(\omega)$, and $S_N(\omega)$ are the PSDs of resistance, conductance, and carrier number, respectively. $\omega = 2\pi f$ represents the angular frequency. R, G, and N are the resistance, conductance, and average number of free carriers, respectively. $\overline{\Delta N^2}$ and

τ_N are the variance of fluctuation in the carrier number and the lifetime of a carrier, respectively. The spectrum of PSD given by Eq. 2.14 is of Lorentzian shape as illustrated in Fig. 2.11. The PSD is constant up to $f = 1/2\pi\tau_N$ and thereafter decreases inversely proportional to the square of frequency.

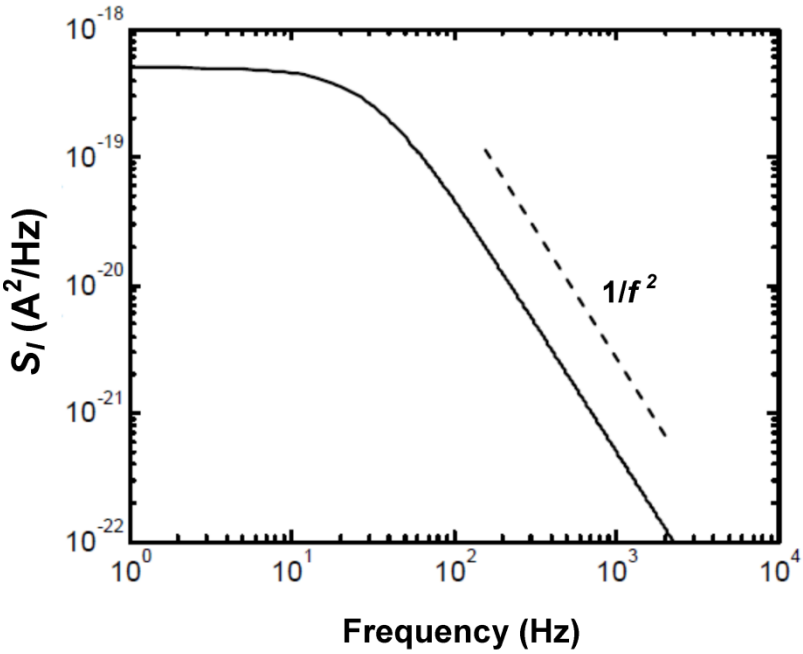

Figure 2.11 Current noise power spectral density of G-R noise as a function of the frequency. The G-R noise spectrum has a Lorentzian shape [66].

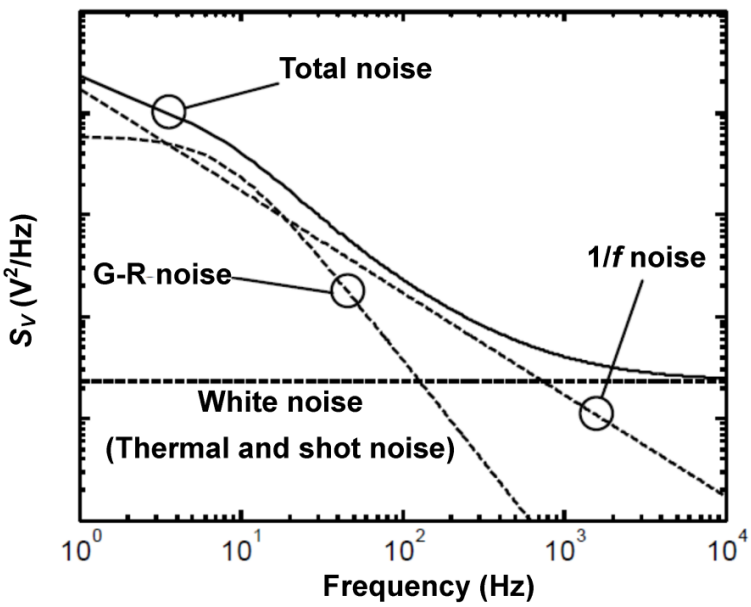

Figure 2.12 Voltage noise power spectral density with respect to the frequency. Total noise in a semiconductor device is a superposition of various types of noises such as white noise (thermal and shot noise), g-r noise, and $1/f$ noise [66].

The G-R noise can be considered as an excess noise and it can be detected by measuring the current and voltage fluctuations in the presence of an external bias. Normally, the measured PSD of any device is consisting of different types of noises including thermal noise, shot noise, and excess noise e.g. G-R noise and 1/*f* noise (will be discussed later) as shown in Fig. 2.12. The PSD of total noise S_{Total} can be written as:

$$S_{Total} = S_{White} + S_{Excess} \tag{2.15}$$

where S_{White} and S_{Excess} are the PSD due to the white noise (thermal and/or shot noise) and excess noise (G-R and/or 1/*f* noise), respectively.

2.4.4 Flicker noise

When a semiconductor device with a resistance of *R* is in potential equilibrium at a temperature *T*, thermal noise is observed due to the Brownian movement of the electrons. If a current flows through the device, there will no longer be equilibrium and an additional noise may be observed. The power spectrum of this observed noise is proportional to the current and increases as an inverse of the frequency, therefore this noise is referred as 1/*f* noise or flicker noise [60]-[65].

The 1/*f* noise is dominant at low frequencies (up to 10^{-6} Hz) and can be suppressed at higher frequencies typically above several kHz. The 1/*f* noise is not only observed in wide variety of semiconductor devices under biasing conditions but also in a diverse range of observations elsewhere. In 1978, Gardener reported this noise in connection with the height of river Nile followed by the Machlup's experiment in 1981, in which he observed it in earthquakes and thunderstorms. Biological systems and musical instruments also exhibit the 1/*f* noise [50]. In this work, we will restrict ourselves to the 1/*f* noise due to electrical conductance only.

The main reason for the generation of 1/*f* noise in a semiconductor device is material defects and fabrication imperfections. The 1/*f* noise is sometimes used to model the fluctuations of the device parameters with time. There are two main physical mechanisms behind any fluctuation in the current i.e the fluctuations in the number of carriers or the fluctuations in mobility. Based on these physical mechanisms, two different competing models have appeared in the literature to explain 1/*f* noise. The first model is based on a number fluctuation known as the surface model developed

by McWorther in 1957 [60] whereas the second model is a mobility fluctuation based bulk model proposed by Hooge in 1969 [61]. Both theories are supported by the several experimental facts, thus the noise community is divided in to two groups over the noise.

Number fluctuation model

A very simple and the most accepted model for the noise characterisation in metal-oxide semiconductor transistors (MOST) was proposed by McWorther [60]. This model suggests that the 1/*f* in MOST originated due to the trapping of charge carriers in the traps located along the semiconductor-oxide interface. Therefore, it is assumed that the 1/*f* noise is caused by the G-R process between the traps and the conduction band at the surface. When many different spectras of G-R noise, where free carriers are randomly and independently trapped and released with different lifetime, are superimposed, one can obtain the 1/*f* noise spectra created from the Lorentzian process as shown in Fig. 2.13.

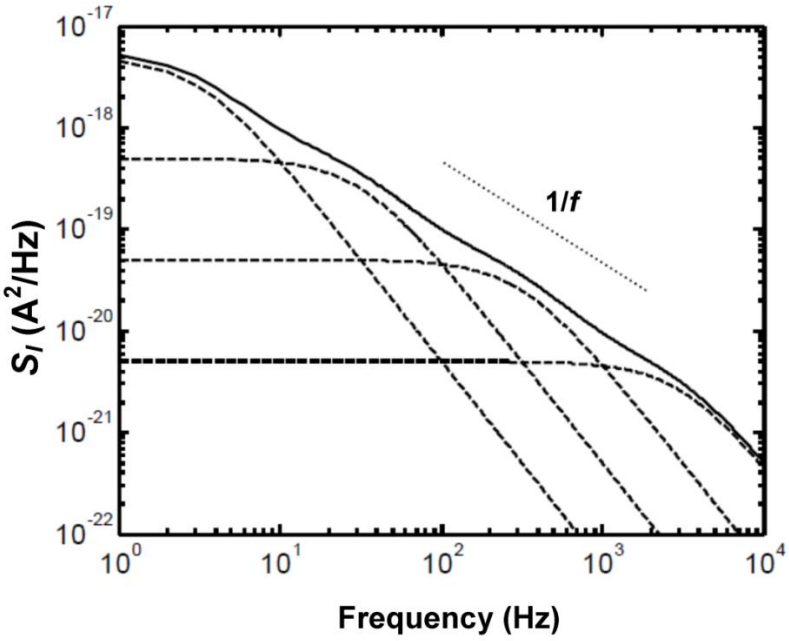

Figure 2.13 The 1/*f* noise can be achieved by sumperimposing the different G-R noise spectras of Lorentzian shape [66].

Despite of its popularity this model could not explain the 1/*f* noise in a wide variety of devices that were not the interface between two materials. However, it is widely accepted that the trapping and de-trapping processes are the main cause of 1/*f* noise. The latter noise experiments, performed by Hooge and Hoppenbrowers on

continuous gold films, strongly objected to Mcworther model with an explanation that the 1/*f* noise is a bulk effect rather than a surface effect [61].

Mobility fluctuation model

While working on this noise with continuous gold films, Hooge in 1969 interpreted 1/*f* noise as a bulk effect [61]. Mobility fluctuation is the origin of the noise in this model; hence, it is known as the mobility fluctuation model or sometimes also referred to as Hooge model. The empirical relation for the 1/*f* in a homogenous sample can be written as [67]:

$$\frac{S_I}{I^2} = \frac{S_V}{V^2} = \frac{S_G}{G^2} = \frac{\alpha_H}{N}\frac{1}{f}\,, \tag{2.16}$$

where S_I, S_V, and S_G are the PSDs of current, voltage, and conductance, respectively, N is the number of charge carriers and α_H is a dimensionless constant referred to as Hooge's constant with a value of about 2×10^{-3}.

The conductivity σ of an extrinsic semiconductor is given as:

$$\sigma = \frac{q}{V_S}\sum_{i=1}^{N}\mu_i = \frac{qN\overline{\mu}_i}{V_S} = qn\overline{\mu}_i = qn\mu\,, \tag{2.17}$$

where N is the number of conducting carriers in a volume V_S. μ_i represents the mobility of an individual carrier, $n = N/V_S$ is the charge carrier density, and $\overline{\mu}_i = \mu$ is the average of μ_i.

The conductivity fluctuates due to the fluctuations in individual carriers and can be written as:

$$\Delta\sigma = \frac{q}{V_S}\sum_{i=1}^{N}\Delta\mu_i\,. \tag{2.18}$$

Assuming that the fluctuations in the carriers are independent of each other, hence, $\overline{\Delta\mu_i.\Delta\mu_j} = 0$ for $i \neq j$, and

$$\overline{(\Delta\sigma)^2} = \frac{q^2}{V_S{}^2}\sum_{i=1}^{N}(\Delta\mu_i)^2 = \frac{q^2}{V_S{}^2}N\overline{(\Delta\mu_i)^2} = q^2n^2\frac{\overline{(\Delta\mu_i)^2}}{N}\,. \tag{2.19}$$

Therefore, the PSDs of conductance (S_σ), average mobility (S_μ), and individual mobility can be written as:

$$\frac{S_\sigma}{\sigma^2} = \frac{S_\mu}{\mu^2} = \frac{S_{\mu_i}}{N\mu_i^2}. \tag{2.20}$$

Using Eqs. 2.16 and 2.20, the PSD of individual mobility fluctuation of a free charge carrier then becomes:

$$\frac{S_{\mu_i}}{\mu_i^2} = \frac{\alpha_H}{f}. \tag{2.21}$$

The above expression suggests that the mobility of an individual free charge carrier fluctuates with $1/f$ spectrum. Therefore, α_H is dependent on the variance of the mobility of the individual carrier without having any dependence on the number of carriers.

The Hooge's mobility fluctuation model has been employed successfully to explain $1/f$ noise in bulk semiconductors and metals, even though there is no fundamental strong explanation behind the mobility fluctuations. Several attempts have been made to develop theoretical background to support Hooge's mobility fluctuation theory including energy fluctuation theory [68] and Handel's quantum theory [65] (which will be discussed in Chapter 3) but so far none of them is widely accepted. Despite of this $1/f$ noise, in wide variety of semiconductor devices, is still being described efficiently by the empirical relation of Hooge's model.

2.5 Planar nanoelectronic device

2.5.1 Ballistic rectifier

The first ballistic rectifier was fabricated from modulation doped GaAs/AlGaAs heterostructures, which contained a 2DEG located 37 nm below the wafer surface [69]. The sheet carrier density and mobility of 2DEG at a temperature of 4.2 K were about 5×10^{11} cm^{-2} and 5×10^{5} cm^2/V.s, respectively. The ballistic rectifier was made of a nanoscale ballistic cross junction and a triangular antidot at the centre. The device geometries were defined using electron-beam lithography (EBL) and wet chemical etching. Due to the insertion of a triangular antidot at the centre of the device, the device symmetry was broken and as a result an unusual nonlinear voltage-current characteristic was observed. Since the size of the central part of the

device was much smaller than the electron mean-free path (~5.8 μm) at 4.2 K, the electron transport was ballistic.

Figure 2.14 (a) shows an atomic-force micrograph of the central part of a typical ballistic rectifier fabricated from the 2DEG of an InGaAs/InP substrate. The deep trenches were chemically etched away from the sample forming a triangular antidot and insulating lines between the channels. The four channels, i.e., source, drain, upper, and lower, are denoted as *S*, *D*, *U*, and *L*, respectively. The arrow indicates the typical trajectories of electrons originating from *S* and *D* and suggests that the electrons will always be accumulated at the *L* terminal. As a result, a negative voltage V_{LU} will be induced irrespective of the electron originating terminal. This entirely different working principal is similar to that of a bridge rectifier which requires four individual diodes as sketched in Fig. 2.14 (b).

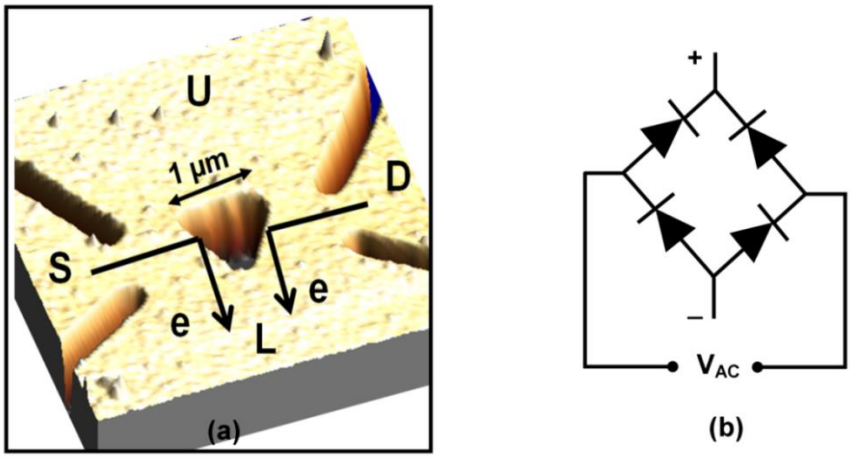

Figure 2.14 (a) Atomic-force microscope image of the central part of a ballistic rectifier. The trenches were etched away by wet chemical etching, forming a triangular antidot in the middle and four channels *S*, *D*, *U*, and *L*. The input current is applied through *S* and *D* while the output is measured between *L* and *U*. The arrows show the typical electron trajectories originating from *S* and *D*. However, the device operation is based on a new working principle but is similar to that of a bridge rectifier as shown in (b).

The input current was applied to the device through the *S* and *D* terminals, while the output V_{LU} was measured between the *L* and *U* terminals. The electrons can only be transmitted when the applied current is non-zero, i.e., $I_{SD} \neq 0$ [70]. The applied electric field between *S* and *D* decides the electron transmission along the trajectories. Due to the mirror symmetry along the central *L* and *U* axis, the V_{LU} is expected to remain the same even if the sign of I_{SD} is changed as below [69]:

$$V_{LU}(I_{SD}) = V_{LU}(-I_{SD}). \tag{2.22}$$

Figure 2.15 shows the V_{LU}-I_{SD} characteristics of the device measured at T = 4.2 K (solid line) and 77 K (dotted line). The ballistic rectifier worked well at helium temperatures, as temperature increased from T = 4.2 K to T = 77 K, a weaker rectification was observed due to more electron scattering from the phonons as the mean free path length became shorter (about 1-2 μm) [69]. The devices fabricated without a triangular antidot at the centre have also exhibited a similar rectifying effect [71]-[73].

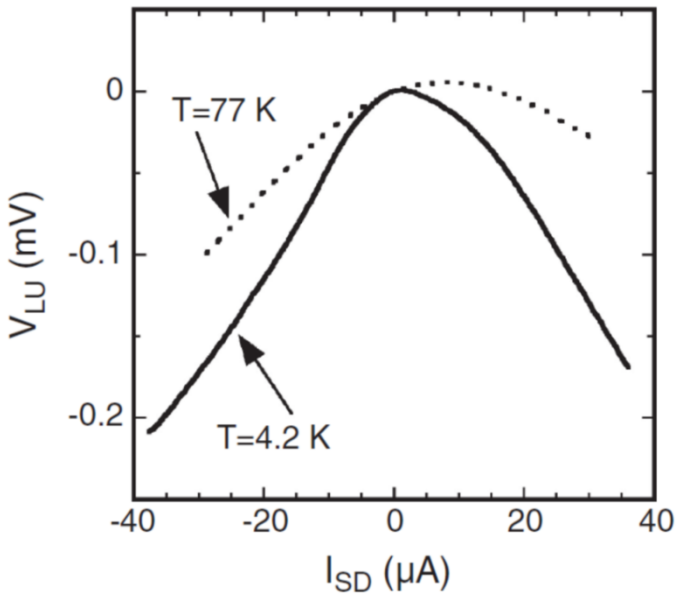

Figure 2.15 The output voltage measured between L and U as a function of input current through S and D at T = 4.2 K (solid line) and 77 K (dotted line) [69]. Ideally the curve should be symmetric at the both sides of I_{SD} = 0 V. However, due to fabrication imperfections a slight asymmetry was observed.

The nonlinearity in V_{LU}-I_{SD} characteristics was observed as a consequence of inserting a triangular antidot at the centre of the device. Hence, this artificial scatterer plays a vital role in inducing a rectifying effect from the device without any doping junction or barrier structure along the direction of current conduction [69]. Due to the in-plane nature of the device geometry, i.e., the electrical contacts are in the same plane of the device active region, the parasitic capacitance between contacts is substantially smaller than that of a conventional vertical device of the same size. Furthermore, the device is able to detect very small signals without need of any external bias [74].

The ballistic rectifier, fabricated from InGaAs/InP has been demonstrated to work up to 50 GHz as shown in Fig. 2.16 [75]. However, the cut-off frequency of the device was estimated to be much higher possibly up to the THz regime as envisaged by the Monte Carlo (MC) simulations [76],[77]. The inset of Fig. 2.16 shows that the rectified output was linearly proportional to the applied input microwave power, which means that the device was exhibiting square-law operation [75]. This unique characteristic of the device allows for the generation of second harmonic signals without producing third or higher harmonics [78]. Despite impedance mismatch, estimated voltage responsivity of the device was found in the order of few hundreds of millivolts per milliwatt [75].

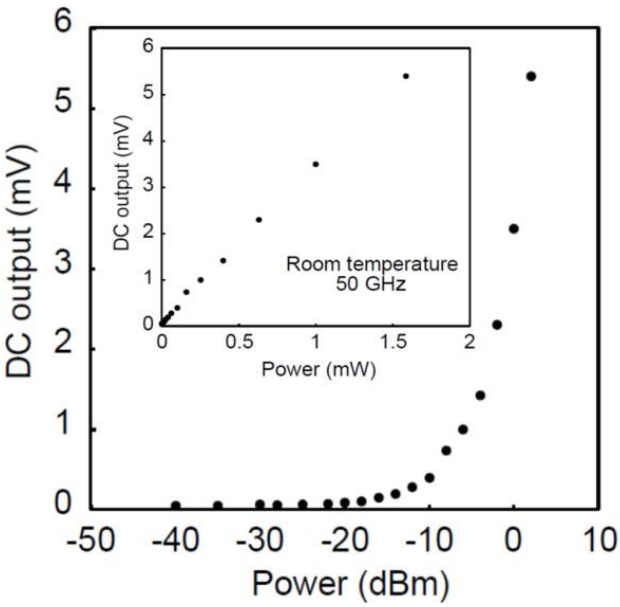

Figure 2.16 Room temperature output DC voltage of a ballistic rectifier as a function of microwave power applied at 50 GHz [75]. Inset shows the linear dependence of rectified output on applied microwave power which means that the device was operating in the square-law region.

2.5.2 Self-switching device

A new type of unipolar nanodiode also known as self-switching device was conceptualised and realised by Song *et al.* in 2003 [79],[80]. Figure 2.17 (a) shows the schematic illustration of a typical SSD fabricated from a hetereostructure. Being a unipolar two-terminal device, SSD exhibits a nonlinear current-voltage (*I-V*) characteristic which resembles to that of a conventional diode, as shown in Fig. 2.18 (a), but without using doping junctions or tunnelling barriers.

SSD can be fabricated by tailoring two L-shaped trenches to break the symmetry of a narrow semiconductor channel by using standard nanolithography e.g. EBL and an etching process. The operation of the SSD resembles to that of a side gated transistor (SGT) which is based on an electrostatic modulation of charge carriers caused by in-plane gated structures at the both sides of the etched channel [81]. These channels introduce depletion regions because of the surface states at the etched geometries, meaning the effective channel width of a SSD is actually narrower than its physical size as shown in Fig. 2.17 (b). The depletion region tries to pinch-off the effective channel at unbiased conditions. An applied voltage *V*, to the right side of the device in Fig. 2.17 (a), not only changes the potential profile along the channel but also either narrows or expands the effective channel width depending upon the sign of voltage. If a negative *V* is applied, the negative charge wells around the trenches completely pinch off the channel and as a result no current can flow through the channel as illustrated in Fig. 2.17 (c). In contrast, a positive *V* in Fig. 2.17 (d) widens the channel width by counteracting the lateral depletion region due to the electric field from the both sides of the trenches. This allows current to flow easily and gives a rise to diode like *I-V* characteristic as shown in Fig. 2.18 (a) [79]. Unlike a conventional diode, the mechanism of an SSD is based on the geometrical symmetry breaking at the nanoscale.

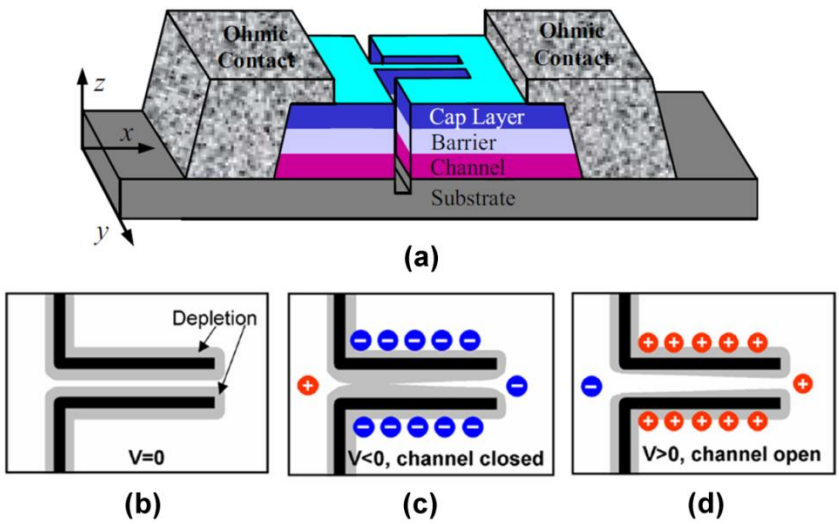

Figure 2.17 (a) Three-dimensional schematic view of a typical SSD including the details of a heterostructures [82]. (b) Due to the surface states on the etched trenches, the channel is depleted at $V = 0$ V. (c) At negative bias ($V < 0$), the effective channel is closed. (d) A positive voltage ($V > 0$) increases the effective channel width for the current conduction. This self-switching mechanism gives a rise to diode-like *I-V* characteristic [79].

Turn-on voltage of the SSD can be tuned by varying the physical width independent of material property as shown in Fig. 2.18 (b) [79],[83]. As expected, the narrower channel SSD exhibits a large turn-on voltage. This functionality offers greater flexibility making it ideal for radio frequency (RF) applications. The MC simulation of the potential barrier in three-dimensional and one-dimensional along the channel of the SSD is shown in Figs. 2.19 (a) and (b), respectively [83]. As expected, a positive *V* to the right terminal lowers the potential barriers which allow electrons to move freely into the channel. While a negative *V* impedes the electron conduction which results in a nonlinear *I-V* characteristic of the device.

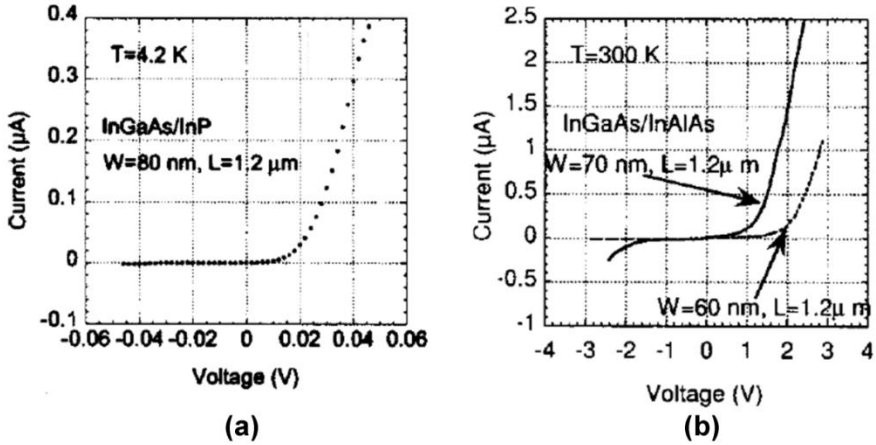

Figure 2.18 (a) *I-V* characteristics at T = 4.2 K of an SSD fabricated from InGaAs/InP substrate with channel width (W) and length (L) of 80 nm and 1.2 μm, respectively [79]. (b) *I-V* characteristics of two SSDs fabricated on InGaAs/InAlAs substrate with different W and L = 1.2 μm. Turn-on voltage of the device was increased when W decreased from 70 nm to 60 nm [79].

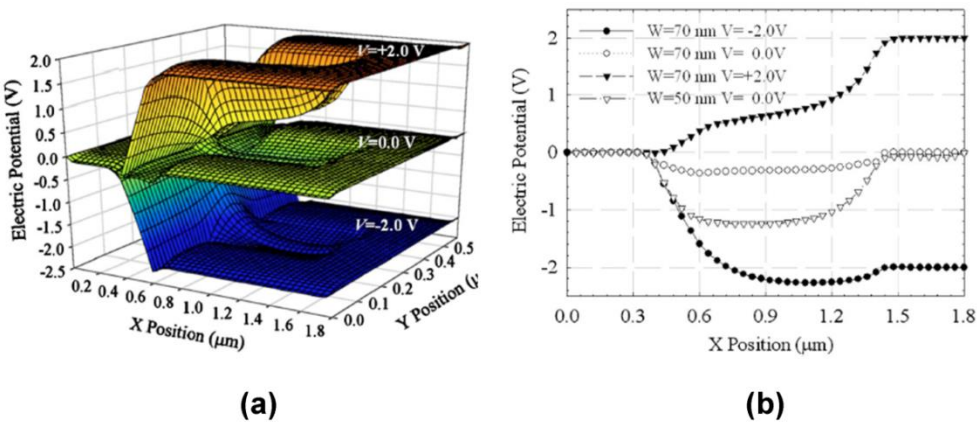

Figure 2.19 Electric potential along the channel in a SSD with W = 70 nm for applied voltages V = -2, 0, +2 V, respectively (a) Three-dimensional chart and (b) one-dimensional profile [83]. The potential profile at equilibrium for the SSD with W = 50 nm is also plotted.

Since its inception, SSDs have been realised in a variety of materials including 2DEG in InGaAs [79],[84], GaAs [85], GaN [86],[87], InAs [88],[89], silicon-on-insulator (SOI) [90],[91], and both organic [92],[93] and metal oxide [94]-[96]. The room temperature detection of microwave [95], [97]-[99] and THz frequencies [85]-[89] and MC simulations [100]-[104] showing the possibility as a THz emitters are a few of the recent developments.

The device planar architecture simplifies the fabrication process of the device. Hence, a large number of SSDs can be connected in parallel by placing the individual devices next to each other without the need of interconnection layer. More importantly, large area and cost effective lithography techniques such as nanoimprint lithography can be utilised to define high density integrated structures [93],[105]. Another benefit of fabricating a large array of SSDs is the reduction in the overall device impedance which in turn improves the noise performance of the device [106]. Figure 2.20 (a) shows approximately 2000 SSDs connected in parallel fabricated by EBL. The large array reduced the overall impedance of the device improving the impedance mismatch; as a result the low-frequency noise in Fig. 2.20 (b) was improved significantly without reducing the detection sensitivity which is comparable with state-of-art Schottky diodes [106].

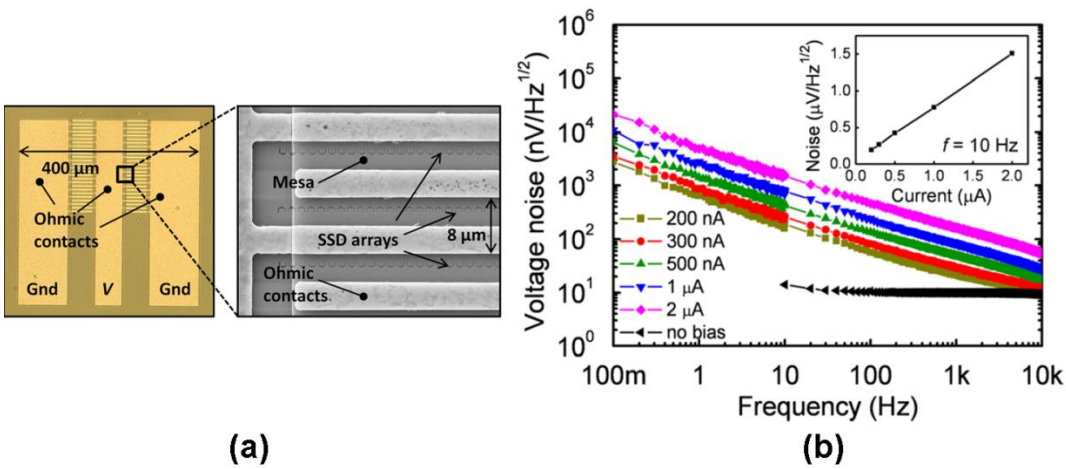

Figure 2.20 (a) Optical image of the interdigital structure and coplanar waveguide with scanning electron microscope (SEM) of SSDs array fabricated within the interdigital structure fingers. (b) Room-temperature voltage-noise spectra of the SSD array measured at different biases. The inset shows the linear dependence of the voltage noise as a function of the current at 10 Hz [106].

The nonlinear behaviour of the SSD is the greatest advantage over a conventional device since its planar architecture provides a low parasitic capacitance which allows the high speed rectification at 1.5 THz at room temperature [85] and 2.5 THz below 2.5 K [84]. A zero-turn-on voltage can be achieved by carefully designing the channel width which allows SSD to be used for RF rectification without requiring any external bias.

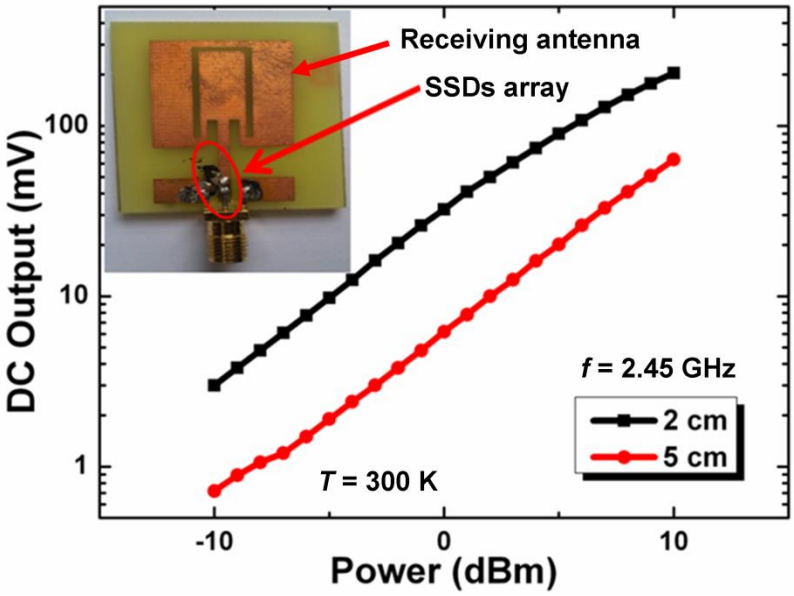

Figure 2.21 Rectified DC output voltage (by SSDs array coupled to microstrip antenna) as a function of transmitted power at 2.45 GHz at room temperature. Both the transmitting and receiving antennas were kept at 2 and 5 cm far away from each other. The CPW-fed C slot microstrip antenna coupled with the SSDs array is shown in the inset [99].

Low-cost semiconductor materials such as polymer and metal-oxide (ZnO) thin films have demonstrated the RF rectification even though their mobilities are relatively low [92],[93]. This will open up opportunities in the RF field where simple and low cost technology is required. An ideal application would be to use them for RF energy harvesting [107] or as a radio frequency identification (RFID) tags [108]. Recently, SSDs array shown in Fig. 2.20 (a) was coupled with CPW-fed C slot microstrip antenna, as shown in the inset of Fig. 2.21, to work at 2.45 GHz for such applications [99]. In this experiment, RF signals received by the antenna were directly coupled to the device which in turn produced a rectified DC output voltage. A similar antenna was used for transmitting the RF signals generated by a microwave source.

2.6 Conclusions

The basic properties and physics background for some topics related to this research is presented in this chapter. Understanding III-V semiconductors including heterostructures and 2DEG layers was helpful while doing experiments with the ballistic rectifier in Chapter 3, which was fabricated from 2DEG in InGaAs/InP heterostructures. The electronic transport phenomena in mesoscopic nanostructures have also been described briefly. The next section dealt with the structural and electronic properties of graphene followed by the graphene synthesis techniques. The more details about the graphene fabrication process using exfoliation and CVD techniques are given in Chapters 4 and 6, respectively.

Some fundamentals of noise, which is a natural phenomenon associated with every semiconductor device, are then presented. The white noise is quite unavoidable and ubiquitous, however the $1/f$ noise may be avoided in well-designed semiconductor devices as it depends upon the material defects, interfaces or fabrication imperfection. Hence, the $1/f$ noise component has been used as a reliability or diagnostic tool for the analysis of the ballistic rectifier in Chapter 3.

In the last section, a brief introduction of the ballistic rectifier and SSD has been given as these devices were the centre of the research. Both the devices exhibit nonlinear characteristics and can be employed in many practical applications including RF detection. The next few chapters are solely dedicated to optimise the device properties fabricated from III-V semiconductor and graphene.

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Chapter 3

Low-frequency noise of a InGaAs/InP ballistic rectifier

3.1 Introduction

Due to the planar nature of the device architecture, i.e., the contacts are in the same layer as the device active region, the ballistic rectifiers demonstrate very small internal capacitance [1], [2]. Thus, the frequency response does not suffer as much RC charging time limitations in contrast to conventional vertical multilayered diode structures of same size. With this low parasitic capacitance and the ballistic nature of electrical transport, it is possible to develop ballistic rectifiers for GHz and THz applications as envisaged by Monte Carlo (MC) simulations [3], [4]. The room temperature operations of such devices have been demonstrated up to a frequency of 50 GHz. The voltage responsivity of these devices was estimated to be in the order of few hundred millivolts (mV) of dc output per milliwatt (mW) of input power [5].

For comparison with commercially available microwave and THz detectors, the noise properties of the ballistic rectifier are as important as its speed. In most of the terahertz applications, the rectifiers are modulated at low frequencies and the signals are detected by utilizing the direct or heterodyne detection scheme [6]. Hence, the low-frequency noise properties of the ballistic rectifiers are a significant to be studied. The low-frequency noise is considered as an excess noise which arises in a

device due to material defects and/or fabrication imperfections [7]. A well-engineered semiconductor device does not demonstrate this excess noise. Therefore, the low-frequency noise is commonly being used as an indicator of quality and reliability for the analysis of various devices [8]-[12].

In this experiment, a ballistic rectifier was fabricated onto a high-mobility two-dimensional electron gas (2DEG) in an InGaAs/InAlAs heterostructure material. Details of the device fabrication process are included in this chapter. The device was characterised at room temperature up to 3 GHz (the highest frequency generated by the network analyser). The later sections of this chapter elaborate the low-frequency noise characterisation and noise equivalent power (NEP) of the ballistic rectifier. The observed noise findings were analysed using different theories of flicker noise. Furthermore, a quantitative model of the observed noise at finite biases in a device with variable width along the channel was proposed which revealed that the narrowest part of the electron channels had a dominant role in the device noise properties.

3.2 Device fabrication

The Ballistic rectifier was fabricated out of a commercially available lattice matched InGaAs/InAlAs heterostructures grown on InP substrate (purchased from IQE Inc.). The 2DEG, where the electron charge carriers are confined for current conduction, was located 25 nm below the top surface as shown in Fig. 3.1 (a). The room temperature carrier density and mobility, as determined from Hall measurements by van der Pau method, were 1.3×10^{12} cm^{-2} and 1.04×10^{4} $cm^{2}/V.s$, respectively which yielded a mean-free path length λ of 194 nm at room temperature. The first step in the fabrication of ballistic rectifier was the isolation of various radio frequency (RF) mesa structures. Photoresist S1805 was used as a mask layer for photolithography. Then orthophosphoric peroxide solution (H_3PO_4:H_2O_2:H_2O) was used as a wet chemical etchant. The ohmic contacts were fabricated by the thermal evaporation of 65 nm of Ge/Au/Ni alloy followed by 200 nm of Au and annealing at 260 °C for 90 seconds in the furnace with a flow of nitrogen gas. The positive resist polymethyl methacrylate (PMMA) with a molecular weight (MW) of 950 K, diluted in 4% anisole, was then used as masking layer on the samples. The electron-beam lithography (EBL) was used to expose the patterns for the ballistic rectifier into the

PMMA as shown in Fig. 3.1 (b). After development, the devices were etched through the 2DEG into the substrate using $Br_2/HBr/HNO_3$ based wet-chemical etching.

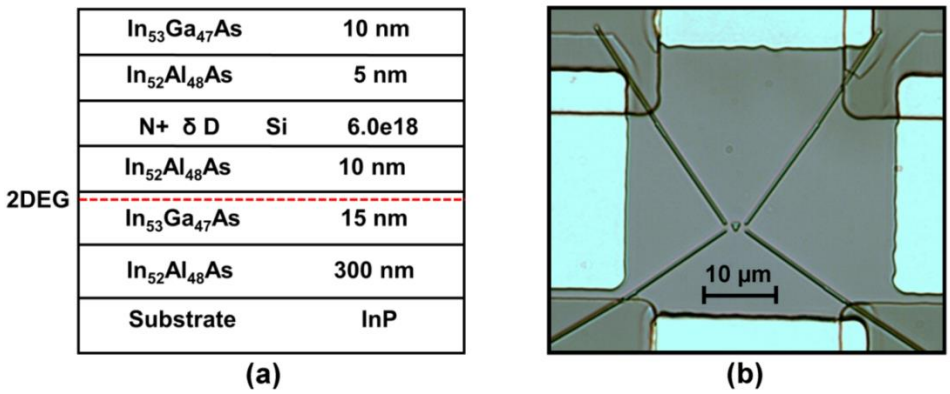

Figure 3.1 (a) Schematic structure of the material used for the device fabrication. (b) The optical microscopic image of a ballistic rectifier.

Figure 3.2 (a) shows an atomic-force microscope (AFM) image of the central part of a fabricated ballistic rectifier. The lithographic width of source (*S*) and drain (*D*) channels was 800 nm while the width of the lower (*L*) and upper (*U*) channels was 2.6 μm. The triangular antidot (an artificial scatter), which was intentionally placed at the centre of the device, had an upper side length and height of 1 μm each. The arrows in Fig. 3.2 (a) indicate the typical direction of ejected electrons from the *S* and *D*.

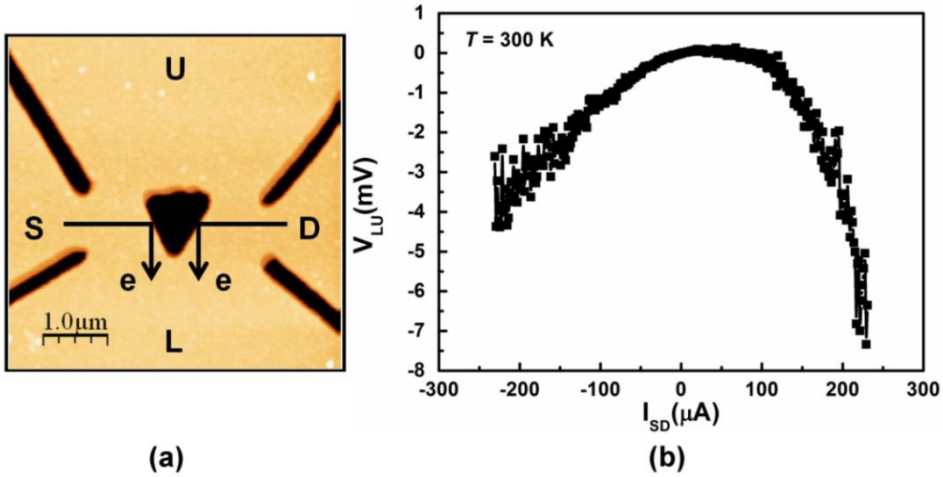

Figure 3.2 An atomic-force microscope image of the central part of a ballistic rectifier showing the direction of typical electrons trajectories from *S* and *D* guided by the antidot to the lower channel. (b) The output voltage V_{LU} between *L* and *U* terminals as a function of input current through *S* and *D* terminals. Slight asymmetry in the curve along $I_{SD} = 0$ was due to the fabrication imperfections.

The nanoscale triangular antidot placed at the centre of ballistic rectifier was responsible for the guided electron flow to the *L* terminal. The input signal was applied to the device through *S* and *D* terminals while detecting the output simultaneously at *L* and *U* terminals. The device geometry means that most of the electrons leaving *S* and *D* were diverted to *L* by the anitdot and as a result, a negative potential was developed between *L* and *U* irrespective of the current direction between *S* and *D* [1]. Figure 3.2 (b) shows the voltage-current (V_{LU}-I_{SD}) characteristic measured at room temperature. The curve demonstrated the geometrically induced non-linearity of the electrons transport. Furthermore, V_{LU}-I_{SD} characteristic exhibited almost mirror-like symmetry along the central *L*-*U* axis which can be described as [13]:

$$V_{LU}(I_{SD}) = +V_{LU}(-I_{SD}). \tag{3.1}$$

The small deviation from the desired symmetry was due to imperfections in the fabrication process, namely the lithography. The unique non-linear property of ballistic rectifier was the direct result of inserting a triangular antidot at the centre. This is an entirely different mechanism from that of a conventional diode where the nonlinearity relies on the intrinsic properties of semiconductors.

3.3 Microwave detection

In a pure ballistic regime of the electron transport, the output DC voltage (V_{UL}) between *U* and *L* terminals can be illustrated as [2]:

$$V_{UL} \approx \frac{3e}{8\pi E_F} \frac{N_{SD}\sin 2\theta_0}{2N_{LU} - 3N_{SD}(1-\sin\theta_0)^2} V_{SD}^2, \tag{3.2}$$

where V_{SD} is an applied AC voltage between the *S* and *D* terminals, N_{SD} is the number of propagating modes in the *S* and *D* channels while N_{LU} denotes the number of propagating modes in the *L* and *U* channels, *e* and E_F represents the electron charge and the Fermi energy, respectively and θ_0 is about π/4 depending upon the device geometry. The quadratic response of output voltage to input signal is independent of the temperature *T* in Eq. (3.2). However, the exponential response of a normal diode depends on k_BT, where k_B is the Boltzmann constant [14]. Therefore,

the rectification efficiency of ballistic rectifier is entirely independent on the temperature even when applied signal is very small [2].

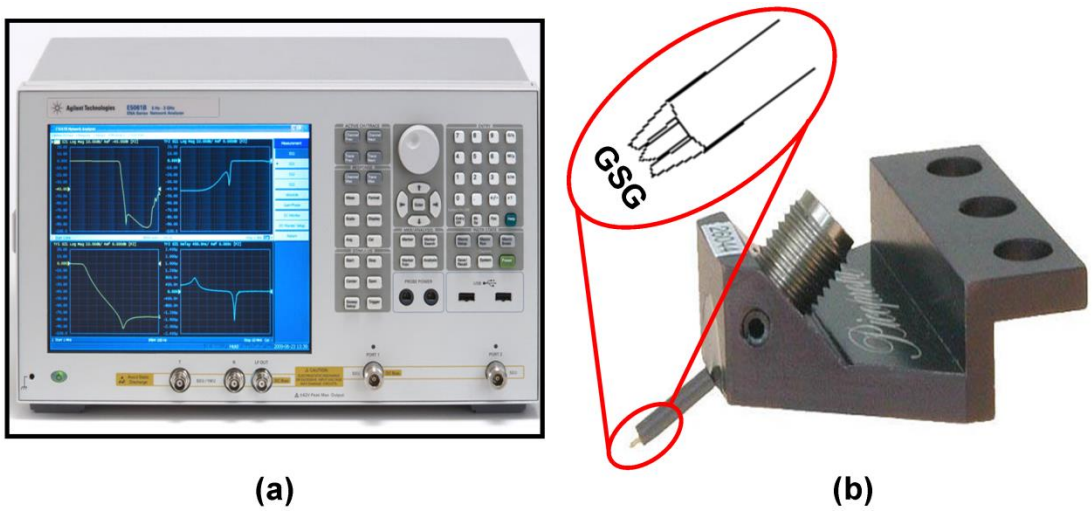

Figure 3.3 (a) Picture of an Agilent network analyser (model: E 5061B ENA Series) which is able to generate RF signal up to 3 GHz with maximum power of 10 dBm. (b) An example of a coplanar RF probe used for the measurements. The inset shows the ground-source-ground (G-S-G) configuration of the probe.

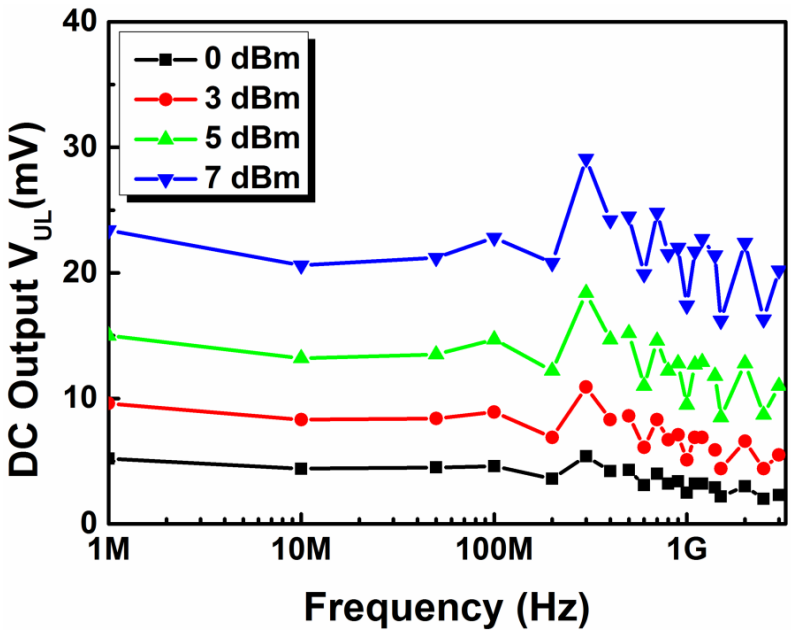

Figure 3.4 The output DC voltage V_{UL} measured between the U and L terminals as a function of signal frequency at the room temperature. The applied microwave signal was varied from 0 to 7 dBm.

In this experiment, the ballistic rectifier was characterised only up to a frequency of 3 GHz, which was the highest frequency generated by an Agilent network analyser (E 5061B) as shown in Fig. 3.3 (a). The coplanar probe with ground-source-ground

(G-S-G) configuration, as shown in Fig. 3.3 (b), was used to couple the microwave power at the input terminals of a ballistic rectifier. Figure 3.4 shows the room temperature output DC voltage as a function of signal frequency. The applied microwave signals were varied from 0 to 7 dBm. The measured results in Fig. 3.4 demonstrated the stable response of the device output in the frequency range from 1 MHz to 3 GHz.

Voltage responsivity (β_v) is a measure of detection sensitivity for a microwave detector. For the ballistic rectifier, it was estimated from the output DC voltage divided by the input microwave power. Figure 3.5 shows the measured responsivity of the device and it was found to be constant between 3.1 to 5.3 mV/mW in the frequency range from 1 MHz to 3 GHz. It is worth mentioning that the above responsivity was achieved at room temperature meaning that only a few electrons can move without many scattering events. Furthermore, the device impedance (Z_{BR}, 3.5 kΩ) was much higher than the impedance of the network analyser (Z_{NA}, 50Ω), hence there was a large impedance mismatch between the device and the signal generator. The actual power delivered (P_d) to the ballistic rectifier can be estimated as [15]:

$$P_d = P_i - P_r, \tag{3.3}$$

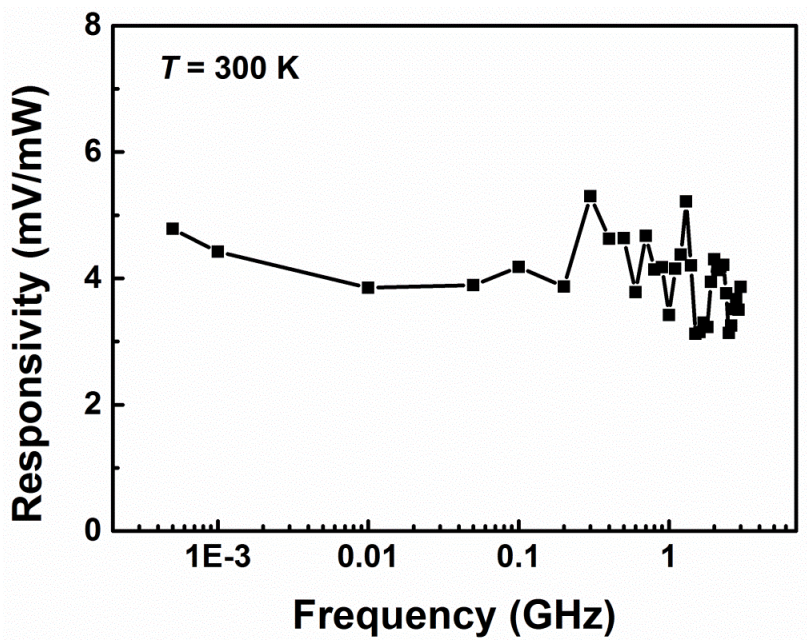

Figure 3.5 The measured responsivity as function of signal frequency at T = 300 K.

where P_i and P_r are the incident and reflected powers, respectively to the ballistic rectifier in Eq. (3.3). The P_r is related to the P_i as $P_r = P_i\,|\Gamma|^2$, where Γ is the voltage reflection coefficient and can be evaluated as below [15]:

$$\Gamma = \frac{Z_{BR} - Z_{NA}}{Z_{BR} + Z_{NA}}. \tag{3.4}$$

Substituting Eq. (3.4) into Eq. (3.3), the P_d can be modified as,

$$P_d = P_i\left(1 - |\Gamma|^2\right). \tag{3.5}$$

By fitting the measured results to Eq. (3.5), it was estimated that only about 5.5 % of the input power was effectively delivered to the device, with the rest reflected. Therefore, it is estimated from the results that the intrinsic responsivity of the device would be around 100 mV/mW. This suggests that further optimizations in the device geometry are required in order to avoid such huge mismatch.

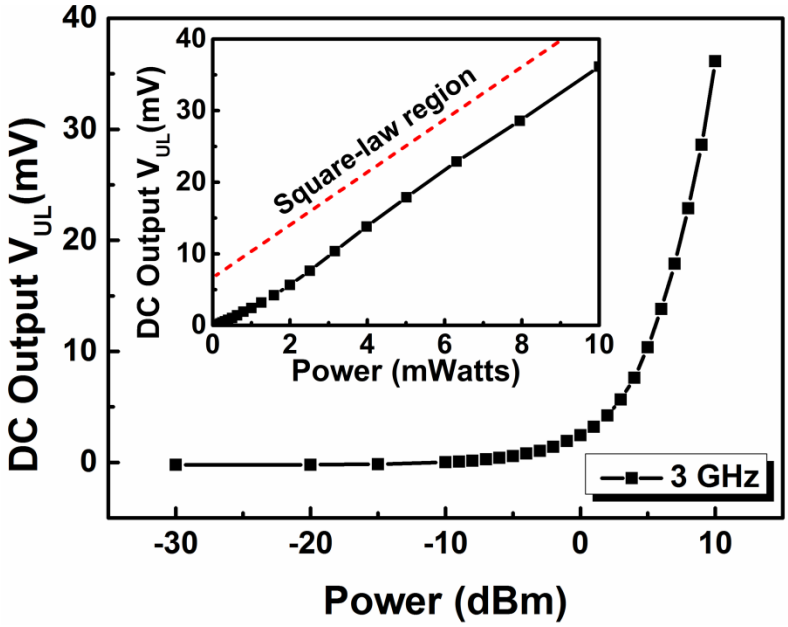

Figure 3.6 The output voltage V_{UL} increased with the increase in the amplitude of input signal between the S and D terminals. The inset shows the measured results as a function of input power at 3 GHz. The linear response suggests that the device was operating in the square-law region.

The square-law response of the ballistic rectifier as depicted in Eq. (3.2) can be seen in the inset of Fig. 3.6. The output DC voltage was measured as a function of input microwave power at room temperature. The frequency of the input signal was fixed at 3 GHz. As expected, the output voltage increased linearly with the increase in

input power. This suggests that the output DC voltage can be fitted to the quadratic fitting $V_{LU} = aV_{SD}^2$ where a is a constant. The results in Fig. 3.6 support the theoretical studies of the prediction of quadratic response to the input signal in accordance with Eq. (3.2). Due to this unique characteristic, the ballistic rectifier may also be used for generating the second harmonic oscillations without generating the third and higher harmonics [5].

3.4 RF rectenna

In 1984, Brown coined the term "rectenna" as the rectifying antenna [16]. The rectenna is an RF receiver and it converts microwave signals into DC voltage. It comprises of an antenna, input filter, and rectifying circuit with an output filter as shown in Fig. 3.7. The antenna is used to couple the RF signals to the rectifying circuit [17]. The input and output filters are usually employed to prevent the reduction in rectifying efficiency due to the generation of harmonics by the nonlinear characteristic of a diode, which is commonly used as a rectifier [18], [19].

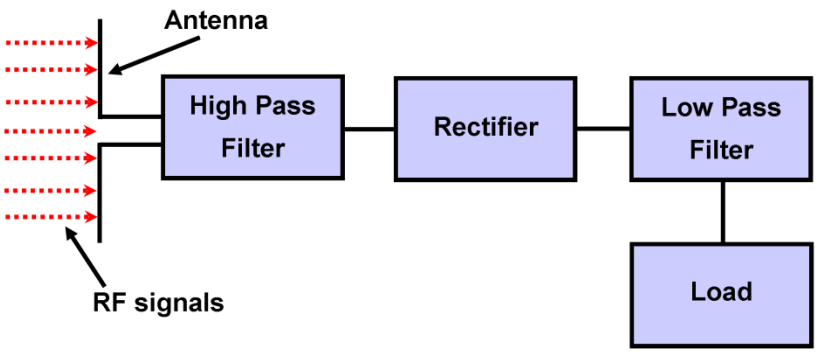

Figure 3.7 Black diagram of a rectenna. It consists of a receiving antenna and rectifying circuits with the input and output filters.

The rapid development of various wireless systems including wireless LAN, FM/AM radio signals, and mobile network signals has significantly increased the RF signals in the environment. This enormous ambient RF power has received much attention for energy harvesting or scavenging applications by employing the rectenna [20]. Most of the rectennas are proposed to harvest the RF energy associated with ultra-high frequency (UHF: 850 to 950 MHz) band [21] and industrial scientific and medical (ISM: 2.45 GHz) band [22].

Another promising practical application of the rectenna is in radio frequency identification (RFID) systems. RFID systems have been explored for various applications such as transportation (vehicle identification, road tolling system), tracking of goods and animals, contactless banking, sensing application, ensuring food safety, and library management system etc. [23]-[26]. A typical RFID system has a transponder (tag) and an interrogator (reader) each with a tuned antenna.

The conventional vertical semiconductor rectifiers such as *p-n* and Schottky diodes are being used in rectenna systems to rectify the RF signals detected by an antenna. The fabrications of these devices require multilevel-lithography techniques which makes them relatively expensive. Nevertheless, due to the device geometry ballistic rectifier can easily be fabricated in single step nanolithography. Therefore, the overall fabrication cost can be reduced significantly by employing large area fabrication methods such as nanoimprint lithography [27].

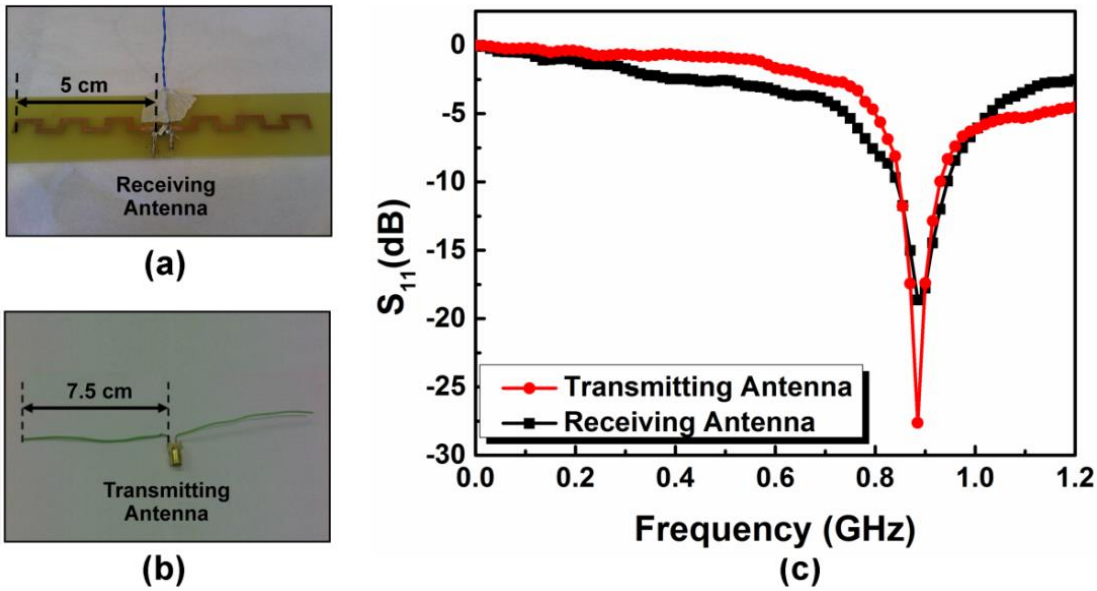

Figure 3.8 (a) Custom-built folded dipole antenna used to receive microwave signals at UHF band frequencies (860-950 MHz). (b) Transmitting dipole antenna built using electrical wires of 7.5 cm length at each terminal of a BNC connector to operate at UHF. (c) The S_{11} parameters for both the antennas as a function of frequency demonstrate the resonance frequency of 890 MHz.

This section demonstrates the RF rectification by the ballistic rectifier employed in rectenna configuration at UHF band frequencies. The device was coupled to a custom-built folded dipole antenna designed at UHF as shown in Fig. 3.8 (a). A half-wave dipole antenna, built using electrical wires, was used as a transmitting antenna,

as shown in Fig. 3.8 (b). The microwave source (Agilent E 5061B) was connected to the half-wave dipole antenna via coaxial cable to transmit RF signals. The transmitting and receiving antennas were designed at the frequency of 890 MHz as shown by their S_{11} parameter in Fig. 3.8 (c).

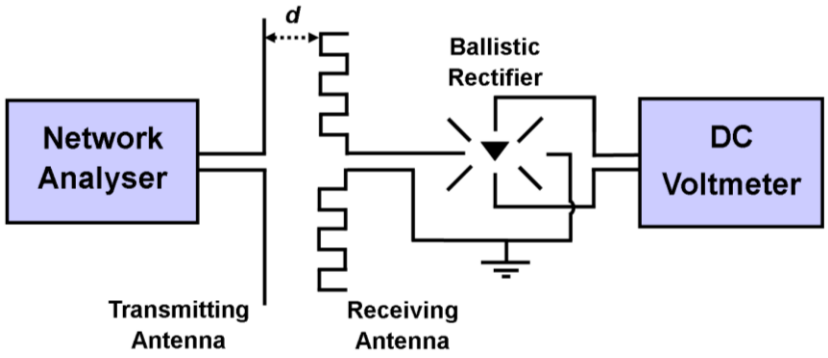

Figure 3.9 The schematic illustration of setup used for the proposed RF rectenna configuration using a ballistic rectifier. Both the transmitting and receiving antennas were positioned at the distance of *d* to each other. Output of the antenna was coupled to *S* and *D* terminals of the device.

The measurement setup is shown in Fig. 3.9. During the experiments both antennas were positioned at a distance *d* of either 2 or 5 cm to each other. Figure 3.10 shows the output DC voltage as a function of input frequency. The signal was transmitted at 10 dBm for the frequency range varied from 720 MHz to 1.03 GHz. The maximum values of the rectified output DC voltage for both distances were obtained at the resonance frequency of antennas, i.e., 890 MHz. The maximum output was obtained only when both antennas were aligned parallel to each other. The magnitude of the peak value decreased with the increase in distance *d* between antennas. The output started reducing to zero, when the transmitting antenna was rotated at different angle to the receiving antenna. This was due to the directional radiation and reception properties of an antenna [28].

The inset of Fig. 3.10 shows the output voltage measured by varying the input power to the transmitting antenna at 890 MHz. The linear response of the output DC voltage to the input power demonstrates that the device was working in the square-law region. This rectified signal from the device may be used to drive the electronic circuitry of a RFID system for data processing. Since the generated output DC voltage was extremely low, startup circuits were essential to generate the higher

voltages for the functioning of an electronic circuitry [29]-[31]. The design and development of such circuits was beyond the scope this present study.

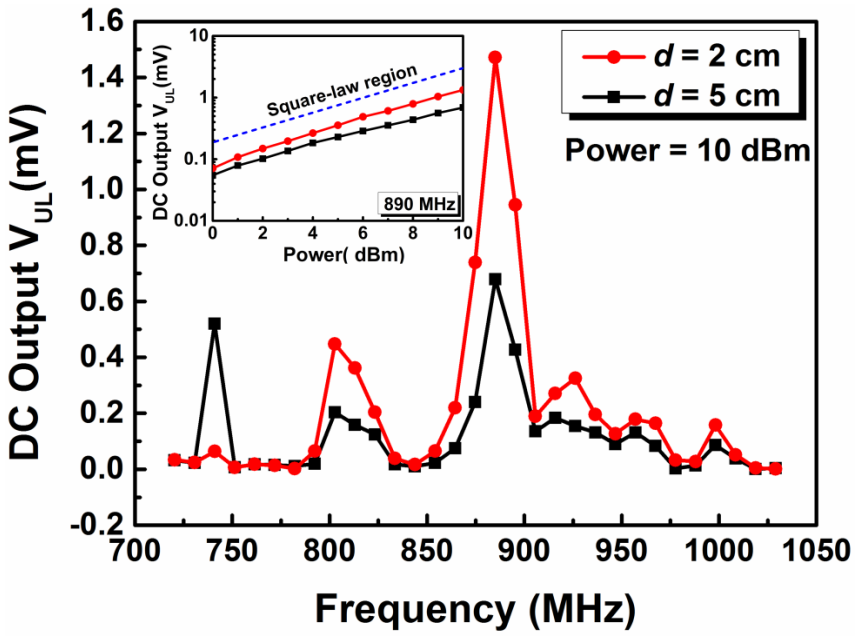

Figure 3.10 The output was measured between *U* and *L* using a DC voltmeter with respect to input signal frequency, as shown in the setup. During the experiments both antennas were kept at a distance *d* of either 2 or 5 cm to each other. The inset shows the detected output voltage with respect to input power at 890 MHz. The linear dependence on the power indicates that the device was operating in the square-law region.

3.5 Noise characterisation

3.5.1 Two-channel cross correlation technique

To measure the noise power spectra of a ballistic rectifier, a setup based on the cross-correlation technique using two independent measurement channels was used [32]. Figure 3.11 shows the schematic diagram of the spectrum analyser used in this noise study. The noise signal generated by the ballistic rectifier was fed into two independent channels simultaneously. In both channels, the amplified noise signal was sampled in the time domain by using a 16-bit analog-to-digital (ADC) convertor. The noise power spectral density in the frequency domain was obtained by the multiplication of the noise signal with its complex conjugate, generated by taking a discrete Fourier transform (DFT). The sampled noise signals $v_1(t)$ and $v_2(t)$ at the output of ADC, consist of a correlated component $s(t)$ from the ballistic

rectifier and uncorrelated components $w_1(t)$ and $w_2(t)$ from each channel having a zero-mean value, can be written as [32]:

$$v_1(t) = s(t) + w_1(t). \tag{3.6}$$

$$v_2(t) = s(t) + w_2(t). \tag{3.7}$$

The power spectrum density $S_s(f)$ of the correlated component $s(t)$ of the ballistic rectifier can be written as:

$$S_S(f) = F\{r_s(\tau)\} = \sum_{\tau=-\infty}^{\infty} r_s(\tau) e^{-j2\pi f\tau}, \tag{3.8}$$

where $r_s(\tau)$ is the autocorrelation function of the device signal $s(t)$. Since the $w_1(t)$, $w_2(t)$, and $s(t)$ are uncorrelated to each other, the autocorrelation $r_s(\tau)$ can be made equal to cross-correlation function $r_{v_1,v_2}(\tau)$ of $v_1(t)$ and $v_2(t)$ as:

$$r_s(\tau) = r_{v_1,v_2}(\tau) = E[v_2(t)v_1(t+\tau)]. \tag{3.9}$$

If a stream of N samples are being processed, the estimated autocorrelation $r_s(\tau)$ can be written as [32]:

$$\tilde{r}_s(\tau) = \tilde{r}_{v_1,v_2}(\tau) = \frac{1}{N}\sum_{t=0}^{N-1} v_2(t)v_1(t+\tau). \tag{3.10}$$

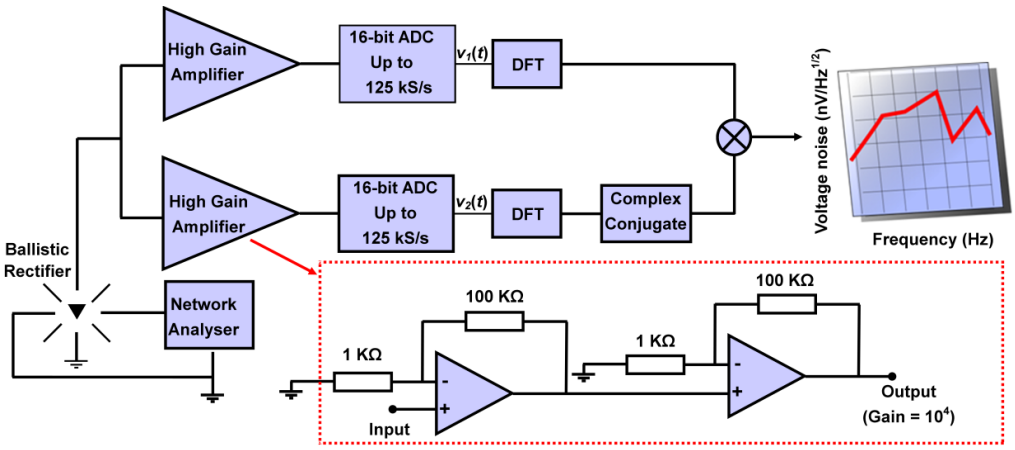

Figure 3.11 Schematic diagram of the noise measurement setup used in this work. The noise signal from the ballistic rectifier was fed into two-independent channels. Each channel consisted of an amplifier, an analog-to-digital converter (ADC) and a discrete Fourier transform (DFT). The power spectral density of the noise was calculated by multiplying the complex conjugate of the signal at one channel by the signal itself at another channel. The dashed box shows the two non-inverting amplifiers cascaded into each other. The closed-loop gain for each channel was approximately 10,000.

Subsequently, the estimated power spectrum density of the correlated component can be evaluated as below:

$$\begin{aligned}\tilde{S}_S(f) &= F\{\tilde{r}_s(\tau)\} = F\{\tilde{r}_{v_1,v_2}(\tau)\} \\ &= \sum_{\tau=-(N-1)}^{N-1} \tilde{r}_{v_1,v_2}(\tau) e^{-2j\pi f\tau} \\ &= \frac{1}{N} \sum_{\tau=-(N-1)}^{N-1} \sum_{t=0}^{N-1} v_2(t) v_1(t+\tau) e^{-2j\pi f\tau} \\ &= \frac{1}{N} \sum_{t=0}^{N-1} v_2(t) V_1(f) e^{2j\pi f\tau} \\ &= \frac{1}{N} V_1(f) V_2^*(f)\ , \end{aligned} \tag{3.11}$$

where $V_1(f)$ and $V_1^*(f)$ are the DFT of one channel and the complex conjugate of the DFT of another channel, respectively. Taking the real part of $\tilde{S}_S(f)$ discards half of the uncorrelated noise power and improves the standard deviation of the fluctuations in the noise power density by a factor of $\sqrt{2}$. Therefore, the final estimate of the noise power spectrum density of the device can be written as:

$$\tilde{S}_S(f) = \frac{1}{N} \mathrm{Re}\{V_1(f) V_2^*(f)\}. \tag{3.12}$$

The spectra of $\tilde{S}_S(f)$ was improved by increasing the total measurement time by repeating the above procedure several times with the new stream of sampled noise data and by averaging it. The resolution bandwidth and the frequency span of the measurement were decided by the selection of sampling frequency f_s. The stream of N samples at f_s, gave a DFT defined in N frequencies equally spaced by $\Delta f = f_s/N$. The values of f_s and N decided the desired span of frequencies from $f_{min} = f_s/N$ to $f_{max} = f_s/2$, hence the resolution bandwidth was equal to f_s/N.

Noise setup

Figure 3.12 shows a picture of the noise measurement circuit. A LabVIEW system was used for the computational processes and control of ADC. The setup was calibrated by measuring the noise power spectra of several thin-film resistors in the range of 1-10 kΩ. Figure 3.13 shows the thermal noise of about 6.69, 8.14, and 12.87

nV/Hz$^{1/2}$ for the resistors having a value of 2.7, 4, and 10 kΩ, respectively. The measured results agreed well with the theoretical values of thermal noise $\sqrt{4k_BTR_{res}}$, where R_{res} represents the resistance [33].

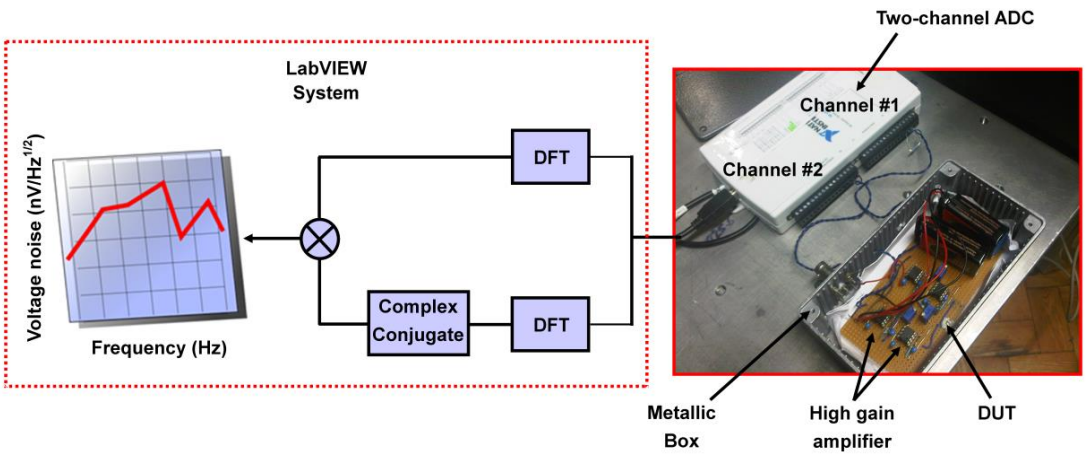

Figure 3.12 The measurement circuit, operated by two 9 V batteries, was sealed in a metallic box. It was connected to the two-channel 16-bit ADC, which was further linked to a LabVIEW system to process the signal and generate the final noise power spectrum of the ballistic rectifier.

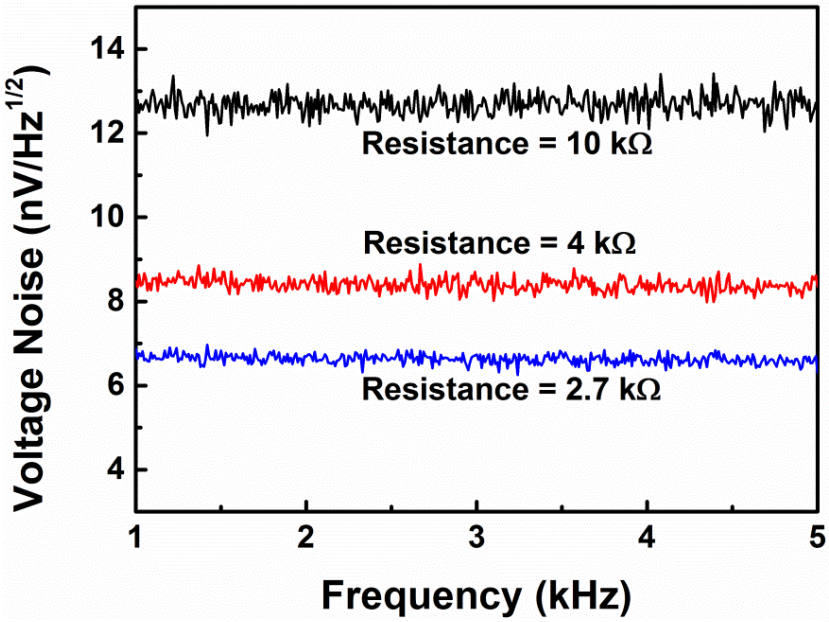

Figure 3.13 Voltage noise measured as a function of frequency for three different values of resistors, i.e., 2.7, 4, and 10 kΩ. The measured results were in agreement with the theoretical values of 6.69, 8.14, and 12.87 nV/Hz$^{1/2}$ for the resistance of 2.7, 4, and 10 kΩ, respectively.

The noise measurements were performed by putting all the circuitry, including the ballistic rectifier, inside a screened box to eliminate 50-Hz interferences. The voltage

fluctuations across the L and U of the ballistic rectifier were fed simultaneously to the inputs of two independent, battery-operated, low-noise amplifiers with a gain of 10^4. The two amplifiers were connected in parallel, and the amplified signal from each of the amplifiers was sampled by a 16-bit analog-to-digital converter (ADC) at a sampling rate of S_{rate} = 125 kS/s for a time period of t_0. The noise power spectrum $S_S(f)$ of the device was obtained by multiplying the discrete Fourier transform (DFT) of the output of one channel with the complex conjugate of the DFT of the other channel as described earlier.

The lower frequency limit of the noise spectra was determined by acquisition time, i.e., $f_L = 1/t_0$. The higher frequency limit was determined by Nyquist's sampling theorem $f_H = S_{rate}/2 \sim 60$ kHz, as well as by the amplifier bandwidth (-3 dB) which was approximately 40 kHz. In order to completely avoid the influence of the above effects, the highest frequency in the noise spectrum measurements was fixed to 10 kHz. Two different time windows of t_0 = 10 s with 100 repetitions and t_0 = 0.1 s with 1000 repetitions were used to measure the noise power spectra for the frequency range of 0.1-10 Hz and 0.01-10 kHz, respectively.

3.5.2 Low-frequency noise

In order to characterise the noise performance of the ballistic rectifier, the applied microwave power was varied from -4 to 7 dBm at 1 GHz as shown in Fig. 3.14. With no microwave power applied, where $1/f$ or flicker noise was not expected, the ballistic rectifier had generated a noise of about 8 nV/Hz$^{1/2}$. This result was in a good agreement with the theoretical value of thermal noise, i.e., 7.6 nV/Hz$^{1/2}$ of the ballistic rectifier due to the resistance of about 3.5 kΩ between L and U.

At a finite microwave power the ballistic rectifier, although not nominally biased by DC, still generated a DC voltage between L and U due to the rectifying effect. Thus, $1/f$ noise arose as shown in Fig. 3.14. As expected, the power of the $1/f$ noise (at 1 Hz) increased almost linearly with the increase of the input microwave power (at 1 GHz), as shown in Fig. 3.15. No obvious change was observed in the noise power spectra when measured at different frequencies of microwave signal.

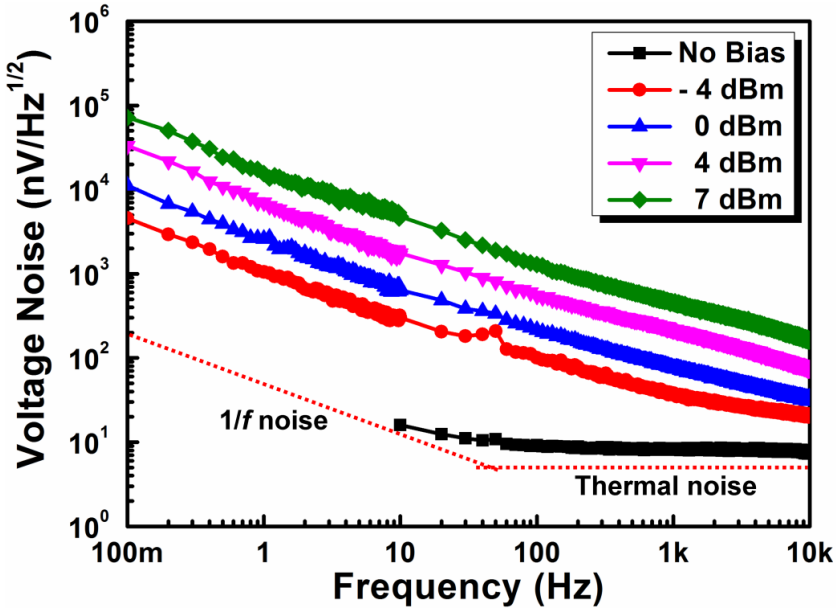

Figure 3.14 Room temperature voltage noise spectra of the ballistic rectifier measured at different microwave powers. At low frequencies, the noise was dominated by the $1/f$ or flicker noise. At zero-bias, the observed value of thermal noise was almost equal to the theoretical value.

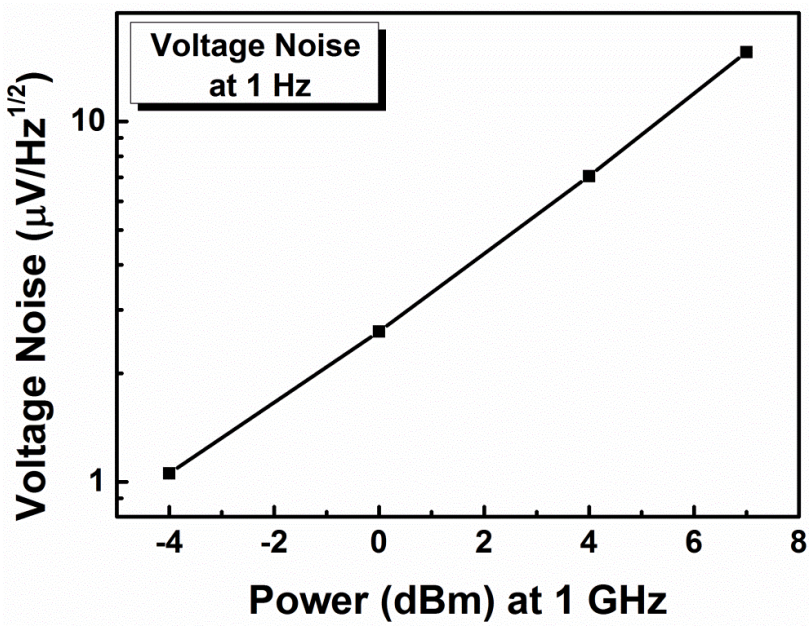

Figure 3.15 The almost linear dependence of the voltage noise (at 1 Hz) measured as a function of applied microwave power (at 1 GHz).

3.5.3 Quantitative modelling of 1/*f* noise

The observed 1/*f* noise may be described theoretically using various available models. The flicker noise originating from the mobility fluctuation can be expressed using Hooge's empirical relation as [34], [35]:

$$\frac{S_I(f)}{I^2} = \frac{S_V(f)}{V^2} = \frac{S_R(f)}{I^2 R^2} = \frac{\alpha_H}{N f^{\beta}}, \tag{3.13}$$

where $S_I(f)$ and $S_V(f)$ are the current and voltage noise power spectra, respectively, N is the number of carriers in the ballistic rectifier channel responsible for conduction, β is a fitting parameter, and α_H is the Hooge's constant.

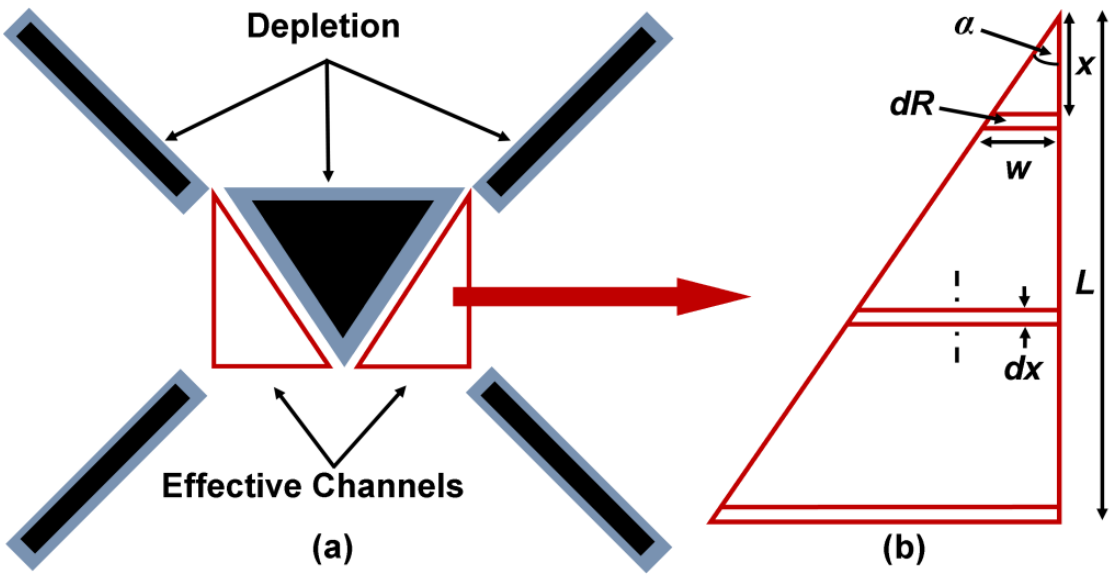

Figure 3.16 (a) Schematic of the centre part of ballistic rectifier indicating the depletion (gray area) due to the etched trenches (dark area). Therefore, between *U* and *L* terminals, a triangular-shape channel (red line) was formed on each side of the triangular antidot, which can be split into *n* equal sections with respect to the resistance (b).

Considering that the device size was much larger than the electron mean-free path, the number of carriers N was estimated based on diffusive electron transport and the resistance between L and U after taking into account the 2DEG mobility μ and A the effective device active area (subtracting the triangular scatterer). Figure 3.16 (a) illustrates the effective channel extended at both sides of the triangular antidot inside a ballistic rectifier. The etched device geometry induced a depletion inside the current channel as shown by the gray shaded area. The electron paths between U and L terminals were including two point-contact-like narrow constrictions. The

resistance between U and L was calculated by splitting each point-contact channel into n equal sections having a width of dx as shown in Fig. 3.16 (b). Each section contributed to the effective overall resistance between U and L. Consider that a small section having a width and length of w and dx, respectively, gave a resistance of dR. Thus, the voltage fluctuation ΔV across this section attributed to the rise in the $1/f$ noise or flicker noise, which can be given by:

$$\Delta S_V(f) = \frac{\alpha_H}{\Delta N f^{\beta}} (\Delta V)^2 , \tag{3.14}$$

where

$$\Delta V = I \frac{dx}{n_{2D} e \mu w} , \tag{3.15}$$

here, I represents the current flowing through the channel; n_{2D} is the carrier concentration and $w = x\tan\alpha$, where α is the angle as shown in Fig. 3.16 (b). The number of carriers available in this small section can therefore be calculated as:

$$\Delta N = n_{2D} x \tan\alpha dx . \tag{3.16}$$

Hence, the voltage noise spectra may be given as:

$$\Delta S_V(f) = \frac{\alpha_H I^2}{n_{2D}^3 e^2 \mu^2 x^3 (\tan\alpha)^3} \frac{1}{f^{\beta}} dx . \tag{3.17}$$

The voltage noise spectra in Eq. (3.17) was integrated from the narrowest part of the constriction (width = w_0) in order to calculate the total voltage noise spectra of the channel:

$$S_V(f) = \int_{w_0}^{L} \Delta S_V(f) dx . \tag{3.18}$$

From the DC resistance between the L and U terminals (~3.5 kΩ), it was estimated that w_0 was in the same order of magnitude as the Fermi wavelength (~22 nm). Hence, $L >> w_0$ and the voltage noise spectra became:

$$S_V(f) = \frac{\alpha_H I^2}{2 n_{2D}^3 e^2 \mu^2 w_0^2 (\tan\alpha)^3} \frac{1}{f^{\beta}} . \tag{3.19}$$

This result revealed that the total noise was independent of L and was completely determined by the narrowest part of the channel. The overall voltage noise power spectra of the ballistic rectifier contributed by the effective channels on both left and right sides of the triangular antidot can be illustrated as:

$$S_{V,total}(f) = \frac{\alpha_H I^2}{4n_{2D}^3 e^2 \mu^2 w_0^2 (\tan\alpha)^3} \frac{1}{f^\beta}. \tag{3.20}$$

The fitting of the experimental data with Eq. (3.20) yielded β = 0.99, close to perfect $1/f$ dependence and α_H between 10^{-4} and 10^{-3} for the reasonable range of α values from 30^0 to 60^0, dependent on the detailed microscopic depletion at the narrowest constriction. Considering α = 45^0, the values of α_H obtained from the measured results as a function of applied microwave power at 100 MHz, 1 GHz, and 2 GHz are shown in Fig. 3.17.

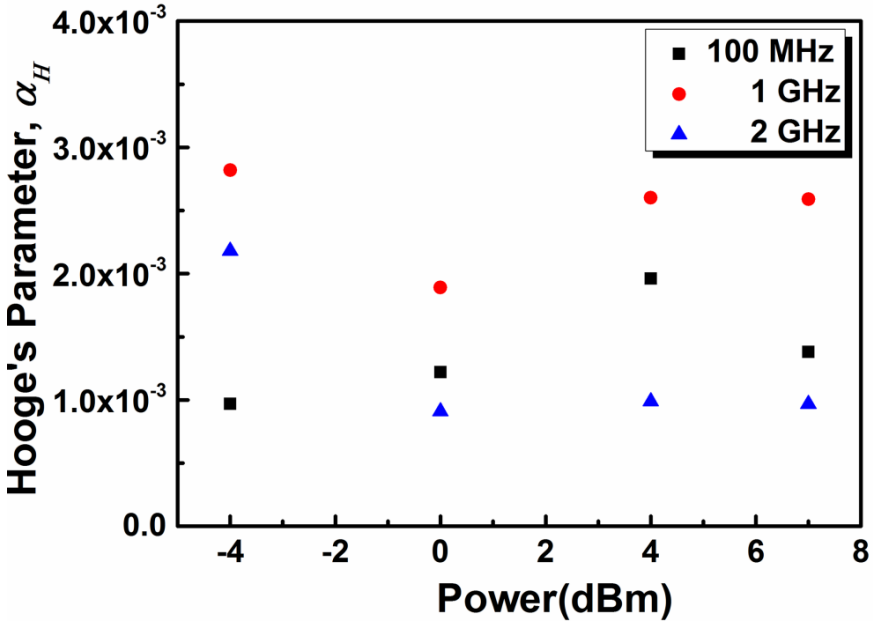

Figure 3.17 Hooge's parameter α_H obtained from the measured room temperature voltage noise spectra as a function of applied microwave power at 100 MHz, 1 GHz, and 2 GHz (considering α = 45^0).

Energy fluctuation model

As per the energy fluctuation model, the mobility fluctuation is attributed to electron-phonon scatterings in the crystal lattice. The value of α_H can be theoretically calculated from the mobility [36]:

$$\alpha_H = \frac{d}{\lambda} = \frac{de}{\mu\sqrt{2k_B T m^*}}, \tag{3.21}$$

where d is lattice constant and m^* is effective mass of an electron. Fitting Eq. (3.21) with the material parameters yielded $\alpha_H = 5\times10^{-3}$ at room temperature.

Quantum theory

Another theoretical model of quantum 1/*f* noise, also known as Handel's quantum theory, is based on the fundamental fluctuation between quantum-mechanical cross sections and scattering rates caused by the interaction of the charged particles and their own fields. The Hooge's parameter as per conventional Handel's theory for quantum 1/*f* noise can be given as [37]:

$$\alpha_H = \frac{4a}{3\pi}\frac{(\Delta\bar{v})^2}{c^2}, \tag{3.22}$$

where $a = e^2/\hbar^2$ is a Sommerfeld's fine structure constant $(137)^{-1}$, c is speed of light in vacuum, and $\Delta\bar{v}$ is the change in velocity of the carrier along the electron path in the interaction process considered. This model predicts a Hooge parameter with a value of few orders of magnitude lower, i.e., $\alpha_H = 10^{-5}$-10^{-9}. It is worth mentioning that despite being criticized [38], [39], Handel's theory is still being used and quite often theoretical predictions are in agreement with the experimental results [40]-[43].

The obtained results in this experiment were in accordance with the phonon scattering based mobility fluctuation model at room temperature. These values of α_H were also consistent with the reported values for the devices fabricated from InGaAs/InAlAs 2DEGs [44]-[47]. Furthermore, no obvious generation-recombination noise was observed, similar to the noise-measurement result of the unipolar nanodiode called self-switching device (SSD) fabricated from the same material [48], [49].

3.6 Noise equivalent power

The NEP, which determines the minimum possible power that a detector can practically resolve, was obtained as the noise power density over the voltage responsivity. It is important to define the threshold sensitivity in terms of the NEP to describe the noise performance of the microwave /THz detectors. The NEP can be

defined as the RF input power required to produce an output signal-to-noise ratio (SNR) of unity for a bandwidth of one hertz. At frequencies high enough to neglect 1/*f* noise, the NEP of the ballistic rectifier was proportional to the thermal noise. Therefore, the NEP can be improved by realising a device with the reduced resistance. The calculated NEP from the measured noise at zero-bias with no input microwave signal is shown in Fig. 3.18. At room temperature, the measured NEP of order of 10^{-9} W/Hz$^{1/2}$ were comparable to well explored thermal THz detectors e.g. golay cell, bolometer [6].

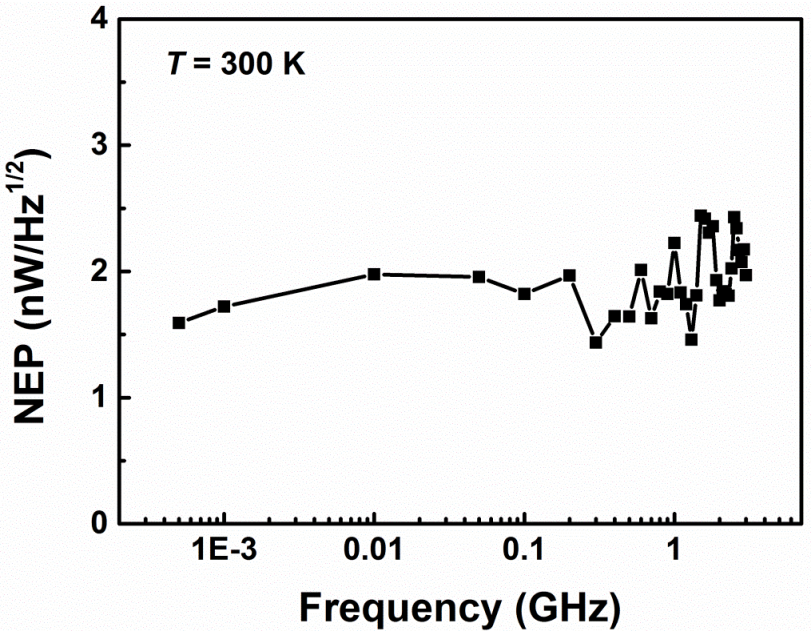

Figure 3.18 The noise equivalent power of the ballistic rectifier obtained from the measured noise at zero bias with no microwave power applied as a function of frequency at T = 300 K.

It is important to consider the corner frequency (f_c), i.e., a frequency at which the magnitude of 1/*f* noise equals to that of the thermal noise. The f_c determines the lowest modulation frequency for beam chopping and other modulation techniques without affecting the noise performance of the device. At 0 dBm, the interpolated f_c was of 138 kHz and it increased linearly with the applied input power as shown in Fig. 3.15.

3.7 Conclusions

In this chapter, the fabrication of a ballistic rectifier onto a 2DEG in InGaAs/InAlAs material has been demonstrated. The RF detection was performed up to the

frequency of 3 GHz at room temperature. The ballistic rectifier exhibited stable output detection for the range of applied RF input. The rectified DC output voltage was in the square-law region of device operation which means that the DC output was linearly proportional to the input microwave power. Despite the impedance mismatch, the intrinsic voltage responsivity was observed around 100 mV/mW.

Further, the ballistic rectifier was demonstrated as a rectenna by coupling with a folded dipole antenna designed at UHF band frequencies. Due to the planar device architecture, cost effective and large area fabrication technique such as nanoimprint lithography could be employed for fabricating these devices at large scale. The RF energy harvesting and RFID applications are the most promising areas where these devices can be employed.

Finally, the low-frequency noise properties of the ballistic rectifier were characterised at room temperature. The observed noise was quantitatively modelled in the diffusive transport regime and it revealed that the narrowest part of the electron channels had a dominant role in the device noise properties. The $1/f$ noise in the device was very well defined by energy fluctuation theory. One of the advantages of the ballistic rectifier is its fast response time since it directly rectifies rather than responding to the heat. By fabricating the ballistic rectifiers of much smaller dimensions to achieve purely ballistic transport using more advanced nanolithography, the responsivity, NEP and hence device quality and reliability could be significantly improved.

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Chapter 4

Graphene ballistic rectifier

4.1 Introduction

The intriguing electronic properties of graphene have recently attracted intense research activities for the development of various electronic devices [1], [2]. In particular, field-effect transistors (FETs) [3], quantum dots [4], *p-n* junctions [5], sensors [6], transparent electronics [7], memory devices [8], and solar cells [9] have been demonstrated with graphene. The lack of bandgap in graphene has restricted the pace of the development of graphene based digital devices [10]. However, researchers are trying their best to open the bandgap in graphene devices [11]-[14].

Graphene has demonstrated a high carrier mobility of about 200,000 $cm^2/V.s$ [15]-[17]. Recently, even higher mobilities in the order 10^6 $cm^2/V.s$ have been reported at low temperatures and low carrier concentration [18],[19]. It is important to note that graphene exhibits such high mobility at relatively high carrier concentration of about 10^{12} cm^{-2}. This carrier mobility of graphene is about 10 times higher than that of III-V semiconductors and approximately 100 times larger than the mobility of silicon (Si) [20]. The charge carriers in graphene can travel micrometres without being scattered even at room temperature. Moreover, the conductivity in graphene can be modulated by applying an electric field to the global back gate [1]. The ambipolar nature of carrier transport in addition to the high carrier mobility in graphene distinguishes it from other conventional semiconductor materials. Therefore,

graphene allows the realisation of nonlinear devices for radio frequency (RF) applications such as rectifiers [21], frequency doublers [22], resonators [23], and RF switches [24].

Another important measure of carrier transport is the carrier saturation velocity. The carrier mobility is best to define the electrical transport in low electric fields. However, the carrier saturation velocity becomes more important at high electrical fields as the steady state carrier velocity starts to saturate in a short gate length FET. Graphene has exceptional carrier saturation velocity and it is expected to be around 4.5×10^{7} cm/s [25], [26]. When compared to the III-V semiconductors, it does not significantly decrease with the increase in electric field [20]. Other exceptional properties of graphene include high thermal conductivity of about 5000 W/mK [27] and excellent mechanical strength [28], making it more suitable than conventional semiconductors for high-field devices.

Despite having a mean-free path length λ of charge carriers in the order of several 100s nm, only a few ballistic transport based graphene devices including nanoscale cross-junctions [29], three-terminal junctions [21], and ballistic nanoribbons [30] have been demonstrated yet. In a ballistic device, charge carriers move freely without scattering in the active area of device or are only scattered by the tailored geometry due to small dimensions when compared to the mean-free path length. In these experiments, two different geometries of ballistic rectifiers (with and without antidot scatterer) were fabricated from monolayer exfoliated graphene on silicon oxide (SiO_2). The nonlinear electrical properties of the devices were characterised at room temperature. Another device was fabricated from chemical vapour deposition (CVD)-grown graphene to demonstrate its capability as a promising rectifier to detect the RF signals.

4.2 Device fabrication

The monolayer graphene used in this study for the fabrication of ballistic rectifiers was deposited by mechanical exfoliation technique [1]. A thermally grown 290 nm thick SiO_2 layer on a highly doped Si was used as a substrate for the graphene. The *p*-doped Si substrate was used as a global back gate to tune the Fermi energy of the device which controlled the carrier concentration in graphene. Before exfoliating

graphene onto the SiO_2, samples were cleaned using acetone and isopropyl alcohol (IPA) followed by oxygen plasma for 5 minutes. High tack low stain tape was used to mechanically exfoliate graphene from highly crystalline graphite with crystal sizes up to 2 mm, sourced from a Canadian deposit. After placing the tape on the surface of a substrate, it was left for one hour to let the graphene relax from any strain. The sample was left in methyl isobutyl ketone (MIBK) at 85 °C on a hot plate until the tape was free from the surface. Further, to remove the glue or other contaminations from the surface of graphene it was left in another beaker of MIBK and then IPA. The sample was placed on a hot plate for 10 minutes at 130 °C to dehydrate the sample and achieve better adhesion. Following this a second tape peal was taken to remove the thickest pieces of graphite. An optical microscope was used to identify the graphene flakes on the substrate using the optical contrast method [31].

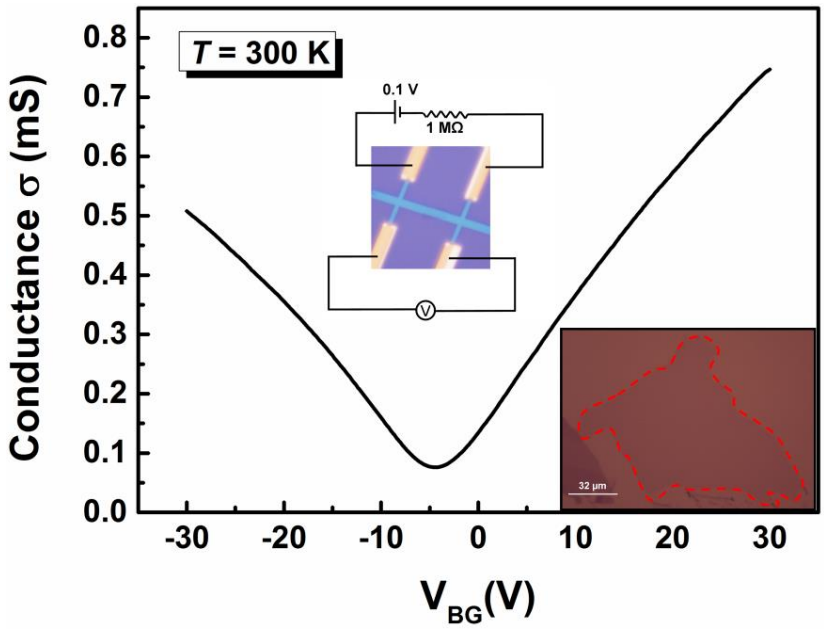

Figure 4.1 Room temperature conductance measured in vacuum as a function of back-gate voltage of fabricated Hall-bar structure on exfoliated graphene grown on 290 nm thick SiO_2. Inset shows the monolayer graphene used for the fabrication and the setup used for the measurement of field-effect mobility.

The graphene flakes were patterned into a Hall-bar geometry by employing electron-beam lithography (EBL) and oxygen plasma etching. A bi-layer resist system was used to create alignment marks and then contacts in two separate lithographic steps. Two layers of polymethyl methacrylate (PMMA) with molecular weights of 495 K and 950 K were spin coated at 5000 rpm and baked at 165 °C for 15 minutes. The ohmic contacts of Cr/Au (3 nm/ 40 nm) were e-beam evaporated onto the graphene.

The lift-off process was performed in acetone using a combination of heating and sonication to remove the excess gold.

Figure 4.1 shows the sheet conductance σ of the fabricated Hall bar structure measured as a function of applied back-gate voltage V_{BG} at room temperature. The standard four probe geometry, as shown in the inset of Fig. 4.1, was used for the measurement. The minimum conductivity was observed at the neutrality or Dirac point V_{DP} with a back-gate voltage of -4 V, which indicates a little extrinsic doping of approximately 2.9×10^{11} cm^{-2}. At small carrier concentrations, the slope of σ against V_{BG} yielded the field-effect mobility μ for holes and electrons of 1572 cm^2/V.s and 1810 cm^2/V.s, respectively. The λ for the fabricated sample was estimated using the following semi-classical relation [32]:

$$\lambda = \left(\frac{h}{2e}\right)\mu\left(\frac{n}{\pi}\right)^{\frac{1}{2}}, \tag{4.1}$$

where h is the plank's constant, n is the carrier concentration and e is the electron charge. From the measured results, Eq. (4.1) yielded the mean-free path length for holes and electrons with a typical carrier concentration of 2.23×10^{12} cm^{-2} were about 27.32 and 31.46 nm.

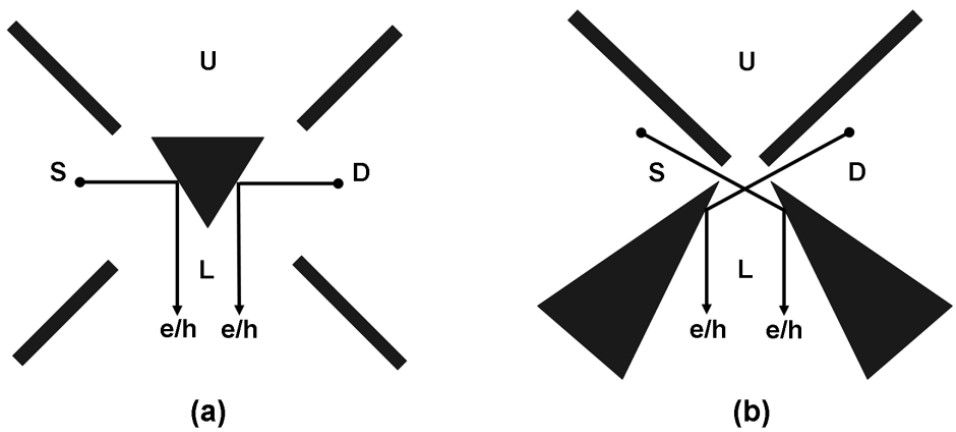

Figure 4.2 The schematic illustration of the different geometries of ballistic rectifiers (a) with and (b) without a triangular antidot, an artificial scatterer, at the centre of device active region. The arrows indicate the typical direction of flow of the charge carriers from *S* or *D* to *L* terminal.

The above fabricated Hall bar structure on graphene was used to fabricate the ballistic rectifiers. Figure 4.2 shows the schematic of the active central region of the ballistic rectifiers with and without triangular antidot (an artificial scatterer) at the

centre. The arrows indicate the typical trajectories of carrier transport and the dark areas represent the etched region. The four terminals of the device, source (*S*), drain (*D*), upper (*U*), and lower (*L*), are denoted in each device. Electron-beam lithography followed by oxygen plasma etching was used to fabricate these devices in the graphene. Figure 4.3 (a) shows a scanning electron micrograph of a typical ballistic rectifier with a triangular antidot at the centre, fabricated from graphene. The lithographic channel width for *S* and *D* was 50 nm while the channel width for *U* and *L* was 220 nm. The triangular antidot had the upper side length and height of 70 nm. An atomic-force microscopic (AFM) image of a ballistic rectifier without an artificial scatterer is shown in Fig. 4.3 (b). The effective channel width of *S*, *D* and *U* channel was 70 nm each. The dimensions of these fabricated devices were comparable to the estimated mean-free path length at room temperature.

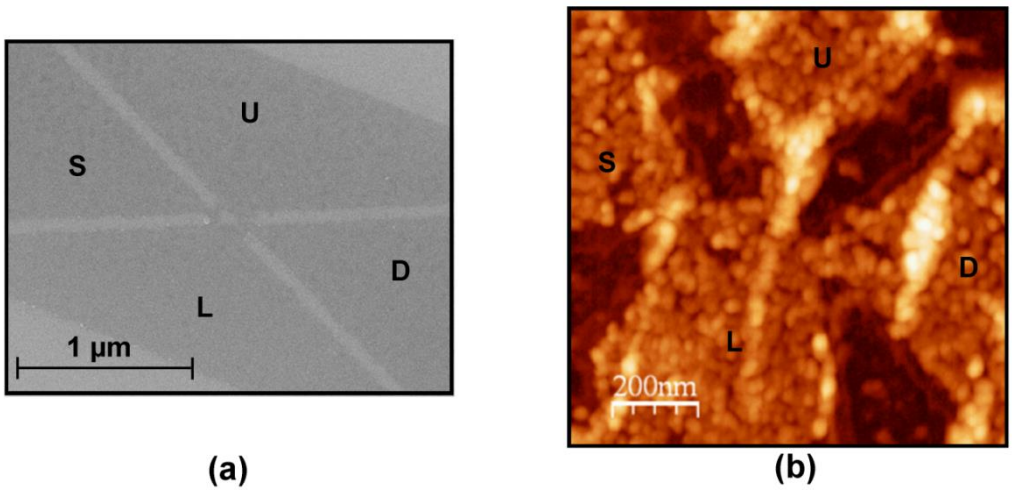

Figure 4.3 (a) Scanning electron micrograph of a graphene based ballistic rectifier with triangular antidot scatterer. (b) Atomic-force microscopic image of a ballistic rectifier without an artificial scatterer, fabricated from graphene.

4.3 Results and discussion

4.3.1 Scattering approach

In a mesoscopic semiconductor structure, the device dimensions are much larger than the mean-free path length. Therefore, the current carriers move from one side of channel to the other without experiencing any random scattering such as lattice defects, impurities, and phonons [33]. The transport of charge carriers in a ballistic device can be controlled or modified in a preferred direction by geometrically

induced scattering. In III-V semiconductor based ballistic devices, the electrical transport is determined by the transmission coefficients of charge carriers at the Fermi level. The Buttiker-Landauer formalism, which treats the transport as a transmission problem, has been widely used to describe the linear transport behaviour of the devices. However, this model has been extended to define the nonlinear transport regime of the ballistic devices based on a scattering approach [34].

The ballistic transport properties of several graphene devices such as three-terminal junctions [35], geometrically induced nanodiodes [36], Schottky-barrier based graphene transistors [37], graphene nanoribbons [38] etc. have been investigated under the purview of Buttiker-Landauer formalism. Du *et al.* [17] has demonstrated that the ballistic contribution to the conductivity of a graphene device depends upon the scattering originated from the boundary confinement [39].

In recent works on nanoscale graphene cross junctions [29],[32],[40], the ballistic effect of transport has been observed by performing bend resistance measurements. In these experiments, they measured so-called four terminal bend resistance $R_{12,43} = V_{43}/I_{12}$ by applying a current I_{12} through contacts 1 and 2 and measuring the voltage V_{43} between contact 4 and 3. In diffusive transport regime of charge carriers, the bend resistance was found to be positive. However, in ballistic transport regime, it was negative which can be explained considering it as a transmission problem. When the ballistic charge carriers were injected ($I_{12}<0$) from contact 1, they directly went towards the contact 3 without transmitting to contact 2. As a result, the accumulation of charge carriers induced a positive voltage V_{43} between contact 4 and 3 which gave rise to the negative bend resistance. This change of sign in bend resistance indicates whether the transport is diffuse or ballistic.

Hence, the carrier transport in ballistic rectifiers fabricated from graphene can also be explained using scattering approach as proposed in Ref. [41]. The ballistic rectifier can be viewed as a ballistic conductor connected via perfect leads to four reservoirs (terminals). Assuming that μ_α and μ_β are the chemical potential of charge carriers in contact α and β, respectively at temperature $T = 0$. In the linear regime, the current I_α in lead α can be written as [42]:

$$I_\alpha = \frac{2e}{\hbar}\sum_{\beta\neq\alpha} T_{\beta\leftarrow\alpha}(\mu_\alpha - \mu_\beta), \tag{4.2}$$

here, $\hbar$ is the reduced Plank's constant and $T_{\beta\leftarrow\alpha}$ is defined as a transmission coefficient. In the nonlinear regime of transport at a finite temperature in the presence of a finite magnetic field, the current through lead α of a ballistic conductor, which is connected to a number of reservoirs, can be given by:

$$I_\alpha = \frac{2e}{\hbar}\sum_{\beta\neq\alpha}\int [f(E-\mu_\alpha) - f(E-\mu_\beta)]\times T_{\beta\leftarrow\alpha}(E,B)dE, \tag{4.3}$$

where $f(E-\mu_\alpha) = [\exp((E-\mu_\alpha)/k_B T)+1]^{-1}$ is the Fermi-Dirac distribution function. $T_{\beta\leftarrow\alpha}(E,B)$ is a transmission coefficient for carriers moving from lead α to β and can be defined as a function of energy E and magnetic field B. At $k_B T = 0$, where k_B is the Boltzmann constant, and $B = 0$, Eq. (4.3) can be written as:

$$I_\alpha = \frac{2e}{\hbar}\sum_{\beta\neq\alpha}\overline{T}_{[\beta,\alpha]}(\mu_\alpha - \mu_\beta), \tag{4.4}$$

where

$$\overline{T}_{[\beta,\alpha]} = \int_{\mu_\beta}^{\mu_\alpha}\frac{T_{\beta\leftarrow\alpha}(E)dE}{(\mu_\alpha - \mu_\beta)}, \text{ if } \mu_\alpha > \mu_\beta \tag{4.5}$$

$$= \int_{\mu_\alpha}^{\mu_\beta}\frac{T_{\alpha\leftarrow\beta}(E)dE}{(\mu_\beta - \mu_\alpha)}, \text{ otherwise.} \tag{4.6}$$

Equations (4.5) and (4.6) show that the transmission of carriers from a reservoir, having chemical potential higher than the lowest chemical potential, contribute to the net current flow and therefore, can be used to estimate the resistance of conductor.

In the absence of any input, the angular distribution $P(\theta)$ of the charge carriers coming out of S and D channel of ballistic rectifier can be expressed as:

$$P(\theta) = \frac{1}{2}\cos(\theta), \tag{4.7}$$

where θ is the angle between charge carrier and channel direction, and lies between -π/2 to π/2. Hence, even at $V_{SD} = 0$, the charge carriers coming out from source are collimated. Let θ_0 is the minimum ejection angle of charge carrier coming out from S

or D to be scattered by an artificial triangular antidot to the lower channel. The transmission coefficients at zero bias can be obtained as [42]:

$$T_{L\leftarrow S} = T_{L\leftarrow D} = T_{D\leftarrow L} = T_{S\leftarrow L}$$

$$= N_{SD} \int_{-\pi/2}^{\theta_0} P(\theta) d\theta = \frac{N_{SD}(1+\sin\theta_0)}{2} . \tag{4.8}$$

Similarly,

$$T_{U\leftarrow S} = T_{U\leftarrow D} = T_{D\leftarrow U} = T_{S\leftarrow U}$$

$$= N_{SD} \int_{\theta_0}^{\pi/2} P(\theta) d\theta = \frac{N_{SD}(1-\sin\theta_0)}{2} . \tag{4.9}$$

Here, N_{SD} is defined as the number of occupied transverse confinement modes in S and D channels at a specific Fermi level.

Considering that the charge carriers, moving from S to D at V_{SD} = 0, have the velocity components v_x and v_y along the direction of channel and in the perpendicular direction, respectively. When a negative V_{SD} is applied, the ejected carriers from S will collimate. Therefore, the ejection angle of electrons will change from θ = arctan[v_y/v_x] at I_{SD} = 0 to a smaller angle of arctan[$v_y/(v_x+\Delta v)$]. This will increase the transmission probability of ejected carriers from S to move into L. Thus, the transmission probabilities can be expressed as:

$$T_{L\leftarrow S}(I_{SD}<0) - T_{L\leftarrow S}(I_{SD}=0) = \frac{N_{SD}}{2}(\sin\theta_e - \sin\theta_0) , \tag{4.10}$$

$$T_{U\leftarrow S}(I_{SD}<0) - T_{U\leftarrow S}(I_{SD}=0) = -\frac{N_{SD}}{2}(\sin\theta_e - \sin\theta_0) , \tag{4.11}$$

where θ_e can be determined by:

$$\theta_e = \theta_0 + \arcsin[(\Delta v / v_F)\sin\theta_0] , \tag{4.12}$$

here, v_F is the Fermi velocity and can be related to Δv by assuming that the number of occupied modes in S and D channels are neglected:

$$\frac{\Delta v}{v_F} = -\frac{\hbar}{N_{SD} e E_F} I_{SD} . \tag{4.13}$$

The output of a ballistic rectifier can be determined by the relative changes in transmission coefficients $\Delta T/T$ instead of absolute changes in transmission coefficients ΔT. Therefore, Eq. (4.4) can be written as:

$$I_\alpha \approx \frac{2e}{\hbar}\sum_{\beta\neq\alpha}\overline{T}_{[\beta,\alpha]}(I_{[\beta,\alpha]})(\mu_\alpha-\mu_\beta)\,, \tag{4.14}$$

where $\overline{T}_{[\beta,\alpha]}(I_{[\beta,\alpha]})$ is equal to $\overline{T}_{\beta\leftarrow\alpha}(I_\alpha)$ if $\mu_\alpha > \mu_\beta$ and $\overline{T}_{\alpha\leftarrow\beta}(I_\beta)$, otherwise.

The four terminal resistance can be calculated by $R_{SD,LU} = V_{LU}/I_{SD}$. For $V_{SD} < 0$ [42]:

$$R_{SD,LU} = \frac{\hbar[T_{L\leftarrow S}(I_S)T_{D\leftarrow U}(I_U)-T_{D\leftarrow L}(I_L)T_{U\leftarrow S}(I_S)]}{2e^2X}\,, \tag{4.15}$$

where $I_S = I_{SD}$ and $I_L = I_U = 0$.When net current between upper and lower channel is zero, the transmission coefficients $T_{D\leftarrow L}$ and $T_{D\leftarrow U}$ will not have any significant effect on the resultant voltage. X is a function of individual transmission coefficients and is also insensitive to applied voltage or current. For the ballistic rectifier, at $\theta_0 \approx \pi/4$, $T_{S\leftarrow D} = T_{D\leftarrow S} = 0$ and $T_{L\leftarrow U} = N_{LU}/3$, where N_{LU} is the number of occupied transverse quantum confined modes in L and U, X is described as given below, assuming that $N_{LU} > N_{SD}$:

$$X = N_{SD}[2T_{L\leftarrow S}T_{U\leftarrow S} + T_{L\leftarrow U}N_{SD}] = \frac{N^2{}_{SD}N_{LU}}{3}\,. \tag{4.16}$$

Substituting Eqs. (4.8), (4.9), (4.10), (4.11) in to Eq. (4.15) yields:

$$V_{LU} = R_{SD,LU}I_{SD} = \frac{3\hbar}{4e^2}\frac{\sin\theta_e-\sin\theta_0}{N_{LU}}I_{SD}(<0)\,. \tag{4.17}$$

When $V_{SD} > 0$, it can be written as:

$$V_{LU} = -\frac{3\hbar}{4e^2}\frac{\sin\theta_e-\sin\theta_0}{N_{LU}}|I_{SD}|\,. \tag{4.18}$$

In the limit of $|I_{SD}| \to 0$, V_{LU} can be written as:

$$V_{LU} = -\frac{3\pi\hbar^2}{4e^3E_FN_{SD}N_{LU}}I^2{}_{SD}\,. \tag{4.19}$$

It is interesting to note in Eq. (4.19) that the rectified output voltage V_{LU} is independent of temperature. Therefore, even at very small input signal, the ballistic rectifier does not need any threshold voltage or turn-on voltage to operate [43].

4.3.2 DC characterisation

When a DC current I_{SD} was applied between the *S* and *D* terminals, the ejected electrons from *S* or *D* were deflected by a triangular antidot to the terminal *L* as indicated in Fig. 4.2 (a) [44]. Therefore, electrons were accumulated in the lower terminal of the ballistic rectifier; as a result, a negative V_{LU} was induced between the *L* and *U* terminals. Correspondingly, when holes were the majority charge carriers, the induced voltage between *L* and *U* terminals was positive. However, in the ballistic rectifier without an artificial antidot at the centre as shown in Fig. 4.2 (b), the two narrow channels connecting *S* and *D*, slanted by 30^0 from the perpendicular axis of the longitudinal channel between *L* and *U*, were responsible for the rectifying effect from the device [45].

Due to the ambipolar nature of the graphene, the carrier types inside the device can be changed from electrons to holes or vice-versa by adjusting the back-gate voltage around the neutrality point. The ballistic rectifiers are very sensitive to the back-gate voltage, as the mobility increases exponentially towards the neutrality point and the device efficiency depends very strongly on mobility. Therefore, the universal back gate was tuned to find the optimum back-gate voltage suitable for the best rectifying properties from the device. The output voltage V_{LU} measured as a function of V_{BG} at fixed V_{SD} = 3 and -3 V at room temperature is shown in Fig. 4.4 (a). The V_{LU} had a strong dependence on the V_{BG}. Figure 4.4 (b) shows the calculated asymmetric output $[V_{LU}(I_{SD}) + V_{LU}(-I_{SD})]/2$ with respect to the back-gate voltage calculated for V_{SD} = ± 3 and ± 2 V. The rectified output voltage was switched from positive to negative at V_{SD} = 3 V as shown in Fig. 4.4 (a). To the left of neutrality point (V_{DP} = -4 V) where the dominant charge carriers were holes a positive rectified V_{LU} was observed. However, to the right a negative V_{LU} was induced due to electrons being the dominant carrier type. The results in Fig. 4.4 (b) show that the maximum value of asymmetry in V_{LU} was obtained at a back-gate voltage of -15 V. This suggested that the maximum nonlinear behaviour from this device could be observed only at V_{BG} = -15 V, where the dominant charge carriers were holes.

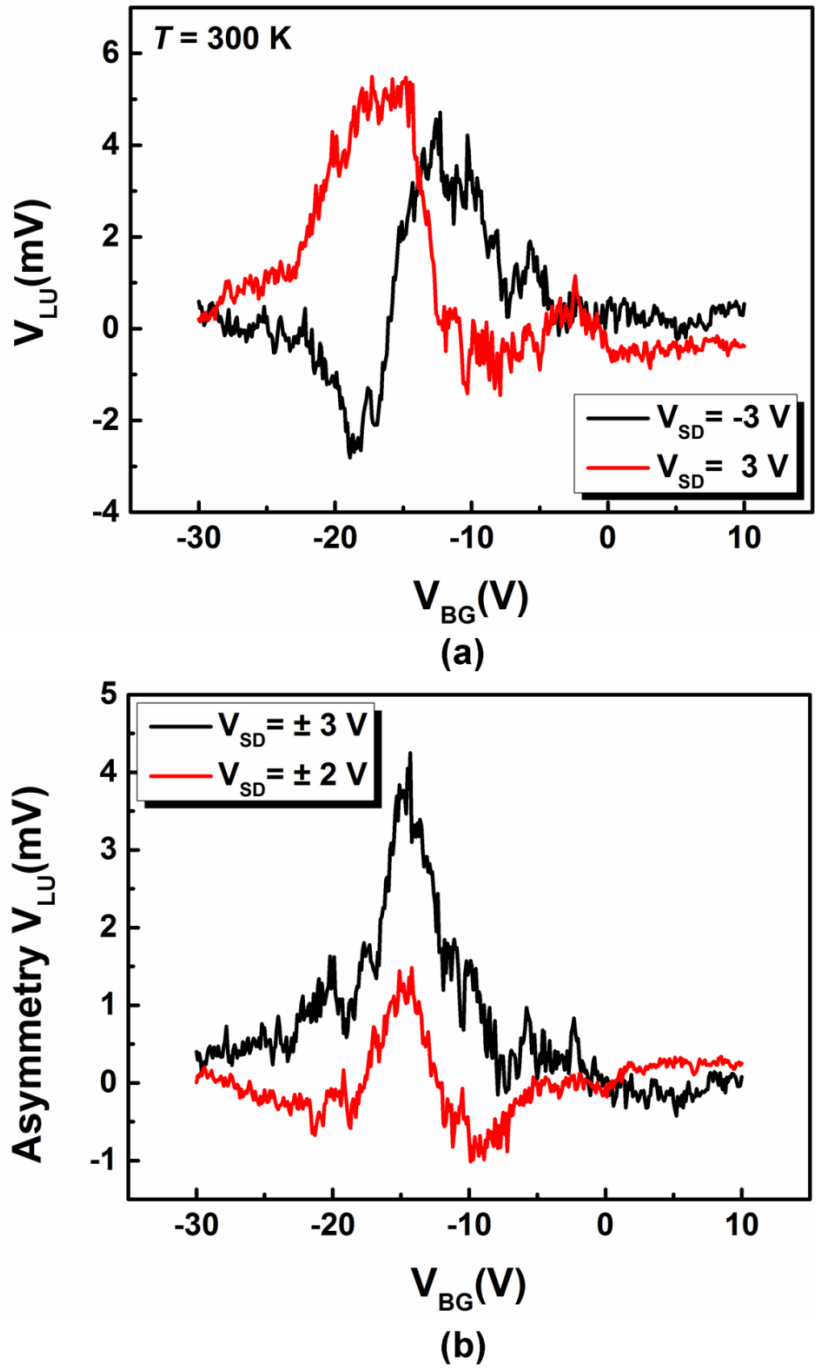

Figure 4.4 (a) The output voltage V_{LU} as a function of back-gate voltage V_{BG} of a ballistic rectifier without antidot at centre. The measurements were performed by keeping V_{SD} fixed at -3 and 3 V, respectively at room temperature. (b) The asymmetric output $[V_{LU}(I_{SD}) + V_{LU}(-I_{SD})]/2$ with respect to back-gate voltage when V_{SD} was fixed at ± 3 and ± 2 V.

Figure 4.5 shows the voltage-current (V_{LU}-I_{SD}) characteristic of a ballistic rectifier without antidot scatterer. The measurements were performed at the back-gate voltage of -15 V at room temperature. As expected, the device exhibited geometrically induced rectifying effect. Theoretically, due to the symmetric device geometry V_{LU} (I_{SD}) = + V_{LU} (-I_{SD}) should be expected. However, for a real device as shown in Fig. 4.3 (b), lithography may not be perfect. As a result, a symmetric voltage-current characteristic about I_{SD} = 0 might not be expected similar to the obtained results [44].

Using Eq. (4.19), the theoretically calculated voltage-current characteristic for the range of applied I_{SD} at the back-gate voltage of -15 V, where n was 1.1×10^{12} cm^{-2}, is shown in Fig. 4.5. The experimental results were very well fitted to the theoretical curve. These experimental results suggest that the electrical conduction of a ballistic rectifier fabricated from graphene can be explained using the theoretical framework of Büttiker-Landauer formalism based on the scattering approach.

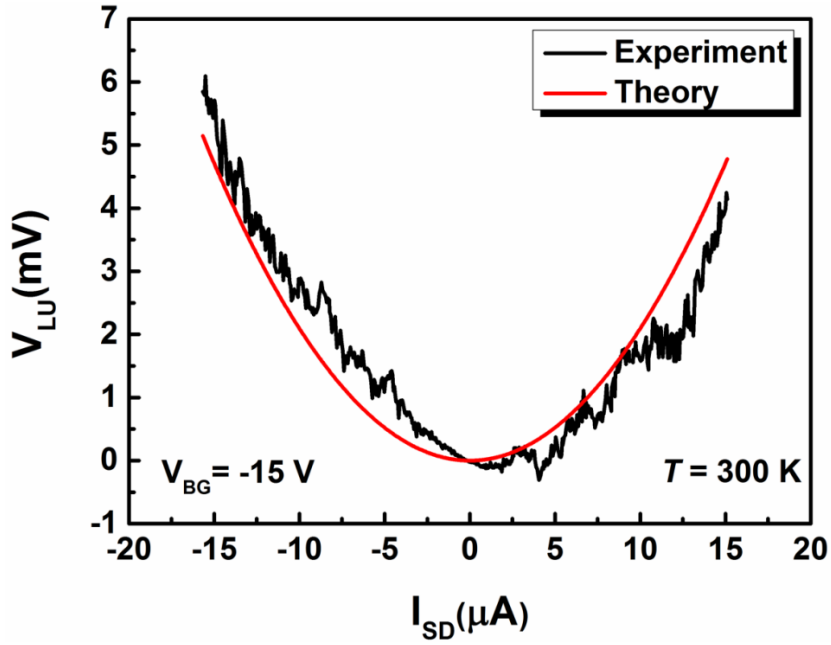

Figure 4.5 Room temperature voltage-current characteristic of the ballistic rectifier without antidot scatterer at the back-gate voltage of -15 V. The measured results were fitted to the theoretical curve calculated using Eq. (4.19).

The intrinsic voltage responsivity (β_V), which is a detection sensitivity of the microwave detector, can be extracted from the nonlinear V_{LU}-I_{SD} characteristic of the ballistic rectifier:

$$\beta_V = \frac{V_{LU}}{P_{in}}, \tag{4.20}$$

where, P_{in} is the input power applied to S and D terminals of the device. Considering the device impedance of 100 kΩ at V_{BG} = -15 V, the intrinsic β_V was estimated to be 214.38 mV/mW.

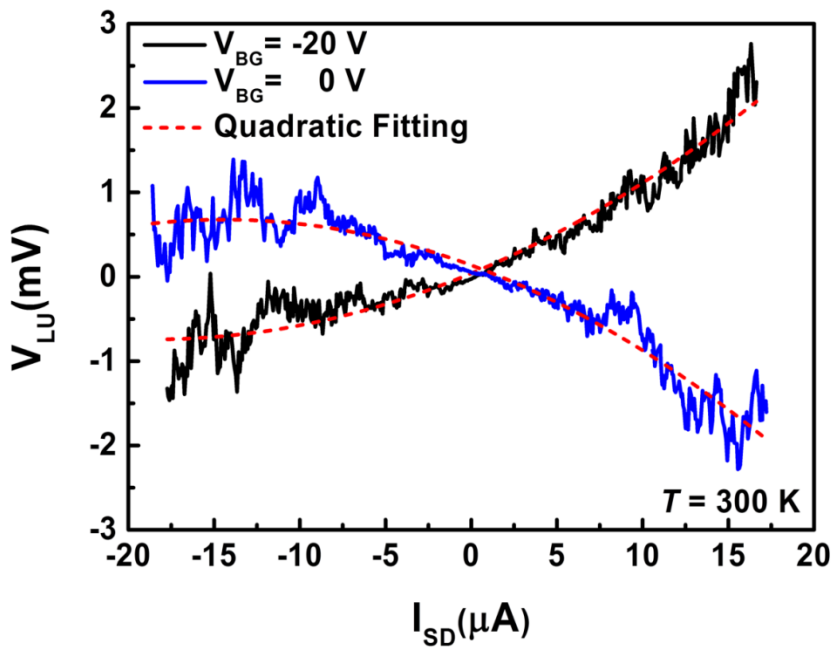

Figure 4.6 To the left (-20 V) or right (0 V) of the neutrality point (V_{DP} = -4 V), the rectified output voltage was of positive or negative sign, respectively. The output voltage V_{LU} was fitted to quadratic fitting which validates the observations of Eq. (4.19) even in less pronounced rectifying effect of the device.

The V_{LU}-I_{SD} characteristics were also measured at different back-gate voltages to find out the effect of gate induced rectifying properties of the device. Figure 4.6 shows the output voltage V_{LU} measured as a function of input current I_{SD} at a back-gate voltage of -20 V and 0 V at room temperature. A change of sign from positive to negative was observed in the output voltages when the majority charge carriers were tuned from holes (V_{BG} = -20 V) to electrons (V_{BG} = 0 V). The measured results were fitted the quadratic model as described by Eq. (4.19). The device exhibited a less pronounced rectifying effect at these gate voltages due to a small mean-free path length when compared to the device dimensions. This means that only a small fraction of the carriers would travel ballistically through the device. The impedance of the device at V_{BG} = -20 and 0 V was around 75 and 65 kΩ, respectively. The nonlinear component of the V_{LU}-I_{SD} characteristics in Fig. 4.6 yielded the intrinsic β_V

of 41.25 mV/mW and 25 mV/mW at V_{BG} = -20 and 0 V, respectively. The decrease in the responsivity was evident from the measured results as shown in Fig. 4.6 due to the less pronounced rectifying effect.

4.3.3 AC characterisation

Figure 4.7 (a) shows the V_{LU}-I_{SD} characteristic of a ballistic rectifier with a triangular antidot at its centre as shown in the inset of Fig. 4.7 (b). The dimensions of the active region were larger than the mean-free path length, meaning the symmetric output was smaller as shown in Fig. 4.7 (a). As reported earlier in Ref. [44], a less pronounced nonlinear rectifying effect might be expected from such a device. The device exhibited the impedance of 55 kΩ at V_{BG} = 0 V. Fitting of the measured results to Eq. (4.20) gave an intrinsic β_V of 110.92 mV/mW, which can be improved by ensuring the ballistic or quasi-ballistic transport of the charge carriers at room temperature.

In order to characterise the rectification properties of the ballistic rectifier an AC current at 1 kHz was applied between *S* and *D* of the device and the induced DC output voltage was measured simultaneously between *L* and *U*. Figure 4.7 (b) shows the rectified output V_{LU} as a function of applied input AC current measured at the room temperature. The error bars were based on 100 readings of the output DC voltage. From these results, the measured β_V was 66.68 mV/mW.

The device exhibited a quadratic response to the input current, indicated by the quadratic fit $V_{LU} = aI_{SD}^2$, where V_{LU} is the output DC voltage, I_{SD} is input AC current, and a is a constant. The quadratic characteristic means that the DC output would be a linear function of applied microwave power [46].

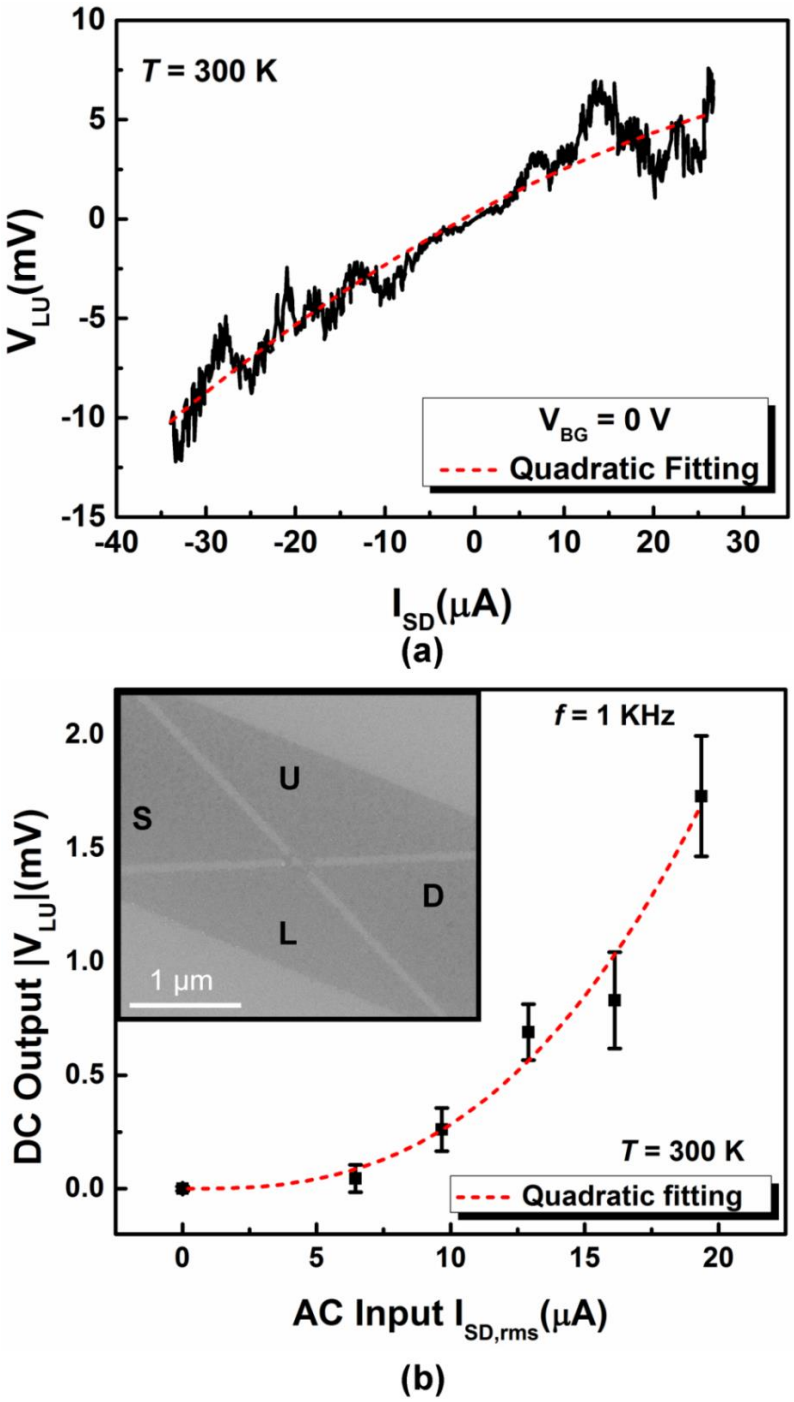

Figure 4.7 (a) V_{LU}-I_{SD} characteristic at V_{BG} = 0 V for a ballistic rectifier with triangular antidot at T = 300 K. (b) The rectified DC output voltage was measured at room temperature with respect to AC rms current. The error bars were plotted by taking 100 readings of output DC voltage at the frequency of 1 kHz. The measured results were fitted to quadratic fitting which means that the output was proportional to the square of applied input current. The inset shows the scanning electron microscope (SEM) image of the device.

4.3.4 RF rectification

In this experiment, CVD-grown monolayer graphene transferred onto a 300 nm thick SiO_2 substrate was used for the fabrication of ballistic rectifier. The details about the graphene fabrication are given in chapter 6. CPW-fed electrical contacts, suitable for RF measurements, were patterned onto the graphene using standard photo-lithography followed by oxygen plasma etching, as shown in Fig. 4.8 (a). All the fabricated samples exhibited *p*-type doped characteristics in the ambient environment. The estimated field-effect induced mobility for holes was about 644 $cm^2/V.s$ at room temperature, which is quite comparable to the commonly reported values [47]. The observed *p*-type doped characteristics and reduced mobility were presumably due to the adsorbents/residues left behind by the CVD fabrication processes and optical resist [48].

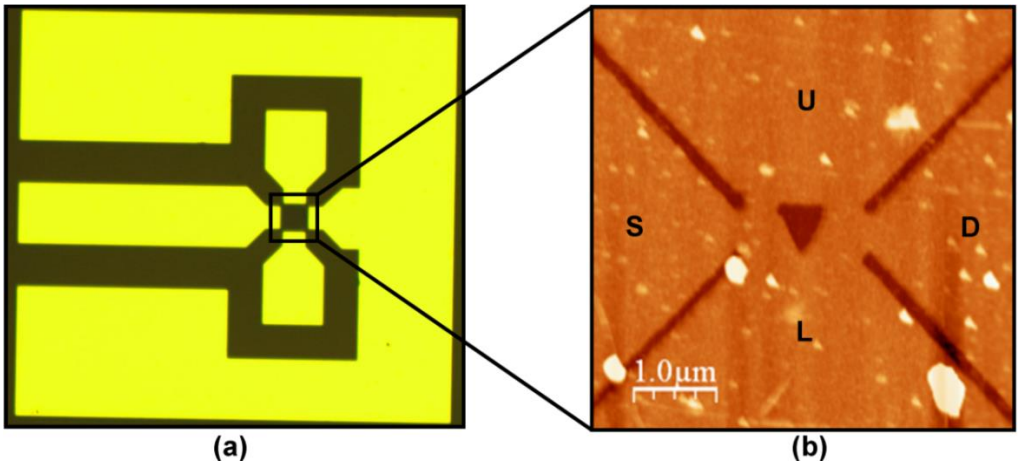

Figure 4.8 The optical microscopic image of a RF contact on CVD-grown graphene. (b) An atomic-force micrograph of the centre part of the device indicating terminals source (*S*), drain (*D*), upper (*U*), and lower (*L*).

The ballistic rectifiers used in this study were also fabricated using EBL and oxygen plasma etching. Figure 4.8 (b) shows an atomic-force micrograph of the central part of device specifying the four terminals *S*, *D*, *U*, and *L*. The room temperature voltage-current characteristic of the device at different back-gate voltages is shown in Fig. 4.9. Since, the device dimensions were larger than the mean-free path length, ballistic transport might not be expected from the device. However, the device output was fitted to a quadratic model as shown in the inset of Fig. 4.9. It means that despite of larger dimensions, the device output followed the quadratic behaviour to the input signal in analogy with the calculations in Eq. (4.19) even in a weak nonlinear

transport regime. At V_{BG} = 0 V, the device impedance was about 3.7 kΩ. From the nonlinearity of V_{LU}-I_{SD} characteristic the intrinsic β_V was found to be around 55.57 mV/mW.

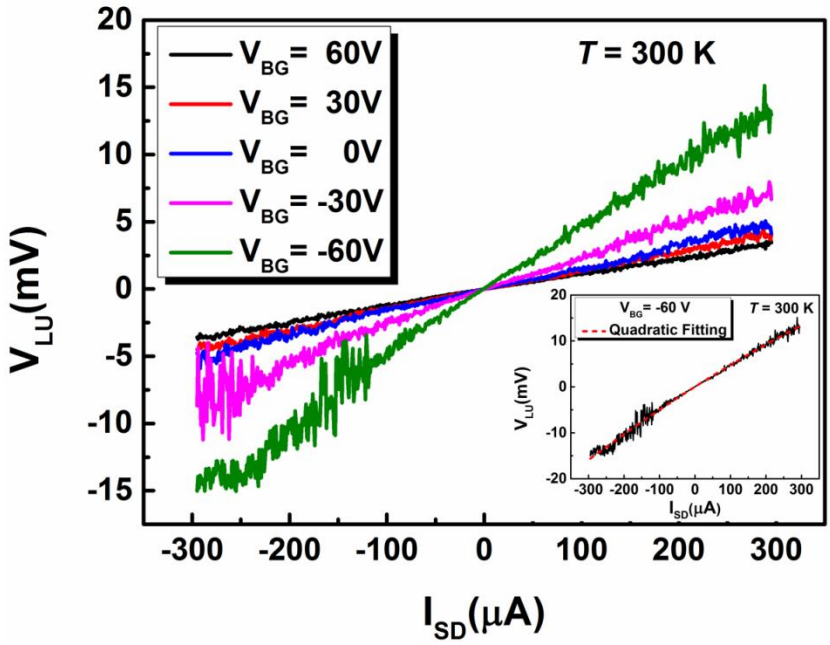

Figure 4.9 The voltage-current characteristics of a ballistic rectifier fabricated from CVD-grown graphene at different back-gate voltages measured at room temperature. The inset shows the quadratic fitting of output voltage to the input current.

An Agilent network analyser E 5061B was used as a microwave source for the characterisation of the RF properties of this ballistic rectifier. The RF signals were applied at *S* and *D* terminals using RF probes in ground-source-ground (G-S-G) configuration and output DC voltage was measured between *L* and *U* terminals using a DC voltmeter. Figure 4.10 (a) shows the rectified output DC voltage against the input frequency measured at room temperature. The applied microwave power was varied from 0-10 dBm at the back-gate voltage of 0 V. The response from the device was stable up to a frequency of 100 kHz. It started decreasing gradually beyond this frequency due to the intrinsic cut-off frequency limit. The observed cut-off frequency in the measurements matched the estimated intrinsic cut-off frequency $f = 1/2\pi RC$ (~1.6 MHz), calculated using the device impedance (~3.7 kΩ) and intrinsic gate capacitance (~2.65×10^{-11} F).

The measured β_V of the device was estimated from the measured DC output in the square-law region of device operation; it was found to be around 2.02 mV/mW. The

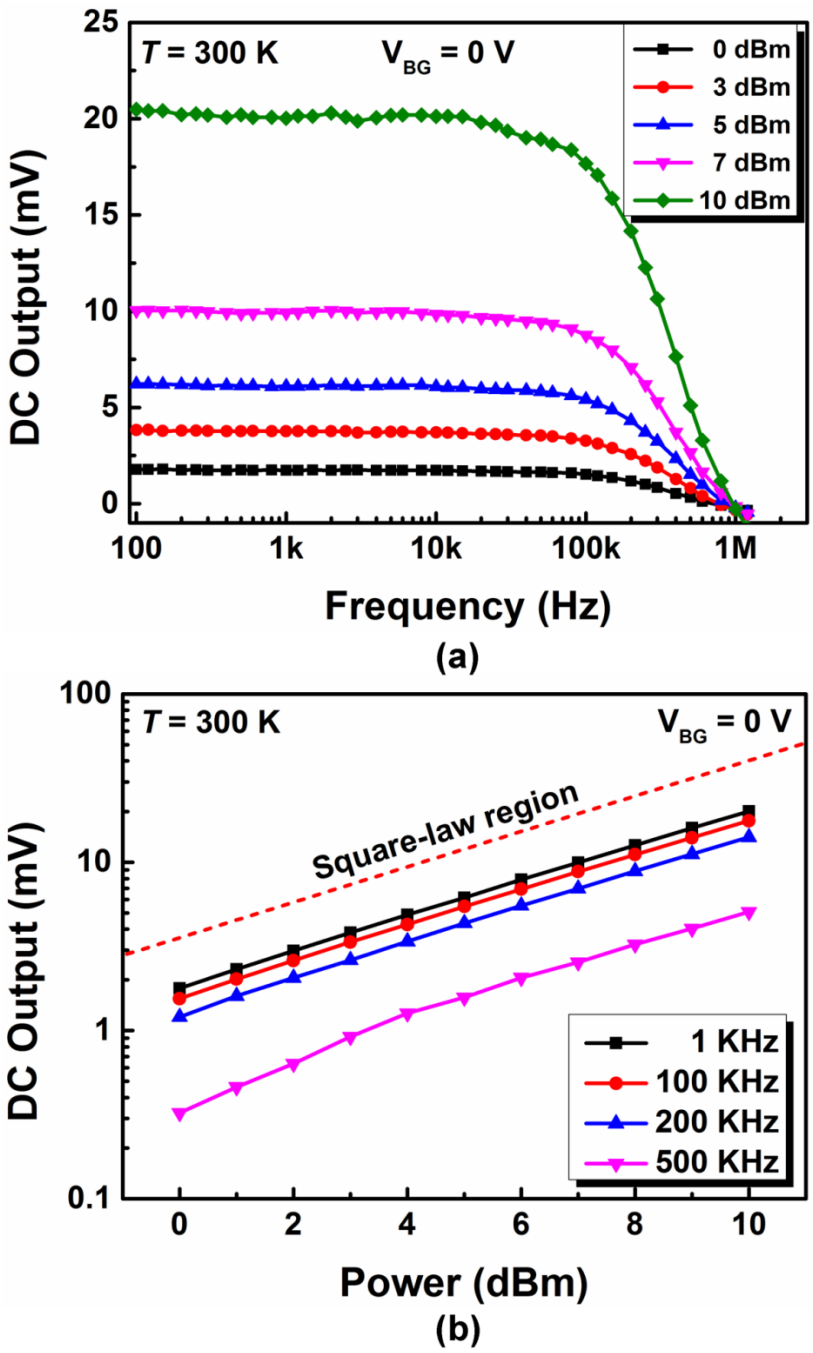

Figure 4.10 (a) Room temperature RF response as a function of input frequency at the back-gate voltage of 0 V measured by varying the RF power from 0 to 10 dBm. (b) The square-law operation of the device at the different frequencies of 1, 100, 200, and 500 kHz with respect to the applied microwave power.

β_V was observed from a device with larger dimensions than the mean-free path length at room temperature. Hence, only a few charge carriers could travel without being scattered in this device. Furthermore, the device impedance (~3.7 kΩ) was higher than the impedance of the RF signal generator (50 Ω). Therefore, there was an

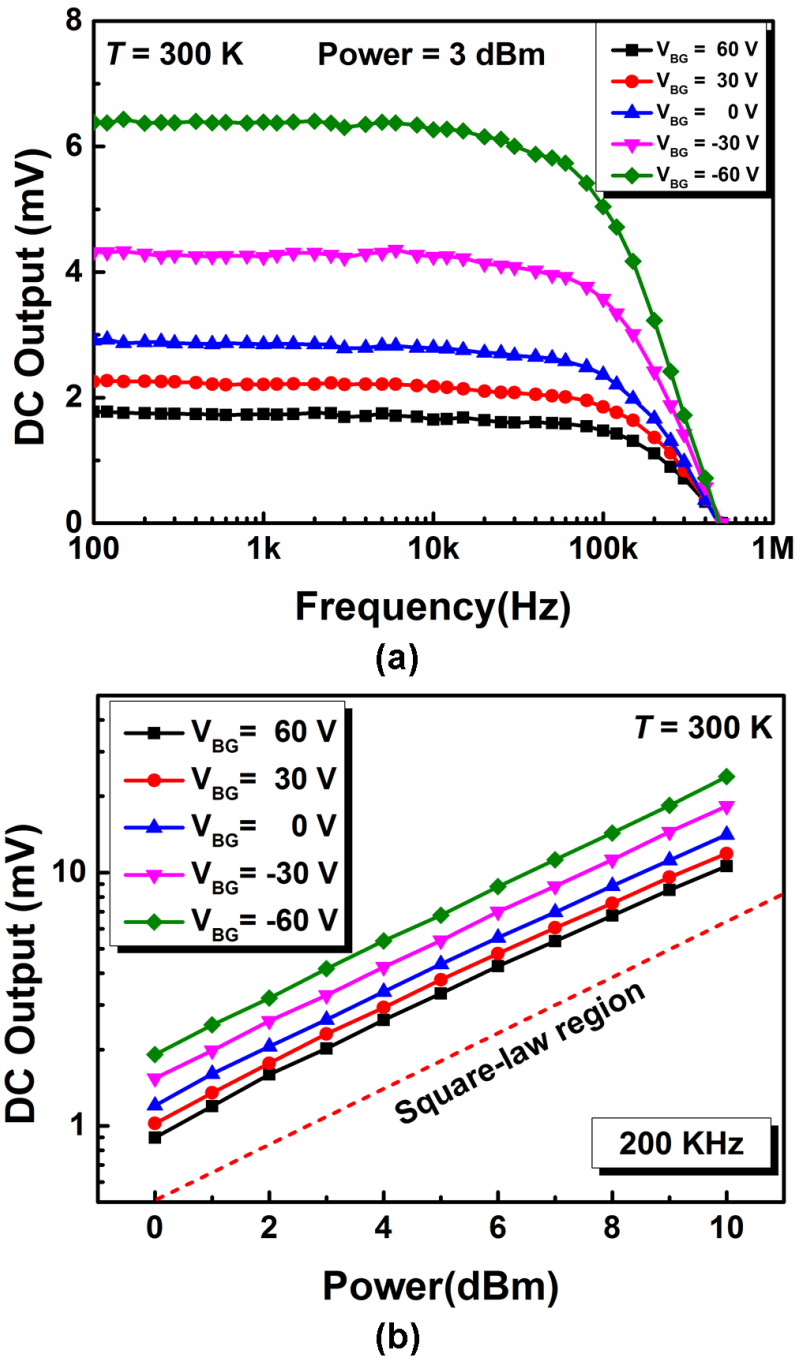

Figure 4.11 (a) The output voltage increased when more charge carriers were introduced in the device by tuning the back-gate voltage to the left of neutrality point. (b) The output voltage was linearly proportional to the input microwave power at different back-gate voltages varied from -60 to 60 V, which suggests that the device was exhibiting a square-law operation.

impedance mismatch between the device and signal generator. From the results it was estimated that only 5.26 % of input power was delivered to the device, with the rest reflected. Considering that all the power was delivered to the device, the estimated β_V of 38.47 mV/mW was quite comparable to the value obtained from DC

voltage-current characteristic. Figure 4.10 (b) shows the output DC voltage with respect to applied power at different frequencies of 1, 100, 200, and 500 kHz. The observed results were in the square-law operation (similar to a slope shown by the red-dotted line).

The above sets of experiments were repeated at different back-gate voltages to find out the effect on the RF response of the device. The back-gate voltage was used to tune the Fermi energy of graphene which, however, changed the carrier concentration in the device. The output response was measured with an input power of 3 dBm at different back-gate voltages varying from -60 to 60 V as shown in Fig. 4.11 (a). When the back-gate voltage was far away to the left from the neutrality point (V_{DP} = ~80V, in this case) the induced output voltage was large due to the high carrier concentration induced by the back gate. As the back-gate voltage approached the neutrality point, the output reduced significantly. This was attributed to a reduction in charge carriers inside the channel.

Figure 4.11 (b) shows that the output response measured as a function of applied microwave power at different back-gate voltages near the 3-dB cut-off frequency (200 kHz). The noise equivalent power (NEP), which determines the minimum possible power a detector can resolve, is proportional to thermal noise of the device. From the measured results at a back-gate voltage of 0 V, the estimated NEP was about 3.87 nW/Hz$^{1/2}$, which is close to that of commercially available uncooled thermal THz detectors [49].

4.4 Conclusions

In this work, mechanically exfoliated graphene on a 290 nm thick SiO_2 substrate was used for the fabrication of ballistic rectifiers. Two different geometries of ballistic rectifier, i.e., with and without triangular antidot, were fabricated and electrically characterised at room temperature. The device dimensions were comparable to the mean-free path length, hence, geometrically induced rectification was observed in the ballistic or at-least quasi-ballistic regime of carrier transport. The change of sign in the output voltage was observed with the change of back-gate voltage with respect to the neutrality point which tuned the carrier types from holes to electrons or vice-versa. The measured DC output response of the device was found to be quadratic

with an input AC current of 1 kHz. The highest intrinsic β_V of the ballistic rectifier was found to be 214.38 mV/mW at room temperature.

Ballistic rectifier fabricated from CVD-grown monolayer graphene has demonstrated the exceptional RF rectification at room tempetaure. Despite the larger device dimensions and impedance mismatch during the measurement, the device exhibited the stable detection (DC output) of the RF signals in the square-law region at room temperetaure. At V_{BG} = 0 V, the estimated NEP of the order of 10^{-9} W/Hz$^{1/2}$ was comparable to that of an uncooled thermal THz detectors.

More advanced nanolithography may be employed to fabricate the devices of much smaller dimensions which will ensure the ballistic transport, and hence nonlinear characteristics. By producing graphene on atomically flat, low-interface charge, insulating substrates will further improve the carrier mobilities. The increase in carrier mobility will improve the responsivity and the NEP. In addition, the device speed also scales with the carrier mobility; the graphene based ballistic rectifiers are expected to operate at THz frequencies.

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Chapter 5

Graphene nanodiode

5.1 Introduction

Graphene is a carbon allotrope where sp^2-bonded carbon atoms are densely arranged in a two-dimensional honeycomb structure [1]. The unique band structure of graphene exhibits a quasi-linear dispersion relation between energy and wave number, so that the carriers lose their effective mass and can be described by a massless Dirac equation [2]. The valence and conduction bands of graphene are cone shaped and degenerate at the corners (known as *K* points) of the hexagonal Brillouin zone. Hence, graphene is a semimetal or a semiconductor with zero bandgap with finite minimum conductivity [3]. This zero bandgap makes it impossible to switch-off a graphene based device, which in turn limits the on/off current ratio [4]. To overcome this bottleneck a lot of theoretical and experimental studies have been focused on engineering a bandgap in graphene.

The most common approach to open a bandgap is to tailor the graphene film in one dimension, i.e., narrow graphene nanoribbon (GNR) [5]-[8]. The GNRs are categorized as armchair nanoribbons and zigzag nanoribbons. The bandgaps in GNRs originate due to the quantum confinement and edge effects of electron wave function in the transverse direction [9]. The bandgap in both types of GNRs is inversely proportional to the width of nanoribbons. In recent experiments, the GNRs less than 15 nm wide have demonstrated a bandgap of 300-400 meV [6],[7]. Several

approaches have been reported to fabricate the GNRs including unzipping carbon nanotubes (CNTs) [10], chemical processes [7], reduction of graphene oxide [11], and lithographic pattering and etching [12]. Another technique to open a bandgap is to bias bilayer graphene [13]-[16]. Theoretical and experimental studies have demonstrated that the applied electric field can induce a bandgap up to 250 meV [14],[15]. Recently, other methods such as applying strain to graphene [17],[18], irradiation of graphene with an ion beam [19], and graphene growth on MgO [20] have been proposed to induce a bandgap.

An ultra-high mobility (200,000 $cm^2/V.s$ [21]), high carrier velocity (4.5×10^7 cm/s [22]), and electric-field induced ambipolar carrier conduction have made graphene a promising material for field-effect transistors even at the expense of low on/off ratio. The field effect in a graphene device is achieved by applying a back-gate voltage to induce carrier modulation. When the Fermi level moves into the valence or conduction band, the holes or electrons begins to dominate the current transport. The GNR based field-effect transistors demonstrate a very large current on/ off ratio due to the localized edge states even at room temperature [23],[24]. Furthermore, graphene based field-effect transistor (GFET) on Si/SiO_2 have been demonstrated to work up to the frequency of 427 GHz, though the projected intrinsic cut-off frequency is more than 1 THz [4],[25],[26]. Recently, the lateral charge density of the GFET channel has been electrostatically modulated using an alternative gate arrangement, where the gates are located in the same plane next to the channel instead of located above or underneath [27]-[29]. The advantage of this architecture is the single step fabrication of side gates and channel. Furthermore, it does not require the deposition of any top-gate dielectric which often degrades the mobility and also causes the hysteresis in the graphene channel. The side-gate induced field effect over a large voltage range can be promising for on/off ratios comparable to that of global back-gate or top-gate schemes [29].

Historically, diodes were invented first; with much less stringent material requirements. The first application of crystal based diodes to detect radio waves was demonstrated by an Indian physicist Jagadish Chandra Bose in 1894 [30], whereas the solid-state transistor was invented in 1947 [31]. The speed is more important for a diode in most applications rather than the on/off ratio. Thus, it is easier to design a fast diode by employing graphene because of its high mobility and carrier speed. The

functionality of a graphene diode does not require a bandgap or multi-layer structure. The diodes play a key role in communications, detection, mixing, and imaging due to its nonlinear characteristic, operating speed, threshold voltage, and ease of integration with rectenna. Usually, the diode is preferred rather than the transistor for very high switching speed applications.

This chapter presents the first experimental investigation of the graphene nanodiode, also known as self-switching device (SSD) [32]. The graphene SSD utilizes the intriguing properties of the graphene nanochannel and a side-gate scheme. The operation of SSD is based on an asymmetric nanochannel, which produces a nonlinear current-voltage (*I-V*) characteristic. This geometrically induced strong nonlinear *I-V* characteristic is similar to that of a conventional diode. However, this device does not require any *p-n* junction or Schottky barrier along the direction of current conduction. The planar nature of the device architecture has allowed the fabrication of an array of 22 SSDs connected in parallel. The DC characterisation of the fabricated devices was performed in ambient environment. The device has demonstrated the exceptional RF properties in contrast to graphene *p-n* junctions [33].

5.2 Self-switching effect

The self-switching device can be fabricated by tailoring the boundaries of a narrow semiconductor channel to break its symmetry as shown in Fig. 5.1 (b). The graphene SSD can be regarded as a graphene nanochannel based double side-gated transistor (SGT) that is connected as a diode by short circuiting the drain and both gates together [34].

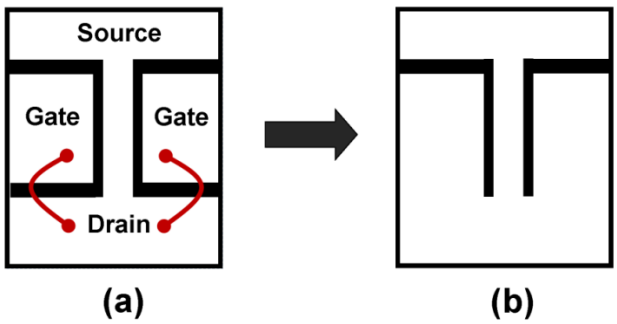

Figure 5.1 (a) Schematic diagram of the side-gate transistor. (b)When the gates are connected to the drain, the structure is analogous to a self-switching device.

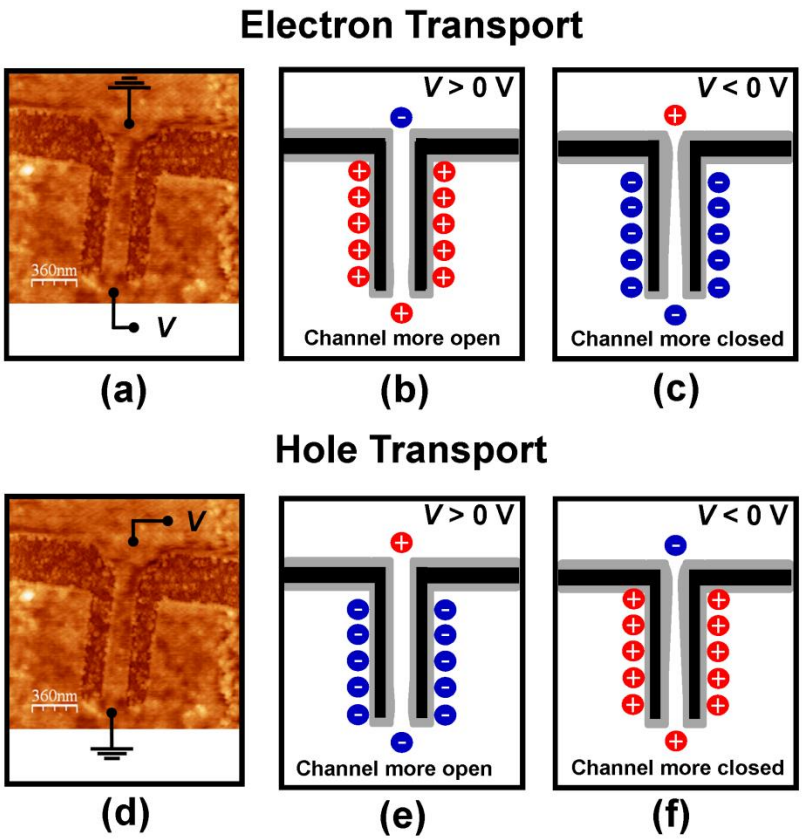

Figure 5.2. (a) The atomic-force micrograph of a typical SSD fabricated from graphene. (a) and (d) show the bias connections at the two terminals of the device for electrons and holes transport regime, respectively. The effective channel width increases (b) and (e) for the positive bias V > 0 V. However, a negative bias V < 0 V in (c) and (f) reduces the channel width, which gives a rise to diode-like *I-V* characteristic.

The graphene SGT is a planar field-effect transistor, in which the gate electrodes are located on the sides of a conducting one dimensional graphene sheet as illustrated in Fig. 5.1 (a). The device terminals are denoted as source, drain and gate electrodes. The two gate areas of the SGT are insulated from the conducting channel, and hence from source and drain, by the etched trenches shown by the dark area lines.

The key fabrication step of the SSD is to create two L-shaped insulating grooves. An atomic-force micrograph of a typical graphene SSD is shown in Fig. 5.2 (a). The broken symmetry of the device was established by extending the trenches to the device boundary which ensured that the current can only flow through the channel. Figures 5.2 (a) and (d) demonstrate the bias connection when the electrons and holes were the majority carriers in channel, respectively. When electrons were the majority carriers and there was a negative voltage ($V < 0$ V), the negative charges around the channel pushed the electrons out of the channel, thus resulting in the device

becoming more resistive as depicted in Fig. 5.2 (c). However, a positive voltage (V > 0 V) increased the positive charges around the trenches, which attracted electrons into the channel, making it more open and conducting as illustrated in Fig. 5.2 (b). Therefore, the device favoured current flow only in one direction and as a result nonlinear *I-V* characteristic similar to that of a conventional diode was obtained [32]. The above described mechanism, which leads to a preferred direction of current flow, may be referred to as the self-switching effect of the device. Correspondingly for positive charge carriers (holes), the opposite voltages had to be applied across the device to obtain the similar self-switching effect as illustrated in Figs. 5.2(d)-(f) [35].

This operation does not require the ballistic transport of charge carriers, since the device dimensions are an order of magnitude larger than the mean-free path length. Hence, the SSDs differ from the ballistic rectifiers which have been demonstrated working at room temperature in chapter 3 and 4.

5.3 Nonlinear *I-V* characteristic analysis

Being a nonlinear device, the SSD can be used to rectify an AC signal which is converted to DC output. The detection properties of such rectifiers depend upon the nonlinear *I-V* characteristics [36]. Therefore, it is important to analyse the *I-V* characteristic of SSD as a low level detector such as diode. The *I-V* characteristics of SSDs can be written as [37]:

$$I = f(V)\,. \tag{5.1}$$

The voltage across the SSD may be given as the superposition of an applied DC bias V_0 and an AC input voltage $v_{AC} = v_0 \cos(\omega t)$:

$$V = V_0 + v_{AC}\,. \tag{5.2}$$

The Taylor series expansion of Eq. (5.1) about V_0 leads to the small signal approximation of the current:

$$I = I_0 + \frac{v_{AC}}{1!} f^{(1)} + \frac{v_{AC}^{\;2}}{2!} f^{(2)} + \frac{v_{AC}^{\;3}}{3!} f^{(3)} + \cdots + \frac{v_{AC}^{\;N}}{N!} f^{(N)}\,, \tag{5.3}$$

where $I_0 = f(V_0)$ is the DC bias current, $f^{(N)}$ is the Nth order derivative of $f(v)$ with respect to V. Substituting $v_{AC} = v_0 \cos(\omega t)$ in Eq. (5.3) yields:

$$I = I_0 + \left[\frac{v_0^{\,2}}{4} f^{(2)} + \frac{v_0^{\,4}}{64} f^{(4)} + \cdots \right] + \left[v_0 f^{(1)} + \frac{v_0^{\,3}}{8} f^{(3)} + \cdots \right] \cos(\omega t) + \cdots \quad (5.4)$$

As can be observed, the first bracket term in Eq. (5.4) is equal to the DC rectified current Δi. In a small-signal approximation, i.e., low-level input power, the higher order terms become insignificant; hence Δi can be written as:

$$\Delta i = \frac{v_0^{\,2}}{4} f^{(2)} + \frac{v_0^{\,4}}{64} f^{(4)} . \quad (5.5)$$

Therefore, in an open-circuit configuration, the rectified DC voltage Δv can be given as:

$$\Delta v = \Delta i R_D = \frac{\Delta i}{f^{(1)}} = \frac{v_0^{\,2}}{4} \frac{f^{(2)}}{f^{(1)}} , \quad (5.6)$$

where $R_D = 1/f^{(1)}$ is the differential resistance of the SSD and $f^{(2)}$ is referred to as the bowing coefficient in I-V function. Equation (5.6) shows that in the small-signal approximation, the detected open-circuit voltage is proportional to the square of microwave input signal. This behaviour is known as the square-law operation of the device. This square-law response is a desirable trait for the microwave detector [37].

5.4 Self-switching device

5.4.1 Device fabrication

Mechanically exfoliated monolayer graphene produced on silicon oxide (SiO_2) similar to one in Chapter 4, used for the fabrication of ballistic rectifiers, was utilised for the fabrication of SSD. The neutrality point or Dirac point (V_{DP}) of the fabricated Hall bar structure was observed at the back-gate voltage of -4 V. The field-effect mobility for holes and electrons were 1572 and 1810 cm^2/V.s, respectively. The patterns of SSD were exposed in the polymethyl methacrylate (PMMA) coated Hall bar structure of the graphene by employing electron-beam lithography (EBL). The insulated grooves of the device were etched using low power oxygen plasma.

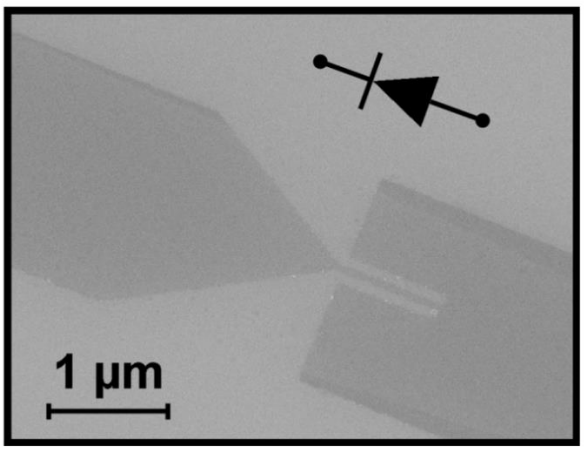

Figure 5.3 Scanning electron micrograph of a typical SSD fabricated from monolayer graphene. The channel width and length of the device were 90 nm and 880 nm, respectively. The schematic of diode shows the preferred direction of current flow when electrons were the majority carriers.

Figure 5.3 shows a scanning electron microscopic image of a typical SSD fabricated from monolayer graphene. The channel width and length of the fabricated device were 90 and 880 nm, respectively. The schematic of diode demonstrates the preferred direction of current flow considering that the electrons were the majority charge carriers in the SSD channel. The trenches which isolate the two terminals of the device were intentionally made wider than that of along the channel boundaries. This was done in order to reduce the capacitive coupling between two terminals which helps to improve the cut-off frequency, hence the operating speed of the device [38]. The trenches along the channel are significant as they not only insulate the device with the side electrodes but also induce an asymmetry in the channel.

5.4.2 Results and discussion

Figure 5.4 shows the *I-V* characteristic of the graphene SSD fabricated from monolayer graphene as shown in Fig. 5.3. The measurements were performed using an Agilent parametric analyser E 5270B. The room temperature *I-V* characteristic in Fig. 5.4 was measured at the back-gate voltage of 0 V. It is worth mentioning here that to the right of neutrality point (i.e., V_{DP} = -4 V) electrons were the majority carriers. Hence, the field-effect induced electrons movement inside the channel had played an important role in obtaining the nonlinear *I-V* characteristic.

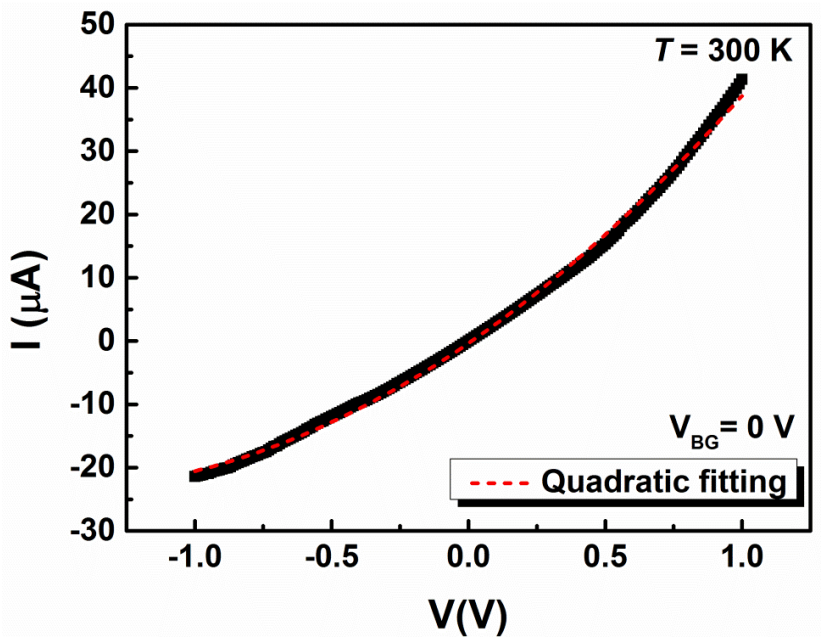

Figure 5.4 Room temperature current-voltage characteristic of graphene SSD fabricated from monolayer exfoliated graphene on SiO_2 at the back-gate voltage of 0 V.

The operation of graphene SSD can be analysed as a standard metal-oxide-semiconductor field-effect transistor (MOSFET), but connecting the drain and the gate together [39]. Using Shichman-Hodges model [40], the current I can be given as [41]:

$$I = zWJ = zWqnv_d = zWQv_d \,, \tag{5.7}$$

where z is thickness of the channel, W is width of the channel, J is the current density, q is the carrier charge, n is the carrier density, and v_d is the drift velocity. Q is the charge induced by the gate and can be written as:

$$Q = \frac{-C(V_G - V_T - V(y))}{W}, \tag{5.8}$$

here, C is the capacitance, V_G is the gate voltage, V_T is the threshold voltage, and $V(y)$ represents the potential in the channel as a function of y along the channel. For a traditional semiconductor, the drift velocity can be evaluated as:

$$v_d = -\mu \frac{dV(y)}{dy}, \tag{5.9}$$

where μ is the mobility. Substituting Eqs. (5.8) and (5.9) into Eq. (5.7), I becomes:

$$I = \mu z C\left(V_G - V_T - V(y)\right)\frac{dV(y)}{dy}. \tag{5.10}$$

The continuity implies $\int I dy = IL$, where L is the channel length. Hence, by integrating, the $V(y)$ side, between 0 and the drain voltage V_D results in Eq. (5.11).

$$I = \frac{\mu z C}{L}\left(\left(V_G - V_T\right)V_D - \frac{V_D^{\,2}}{2}\right). \tag{5.11}$$

In the case of monolayer graphene, in the intrinsically doped regime, V_T will be 0 since there is no bandgap. For the SSD, $V_G = V_D = V$ and the capacitance $C = C_{SSD} = C_H$ will be due to the horizontal trenches along the channel. Thus, Eq. (5.11) simplifies to a square-law:

$$I = \frac{\mu z C_{SSD}}{L}\frac{V^2}{2} = KV^2. \tag{5.12}$$

Here, $K = \mu z C_{SSD}/2L$ is a fitting parameter. C_{SSD} can be extracted from the measured *I-V* characteristic by fitting to Eq. (5.12), as the mobility and length of the device are known parameters.

SSD capacitance

As described earlier, the operation of SSD relies on the field effect of bias induced charges around the nanochannel. Changes in the applied voltage move charges both within the channel and in the both sides of trenches which isolate the two terminals of the device. As a result, the device exhibits the intrinsic (C_H) and extrinsic (C_V) capacitances caused by the horizontal and vertical trenches around the channel, respectively as illustrated in Fig. 5.5 (a). Simplified equivalent circuit in Fig. 5.5 (b) shows that the total capacitance C_T of SSD can be obtained by evaluating C_H and C_V. The extrinsic capacitances, also referred as parasitic capacitances, do not contribute to the nonlinear property of the *I-V* characteristics [42], hence should be minimised by making wide trenches as discussed earlier. Because of the planar geometry of the device structure, i.e., contacts are on the same side of device active region, such capacitances are smaller to that of a conventional vertical diode of same size [32].

The technique of conformal mapping was utilized to calculate the capacitances [43]. Figure 5.6 (a) shows a schematic illustration of the in-plane geometry of a trench, which consists of two conducting infinitely long coplanar strips [44], i.e., the

graphene sheet in this case, having a width of *s* and separated by a trench of width *d*. Graphene is an atomically thin semiconductor with a thickness of about 0.335 nm. Hence, the strips of graphene in Fig. 5.6 (a) can be considered as embedded in the dielectric medium with a relative dielectric constant ε_r = (3.9+1)/2, where 3.9 and 1 are the dielectric constants of SiO_2 and air, respectively, as shown in Fig. 5.6 (b). For symmetry, the upper half-plane *t* as shown in Fig. 5.6 (c) is transformed conformally onto a rectangle by the elliptical integral, which follows the Schwarz-Christoffel formula, and can be defined through the relation [44],[45]:

$$Z(t,k) = \int_0^t \left[\left(1-t^2\right)\left(1-t^2k^2\right)\right]^{-1/2} dt \tag{5.13}$$

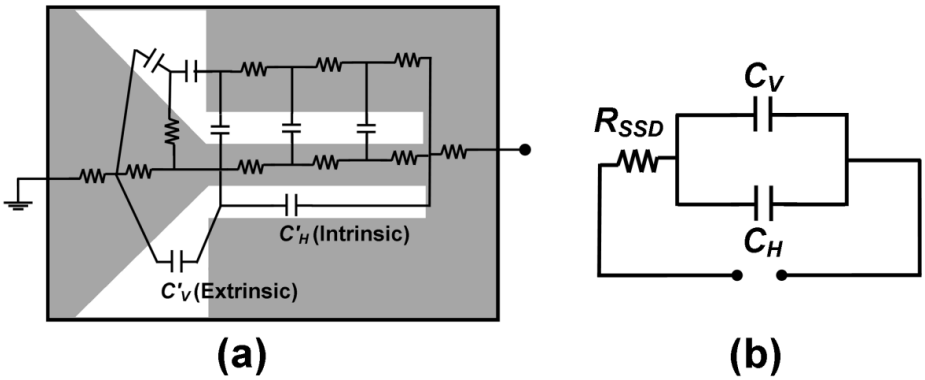

Figure 5.5 (a) Possible equivalent circuit of the SSD illustrating the intrinsic (C'_H) and extrinsic (C'_V) capacitances due to the horizontal and vertical trenches, respectively [42]. (b) Simplified equivalent circuit suggests that both the capacitances are in parallel to each other.

In general, the upper limit integral is said incomplete and for t = 1, the complete integral of the first kind is K (k) where k is the modulus [43],[44]. The complementary modulus can be defined through $k' = \sqrt{1-k^2}$ and the complete integral of modulus k' is K' (k) = K (k').

The capacitance of two neighbouring conducting graphene strips at the both sides of one vertical trench can be calculated analytically as [44]:

$$C'_V = \varepsilon_0 \varepsilon_r \frac{K'(k)}{K(k)}, \tag{5.14}$$

where, ε_r is an average of the dielectric constants of two half-planes, i.e., air and SiO_2. The k can be defined in terms of s and d as:

$$k = \frac{d}{2s+d}. \tag{5.15}$$

For wide strips of graphene (s >> d), the logarithmic approximation $k \approx 4\exp(-\pi K'/K)$ can be substituted into Eq. (5.14) [46], and it becomes:

$$C'_V = \varepsilon_0 \varepsilon_r \frac{K'(k)}{K(k)} = \frac{1}{\pi}\ln\frac{4}{k} \approx \frac{1}{\pi}\ln\left(8\frac{s}{d}\right). \tag{5.16}$$

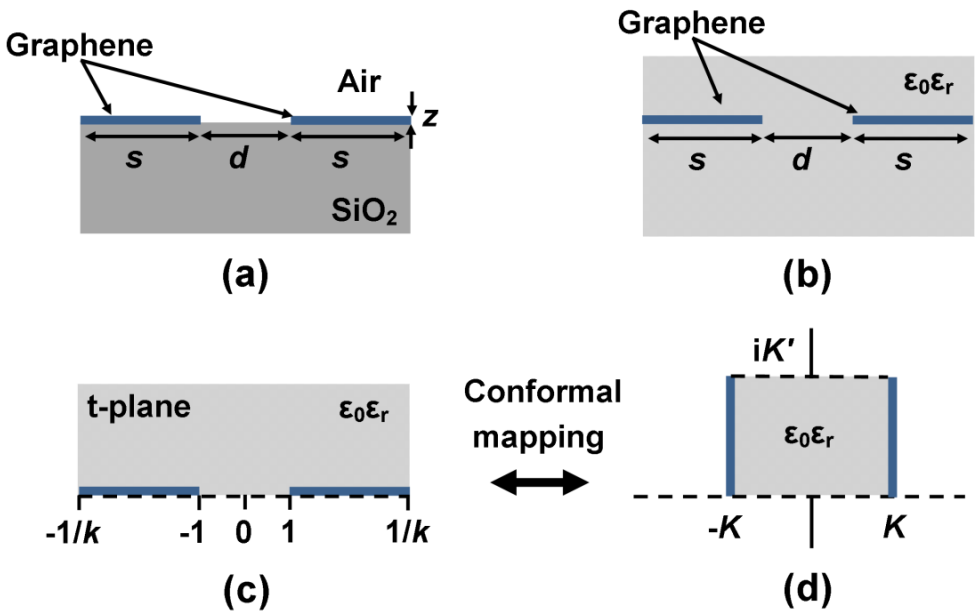

Figure 5.6 (a) Schematic illustration of a trench in a graphene sheet, used to calculate the extrinsic capacitance. (b) In order to calculate the extrinsic capacitance, the graphene strips are considered as embedded in a dielectric medium with relative dielectric constant ε_r. (c) The upper half-plane with graphene sheet as coplanar strips. (d) Equivalent rectangular geometry of (c) after applying the conformal mapping.

In the most relevant range $10^{-2} < d/s < 1$, the expression for the extrinsic capacitance in Eq. (5.16) can be further simplified by an approximation of zeroth order and the total capacitance per unit length amounts to ~$2\varepsilon_0\varepsilon_r$ [46]. However, Eq. (5.16) needs to be evaluated for obtaining more accurate value. The overall extrinsic capacitance C_V will be equal to twice of C'_V due to two vertical trenches, as shown in Fig. 5.5 (a), and can be written as:

$$C_V = 2C'_V = 2\varepsilon_0 \varepsilon_r \frac{K'(k)}{K(k)} \approx \frac{2}{\pi}\ln\left(8\frac{s}{d}\right) \tag{5.17}$$

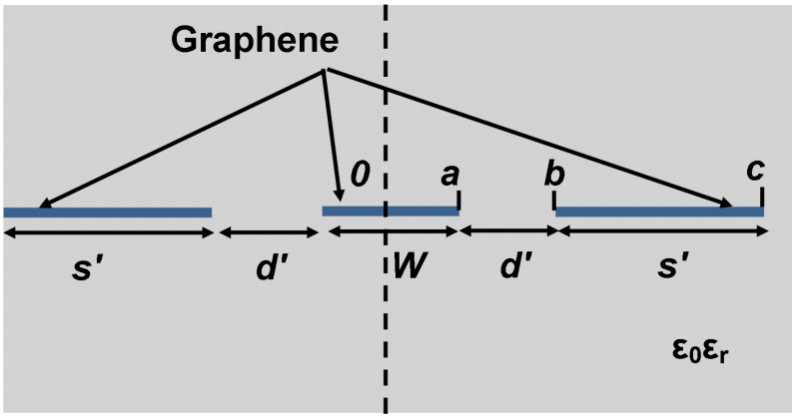

Figure 5.7 Schematic illustration of horizontal trenches of SSD used for the calculation of intrinsic capacitances. The structure can be viewed as a coplanar waveguide.

In contrast, the intrinsic capacitances of SSD are mainly due to the horizontal trenches, which play a key role in obtaining the nonlinearity in *I-V* characterstic. Figure 5.7 shows the cross-sectional view of the SSD channel of width *W* separated from two electrodes of *s′* width at the both sides by two horizontal trenches of width *d′*. The capacitance can be calculated by involving only one quarter of the plane because of the symmetry. The resultant pair of graphene strips in upper half-plane can be analysed as above and the total capacitance for whole structure in Fig. 5.7 can be evaluated as [44]:

$$C_H = 4\varepsilon_0\varepsilon_r \frac{K(k_1)}{K'(k_1)} \tag{5.18}$$

where

$$k_1 = \frac{a}{b}\sqrt{\frac{c^2 - b^2}{c^2 - a^2}} \tag{5.19}$$

here $a = W/2$, $b = (W/2+d')$ and $c = (W/2+d'+s')$ as shown in Fig. 5.7. The intrinsic capacitance (per unit length) in Eq. (5.18) can be simplified to $\sim 4\varepsilon_0\varepsilon_r$ for the typical values of W/d' in the range of 1-10, where $K/K' \approx 1$ [46].

For the device shown in Fig. 5.3, Eqs. (5.17) and (5.18) yielded $C_V = 2.76 \times 10^{-17}$ F and $C_H = 10.6 \times 10^{-17}$ F. Fitting the measured results to Eq. (5.12) gave $C_H = 16.17 \times 10^{-17}$ F. It is worth mentioning that the value of C_V cannot be determined from the *I-V* characteristics because it only becomes pronounced at high frequency applications. The measured value of C_H is in accordance with the theoretically calculated value of

the intrinsic capacitance. The above quantitative calculations were performed by considering graphene as a perfect conducting sheet, due to which it has resulted in the smaller values than that of the measured ones. The measured value of C_H for graphene SSD is an order of magnitude lower than that of earlier reported for Si SSD (250×10^{-17} F) [47].

Intrinsic responsivity

The intrinsic voltage responsivity, also known as detection sensitivity, β_V of the SSD can be defined as the ratio of detected output voltage over the applied microwave input power, considering that the input power is totally absorbed by the device. In a square-law operation, it can be determined from the nonlinear behaviour of the *I-V* characteristics [48]. The zero-bias intrinsic β_V can be written as:

$$\beta_V = -\left.\frac{\frac{d^2V}{dI^2}}{\frac{dV}{dI}}\right|_{I_0=0} . \tag{5.20}$$

From the measured results, Eq. (5.20) yielded the intrinsic β_V of 21,840 mV/mW. The observed value of responsivity is better than that previously achieved in GaAs SSDs (up to 19,000 mV/mW) and InGaAs SSDs (up to 9,600 mV/mW) [49]. Unfortunately, the device was burnt during the measurement before the real RF measurement to extract the measured β_V. Moisture, chemical contaminations, and nanoparticles of graphene/graphite produced during the fabrication process were the main reason to cause the burnout.

5.5 SSDs array

5.5.1 Device fabrication

The planar architecture of an SSD permits the fabrication of simple circuits without using interconnection layers which in turn minimizes the parasitic elements. A linear array of SSDs connected in parallel can be fabricated by simply placing individual SSDs next to each other. The fabrication of an array of SSDs reduces the overall impedance of the device, thus reduces the thermal noise. Furthermore, the increase in charge carriers responsible for the current conduction also averages out the impact of

1/*f* or flicker noise [50]. Figure 5.8 (a) shows an optical microscopic image of a linear array of 22 SSDs connected in parallel. CVD-grown monolayer graphene was used for the fabrication of an array. The graphene films were transferred to a thermally grown 300 nm thick SiO_2 substrate. A highly *p*-doped Si substrate was used as a global back gate to modulate the carrier concentrations in graphene.

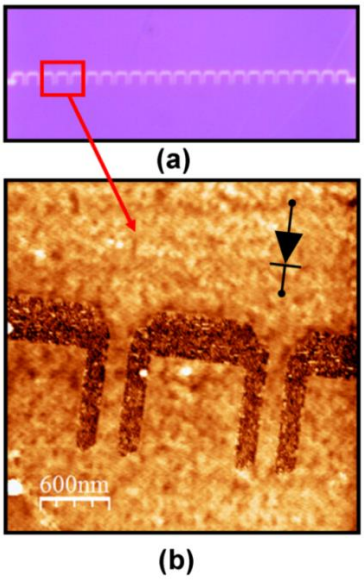

Figure 5.8 (a) The microscopic image of 22 SSDs connected in parallel fabricated from CVD-grown graphene. (b) The atomic-force micrograph of two SSDs connected in parallel shows the lithographic channel width and length of about 180 nm and 1 μm. The schematic of diode shows the direction of current conduction in the hole transport regime.

The RF contacts were patterned onto the graphene using standard photo-lithography followed by oxygen-plasma etching. All the fabricated devices exhibited *p*-type doping and the neutrality point was found to be far away to the right of 0 V (V_{DP} > 80 V). The field-effect mobility of 644 $cm^2/V.s$ was estimated for this device. Adsorbents/ residues left behind by photo-lithography fabrication processes were the main reason for having such low mobility [51]. Figure 5.8 (b) shows an atomic force micrograph of two SSDs connected in parallel. The lithographic channel width and length of a SSD were 180 nm and 1 μm, respectively.

5.5.2 Results and discussion

Figure 5.9 shows the room temperature *I-V* characteristics of the SSDs array, fabricated from CVD-grown monolayer graphene, at different back-gate voltages varied from -30 to 30 V. The device exhibited a very small nonlinearity to that of the

device fabricated from exfoliated graphene. This would be attributed to the wide channel of individual SSD. However, the device exhibited the quadratic response predicted by Eq. (5.12) as shown by dashed lines in Fig. 5.9.

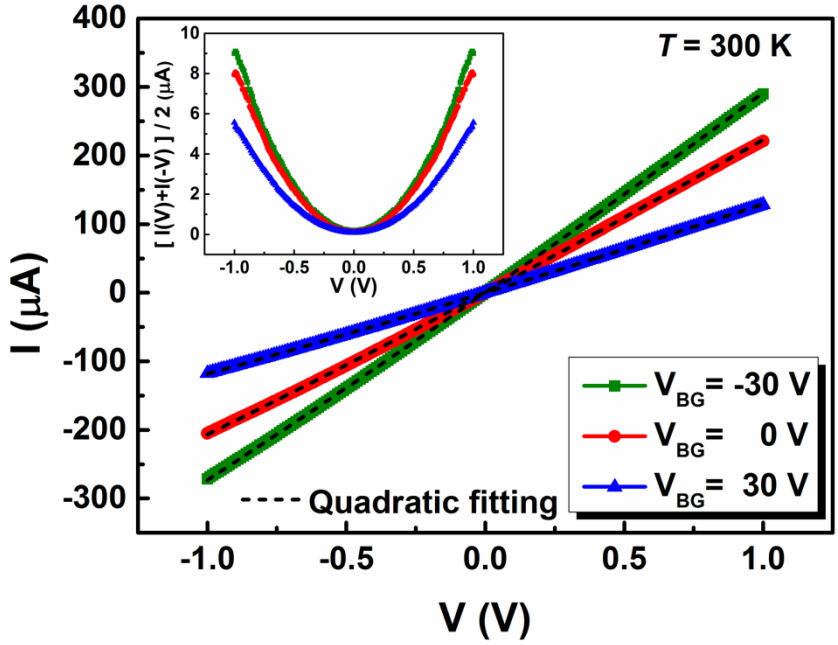

Figure 5.9 Room temperature *I-V* characteristic of the array of 22 SSDs connected in parallel fabricated from CVD-grown monolayer graphene on SiO_2 at different back-gate voltage ranging from -30 to 30 V. The inset shows the calculated nonlinear output as a function of bias voltage for the device at V_{BG} = -30, 0, 30V. The *I-V* characteristics were fitted to the quadratic fitting (dashed line) as described by Eq. (5.12).

The intrinsic capacitance of the SSD array was estimated from the measured data by fitting to Eq. (5.12). The measured value of $C_H = 5.61 \times 10^{-15}$ F, at $V_{BG} = 0$ V, was quite comparable to the theoretically calculated value of 1.44×10^{-15} F. Using Eq. (5.17), the theoretically estimated value of the extrinsic capacitance was around 0.71×10^{-15} F. The measured values of capacitances at different back-gate voltages were almost same.

Despite of almost linear like response, the nonlinearity, i.e., $[I(V)+I(-V)]/2$, was estimated from the measured results as shown in the inset of Fig. 5.9. To detect radio frequency (RF) signals, the nonlinear *I-V* characteristic near zero-bias of the SSDs is required [37]. The setup used for the RF measurement is shown in the inset of Fig. 5.10 (b). The RF signals were generated by an Agilent network analyser E 5061B.

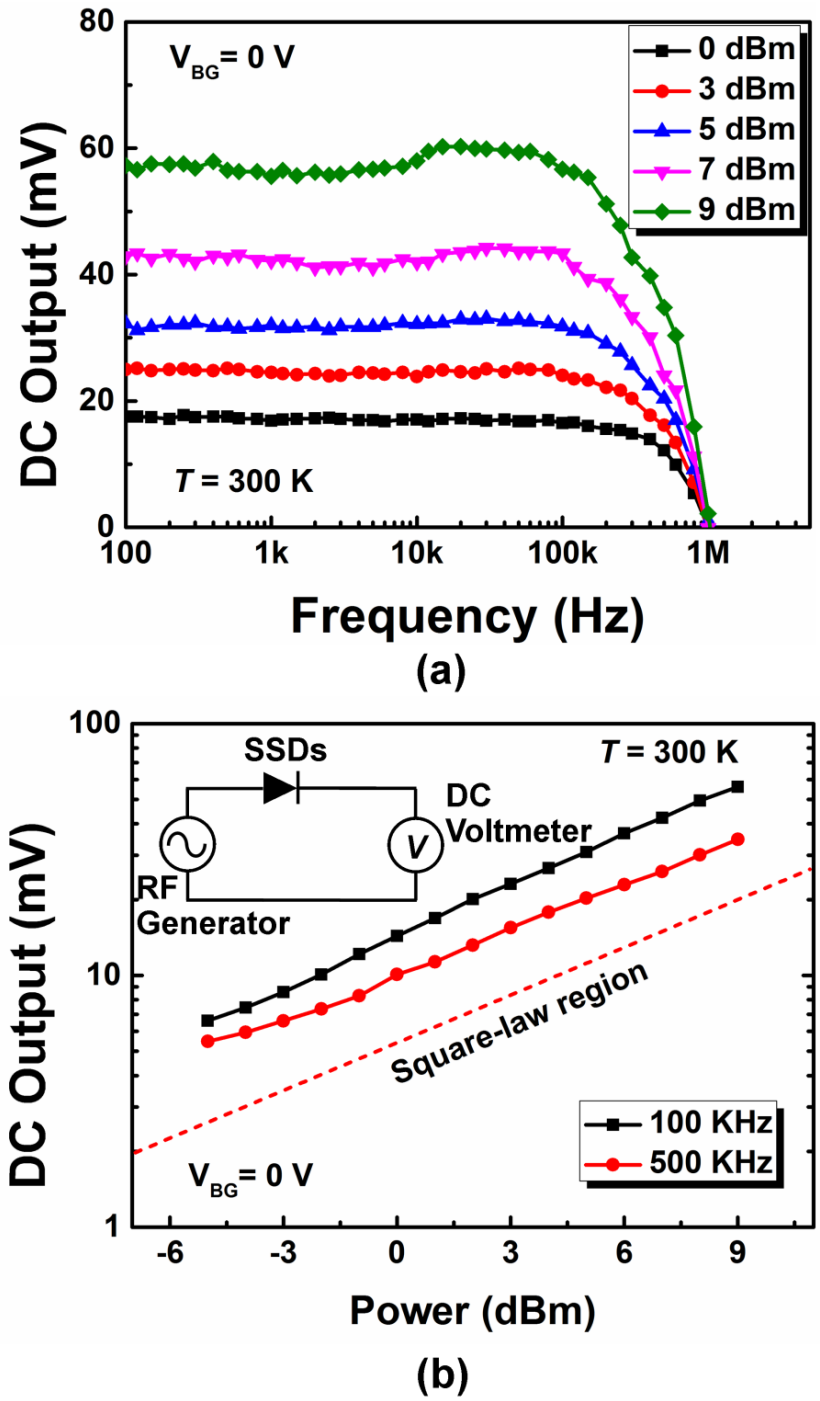

Figure 5.10 (a) The frequency response was obtained up to 1 MHz, which was the cut-off frequency. (b) The DC output voltage followed the so called square-law which means that the DC output was proportional to the input power. The inset shows the setup used for the RF characterisation of SSDs.

The rectified output from the device was measured using a voltmeter. Figure 5.10 (a) shows the rectified DC output voltage measured as a function of input signal frequency. The RF power was varied from 0 to 9 dBm. The response obtained at room temperature was stable up to 100 KHz, however, the device worked up to a

frequency of ~1 MHz. The gradual reduction in the output after 100 kHz was expected due to the cut-off frequency limit [36]. The zero-bias resistance (R_0 ~ 4.6 kΩ) and gate capacitance (C_G ~ 2.65×10^{-11} F) due to the SiO_2 yielded an intrinsic cut-off frequency ($f = 1/2\pi R_0 C_G$) of 1.2 MHz, which was in good agreement with the measured RF response of the device. The measured DC output was linearly proportional to the applied microwave power at the frequencies of 100 and 500 KHz as shown in Fig. 5.10 (b), which suggests that the device was operating in the square-law region in an analogy with the calculations in Eq. (5.6).

Figure 5.11 shows the output DC voltage of the device as a function of input power at different back-gate voltages varied from -30 to 30 V. The variation in cut-off frequency from about 200 kHz to 2 MHz was observed due to the change in the charge carrier concentration at different back-gate voltages, which in turn altered the device impedance as shown in the inset of Fig. 5.11.

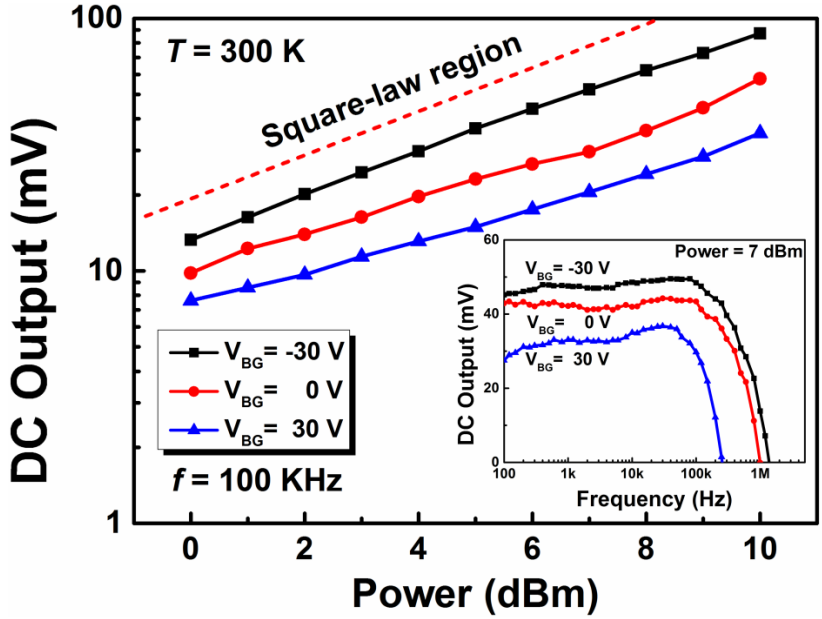

Figure 5.11 The device exhibited square-law operation at different back-gate voltages in analogy with Eq. (5.6). In the inset, frequency response demonstrated the shift in cut-off frequency from about 200 kHz to 2 MHz at different back-gate voltages. This change was observed due to the alteration in carrier concentration, thus the effective impedance of the device, at different voltages.

The network analyser is normally modelled by a RF signal generator with an output impedance (Z_{NA}) of 50 Ω. Since the R_0 of the SSD array at zero-bias, varied from 3.5 to 7.9 kΩ at V_{BG} from -30 to 30 V, respectively, was much higher than Z_{NA}. Hence, a large impedance mismatch between the signal generator and device was expected by

assuming no power loss in the coaxial connections. The mismatch in impedance can be found by calculating the actual RF power delivered P_d to the device as described in chapter 3. It was estimated that only of about 4.2 % of power was delivered to the device at V_{BG} = 0 V (R_0 ~ 4.6 kΩ), with the rest reflected.

The measured β_V was calculated from the output DC voltage divided by the input microwave power [37]. At V_{BG} = 0 V, room temperature β_V was found to be around 9.8 mV/mW, when only 4.2 % of power was delivered to the device. However, the intrinsic β_V of 354.99 mV/mW was estimated from the *I-V* characteristics, which is quite close to a typical value of β_V for a conventional diode ranging from 400-1500 mV/mW [36]. It can be evident from Fig. 5.12, that β_V decreased linearly with the increase in back-gate voltage which increases the device impedance accordingly. The intrinsic β_V can be improved significantly by reducing the value of device resistance at zero-bias.

Noise equivalent power

The low value of zero-bias impedance not only improves the impedance mismatch but also reduces the thermal noise of the device. The thermal noise can be defined as $\sqrt{4kTR_0}$ and is related to the noise equivalent power (NEP) [52]. The NEP is an important parameter to define the zero-bias noise performance of the device. At frequencies high enough to neglect the excess noise, the NEP can be calculated from the thermal noise and the measured β_V [48], which is proportional to the thermal noise and hence to $\sqrt{R_0}$:

$$NEP = \frac{\sqrt{4kTR_0}}{\beta_V} . \tag{5.21}$$

Figure 5.12 shows the NEP as a function of back-gate voltage, estimated from the measured results by fitting to Eq. (5.21). The linear increase in NEP was directly correlated to the change in back-gate induced current carriers. The obtained values of NEP are three orders of magnitude higher than the state-of-art Schottky diode produced by Virginia Diodes Inc. [48].

The NEP can be improved by connecting several SSDs in parallel which in turn reduces R_0. The planar nature of device is suitable for obtaining such a large array

without introducing parasitic elements due to the interconnects. Balocco *et al*. [53] have demonstrated that the overall noise in a very large SSD array can be minimized to that of a single device. Considering that the Δi_s and n_s are the rectified DC current and rms noise generated by a single SSD, respectively. The total current rectified (ΔI) by M SSDs connected in parallel can be written as:

$$\Delta I = M \times \Delta i_s \,, \tag{5.22}$$

and the total rms current noise N is:

$$N = \sqrt{M \times n_s^2} \,. \tag{5.23}$$

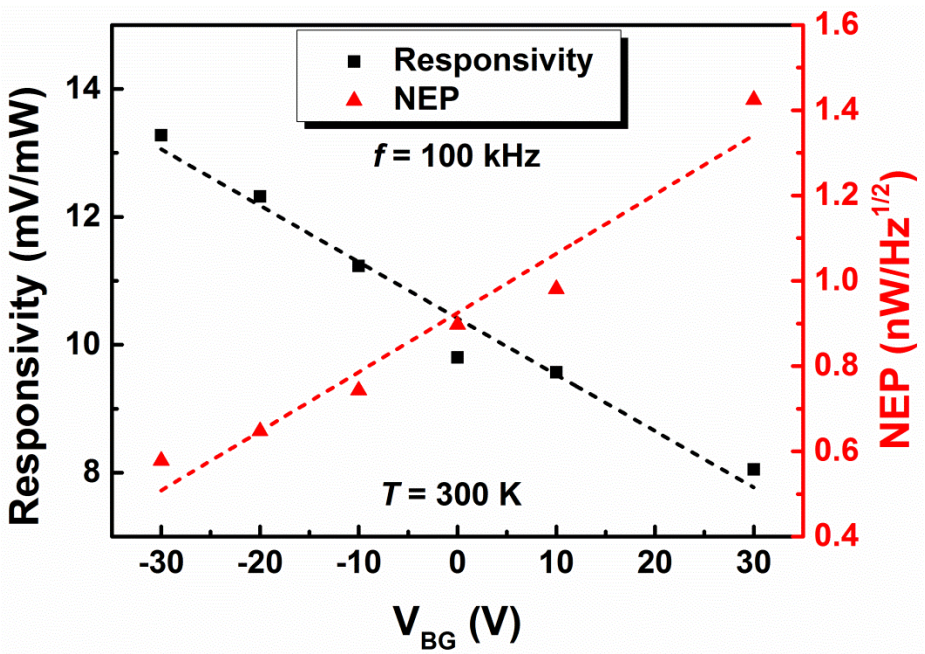

Figure 5.12 The voltage responsivity β_V and noise equivalent power of SSD array as a function of back-gate voltage measured at room temperature. The NEP and β_V increases and decreases, respectively, almost linearly with the increase of back-gate voltage which in turn increases the zero-bias resistance of the array.

The signal-to-noise ratio (SNR) of the array, $\left(\frac{S}{N}\right)_{Array}$ can be evaluated as:

$$\left(\frac{S}{N}\right)_{Array} = \frac{\Delta I}{N} = \frac{M \times \Delta i_s}{\sqrt{M \times n_s^2}} = \sqrt{M} \times \left(\frac{S}{N}\right)_{Single} . \tag{5.24}$$

Here, $(S/N)_{\text{Single}}$ represents the SNR of a single SSD. The SNR of M elements in an array is $\sqrt{M}$ times higher than that of a single SSD. Further optimizations including

the reduction in channel width and increase in number of SSDs, are needed to improve the microwave detection sensitivity, and hence the SNR.

5.6 Conclusions

The first experimental investigation of graphene self-switching devices has been demonstrated in this chapter. The nonlinear *I-V* characteristics have been obtained by simply tailoring a two-dimensional graphene sheet into a one dimensional channel surrounded by the side-gate like electrodes. Graphene is a zero-gap semiconductor; however, the functionality of the SSD does not require any bandgap. The nonlinearity in the *I-V* characteristic of the device was achieved purely due to the side-gate electrodes induced flow of charge carrier in the preferred direction irrespective of the carrier type.

The structure of SSD was conformally mapped onto a rectangular geometry using Schwarz-Christoffel formula to analyse the intrinsic and extrinsic capacitances, caused by the etched trenches around the channel and between two terminals of the device, respectively. The intrinsic capacitance (C_H = 16.17 × 10^{-17} F) estimated from the measured results was found to be an order of lower than that of Si SSD (250 × 10^{-17} F).

The estimated intrinsic voltage responsivity from the nonlinearity of *I-V* characteristic was around 21,840 mV/mW. The observed value of graphene SSD is the highest among all the devices fabricated from different substrates, which have been reported so far. The SSDs array has demonstrated the RF rectification in ambient conditions unlike the graphene *p-n* junctions. Though, the cut-off frequency (~ 1 MHz) was limited by the device impedance at zero-bias and the back-gate associated capacitance due to SiO_2. The NEP at V_{BG} = 0 V was estimated to be of the order of 10^{-9} W/Hz$^{1/2}$, which is comparable to that of uncooled thermal THz detectors.

Based on the nonlinear analysis, a few areas can be suggested to improve the detection sensitivity such as the optimisation of channel width and length and the increase in mobility of graphene. Further, a large number of SSDs in parallel to each other can help in minimising the impedance mismatch with the commercially available RF component, which will improve the voltage responsivity and hence the

noise performance of the device. The deposition of large area graphene on flexible and/or transparent substrates [54] and the use of nanoimprint lithography [55] will allow the fabrication of such large arrays without the need of interconnecting layers.

The intrinsic cut-off frequency of graphene based SSDs can be estimated by calculating the traversal time between the two terminals of the device unlike the conventional *p-n* junction or Schottky diode [56]. Considering the Fermi velocity of charge carriers $v_F = 10^6$ m/s and channel length of SSD $L = 1$ µm, the traversal time between two terminals is $t = L/v_F = 1$ ps, which corresponds to the cut-off frequency of $f = 1/t = 1$ THz. Hence, an intrinsic cut-off frequency greater than 1 THz can easily be achieved by fabricating the device with the same or smaller dimensions from the graphene transferred to an insulating substrate such as boron nitrite (BN), quartz etc., which will reduce the back-gate induced capacitive problems significantly.

The properties of these devices can be determined by the carrier mobilities and the carrier concentrations. The small size of nanochannel can give a rise to number of physical effects influencing its operation. The lateral quantum confinement, Coulomb blockade and the atomic arrangement of carbon atoms at the edges of etched geometry are few to affect the electron conduction in the device channel [57]. The measurements at lower temperatures with or without the magnetic field dependence will allow further investigating these phenomena and their effects on the graphene SSD.

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Chapter 6

Hysteresis of electrical transport in graphene devices

6.1 Introduction

Due to a high carrier mobility [1],[2], saturation velocity [3],[4], and current-carrying capacity [5],[6] graphene is attracting enormous attentions for radio frequency (RF) electronic applications [7]. Recently, a graphene based field-effect transistor (GFET) has been demonstrated with a cut-off frequency of 427 GHz [8]. In RF applications, GFETs do not need a large on/off current ratio as these devices are not supposed to switch-off completely [7]. On the other hand, the carrier mobility is an important measure of the speed of carrier transport in such devices. In most cases, the mobility of graphene is extracted from the slopes of a drain current versus back-gate voltage (I_D-V_{BG}) curve for a GFET. In this method, the influence of chemical reactions and charge trapping cannot be avoided due to the relatively long DC measurements. Hence, the mobility values are underestimated due to the lower carrier concentration inside the channel [9]. Further, the improved mobility is a desirable figure of merit for the design of novel graphene based devices such as the ballistic rectifier and self-switching device (SSD), which have been demonstrated to work at room temperature in Chapters 4 and 5, respectively.

The large surface to volume ratio of graphene allows all of its atoms to be exposed to the surrounding environments [10],[11], the electrical properties are severely

affected by intrinsic and extrinsic parameters such as chemical adsorbates [12], substrate material [13], defect density [14], fabrication methods [15] etc. Consequently, GFETs demonstrate variable electrical transport properties, particularly the carrier mobility. Nevertheless, such a high sensitivity to the surroundings is desirable for sensing applications [16],[17].

Recent field-effect studies of graphene on Si/SiO_2 show a back-gate bias dependent hysteresis in I_D-V_{BG} characteristics [18]-[22]. The hysteresis behaviour in graphene varies depending on the back-gate voltage sweep rate and range [23]-[25]. The observed hysteresis is usually ascribed to the environmental interactions such as impurities on the graphene and/or SiO_2 surface [18],[26], water molecules adsorbed on the graphene [20], and trapping sites at the interface of graphene and SiO_2 [25]-[28]. However, there is no broad consensus about the origin of the hysteresis yet.

Thermal annealing [29] and vacuum treatment [18] are found to be more effective to supress the hysteresis. Other methods including the use of a hydrophobic polymer layer (e.g. hexagonal boron nitrite (hBN), hexamethyledisilzane (HMDS), and parylene) between the graphene and the SiO_2 [30]-[32], siloxane terminated SiO_2 substrate [33], and chemical treatment of the SiO_2 [34] have also been reported to destroy the electric-field induced hysteresis in graphene devices.

To date, the time dependence of charge trapping and/or de-trapping behaviour of GFETs in atmospheric conditions have not been explored in detail. Therefore, in this work a systematic study of the hysteretic characteristics of chemical vapour deposited (CVD) monolayer graphene based field-effect transistors in ambient conditions is presented. A quantitative investigation of the characteristic time constants of charge trapping and/or de-trapping was performed at different back-gate voltages.

Further, it has been demonstrated that nitrogen gas exposure helped highly *p*-doped graphene to return to its ambipolar characteristics with improved charge carrier mobilities. The time constants of charge trapping and de-trapping were increased significantly due to the incorporation of nitrogen atoms into the graphene lattice, which created the structural defects including bonding disorder and vacancies [35]. Finally, ultra-short pulse characterisation was employed to reduce the time constants from tens of seconds to microseconds.

6.2 Device fabrication

The large area monolayer graphene film used in these experiments was grown on a copper (Cu) foil using CVD technique [36]. The Cu foil was heated to 1000 °C with a flow of H_2 at 20 standard cubic centimeters per minute (sccm) with a reactor pressure of 200 mTorr. Then, in order to remove the native oxides and to increase the grain size of Cu, the Cu foil was annealed at 1000 °C for 30 minutes. In the CVD chamber, a mixture of H_2 and CH_4 with flow rates of 20 and 40 sccm, respectively was introduced at the growth temperature of 1000 °C and chamber pressure of 600 mTorr. After the graphene growth, the sample was cooled down rapidly to room temperature with a flow of hydrogen gas. The CVD graphene film was then transferred using wet-etching onto a thermally grown 300 nm thick SiO_2 on Si substrate. Highly doped *p*-type Si substrate was used as a global back gate to tune the Fermi energy of graphene. Details of graphene transfer process can be found elsewhere [36].

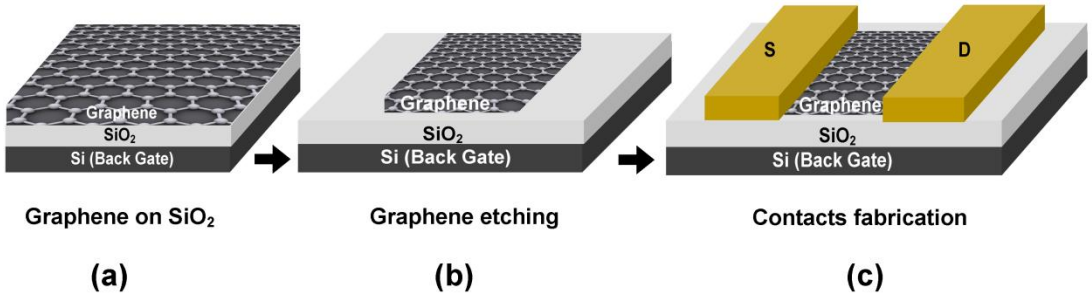

Figure 6.1 Schematic representation of process flow to fabricate a typical GFET. (a) The graphene film was grown on Cu-foil using CVD method and then transferred onto the Si/SiO_2 substrate. (b) The patterns of ohmic contacts on graphene were etched using oxygen plasma. (c) Finally, the electrical contacts of Cr/Au (5/100 nm) were thermally evaporated.

Figure 6.1 illustrates the schematic fabrication flow of the GFETs. Firstly, a positive photoresist S 1805 was used as a mask layer. The undesired graphene was etched away using low power oxygen plasma. Then ohmic contacts were patterned on the graphene with the same resist followed by the thermal evaporation of 5 nm of Cr followed by 100 nm of Au. The lift-off process was then performed in hot acetone to remove the excess gold from the sample. The width *W* and length *L* of the fabricated GFETs were 25 and 37 µm, respectively.

6.3 Results and discussion

6.3.1 Hysteresis of electrical transport

The I_D-V_{BG} characteristics of GFETs were measured using an Agilent parametric analyser E 5270B. Figure 6.2 (a) shows the drain current of GFET measured as a function of back-gate voltage. To bias the device, a constant voltage of 100 mV was applied to the drain of GFET. The field-effect mobility μ of the device was deduced from the I_D-V_{BG} characteristic as [21],[24]:

$$\mu = \frac{L}{C_G W V_D} \frac{dI_D}{dV_{BG}} = g_m \frac{L}{C_G W V_D}, \tag{6.1}$$

where C_G is the effective gate capacitance, V_D is the drain voltage, and $dI_D/dV_{BG} = g_m$ can be calculated from the slope of the transfer characteristics. Fitting Eq. (6.1) with the measured results yielded a mobility for holes of about 257.39 cm^2/V.s in both vacuum and air. Nevertheless, the mobility for electrons was estimated to be around 64.35 cm^2/V.s in air. The field-induced charge density n in a GFET can be obtained from [20]:

$$n = \frac{C_G (V_{BG} - V_{DP})}{e}, \tag{6.2}$$

where e is the carrier charge and V_{DP} is the back-gate voltage corresponding to the minimum conductivity, and it is commonly known as neutrality or Dirac point. In pristine graphene, the neutrality point is usually found at V_{BG} = 0 V. However, in these devices the neutrality point was observed at V_{BG} = 70 V. The high value of neutrality point was attributed to an unintentional *p*-type doping caused by the electron charge trapping of graphene by H_2O/O_2 molecules [37]-[39], SiO_2 dielectric layer [19], photoresist residues or other contaminations [40] etc.

The *p*-doping of GFETs was not fully reversed upon degassing in vacuum at room temperature over a period of time as shown in Fig. 6.2 (a). When the back-gate voltage was swept continuously from -80 to 0 V, then to +80 V, and back to -80 V at the room temperature, a hysteresis in the I_D-V_{BG} characteristics was observed

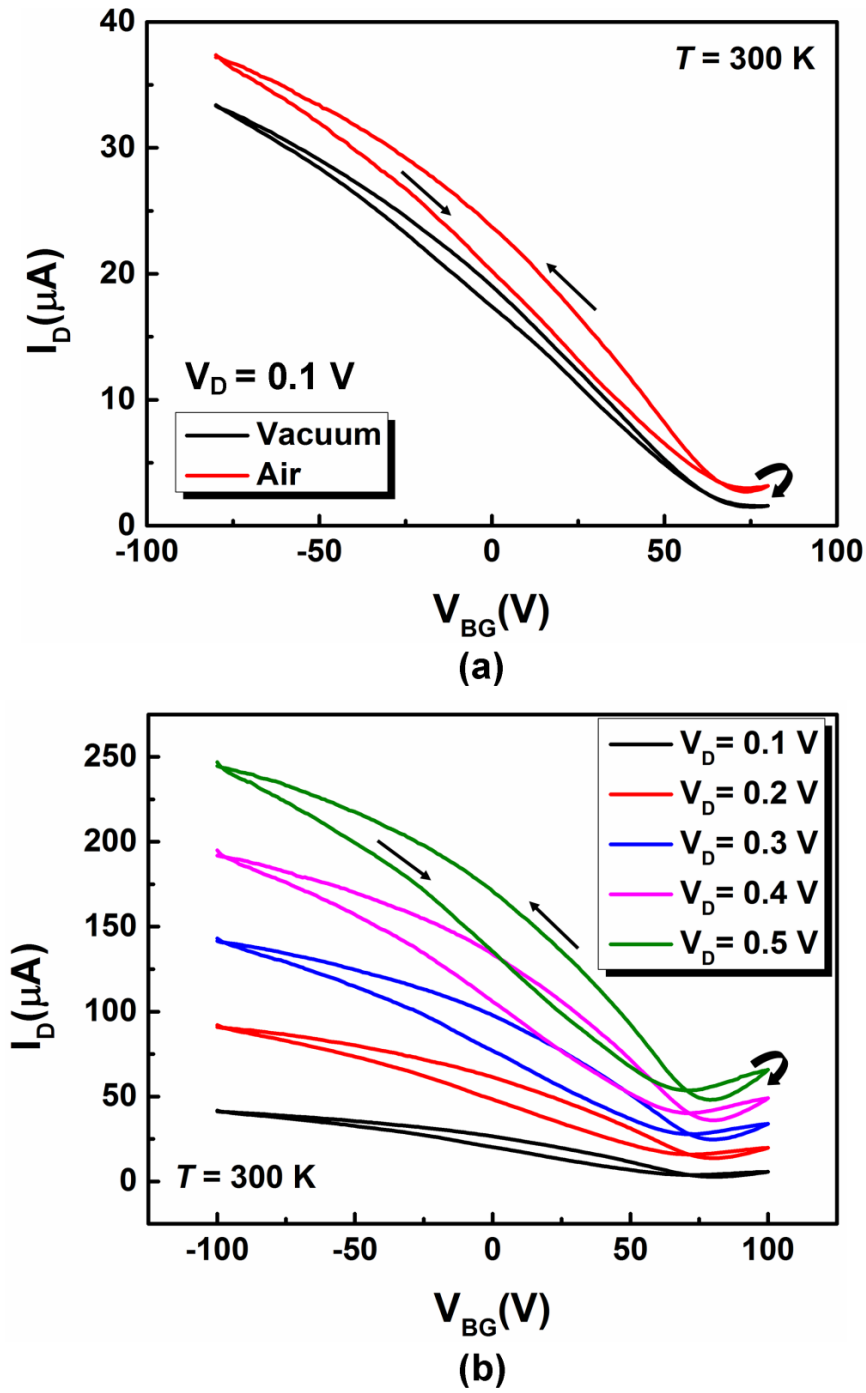

Figure 6.2 (a) Room temperature I_D-V_{BG} characteristics of GFET in air (red line) and vacuum (black line). The I_D in vacuum was slightly reduced from the air due to the removal of loosely bound adsorbates from graphene surface. However, there was no significant difference in hysteresis under both conditions. The hysteresis became bigger with the increase in drain bias voltage (b).

as shown in Fig. 6.2 (a). The similar hysteresis behavior has been observed in carbon nanotubes (CNTs) fabricated on Si /SiO_2 substrates [41],[42]. This phenomenon in these materials was ascribed to dipolar adsorbates such as water and oxygen.

In an atmospheric environment, surface bound water and oxygen molecules upset the carrier concentration in graphene due a electrochemical redox process [43],[44]:

$$O_2+2H_2O+4e \leftrightarrow 4OH^-. \tag{6.3}$$

The negative charges of hydroxyl bonds (OH^-) might induce positive charges by trapping the free electrons from graphene. This results in a pronounced *p*-type behavior and moves the neutrality point towards the positive bias [43].

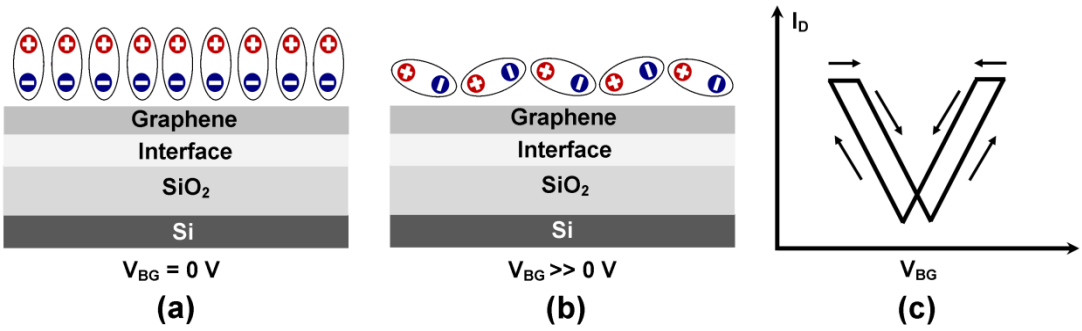

Figure 6.3 Illustration of the polarization of water induced adsorbed molecule dipoles on the surface of graphene at $V_{BG} = 0$ V which leaves *p*-type doped graphene (a). When the back-gate voltage is increased beyond a certain value in (b) the polarization gets disturbed and normalizes only when voltage is swept back to negative values. As a result, device exhibits a positive hysteresis (c).

The water molecules behave like a dipole [25] and are oriented by their negative charges towards the graphene layer at zero back-gate voltage as shown in Fig. 6.3 (a). The induced electric field due to the polarization of dipoles opposes the back-gate voltage up to a certain value of positive voltage. The higher positive back-gate voltage destroys the polarization and the induced electric field becomes zero as illustrated in Fig. 6.3 (b). If the voltage is changed rapidly, the polarization does not get time to restore until the voltage reaches to zero [45]. A further increase in negative back-gate voltage restores the polarization and gives rise to a clockwise hysteresis as shown in Fig. 6.3 (c). Thus, a back-gate voltage sweep in the negative regime typically shifts the neutrality point towards negative back-gate voltages due to charge screening from the trapped electrons of graphene in the adsorbed water molecules [19].

From the measured results, a clockwise hysteresis on the electron conduction side and counter-clockwise hysteresis on the hole conduction side was observed. When devices were measured in a vacuum, the observed hysteresis in Fig. 6.2 (a) remained

almost the same as in air. Hence, it can be argued that the observed hysteresis was not attributed to the water and oxygen molecules on the graphene surface as described above.

It was presumed that the observed hysteresis from CVD-grown GFETs may be attributed to charge trapping at the interface of graphene and substrate [19],[25]. As shown in Fig. 6.4 (a) when a back-gate voltage sweep is started at negative bias, the holes from the graphene started to trap into the trapping sites at the interface of the graphene and SiO_2. Therefore, after sometime the graphene experienced a lower negative gate potential due to the charge screening from trapped holes. Similarly, electrons started to trap into the trapping sites for the regime of positive back-gate voltage sweep as shown in Fig. 6.4 (b). This trapping of electrons gave rise to a clockwise hysteresis. However, the negative back-gate voltage sweep gave rise to a counterclockwise hysteresis due to the trapping of holes as illustrated in Fig. 6.4 (c).

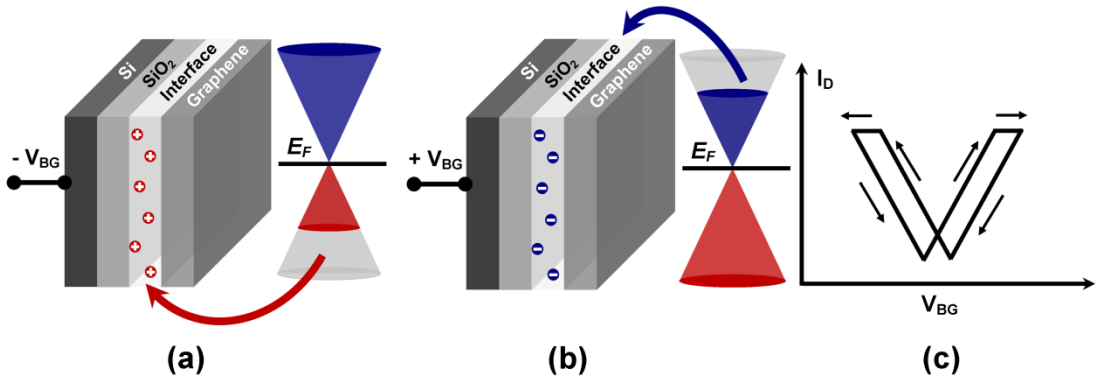

Figure 6.4 Trapping sites at the interface of graphene and SiO_2 play a dominant role in reverse hysteresis mechanism (c). When V_{BG} was negative (a) or positive (b), holes or electrons were injected into the trapping sites, respectively, and gave a rise to the observed hysteresis.

The back-gate voltage sweep shifted the neutrality point of GFETs towards the positive back-gate voltages as observed in Figs. 6.2 (a) and (b). From the measured results, it was confirmed that the charge trapping at the interface of graphene and SiO_2 was the dominant mechanism for observed hysteresis in a vacuum and in air. Furthermore, the hysteresis became larger as the range of V_{BG} or the drain bias voltage was increased as shown in Fig. 6.2 (b).

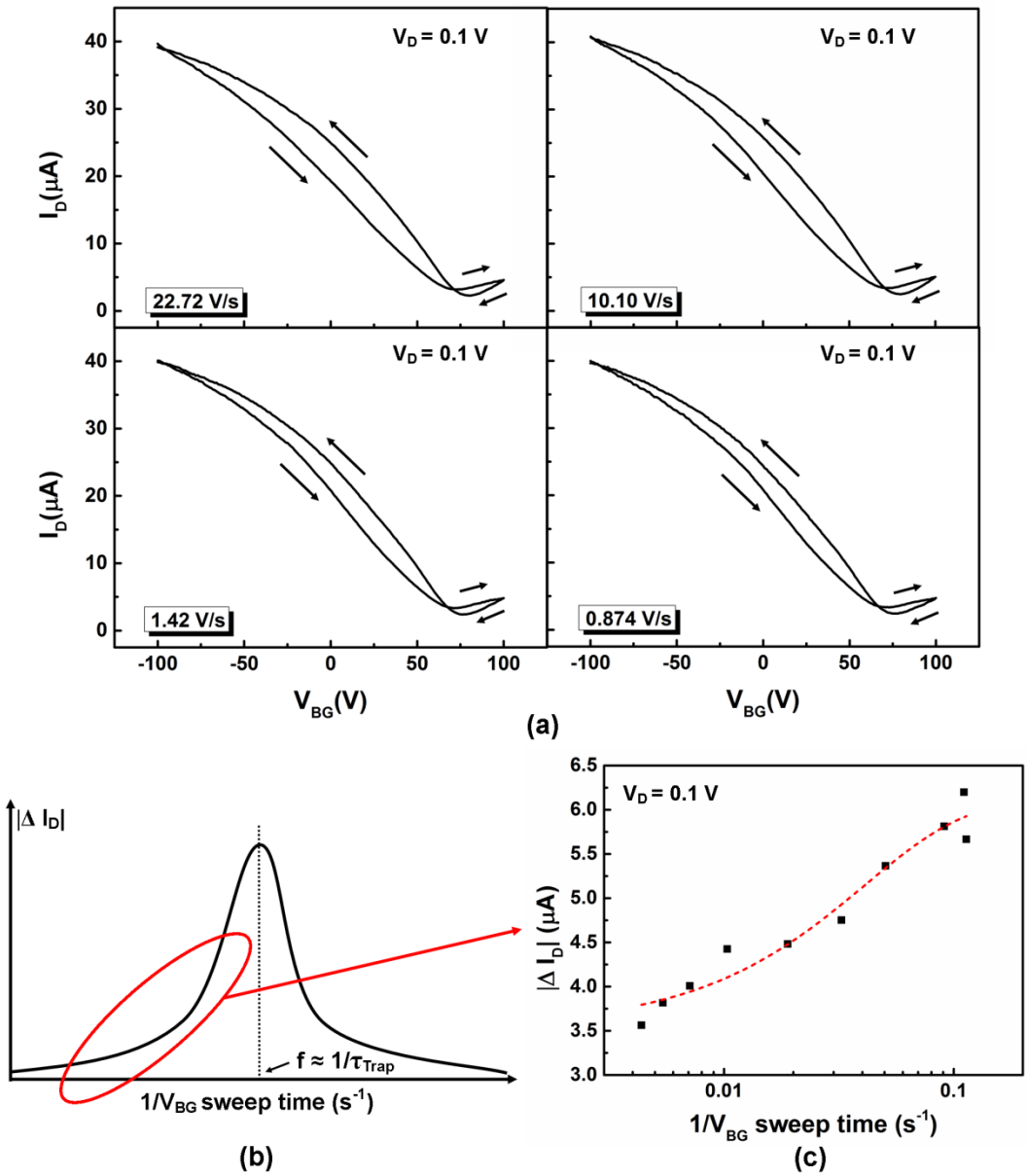

Figure 6.5 (a) The back-gate voltage sweep rate change from 0.874 V/s to 22.72 V/s increased the transconductance hysteresis ΔI_D measured at V_{BG} = 0 V (c). The hysteresis will increase with the increase in sweep rate until the frequency of trapping is equal to the inverse of trapping time constant (b).

Figure 6.5 (a) shows the dependence of hysteresis on the back-gate voltage sweeping rate dV_{BG}/dt. The transconductance hysteresis ΔI_D at V_{BG} = 0 V between forward and reverse sweep was increased with the increase of sweeping rate from 0.874 to 22.72 V/s as shown in Figs. 6.5 (a) and (c).

During the back-gate voltage sweep, the charge traps would be charged or discharged on the time scales comparable to the measurement time. Thus, the device hysteresis would depend on the charge trapping on a time scale. Considering that if

dV_{BG}/dt was much faster or slower than the charge trapping or de-trapping time, the hysteresis might not be expected in the I_D-V_{BG} characteristics. Further, the device hysteresis would almost saturate at the smallest or highest voltage sweeping rates. The maximum hysteresis would only occur when the inverse of V_{BG} sweep time is equal to the inverse of time constant for charge trapping as shown in Fig. 6.5 (b). The maximum time constant for trapping of charge carriers in the trapping sites at the interface of graphene and SiO_2 was estimated to be around 49.81 s, by fitting the measured results in Fig. 6.5 (c). to Eq. (6.5). The total amount of trapped charges can be estimated by the neutrality point shift using [25]:

$$N_{Trap} = \frac{C_G \Delta V_{Dirac}}{2e} \tag{6.4}$$

The calculated value of the trapped charge density using Eq. (6.4) at the interface of the graphene and SiO_2, varied from 1.44×10^{11} to 2.88×10^{11} cm^{-2} for the V_{BG} sweep rate from 0.874 to 22.72 V/s, respectively. These values were found to be in the same order of magnitude as the oxide trap densities, i.e., about 5×10^{11} cm^{-2} [46].

Nitrogen gas exposure

The simplest method to control the semiconducting properties of graphene is the chemical doping by gas exposure [18]. The GFETs were exposed to nitrogen (N_2) gas in a Linkam annealer with a TP 94 temperature control unit as shown in Fig. 6.6. The TP 94 temperature controller is capable of annealing up to 350 °C with a temperature accuracy and stability of 1 °C. Two types of annealing test were performed. The first one was the temperature dependence measurement in which different annealing temperatures, varying from 100-300 °C, were applied to the device in N_2. The second experiment was the time dependence measurement in which annealing time was increased from 30 minutes to 2 hr. at a temperature of 200 °C.

The exposure to N_2 gas manipulated the doping profile of the graphene devices [47]-[49]. The N_2 acted as an *n*-type dopant and shifted the neutrality point towards the negative back-gate voltages as shown in Figs. 6.7 (b) and (c). The I_D-V_{BG} characteristic exhibited the ambipolar transistor effect around the neutrality point. When the back-gate voltage was smaller than the neutrality point, the GFET

operated as a *p*-channel FET and for higher back-gate voltages the device operated as an *n*-channel FET [50].

Figure 6.6 Linkam annealer with TP 94 temperature control unit used to anneal GFET in N_2.

The incorporation of nitrogen atoms in the graphene lattice formed a covalent bond and further modified the electronic properties of the sp^2 bonded carbon atoms locally. A nitrogen atom in the graphene lattice has three common bonding configurations including graphitic (substitutional), pyridinic and pyrrolic N [35]. In the graphitic configuration, N atoms form bonds with three sp^2 hybridized carbon neighbours and the excess delocalized valence electrons lead to *n*-type doping of the graphene. However, in pyridinic or pyrrolic N configuration, N atom bonds have two neighbour sp^2 hybridized carbon atoms and result in *p*-type behaviour. The latter two bonding configurations demonstrate structural disorder and localize the transport of the charge carriers [51],[52]. Similar studies on carbon nanotubes have demonstrated that such N-doping configurations can provide *p*-type and *n*-type conductivity in a channel depending upon the doping process [53].

The observed field-effect mobilities for holes and electrons improved significantly to 386.09 and 257.39 $cm^2/V.s$, respectively after the N_2 exposure. This was due to the *p*-type and *n*-type doping caused by pyridinic or pyrrolic N and graphitic bonding, respectively. However, the conductance of graphene after exposure was found lower than the unexposed GFETs. This might be attributed to the doped N atoms which can create excess defects in the graphene channel. Further, the increase in ΔV_{DP}, as

shown in Fig. 6.7 (d), was due to the co-existence of electron-hole puddles and localization of charge carriers in the disordered graphene [35],[51],[52].

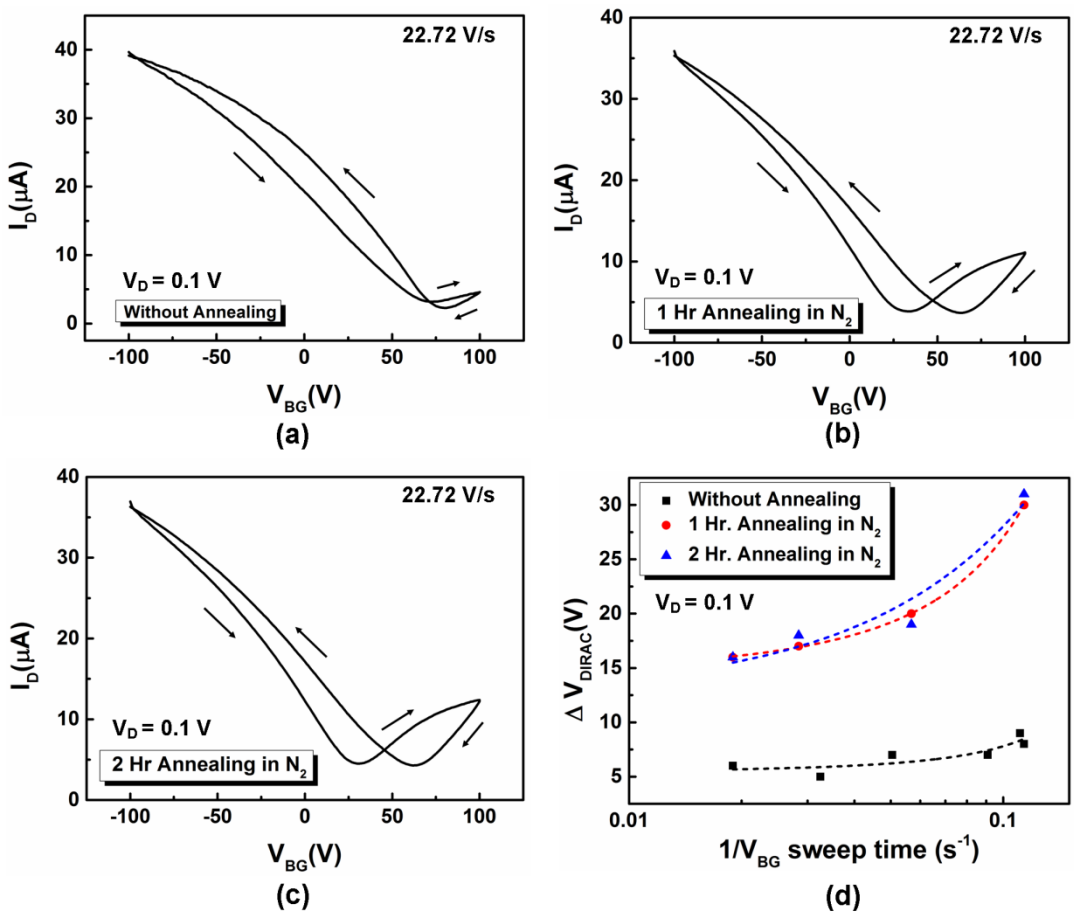

Figure 6.7 (a) The room temperature transfer characteristics of the GFET, measured at dV_{BG}/dt = 22.72 V/s in air, showed a *p*-type characteristics. The estimated field-effect mobility for holes was approximately 257.39 cm^2/V.s. The annealing in nitrogen gas doped the graphene *n*-type, as a result device exhibited ambipolar characteristics around the neutrality point (b) and (c). The estimated field-effect mobility for holes and electrons after 2 hr. annealing was approximately 386.09 and 257.39 cm^2/V.s, respectively. It suggests that both the electrons and holes conduction in the device was improved due to the graphitic and pyridinic or pyrrolic N doping, respectively. The defects incorporated by the nitrogen doping were responsible for the neutrality point shift ΔV_{DP} (d). ΔV_{DP} increased exponentially with the increase in sweep rate as suggested in Fig. 6.5 (b).

6.3.2 Time-domain response

The characteristic time constant of the charge trapping and/or de-trapping to or from the defective or trapping sites can be estimated from the temporal behaviour of the drain current at the various back-gate voltages. To understand the trapping and /or de-trapping mechanism, I_D was measured at different back-gate voltages in air.

Initially, the back-gate voltage was kept at 0 V for about 200 s and then a DC voltage pulse (positive or negative) was applied for 150 s to the back gate of the device. The temporal I_D was measured as a function of elapsed time t while keeping drain voltage V_D fixed at 100 mV. A LabView programme was designed to perform the above task and the measurements were performed using Agilent parametric analyser E 5270B.

Figure 6.8 (a) shows the time response of I_D at a negative back-gate voltage of -20 V. When the V_{BG} was changed from 0 V to -20 V, there was a reduction in the time-dependent current due to the trapping of holes at the interface of graphene and SiO_2. The current reduction was rapid at the beginning but later saturated to a stable value. When the applied voltage (or stress) was removed from the back gate, the current immediately tried to recover back exponentially to its original value with respect to measurement time. This phenomenon was attributed to the de-trapping of holes from the trapping sites [19],[25].

The electron trapping or de-trapping at positive back-gate voltages was analogous to the holes under negative gate voltages. In these devices the neutrality point was far away to the right of V_{BG} = 0 V, hence the holes were de-trapped and trapped during and after the applied back-gate voltage pulse of 20 V, respectively, as shown in Fig. 6.8 (b).

The exponential behaviour of I_D with respect to time was fitted to:

$$I_D(t) = B\left[1 - \exp\left(-\frac{t}{\tau}\right)\right] + I_D(0), \tag{6.5}$$

where B is a proportionality constant, τ is the characteristic time constant for the initial transient behavior of charge trapping and de-trapping, and $I_D(0)$ is the initial value of current at t = 0 s.

Figures 6.8 (c) to (f) show the relaxation of drain currents during and after the applied back-gate pulses at different voltage amplitudes. The measurements with longer pulses had shown almost same characteristics. The back-gate voltage dependence of trapping time constant $\tau_{Trapping}$ estimated using Eq. (6.5) during and after the applied pulse is shown in Fig. 6.9 (a). The $\tau_{Trapping}$ was varied from 21.5 to 49.14 s for back-gate voltages in the range from -100 to 100 V. They are quite comparable to the estimated value of time constant for trapping, i.e., 49.81 s,

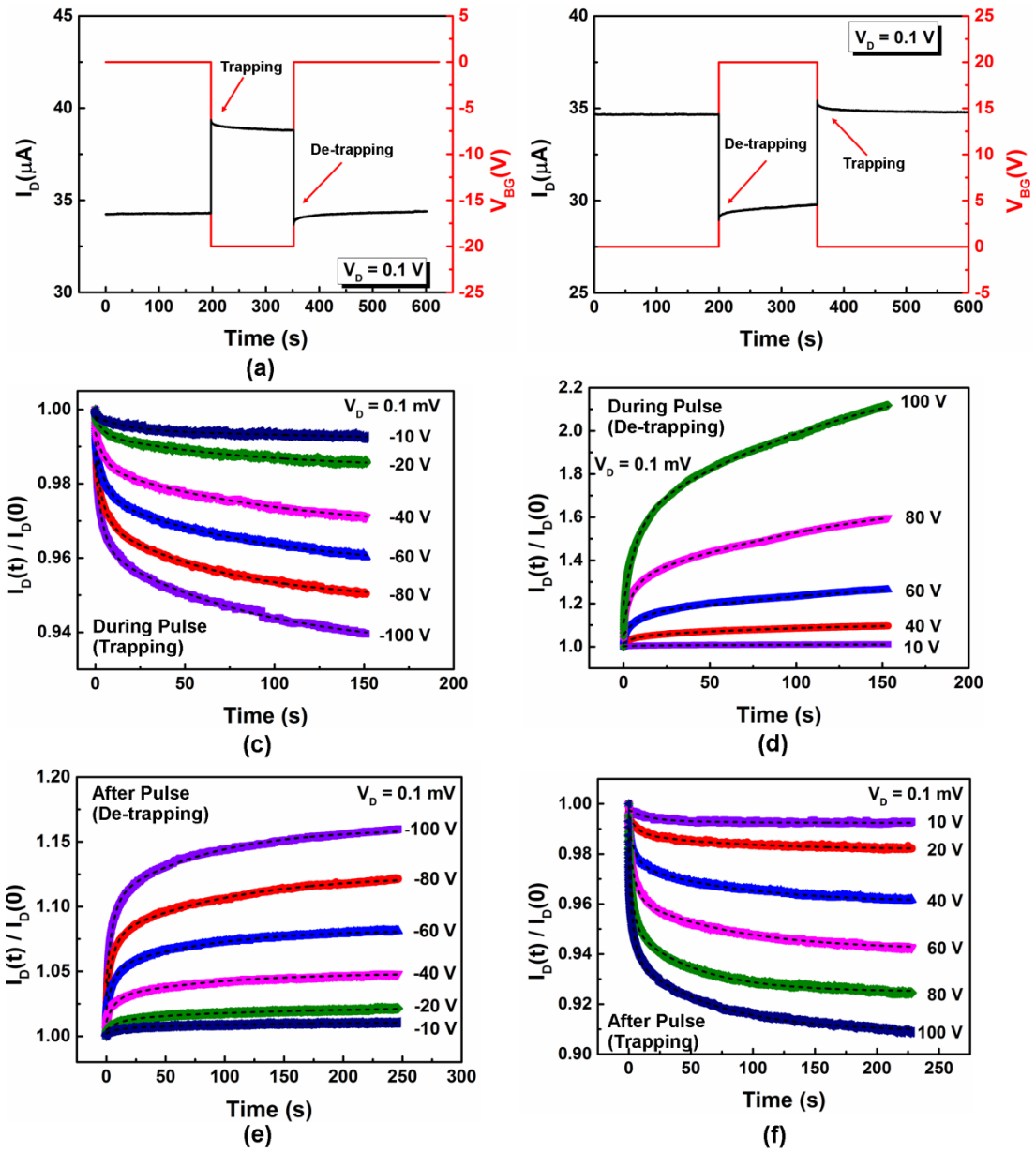

Figure 6.8 (a) Drain current of the GFET as a function of measurement time at a fixed drain voltage of 0.1 V. A DC pulse of -20 V (a) and 20 V (b) was applied at the back gate of the device. When V_{BG} changed from 0 V to (a) -20 V or (b) 20 V, the current rapidly decreased or increased initially indicating the trapping or de-trapping, respectively. After the removal of the voltage, the drain current recovered back by a de-trapping or trapping mechanism in (a) and (b), respectively. (c)-(f) the relaxation of the current during and after the applied back-gate DC pulse at different voltages. The time constants for trapping and de-trapping of charge carriers were estimated by fitting the measured data to $I_D(t) = B[1\text{-}\exp(-t/\tau)] + I_D(0)$ as shown by the dashed lines. The measurements were performed at the room temperature in an atmospheric environment.

obtained from the previous experiment in which V_{BG} sweep rate was changed from 0.874 to 22.72 V/s as shown in Fig. 6.5. The de-trapping time constant $\tau_{De-trapping}$ in Fig. 6.9 (b) for the above voltage range was higher than $\tau_{Trapping}$ and varied from 45.9 to 79.80 s. Therefore, it was concluded that the charge carriers take more time to de-trap from the trapping site than trapping.

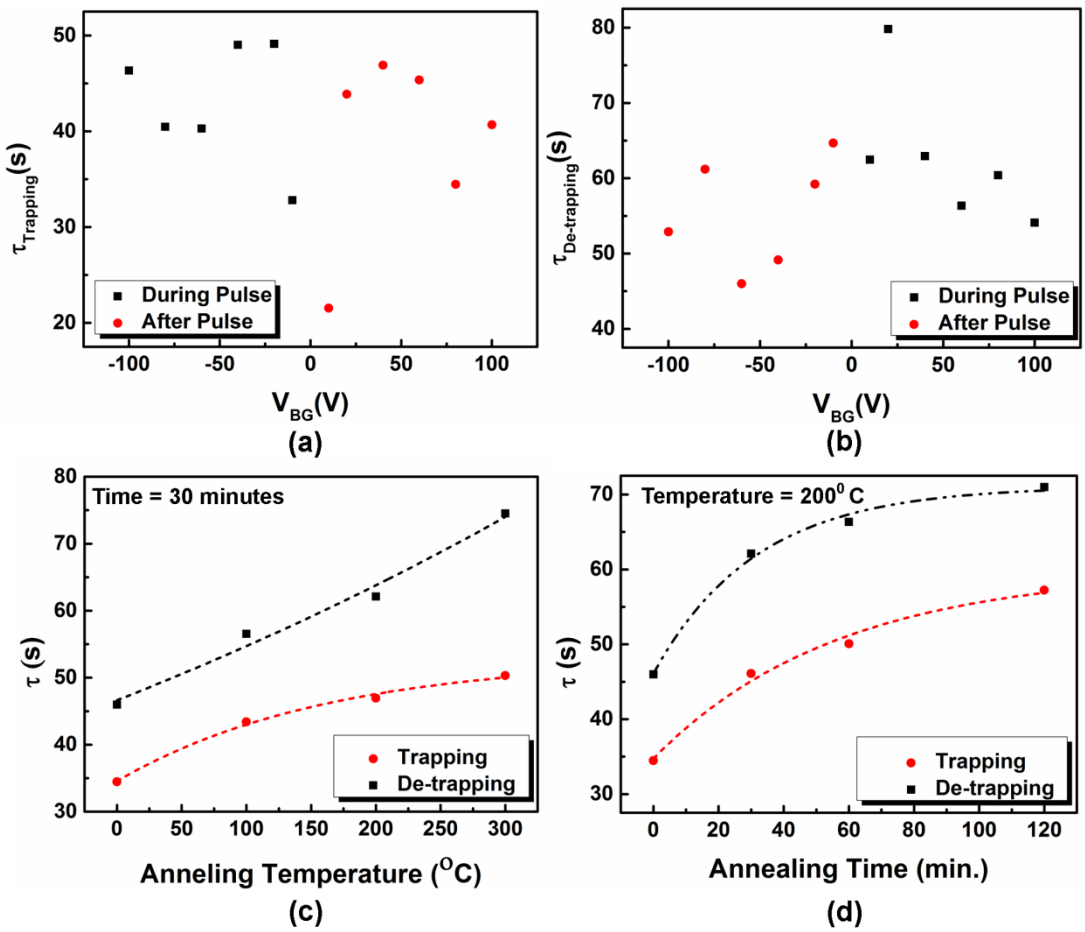

Figure 6.9 (a) The trapping time constant of carriers with respect to applied back-gate voltage during and after the negative and positive back-gate pulse, respectively. (b) De-trapping time constant was larger than the trapping time in (a). The estimated time constant for trapping and de-trapping at the back-gate voltage of 80 V and -60 V, respectively at different (c) annealing temperatures for 30 minutes, and (d) annealing time at 200 °C. The time constant increased exponentially after the annealing possibly due to the increase of nitrogen introduced defects in graphene.

The obtained values of time constants at different V_{BG} suggest that they did not depend significantly on the different signs of applied voltage, which meaning that the charges were trapped at the interface of graphene and SiO_2. The time constant for trapping and de-trapping increased exponentially with the increase in annealing temperature and annealing time, as shown in Figs. 6.9 (c) and (d), respectively. The

increase in time constants after annealing in N_2 was most likely due to the increase in structural disorder e.g. vacancies in bonding configurations etc. in the graphene [51],[52]. From these results, time constants for trapping and de-trapping after nitrogen annealing were found to increase about 55 % when compared to the devices without annealing as shown in Figs. 6.9 (c) and (d).

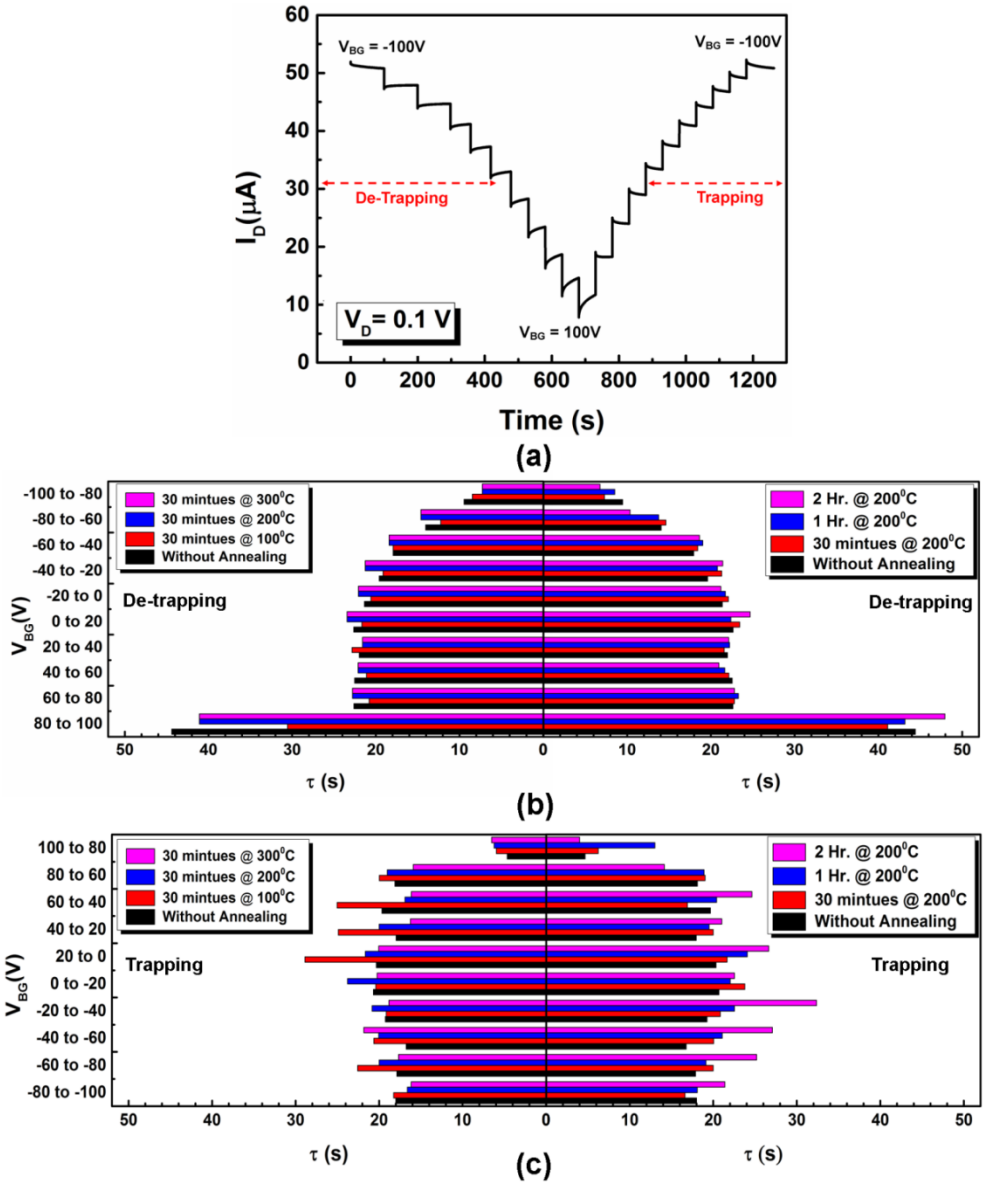

Figure 6.10 (a) I_D response against time for a continuous back-gate voltage sweep from 0 to -100 V, then to 100 V, and back to -100 V. The voltage was changed in steps of 20 V and each voltage was continuously applied to the gate for 50 s. The step like de-trapping and trapping mechanism was observed when the gate was changed from negative to positive and positive to negative, respectively. (b) The estimated de-trapping time constant for different annealing conditions for a back-gate voltage sweep from -100 to 100 V. Trapping time constant in (c) was slightly smaller than that of de-trapping (c) for the same annealing conditions. All the measurements were performed at air ambient.

To further analyse the effect of continuous back-gate voltage change on the trapping or de-trapping mechanism, V_{BG} was varied continuously from 0 to -100 V, then to +100 V and back to -100 V at room temperature in atmospheric environment. The back-gate voltage was swept in steps of 20 V and each voltage was applied for 50 s to the back gate of the device. The time-domain response of the drain current was measured same as before. When the V_{BG} was changed from 0 V to -100 V, initially current started decreasing due to the trapping of holes and later increased at each voltage step until V_{BG} was changed to 100 V, as shown in Fig. 6.10 (a).

The results suggested that I_D always increased when the back-gate voltage changed from more negative to positive values due to the de-trapping of holes or trapping of electrons. Similarly, the trapping of holes or de-trapping of electrons always decreased I_D with the change of V_{BG} from more positive to negative values, as shown in Fig. 6.10 (a). Figures 6.10 (b) and (c) show the estimated time constants for de-trapping and trapping in air with and without annealing in N_2. As observed earlier, $\tau_{Trapping}$ was smaller than $\tau_{De-trapping}$ and these values were higher for the devices exposed to N_2. It is evident from the results that the observed time constants for trapping and de-trapping was smaller to that obtained in Figs. 6.9 (a) and (b). This is due to the fact that in these experiments each step of V_{BG} to the back gate was applied only for the duration of 50 s instead of 150 s. As a result, the number of charge carriers trapped into the defective sites was smaller than that of earlier experiments.

6.3.3 Short pulse characterisation

The DC measurements performed above with different back-gate sweeping rates were not enough to suppress the origin of hysteresis [22],[44]. The time-domain hysteresis of I_D as a function of V_{BG} looked quantitatively similar to those measured at different back-gate voltage sweeping speeds and ranges. Further, it was not easy to estimate the fast transient performance of the device due to long measurement times. It might be expected from the proposed assumption in Fig. 6.5 (b) that the hysteresis can be reduced to almost zero by employing an ultra-fast back-gate voltage sweep rate since the charge carriers will not get the time to trap into the defective sites. Klarskov et.al [54] have demonstrated that despite of having a high voltage sweep rate of ~240 V/s, the hysteresis was observed in vacuum. Therefore, in order to

completely reduce the effect of hysteresis, a highly efficient, fast measurement technique such as short pulse characterisation may be employed [55].

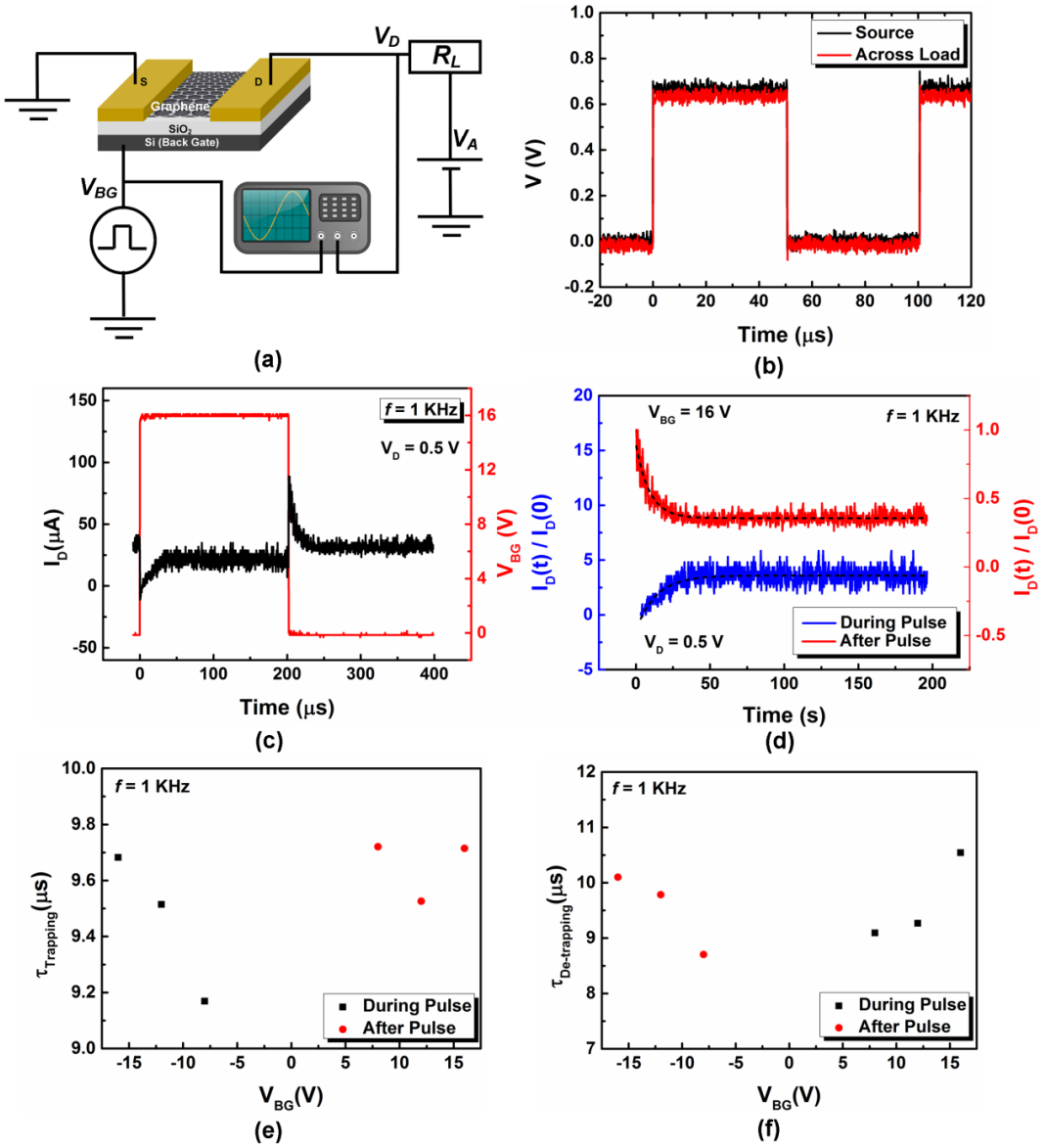

Figure 6.11 (a) The schematic illustration of setup used for the short pulse characterisation technique. The pulse and device response was measured simultaneously using an oscilloscope. (b) Measured voltage response across the source and load resistor suggests no charging or discharging like contribution from the setup. (c) The device response and the back-gate pulse of 16 V generated from an HP 8116A. The pulse signal was generated at a frequency of 1 kHz, and the drain bias to the device was fixed to 0.5 V. The device current response with respect to elapsed time shows the same behavior for de-trapping and trapping as observed in Fig. 6.8 (b). (d) The measured results were fitted to Eq. (6.5), as shown by dashed lines, to estimate the trapping and de-trapping time constants. The time constants for trapping (e) and de-trapping (f) at different back-gate voltages. These time constants were most likely attributed to the filling of the shallow traps rather than the deep trapping of the charge carriers at the interface of graphene and SiO_2. All the measurements were performed in an atmospheric environment.

A short pulse I_D-V_{BG} characterisation technique was used to measure the transfer characteristic with much faster speed than the conventional DC measurement. This technique is commonly used for the characterisation of high-κ dielectric materials [56]-[58]. In this technique, a rectangular V_{BG} pulse generated by a pulse signal generator was applied to the back gate of the transistor, configured as an inverter. The drain voltage V_D at the GFET was measured by a digital oscilloscope during and after the applied pulse.

The schematic diagram of the pulse measurement setup is shown in Fig. 6.11 (a). A pulse source HP 8116A was used to generate a short pulse at 1 kHz with a rise and fall time of ~5 ns. A fixed DC bias V_A of 0.5 V was applied to the drain terminal of the GFET through a load resistance R_L by a Keithley 2400 voltage source, while keeping the source terminal at ground. A resistance of 5 kΩ, almost equal to the device impedance, was chosen as a load. The drain voltage was observed simultaneously to the applied back-gate voltage pulse by the oscilloscope. In order to find out the time constant of experiential setup, a rectangular pulse was applied to R_L without connecting device in between the pulse source and R_L. The resultant response across R_L was measured simultaneously with the applied pulse using an oscilloscope. The measured results, as shown in Fig. 6.11 (b), demonstrate that there was no contribution to the time constant of charging or discharging effect due to the setup when no device was connected.

The drain current, normalised to applied DC bias, can be calculated as [55],[59]:

$$I_D = \frac{V_A}{V_D}\left(\frac{V_A - V_D}{R_L}\right). \tag{6.6}$$

The measured I_D and applied V_{BG} pulse as a function of time is shown in Fig. 6.11 (c). The observed response was similar to that of a DC pulse measurement in Fig. 6.8 (b). The reduction in drain current was too rapid in the beginning due to the initial fast charge trapping. However, the drain current was saturated within tens of microseconds. The back-gate voltage pulses only up to 16 V were applied to the device, which was the maximum output of the pulse generator.

The measured results were fitted to Eq. (6.5), as shown by dashed lines in Fig. 6.11 (d), to estimate the time constants for trapping and de-trapping during and after V_{BG}

pulse. The obtained value of time constants for trapping (from 9.16 to 9.72 μs) and de-trapping (from 8.7 to 10.54 μs) were almost two order higher than that of the device RC time constant (~0.10 μs) which was estimated form the device resistance (~4 kΩ) and the intrinsic gate capacitance (2.65×10^{-11} F). It further ruled out the possibility of obtaining the observed time constants due to the device RC charging effect. The shorter time constants for trapping and de-trapping as shown in Figs. 6.11 (e) and (f), respectively, were most likely due to the trapping and de-trapping of the charge carriers into and from the shallow traps at the interface of graphene and SiO_2, respectively. The mechanism related to slow and deep trapping and de-trapping was absolutely supressed in the measured results due to the fast duty cycle of the applied back-gate voltage pulse. The observed values of time constants were consistent with the reported values for charge carrier trapping at the interface of graphene and SiO_2 obtained by employing short pulsed characterisation [60].

6.4 Conclusions

A systematic experimental investigation performed on GFET devices is reported in this chapter. The devices exhibited *p*-type doped characteristics behaviour due to the water and oxygen redox reaction process which traps the free electron from the surface of graphene in vacuum as well as in air. The water molecules on graphene surface behave like a dipole and contribute to the gate induced hysteresis effect. Such hysteresis can be removed by degassing the samples in a vacuum for over a time period. But the measured results demonstrate that it was not the case in these devices, hence it was considered that the observed hysteresis in characteristics might be due to some other reasons.

The charge carrier trapping at the interface of graphene and SiO_2 was identified as a dominating mechanism for the origin of hysteresis in these devices at room temperature in ambient conditions and in a vacuum. A clockwise hysteresis was observed when electrons were the majority carriers while a counter clockwise hysteresis was found in the case of holes as majority carriers. The amount of hysteresis was changed by varying the back-gate voltage sweep rate. It has been proposed that if the rate of voltage change is very small or very high on the time scales of trapping or de-trapping, the hysteresis can be reduced to zero. Interestingly, the time constants did not change too much for different signs of applied voltage

pulses. This suggests that the effective voltage built by charge trapping sites was not dependent on the charge polarity of adsorbates; hence the trapping was occurred only at trapping centres or defective sites available at the interface of graphene and SiO_2.

The GFETs were chemically doped using N_2 gas, which introduced pronounced *n*-type carrier concentration into the channel. As a result, the device exhibited ambipolar characteristics. On the other hand, the nitrogen atom incorporation in graphene, due to pyridinic or pyrrolic N bonding, substitutes to the structural defects including the bonding defects and vacancies. From the experimental results it was found that the time constants of trapping and de-trapping were increased about 55% to that of un-annealed GFET, which might be due to the increase in structural defects on the graphene surface.

The trapping at the interface was significantly reduced by employing short pulse characterisation technique. The trapping and de-trapping of the charge carriers into shallow traps were the only plausible mechanism responsible for the obtained time constants of order tens of μs. Improved fabrication and cleaning processes for graphene and substrate can lessen the hysteresis problems that arose due to the defects at the interface. Other techniques including passivation of substrate surface and introducing a hydrophobic layer at the interface of graphene and SiO_2 may also be employed as an effective solution to get rid of the charge carrier trapping and de-trapping mechanism.

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Chapter 7

Summary and outlook

7.1 Summary

This research was mainly focused on the advancement of two novel nonlinear planar devices, i.e., ballistic rectifier and self-switching device. Both devices have demonstrated the signal rectification without any need of intrinsic threshold or turn-on voltage at room temperature. This has been achieved due to their unique working principles, which do not rely on *p-n* junction or Schottky barrier along the direction of current conduction unlike conventional rectifiers. These devices have demonstrated an intrinsically low parasitic capacitance, due to the planar nature of their structure, i.e., the contacts are in the same layer as the device active region. In fact, this is the most alluring property of them, which has enabled signal rectification at higher speed than that of a conventional vertical, multi-layered diode of same size. Conventional III-V semiconductor and graphene were used for the fabrication of these devices. Single-layered architecture of both devices has enabled the utilisation of graphene as the active layer. In this work, both mechanical exfoliation and chemical vapour deposition techniques were employed to produce monolayer graphene.

Nonlinear ballistic transport in graphene based ballistic rectifiers with different geometries, i.e., with and without triangular anti-dot scatterer at the centre of nanoscale cross junction, has been investigated at room temperature. These devices

were fabricated from graphene on a thermally grown SiO_2 on *p*-type doped Si substrate, which was used as a back gate. Devices exhibited steering of charge carriers in a predefined output channel independent of input current direction. An intrinsic zero threshold voltage has been achieved in their voltage-current characteristics. Observed ballistic rectification effect was well defined using an extended Landauer-Büttiker formula, based on the scattering approach. As expected, the positive sign of output voltage was observed for *p*-type charge carriers. Negative output voltage and parabolic curve for *n*-type transport were achieved by biasing the back gate.

Graphene SSD realised by tailoring two L-shaped trenches have exhibited a diode-like current-voltage (*I-V*) characteristic without the need for sizable bandgap. The experimental results show a clear nonlinear behaviour around the zero bias. The microwave rectification theory based on the nonlinear *I-V* characteristic was used to thoroughly analyse the measured results. The estimated intrinsic voltage responsivity (detection sensitivity) of device, determined from the bending of the *I-V* characteristic, was found to be 21,840 mV/mW. This result is much better than that previously achieved from the devices fabricated out of III-V semiconductors (up to 19,000 and 9,600 mV/mW in GaAs and InGaAs, respectively). The truly planar layout of the SSD has allowed building structure of an array with several devices connected in parallel in a single lithography step. Interconnection layer which may introduce the parasitic elements was not required. This further made the whole fabrication process simpler and faster. The large number of devices together reduced the resistance of the device, and hence improved the noise performance without affecting sensitivity.

In contrast to other graphene devices, ballistic rectifiers and SSDs have demonstrated a stable frequency response, square-law operation and zero-bias detection at room temperature. On a SiO_2 substrate, the maximum cut-off frequency was impeded by the large gate capacitance. However, it was estimated that the cut-off frequency would be in THz range, if the devices are fabricated from graphene on insulating substrate such as hexagonal boron nitrite (hBN), quartz etc.

In addition, CVD-grown monolayer graphene based devices were then thoroughly investigated in ambient conditions to develop the understanding of hysteresis in their

drain current and back-gate voltage characteristics. The observed hysteresis was strongly dependent on the back-gate voltage sweep rate and range, suggesting the relaxation of charging and discharging effect in the devices. Time-domain current-voltage measurements indicated the charge trapping and de-trapping characteristics with almost same value of time constants irrespective of the applied voltage. Charge transfer from graphene to the trapping or defective sites at the interface of graphene and substrate, or vice versa, was considered as the plausible reason behind the hysteresis. The measured results have further confirmed this by exhibiting clockwise and counter-clockwise hysteresis on the electron and hole conduction side, respectively in their characteristics.

The chemical doping of graphene device in nitrogen gas not only introduced *n*-type carrier concentration but also enhanced the hole carrier concentration into the channel because of graphitic (substitutional) and pyridinic or pyrrolic N bonding, respectively. In contrast, an increase in the time constants of charge trapping and de-trapping was observed in annealed devices when compared to un-annealed devices. It might be attributed to nitrogen incorporation in graphene surface which led to structural disorders including bonding defects and vacancies due to pyridinic or pyrrolic N bonding. The hysteresis was diminished significantly by employing short pulse characterisation technique. The fast duty cycle of the applied back-gate voltage reduced the time constants for charge trapping and de-trapping from tens of seconds to microseconds. The obtained values of time constants were most likely due to the filling of shallow traps rather than the deep traps as the charge carriers will not get enough time to trap (or de-trap) in such fast measurement.

Lastly, the noise properties of ballistic rectifier fabricated from InGaAs/InP heterostructure were explored. Both thermal noise and low-frequency noise, i.e., $1/f$ noise or flicker noise, were characterised at room temperature. In this study, a setup based on cross correlation technique using two independent measurement channels was used for the measurement of noise power spectra. Operation at zero bias has enabled the elimination of flicker noise, which often practically limits the microwave detection capability of diode detectors. The findings have been analysed using different theories of flicker noise. In addition, the observed noise at finite biases was quantitatively modelled in the diffusive transport regime of the charge carriers. It has

revealed that the narrowest part of the current channel had dominated the noise properties of the device.

As a potential terahertz detector, the ballistic rectifier and SSD have demonstrated a noise equivalent power (NEP), of the order of 10^{-9} W/Hz$^{1/2}$, in the range of commercially available, uncooled thermal terahertz detectors such as the Goley cell and bolometer. The capability to perform direct rectification rather than responding to heat enables the fast response time of the devices when compared to other THz detectors.

7.2 Outlook

The ballistic rectifiers and the SSDs are typically employed as rectifiers which need to be coupled with the commercially available microwave systems or any receiving antenna to feed the signal. These systems are normally modelled with an output impedance of 50 Ω. However, the impedance of both devices, i.e. of the order of 10^3 Ω, is much higher which results in a large impedance mismatch. It led to a very low level of power being delivered to the ballistic rectifier and the SSD, which significantly degrades the voltage responsivity and NEP of the device.

The fabrication of ballistic rectifiers with much smaller dimensions using a more advanced nanolithography will help to achieve a ballistic transport and much improved intrinsic responsivity. Alternatively, larger arrays of SSDs connected in parallel, as mentioned previously, will help to minimise the impedance mismatch due to the reduction in overall resistance of the device. Such low impedances will improve the intrinsic responsivity of the device.

The nonlinear characteristics of these devices are another figure of merit which play a key role in attaining the best performance in high-frequency signal rectification. The symmetry at the both sides of central axis of ballistic rectifier along the upper and lower channel can ensure more nonlinearity in the output [1]. In the case of SSD, the reduction in trench widths can help to enhance the nonlinearity in the *I-V* characteristics [2].

The low-frequency noise characterisation, as reported in Chapter 3, can be further employed to evaluate the quality and the reliability of graphene based ballistic

rectifiers and SSDs. Since the mobility of a semiconductor material and the resistance of a device can drastically change at lower or elevated temperatures, it may be worth exploring the noise properties in these temperature regions.

One of the advantages of these devices is their planar architecture, due to which they exhibit a low parasitic capacitance enabling their operation at very high frequencies. The theoretical studies using Monte Carlo simulations of ballistic rectifiers fabricated from III-V semiconductor material have predicted cut-off frequencies in the THz range [3]. It can be verified experimentally. However, such facilities were not available during this research for various reasons. The cut-off frequency for graphene based ballistic rectifiers and SSDs can be increased by fabricating graphene on an insulating substrate e.g. quartz, hBN etc.

The ballistic rectifier made from III-V semiconductor is a much more mature technology than that of graphene, hence it can be utilised for microwave/THz imaging. The devices can be coupled to a well-designed antenna structure e.g. bowtie, spiral or log-periodic. Continuous wave (CW), time-domain (pulsed) THz sources including blackbody and free-electron lasers can be utilised for imaging hidden objects [4]. According to market reports, the requirement for THz imaging devices will grow exponentially until 2021 [5]. These devices can provide a reliable solution to this.

Cost-effective and large-area lithography methods such as nanoimprint lithography (NIL) can be employed to fabricate these devices [6]. A multilevel NIL will be useful for preparing the devices coupled to an antenna in a single step for imaging purposes as discussed above. It will help in lessening the fabrication costs associated with the nanolithography techniques such as electron-beam lithography.

Novel material platforms, on which ballistic rectifiers and SSDs can be fabricated, should be investigated. For example, it has been recently reported by Geim *et al.* in Ref. [7] that graphene and other two-dimensional atomic crystals including hBN, molybdenum disulphate (MoS_2) and other layered oxides can be reassembled as a "Van der Waals heterostructures". These heterostructures have unusual properties and phenomena as well as very high mobility (~10^6 $cm^2/V.s$) which led them to offer an alternative solution to compensate for the shortcomings of graphene. Though, it requires many steps and much more sophisticated techniques to be produced.

The graphene field-effect devices described in Chapter 6 might provide the basic building blocks, but with much improved device design, for the realisation of graphene based integrated circuits as reported in Ref. [8]. The success of such new architectures is mainly determined by their reliability and the manufacturing costs. As suggested by the detailed time-domain investigations of trapping/de-trapping mechanism, the performance of the devices can be improved by reducing the defects sites at the interface of graphene and its supporting substrate.

The best solution to this problem is the introduction of a hydrophobic polymer layer such as hBN, hexamethyledisilzane (HMDS) or parylene etc. between the graphene and the SiO_2 [9]. It can be viewed as novel 2D "Van der Waals heterostructures" as discussed above. Other techniques including thermal annealing [10], vacuum treatment [11], siloxane terminated SiO_2 substrate [12], and chemical treatment of the SiO_2 [13] need to be explored to further develop the insightful understanding of the electric-field induced hysteresis in graphene devices.

As a final remark, I would like to mention the famous quote by Dr. Richard Feynman, the father of nanotechnology: "*There is plenty of room at the bottom*" [14].

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