Control of a Super-capacitor Based Energy Storage System

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List of contents

Final word count: 49300

List of tables

List of figures

List of abbreviations

ADI	Applied Dynamics International
AFE	Active front end
AL	Active load
APEC	Applied Power Electronics Conference and Exposition
CCM	Continuous conduction mode
CRM	Critical conduction mode
DC	Direct current
DCM	Discontinuous conduction mode
DIC	Dual-interleaved converter
DoD	Depth-of-discharge
ESS	Energy storage system
HESS	Hybrid energy storage system
HEV	Hybrid electric vehicle
HIL	Hardware-in-the-loop
HMI	Human machine interface
ICE	Internal combustion engine
IEPNEF	Intelligent Electrical Power Network Evaluation Facility
IGBT	Insulated-gate bipolar transistor
IPT	Interphase transformer
IM	Induction motor
MEA	More-electric aircraft
ODE	Ordinary differential equation
PI	Proportional integral (controller)
PMG	Permanent magnet generator
PWM	Pulse width modulation
RTP	Real-time platform
SMES	Super-conducting magnetic energy storage
SoC	State-of-charge
SRSG	Switched-reluctance starter/generator
TESS	Thermal energy storage system
UPS	Uninterruptible power supply
UTC	University technology centre
ZCS	Zero current switching
ZVS	Zero voltage swtiching

List of symbols

Ax	Switches in the dual interleaved converter (x can be 1 or 2)
ADx	Anti-parallel diodes in the dual-interleaved converter (x can be 1 or 2)
Bx	Switches in the dual interleaved converter (x can be 1 or 2)
BDx	Anti-parallel diodes in the dual-interleaved converter (x can be 1 or 2)
C_1	Low voltage side filter capacitor
C_2	High voltage side filter capacitor
C_{bus}	Bus filter capacitor
C_{para}	Parasitic capacitance
C_{sc}	Super-capacitor capacitance
D	Duty ratio
E	ESS energy
E_{base}	Energy base
E_x	ESS energy using control profiles L, C and H (x can be L, C or H)
E_{max}	Maximum energy operating range
E_{min}	Minimum energy operating range
E_{sc}	Energy stored in super-capacitor
E_t	Target energy
E_t’	Normalized target energy, using a base of E_{max}-E_{min}
I_1	Low voltage side current of the DIC converter
I_2	High voltage side current of the DIC converter
I_{AL}	Active load current
I_{base}	Base current
I_{bus}	Bus current flowing into the bus filter capacitor C_{bus}
I_c	Internal super-capacitor current
I_{ESS}	Energy storage system current
I_{gen}	Generator current
I_L	Load current
$I_{Lf\text{-}avg}$	Average filter inductor current
I_p	Peak current seen by the peak current controller
I_{PMG}	Permanent magnetic generator current
I_{RL}	Resistive load current
I_S	Power source current
I_{sc}	Super-capacitor current
$I_{sc\text{-}L}$	Load current reference component
$I_{sc\text{-}re}$	Recharge power current reference component
$I_{sc\text{-}ref}$	Super-capacitor current reference

$I_{L1\text{-}peak}$	Peak of phase current i_{L1}
L	Inductance of the single leg DC-DC converter
L_x	Self-inductance of the IPT windings (x can be 1 or 2)
L_{diff}	Differential inductance
L_{eq}	Equivalent inductance in parasitic ringing analysis
L_f	Filter inductor
L_M	Mutual inductance
L_r	Inductance ratio of L_{diff}/L_f
M	Voltage ratio of V_1/V_2
M_c	Slope compensation rate in the peak current controller
N_s	Number of super-capacitor modules
P_{ESS}	Output power of the ESS
P_{ESS}^*	Power reference of the ESS
$P_{ESS\text{-}L}$	Load component of the energy storage system power reference
$P_{ESS\text{-}re}$	Recharge component of the energy storage system power reference
$P_{ESS\text{-}ref}$	Energy storage system power reference
P_{gen}	Generator output power
P_L	Load power
P_{Lx}	Load powers (x can be 1 or 2)
$P_{L\text{-}base}$	Load base
$P_{L\text{-}max}$	Maximum load power
$P_{L\text{-}pu}$	Load power in per unit
P_{Lt}	Intermediate load power level
P_m	Phase margin
P_S	Power source output power
P_{Sx}	Power source step response profiles (x can be 1, 2 or 3)
$P_{sc\text{-}L}$	Load component of the super-capacitor power reference
$P_{sc\text{-}re}$	Recharge component of the super-capacitor power reference
$P_{sc\text{-}ref}$	Super-capacitor power reference
$P_{S\text{-}x}$	Power source output power using control profile L, C and H (x can be L, C or H)
R	Resistive load
R_{cs}	Current conversion ratio of the current sensor
R_p	Leakage resistance of the super-capacitor
R_s	Series resistance of the super-capacitor
S_1	Upper switch in a half-bridge circuit
S_2	Bottom switch in a half-bridge circuit
T	Switching period
T_{base}	Time base

V_1	Low voltage side voltage of the DIC converter; input voltage in boost mode, output voltage in buck mode
V_2	High voltage side voltage of the DIC converter; output voltage in boost mode, input voltage in buck mode
V_{bus}	DC bus voltage
V_c	Voltage on the super-capacitor
V_L	Averaged inductor voltage
V_L^*	Reference signal from the PI controller
V_{sc}	Super-capacitor terminal voltage
$V_{sc\text{-}max}$	Maximum operating voltage of super-capacitor
$V_{sc\text{-}min}$	Minimum operating voltage of super-capacitor
$V_{sc\text{-}t}$	Target super-capacitor voltage
a	Coefficient of a polynomial of degree 2
b	Coefficient of a polynomial of degree 2
c	Coefficient of a polynomial of degree 2
db_l	Boundary duty ratios
$f_c()$	Peak current controller characteristic function
f_{osc}	Oscillation frequency of the parasitic elements in the converter
$f_p()$	DIC converter characteristic function
$f_{ref}()$	The characteristic function of the DIC converter with a peak current controller
$f_{sc}()$	DIC converter characteristic function
$f_{ss}()$	Steady-state function of target energy E_t versus load power P_L
i_2	High voltage side current
i_{diff}	Differential current
i_{L1}	Phase current in L_1 winding
$i_{L1[k]}$	Phase current i_{L1} at the k_{th} sub-circuit appeared in a switching cycle
i_{L2}	Phase current in L_2 winding
i_{Lf}	Filter inductor current
k_1	Parameter which define the recharge component equation
k_2	Parameter which define the recharge component equation
k_c	Rate-of-change in source power
$k_{c\text{-}base}$	Base value of k_c
$k_{c\text{-}max}$	Maximum rate-of-change in source power
$k_{c\text{-}max\text{-}pu}$	$k_{c\text{-}max}$ in per unit
$k_{c\text{-}pu}$	k_c in per unit
k_i	Integral term of the PI controller
k_p	Proportional term of the PI controller
k_{pwm}	Gain of the peak current controller current reference

p	The sub-circuit number when peak current appears
s	Laplace operator
v_{Lf}	Filter inductor voltage of the DIC converter
v_{t1}	IPT terminal voltage; transistor A2 voltage
v_{t2}	IPT terminal voltage; transistor B2 voltage
v_{A1}	Upper switch A1 voltage
v_{bias}	Internal bias of the peak current controller
v_{com}	Central tap voltage of the IPT
v_{diff}	Differential voltage on the IPT
v_{gAx}	Gate drive voltage of switch Ax
v_{gBx}	Gate drive voltage of switch Bx
v_{iref}	Current reference of the peak current controller
x_l	DCM operating region number
$\Delta t_{[k]}$	Duration of the k_{th} sub-circuit in a switching cycle
ζ	Damping ratio of the closed loop transfer function
ω_c	Unity gain cross-over frequency
ω_n	Natural frequency of the closed loop transfer function

Abstract

The increasing use of electrical technologies within on-board (aircraft, road vehicle, train and ship) power systems is resulting in complex and highly dynamic networks in which energy storage devices have an important role to play, for example to resolve the instantaneous mismatch between load demand and power availability or to provide the flexibility to optimise overall performance. In this thesis, a multi-level controller for a super-capacitor based energy storage system (ESS) is designed, simulated, emulated and validated experimentally to show its effectiveness in smoothing load and managing state-of-charge of the energy storage system.

This thesis first investigates the low level control of the dual-interleaved converter, particularly at light load where seven discontinuous conduction modes (DCMs) appear. A thorough analysis of these operating modes is given and validated by simulations and experiments. Based on the analysis, an inverse-model-based feed-forward current controller is implemented, offering a low level converter control interface which serves the high level supervisory controller within the energy storage system.

Two supervisory control methods have been proposed in this thesis, both producing a super-capacitor current reference for the low level controller. The first supervisory control not only manages the energy within the ESS but also shields the primary power source from rapid load transients, which has been examined through an emulated ESS in the Intelligent Electrical Power Network Evaluation Facility (IEPNEF). A more advanced supervisory controller is then proposed which in addition to the benefits of the first control, regulates the rate-of-change in power that is drawn from the primary power source in the system. The proposed second control method is implemented within a real super-capacitor energy storage system in IEPNEF, with both simulation and experimental results successfully demonstrating and validating its operation.

Declaration

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Dedication

To my wife Linyu Zhou, and my dear parents Mr Minfu Wu and Mrs Mingfang Yu.

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About the author

In 2005, the author took a joint program operated by the University of Manchester and the North China Electric Power University, where he obtained two bachelor degrees, both in Electrical and Electronic Engineering. After graduation in 2009, he started his PhD in the Power Conversion Group, University of Manchester. He has researched a wide area of power-electronics-related topics, including control of energy storage systems, design and control of isolated and non-isolated DC-DC converters for energy storage systems, and he contributed to the design and development of a microcontroller-based communication system for a cryogenic converter, which forms part of a patent application.

The following papers have been published:

- R. Todd, D. Wu, J. A. dos Santos Girio, M. Poucand, and A. J. Forsyth, "Supercapacitor-based energy management for future aircraft systems," Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2010, pp. 1306-1312.
- C. Jia, D. Wu, I. Hawkins, and A. J. Forsyth, "One-wire communication system for cryogenic converter control," Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference on, 2012, pp. 1-5.
- A. J. Forsyth, C. Jia, D. Wu, C. H. Tan, S. Dimler, Y. Yang, et al., "Cryogenic converter for superconducting coil control," IET Power Electronics, vol. 5, pp. 739-746, 2012.

The work in Chapter 4 has been submitted to the PEMD conference (2014) and is under consideration by Rolls-Royce for a patent application.

Chapter 1 Introduction and literature review

1.1 Introduction

As part of its strategy to meet the G8 objective of reducing global CO_2 emissions in 2050 by 50% compared with 2008 levels [1], the government has set targets to limit the CO_2 emissions of the aviation industry to the 2005 level (37.5 million tonnes) by 2050 [2]. However, the recent rapid rise in air travel of 130% in the last 20 years is predicted to increase by a further 60% by 2050. To meet this challenge the aviation industry is pursuing a wide range of new engine, airplane and systems technologies, one of them being the more-electric aircraft (MEA) concept.

1.1.1 More-electric Aircraft

In the more-electric aircraft, traditional mechanical, hydraulic and pneumatic systems which tend to be heavy, bulky and inefficient are replaced by electric motor drives and power electronic converters, which are expected to be lighter, smaller and more efficient [3]. Furthermore, replacing multiple types of power distribution systems with a single electrical system is likely to bring further reductions in weight and complexity. The perceived merits of the MEA are summarised in [3], including improvements in aircraft-empty weight, fuel consumption, installation and maintenance costs, turn-around times and system reliability.

However, the introduction of many electrical drives and converters (for example those for fuel pumps, environmental control compressors, actuators and avionic systems) not only increases the required capacity of the electrical system, but also creates challenges of managing the energy flows, power quality and network stability. This is due to the high peak powers that may be drawn by some loads, the rapid load transients that may occur, and the fact that many motor drives and power electronic converters have constant power characteristics due to their internal control functions, which result in a negative incremental input impedance characteristic [4, 5]. In such conditions, exisiting power distribution networks especially those with weak power sources may encounter sub-optimal operation or even malfunction, demonstrating an inability to acceptably deal with voltage transients and faults. One approach to help solving the afore-mentioned problems

of energy management, power quality and stability is the use of energy storage systems (ESSs) which are under active consideration and development.

1.1.2 Energy storage system (ESS)

By absorbing and releasing electrical energy at different times with little energy loss, energy storage systems provide a mechanism to reconcile the instantaneous mismatch between load demands and source capacity/availability. This can enable reductions in the peak power rating of sources, leading to potential weight and cost savings, and the capture of energy that would otherwise be lost, for example in regenerative braking systems, often leading to overall energy savings. Metro vehicles in [6] using energy storage systems achieved a 30% saving in energy and a 50% reduction in peak power demand. Furthermore, the possibility of continued operation through a power supply interruption was also mentioned. In grid applications [7], an energy storage system may be used to improve the fault ride through capability of wind generators.

Research in the area of energy storage systems includes improving the characteristics of storage devices (efficiency, lifetime, power density and energy density), improved methods of control to optimise the utilisation of storage devices, optimum combinations of devices to meet application requirements (power density and energy density), and new applications.

As this project concerns an energy storage system that is going to be installed in the Intelligent Electrical Power Network Evaluation Facility (IEPNEF), at the University of Manchester. An overview of the facility is provided in the following section.

1.1.3 IEPNEF

The Intelligent Electrical Power Network Evaluation Facility (IEPNEF) located in the Rolls-Royce University Technology Centre (UTC) at Manchester is a 100kW state-of-art facility that emulates the electrical system of a more-electric aircraft. The facility has been established for devising and developing more electric technologies as part of a national project for future aircraft and land-based vehicles [8-12].

As shown in Figure 1.1, the two variable speed induction motor (IM) drives emulate the high speed spool and low speed spool of a gas engine, working as the major power source

of the electrical system. The high speed and low speed spools are connected through two shafts to a 30kW, switched reluctance, starter/generator (SRSG) and a 70kW, five phase, permanent magnet generator (PMG) respectively. Taking electrical power from both engine shafts is an area of active investigation as part of the more-electric aircraft concept due to the increased operational flexibility that it provides [13].

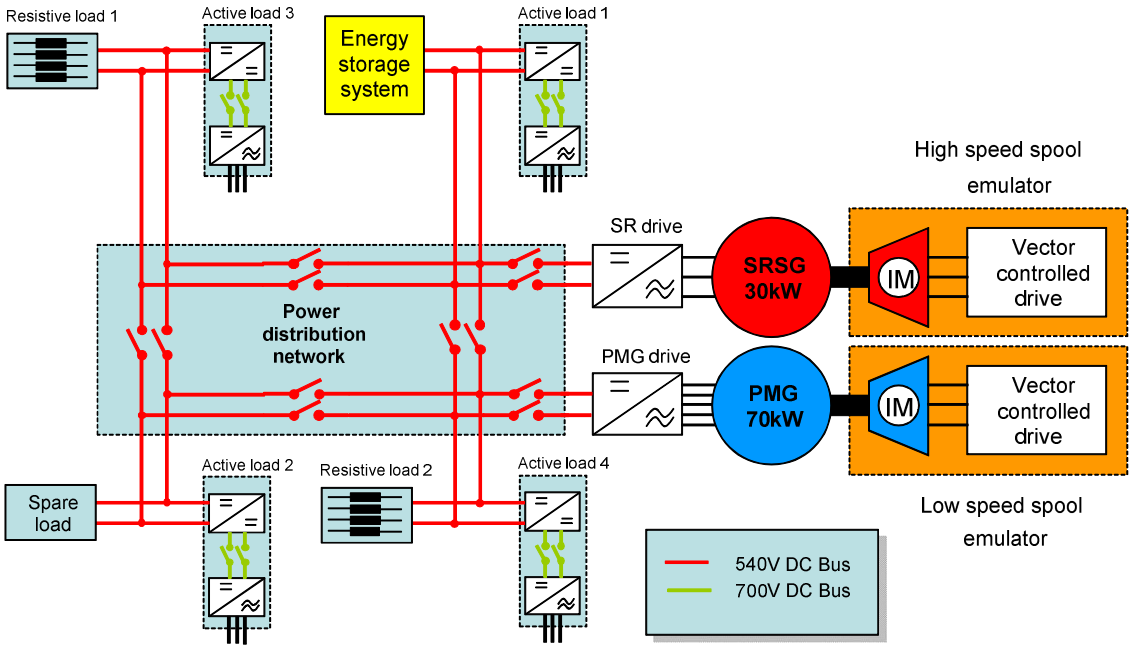


Figure 1.1. IEPNEF system diagram.

The electrical power produced by the two generators is distributed through a high-voltage 540V DC bus structure (power distribution network) to a number of electric loads, which include four bi-directional active loads and two resistive load banks. The whole distribution network is in a ring topology with contactors for fault management and network re-configuration.

The bi-directional active loads on the bus are power electronic based load emulators which replicate the behaviour of real aircraft loads such as actuators, fuel pumps, avionics and environmental control systems. Each active load consists of a 700V DC output active front end (AFE) and a DC-DC converter, Figure 1.2. The active front end (AFE) enables bi-directional power flow, having the ability to transfer power back to the grid. The 700V then feeds a 30kW bi-directional DC-DC converter which converts the voltage to 540V and connects to the power distribution network. The control of both the AFE and DC-DC converter is managed by programmable logic controllers (PLC) though communication

using Control Techniques' CTNet [14]. Overall control is provided by a real-time platform (RTP), manufactured by Applied Dynamics International [15].

A piece of pre-downloaded program is executed within the real-time platform to control the active loads, for example, to emulate an electric actuator. The real-time platform communicates repeatedly with its host computer (not drawn) located in the control room via Ethernet, allowing remote control and monitoring of the active loads. The programming of the real-time simulation platform is undertaken in Simulink.

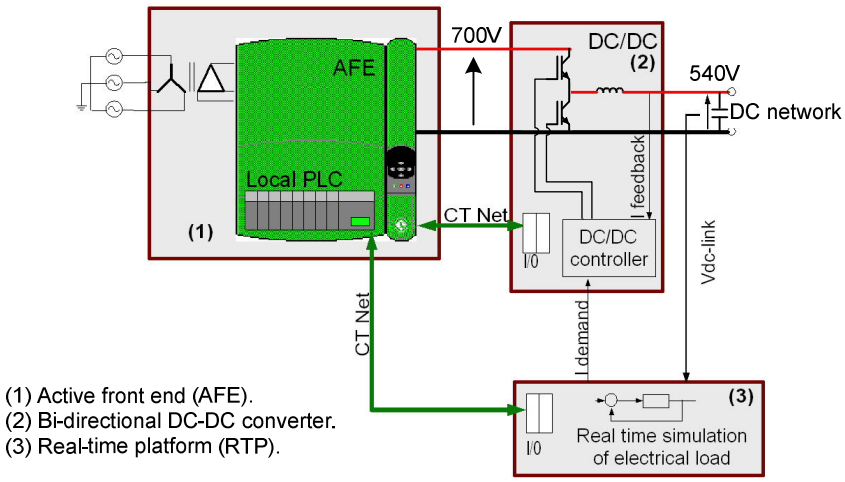


Figure 1.2. Diagram of active load system [8].

Two resistive load banks are available as general background loads, Figure 1.1, each contains four individual resistors of 120Ω, 60Ω, 30Ω and 30Ω. The combination of different resistors can provide load steps of approximately 2.5kW, reaching a maximum of 26.7kW with a 540V bus voltage.

A super-capacitor based energy storage system was added to IEPNEF during the course of this PhD project, and the research described in this thesis has supported that development. However, initially, one of the active load systems was used to emulate the operation of the energy storage system. By doing this, the control algorithm and the benefits of the energy storage system were examined.

1.1.4 Objectives

The overall objectives of this PhD project were to investigate the converter interfacing, operation and control of a super-capacitor based energy storage system for use within an on-board DC electrical system such as the IEPNEF lab. The dynamic electrical loads and

the varying voltages on the storage devices require the ESS converter to operate correctly across the various operating conditions. Therefore, the fundamental behaviour of the converter needs to be fully understood as it is essential to successfully implement current or voltage controllers. The supervisory level energy management strategies are also an important part of the ESS control, to improve system level performance including energy management, system stability, power capability and load smoothing. In this thesis, the target has been set to operate the converter over a wide operating range while maximally utilising the limited ESS energy, and achieving the conflicting requirement of reducing the impact of load changes on the power sources.

1.2 Literature review

A wide range of papers has been published on energy storage systems, the most common application being for hybrid electric vehicles (HEV) [16-21] where the efficiency, output power or the lifetime of the on-board electrical devices (such as batteries) are of most concern. Applications for trains, trams [6, 22-25] and the MEA [26] can also be found. Other papers describe using an ESS as an auxiliary device to improve the stability and power quality of a power grid or micro grid [7, 21, 27-29], and even an application has been reported using a super-capacitor based ESS for elevators [30].

In the following sections, the main components of an ESS are reviewed first, including: the available energy storage sources, energy management strategies, and DC-DC converters and their control. Secondly, a review of simulation methods including hardware-in-the-loop (HIL) simulation is presented.

1.2.1 Energy storage categories

Through history, much effort has been spent on finding new energy sources. From using firewood for keeping warm in ancient times to using nuclear reactions for power generation today, a large variety of energy sources is available for use. However, not all are regenerative or suitable for storage. For example, oil is not regenerative, whilst some other sources like solar power or wind are regenerative but not suitable for direct storage. The power from the sun or kinetic power from the wind has to be converted into other forms for easier storage. The range of energy storage forms can be categorized into five

types: mechanical, thermal, electrical, magnetic and chemical energy (in electro-chemical and thermal-chemical forms) [31], which will be described in this section.

1.2.1.1 Mechanical energy

The kinetic energy of a moving or rotating mass is one form of stored mechanical energy, the flywheel being the most obvious example. The amount of stored energy in a flywheel is proportional to the square of the rotational speed, which is limited by the tensile strength of the material used and the bearing [32]. With the recent advances in super-strong and ultra-light composite materials, and frictionless, high-performance magnetic bearings [31], the flywheel has now become a strong candidate for energy storage systems, featuring high efficiency, high power density, no emissions and a virtually infinite number of charge and discharge cycles [33, 34]. In addition, it is relative easy to monitor the state-of-charge of a flywheel simply by measuring its speed. In [34], a 10MJ flywheel energy storage system is designed with a peak power of 10kW to improve grid power quality; and the work in [35] addresses voltage sag problems in a grid using flywheel energy storage system.

Another form of stored mechanical energy is potential energy. Pumped hydro and compressed air are typical examples of potential energy, which are usually used for grid applications due to their high energy capacity and high output power [36, 37]. These types of storage are important for the economical operation of the grid, for example, to release energy stored during the low demand period at times of peak demand, i.e., load levelling. However pumped hydro power plants consume 1.3kWh to 1.4kWh in pumping for every kWh generated from storage [37] due to the losses associated with evaporation and friction.

1.2.1.2 Thermal energy

Thermal energy can be stored as ‘sensible heat’, ‘latent heat’ or as the heat of a chemical reaction (thermo-chemical) [31]. Sensible heat involves storing energy in the high heat capacity of a storage medium, water, or molten salt, by raising its temperature; whereas latent heat involves using the energy required to make a phase change from solid to liquid and vapour as a storage mechanism; the third form is the heat in reversible chemical reactions, including decomposition of metal hydrides, oxides, etc. [31]. Thermal energy storage systems (TESS) are usually found in cooling or heating systems for buildings and

solar thermal power plants [38]. Due to the need for large storage tanks, thermal storage systems are generally not suitable for the transport industry.

1.2.1.3 Magnetic energy

Magnetic energy is stored in the magnetic field produced by a large current. The superconducting magnetic energy storage (SMES) system operates on this principle, utilizing a superconducting inductor to virtually eliminate conduction loss. The advantages of SMES systems are the high efficiency above 90% [39], the quick, high-power response [40], and applicability in cryogenic climates (-54℃) where other power sources like batteries cease to function [41]. The disadvantages of SMES systems are the high cost [42, 43], the additional cryogenic refrigeration system required to keep the coil in a superconducting state, and the protection required against quench conditions in the superconductor. Due to its extremely high power rating [32], but large size and weight, SMES systems are usually found in power quality applications for the utility grid. For example SMES systems are being evaluated [44, 45] for smoothing output power from wind farms. In [41], the author proposes a small scale SMES for aircraft, however, it has a capacity of 5kWh and weighs 500kg.

1.2.1.4 Electrical energy (including electrochemical energy)

Hydrogen storage systems (fuel-cells), batteries and super-capacitors are widely used technologies for electrical energy storage. Quite a number of applications can be found especially in the transport sector utilizing individual units or the combination of different types of devices in order to combine their best features in cost, energy/power density, response time, and efficiency [32]. Fuel-cells and batteries utilise electrochemical conversions to store energy which tends to result in a device with a high energy density [33]. However, degradation occurs in batteries over a number of repetitive charge and discharge cycles, especially at extreme rates and with over-charging/discharging, which tends to reduce capacity and lifetime [46]. Super-capacitors, on the other hand, store energy by simple charge separation without chemical reaction and tend to have high peak power capability and a long lifetime but low energy density [33, 47].

Fuel-cell

The fuel-cell combines oxygen with a hydrogen fuel and converts them electrochemically into water, heat, and the production of electricity [48]. The absence of any greenhouse gas emissions makes fuel-cells an attractive energy source for many applications including road vehicles [49]. Regenerative fuel-cell are devices that combine the function of electricity production and hydrogen production for energy storage [33].

Some key features of fuel-cells include:

1. a low and poorly regulated output voltage which requires series connections to increase the output voltage and/or power electronic control to stabilise the voltage [50];
2. clean operation with low emissions [42] and a high energy density (typically 200Wh/l - 300Wh/l), which is much greater than that of batteries [50];
3. the temperature, gas flows, pressure, and humidity of the cell have a strong influence on the behaviour and performance [42, 51];
4. high efficiency is possible (40%-70%) [48], but is affected by the temperature and pressure conditions, and so it is important to control these conditions for maximum efficiency [52];
5. slow response due to limits of the mechanical devices required for maintaining the temperature, pressure and humidity. Therefore, during rapid electrical load transients, the fuel-cell may suffer partial over temperature or over-air pressure conditions which shorten the lifetime of the fuel-cell [53];
6. the main challenges for fuel-cell technology include the high price, the durability of the system and the fuel storage mechanism [54].

Batteries

Among the various kinds of rechargeable batteries, lead-acid batteries are still the most widely used, which first appeared in the mid 1800's [33]. Their advantages are the low price and high energy density [31]. Nickel cadmium (NiCd) batteries became widely used between 1970 and 1990, but have recently been replaced by lithium-ion and nickel metal hydride (NiMH) batteries which offer the advantages of longer life cycle, less pronounced 'memory effect' and higher energy density [33]. Some other types of rechargeable batteries are summarised in Table 1.1 together with the afore-mentioned batteries.

Table 1.1 Battery technologies summary [50]

Technology	Capacity (Ah)	Cycle life (Cycles)	Energy density (Wh/kg)	Power density (W/kg)	Cell voltage (V)
Nickel-Cadmium	100-180	2000	50-60	200	1.35
Iron-Air	-	200	80	30-40	-
Iron-Nickel Oxide	200-600	920	50-250	100	-
Lead-Acid	100-1500	1000-1500	20-50	80-300	2.1
Nickel-Metal Hydride	100-250	1000	50-60	200-250	1.25
Lithium	100	1200	40-150	100-400	3.6
Sodium-Sulphur	230-300	600-800	80-120	90-200	2.08
ZEBRA	-	>1200	80-100	150-200	2.58
Zinc-air	-	-	200	100	-
Zinc-Bromine	120	350-500	70-90	80-100	1.79
Zinc-Nickel oxide	300	-	70	200	-

The main application areas for battery storage reported in the literature include portable equipment, vehicles, industrial applications, uninterruptible power supplies (UPSs) and load levelling for grid systems [25, 29, 31, 33, 55]. Lithium-ion batteries and Ni-MH batteries tend to be preferred in portable applications [31]. Hybrid electric vehicles (HEVs), such as the Toyota Prius and the Honda Accord, use sealed Ni-MH batteries [56, 57]; some new battery technologies, like the ZEBRA battery, are also used for HEVs [58, 59]. For grid applications, large battery storage using lead-acid batteries existed early in the 1930s and had 186MWh capacity [32]. However more recently lithium-ion cells are being used, for example, by Siemens [60].

One of the problems of batteries is the aging process. The longevity of batteries is significantly affected by the depth-of-discharge (DoD) [61], extreme temperatures, over-charging or over-discharging, and the rate of charge or discharge [46, 62, 63]. Some of the other disadvantages of batteries include the toxic materials used in manufacturing [31] and the safety issues such as gas release during over-charging, and protection against thermal runaway [46, 64].

Super-capacitors

Super-capacitors, also known as ultra-capacitors or electric double-layer capacitors, store electrical energy in the electric field between two electrodes [32]. Compared to conventional capacitors with mF or μF capacitance, super-capacitors are designed to have a large electrode surface area and use high permittivity dielectric, therefore attaining very high capacitance ratings (up to kF).

The key features of super-capacitors are:

1. low output voltage (2.7V per cell); therefore series connection of cells with balancing is necessary [32];
2. high power density (2kW/kg) [32, 48], but low energy density [54];
3. nearly unlimited charge/discharge cycles and a long life time of ten years [32, 43];
4. high in-out efficiency, above 95% [32, 48], but the self-discharge rate is also high (5% per day) compared with batteries [32];
5. state-of-charge (SoC) is simple to monitor by measuring the voltage [32];
6. easy installation, compact size [32] and adaptability in adverse environments (hot, cold, and moist) [43].

However, among the merits of the super-capacitors, the most dominant feature is their high power characteristic which has resulted in them finding applications in many fields. Iwanski [28] reports the use of super-capacitors for smoothing wind turbine output power in a micro-grid. The authors of [22, 24, 65] use super-capacitors for on-board and sub-station energy storage for metro trains. Curti [16] improves the dynamic performance of a battery bank using super-capacitors in an HEV. Zhang uses super-capacitors to improve the power quality of an aircraft electrical system in [66, 67].

A typical operating regime for a super-capacitor bank is to allow the voltage to vary over a 2:1 range, which enables 75% of the maximum stored energy to be used within a system application [48]. A greater depth-of-discharge is normally avoided since it results in very high capacitor currents for a given power level and places extreme demands on the interfacing DC-DC converter [52, 68].

Hybrid energy storage systems (HESS)

As a summary, the features of different energy storage technologies are compared in terms of their energy capacity and power capability as shown in Figure 1.3.

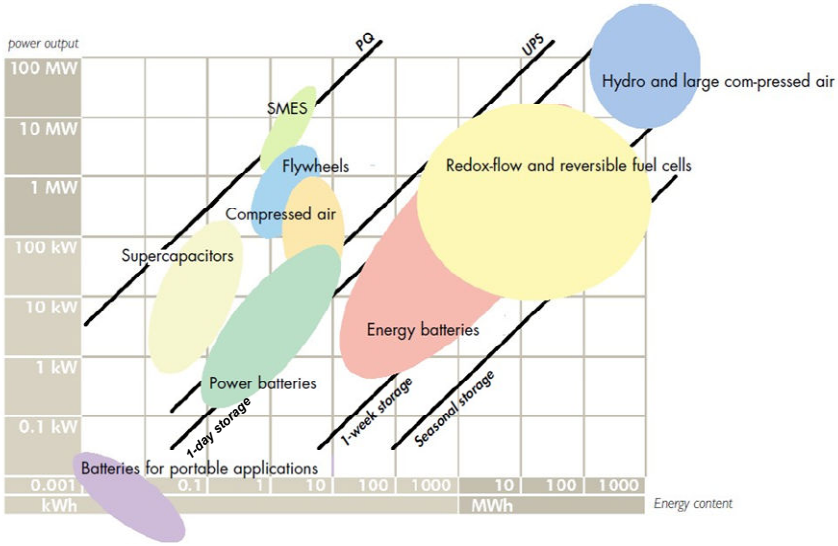


Figure 1.3. Power against energy plot for various energy storage technologies [32].

Due to their different characteristics, multiple energy sources are sometimes combined. These combinations come in many variations, but all share a common trend of combining fast, high power devices and slow, high energy devices [54]. For example, the slow responding fuel-cell is often equipped with auxiliary storage devices to improve its dynamic performance, lifetime and operational safety [21, 69]. Thounthong improved the dynamics of a fuel-cell first by utilizing a battery bank as a secondary source in [21], and later added a super-capacitor for further improvement [70]. Another widely used combination is of a battery and super-capacitor for an HEV, in which the super-capacitor is used for improving battery lifetime and fuel-economy [16-19, 27, 61, 71-73]. In addition, other hybrid energy storage systems are reported in the literature:

1. battery and super-conducting magnetic coil [74];
2. battery and flywheel [75];
3. fuel-cell, batteries and super-capacitor [20, 52, 70];
4. fuel-cell and super-conducting magnetic coil [45];
5. compressed air and super-capacitor [76].

For the energy storage system to be used on the target on-board electrical system in this thesis, super-capacitors are the ideal candidate because of their high power density and high peak power it can provide to improve the stability, power quality of the system.

1.2.2 Energy management strategies for the energy storage system

Due to the finite energy in an energy storage system (ESS) and the need to ensure appropriate power sharing with other sources, it is necessary to deploy high level energy management strategies to optimise the overall performance of an electrical system containing an ESS.

Considerable research work has been undertaken on energy management strategies for ESS. However, there is no general way of judging whether one particular strategy is superior to others, since they tend to have different goals. These goals include supplying power demands, optimising efficiency, managing energy storage, and ensuring power quality and stability of an electric system. Furthermore some efforts have been made to consider multiple objectives, most commonly seen in strategies using fuzzy logic or neural networks. In the following section, energy management strategies are categorized in terms of their different goals, followed by a review of implementation methods.

1.2.2.1 Energy management strategy goals

Common goals of energy management strategies are summarised in Figure 1.4, and will be described in the following section.

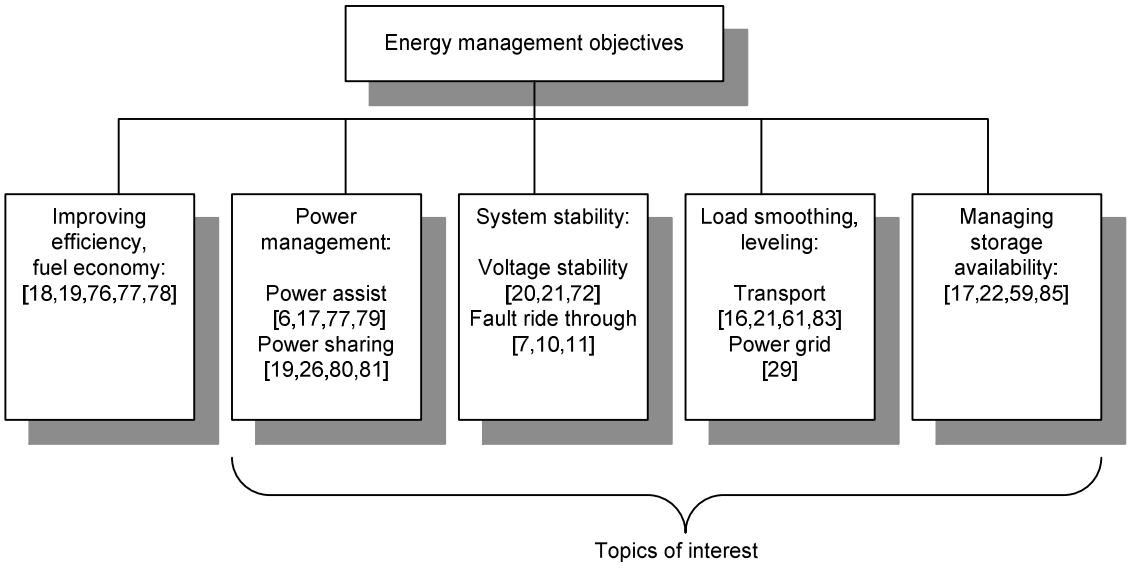


Figure 1.4. Energy management objectives.

Improving efficiencies in devices or at system level

One interest of many researchers is minimising the losses in individual devices or minimising overall system losses (improving efficiency), which is a very common objective in HEV applications for the purpose of improving fuel-economy. There are also non-HEV applications as in [76] which proposes a maximum-efficiency-tracking control during charging and discharging of a compressed air storage system by using an oil-hydraulic machine and super-capacitors.

In the HEV application in [77] comprising a 123kW ICE, a 33kW traction motor and NiMH batteries, an engine efficiency map is created on which the control is based. As auxiliary devices, the traction motor and batteries are used to balance the vehicle power and adjust the engine output power to achieve the most efficient operating point of the engine. However, this strategy only concerns the efficiency of one device, the engine only.

A more direct and effective method is proposed in [78], where the author manages to enhance the fuel-economy of a battery powered EV by minimizing the total depth-of-discharge (DoD) of the batteries based on known driving cycle profiles. Equations are derived for determining the power sharing between the main power source (batteries) and the auxiliary source (super-capacitors) at any moment of the driving cycle to achieve the goal of minimum total depth-of-discharge. For practical use, the author then proposes a self-learning neural network control, which is trained with the optimum current sharing profiles that were obtained in the off-line study.

Similar but improved, work in [18] and [19] uses real-time loss minimization algorithms to distribute the load between different energy sources on a general DC bus system. Equations are derived for calculating the losses present in all on-bus devices, with constraint equations used to prevent devices being completely depleted. In comparison with the minimum depth-of-discharge strategy [78] described in the last paragraph, an important feature of this method is that the control action is updated continuously without tracing the history or foreseeing the trend of loads. The strategy is claimed to suit any unknown load profile. As validation, the author has simulated the algorithm using three different driving cycles showing significant loss reduction.

Power management in supplying load demands

One of the simplest strategies for controlling an energy storage device is the so called 'full load powering' mode whereby the storage system is commanded to provide the full power requirements of a dynamic load element [17]. As a consequence, the main power source in the system does not experience any change in load demand, which ensures the whole electrical system always remains in a steady operating condition. Similarly if the load regenerates, the energy storage device absorbs all the power. However, this strategy is not suitable for long lasting load variations, since the ESS will cease to function once its energy reserves are depleted or it is fully charged.

The energy storage device may also assist the main power source to provide extra power, or reduce the peak power required from the main power source than compared with using it alone. In both [79] and [77] for a train and an HEV application, a battery powered electric motor is coupled on the same power train with an internal combustion engine (ICE). In 'hard acceleration' mode, the electric motor assists the engine so as to achieve better acceleration performance. On the other hand, in [6], a tram application, the peak power requirement was reduced by up to 50% by using super-capacitors to mitigate the voltage drop on the tram power supply lines.

In contrast to the two examples above which operate the storage devices aggressively, a milder strategy is when power demand is split between the main power source and the ESS, or between multiple, parallel connected but dissimilar storage devices in a hybrid energy storage system. In [19], a technique is described for splitting the power demand between super-capacitors and batteries with a coefficient, whose choice is however not well explained. The power management strategies in [80] give priorities, loading a battery until it reaches its current limit and then using a super-capacitor to provide the remaining power. A hybrid ESS containing super-capacitors and dump resistors is proposed in [26] where fuzzy logic control is used to split the power and minimize the wasted energy in the resistors. Also, [81] uses a wavelet-based load sharing algorithm to decompose the load into high frequency and low frequency components to control a fuel-cell/super-capacitor combination on-board a hybrid electric vehicle.

Improving power quality and voltage stability

To manage the power quality in an electrical system, research in [20, 21] proposes a technique for stabilising and regulating the voltage of a distribution bus whereby a super-capacitor is responsible for regulating the voltage, while the generator, battery and fuel-cell are operated with relatively slow-acting current controllers so as to improve their life expectancy. A similar technique for bus voltage stability is applied in [72], and the author also proposes a start-up sequence in which the generator must first charge the super-capacitor to a minimum voltage level. In [7], a technique is proposed to improve the fault ride through capability of a wind generation system by using super-capacitors. In [10, 11] the authors investigate super-capacitor-based techniques for mitigating the system voltage transients that may occur in a DC network following generator faults.

Limiting dynamic change of output power from power sources

The author in [82] notes that in some aerospace applications the electrical loads can be highly dynamic resulting in high rates-of-change of power being demanded from the sources, such as fuel-cells and gas-turbine-driven generators. This in turn can lead to excessive wear and lifetime reduction in the sources. The use of energy storage systems is discussed to reduce the rate-of-change of power that is imposed on the sources and thereby improve lifetime.

A direct and effective solution is to use a rate limiter to constrain the rate-of-change in output power or current for the main power source. In [21], a fuel-cell is the main power source and its maximum rate-of-change of current is set at $\pm$4A/s. The difference between the load demand and fuel-cell output power is provided by an auxiliary super-capacitor.

Work in [61, 71, 83, 84] uses low-pass filters (LPFs) to provide a rate-limited demand signal to sensitive power sources. Figure 1.5 shows one example of such control proposed in [83]. After a step increase in load P_{load}, the filtered low frequency component P_{gen} forms the command to the slow power sources, while the rapid high frequency component P_{sc} commands the faster auxiliary sources (the super-capacitor in this case). The ΔP_{sc} component is intended to manage the state-of-charge of the super-capacitor and tends to vary relatively slowly. Rule-based control is suggested for ΔP_{sc}, depending on the vehicle speed, super-capacitor voltage Usc and other information like management strategies.

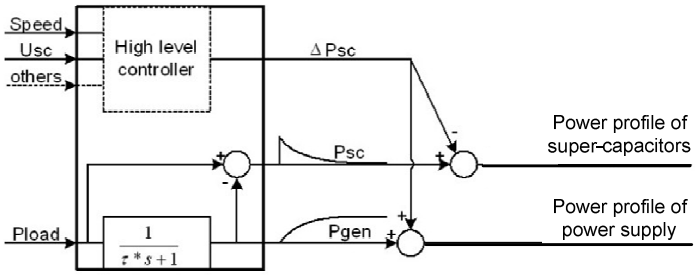


Figure 1.5. Control strategies of using LPF in [83].

However, determining the time constant for the low-pass filter is a challenge, since this affects the level of utilisation of the energy storage system [16] and the extent of the performance improvement. In [29], time constants of t=60s and 1800s are considered for a wind farm application which includes large-scale energy storage. Other research, [16], focuses on selecting suitable time constants for a hybrid energy storage system in an HEV, in which a time constant of the order of seconds is suggested considering the worst case conditions of load level and the energy storage capacity. However, the primary criterion for time constant selection is the overall system efficiency.

As an alternative to the use of a constant rate limiter or a low-pass filter, the author of [24] uses a Kalman filter to calculate a dynamic average of the total required power for the main power source to follow.

Managing storage availability

Another aspect of energy storage system control considered by numerous authors is the availability of the energy storage, that is, the ability to either source or sink power given the finite capacity of the device. A generally accepted rule is that the state-of-charge (SoC) should be low when there is a possibility of returned or regenerated energy and the state-of-charge should be high when the load level is low.

For ground vehicle applications, much research work relates the SoC with the vehicle speed, since returned power from the vehicle is usually from regenerative braking and is therefore most likely to occur at higher vehicle speeds. A suitable state-of-charge setting in real-time guarantees both the power capability and margin for energy storage.

The author of [59] uses a pre-defined charge curve (Figure 1.6) to determine the target state-of-charge for the super-capacitors during vehicle operation. Since it is a hybrid energy storage system, the target state-of-charge is not only inversely correlated to the

vehicle speed, but also positively correlated to the battery depth-of-discharge (DoD). However, it is not explained in detail how this charge curve is created.

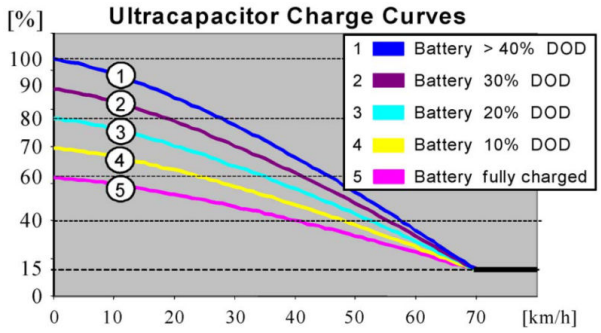


Figure 1.6. State-of-charge of super-capacitor against vehicle speed and battery DoD [59].

Work in [22, 85] uses the speed of a running train as the reference for the SoC control of the on-board super-capacitor for accommodating possible future acceleration or deceleration. A two-level, nested PI controller is used, with the outer loop controlling the super-capacitor voltage to track the target reference and the inner loop regulating the super-capacitor current. As the of speed of the vehicle varies, the reference also changes and the super-capacitor charges or discharges.

Another example of managing state-of-charge is described in [17] where the total stored energy in an HESS comprising super-capacitors and batteries is replenished, always having the ability to sustain a 10s load pulse of a given power.

1.2.2.2 Control methods

This sub-section reviews some of the main control structures and methods described in the literature for implementing the energy management strategies and targets described in the previous section.

The most common and simple approach is voltage control (often with a nested inner current loop control), which is typically seen in applications where there is a requirement for an ESS to stabilise a bus voltage [20, 21]. Alternatively a similar approach is used where the voltage of a super-capacitor or battery is set according to a state-of-charge controller [22, 85]. For example, [28] describes a DC system using a super-capacitor based ESS that utilizes two voltage controllers for both the super-capacitor voltage and bus voltage, which is shown to be an effective way of maintaining both bus voltage and super-capacitor voltage at the required values. Straightforward current control is also used, for

example, in applications [21, 58] where there is a requirement to command the storage system to compensate for load changes within a system.

More advanced forms of control in which multiple factors may be considered together, for example, efficiency and voltage stability, can be achieved using fuzzy logic [77, 86, 87] or neural network control [58, 78]. Nevertheless, these control methods are either complicated or can demand high processing power for real-time implementation. Ortuzar in [58] uses neural networks to achieve maximum efficiency of an HEV by training the neural networks with various sets of data of known driving cycles, in each of which the most efficient current for a given load is calculated. Moreno in [78] uses 10 driving cycles as learning material, and 20 driving cycles as validation, which is shown to provide a further 3.3% improvement in the km/kWh indictor compared to his previous work using simpler state-of-charge (SoC) control in [59].

Rule-based control methods are suggested for some applications in which high level rules are set to determine when devices should be charged or discharged, for example, charging a super-capacitor when its voltage falls below a pre-defined value. Chan in [25] used a well defined flow chart for determining when to charge and discharge super-capacitors in a railway energy storage substation. Rizzo [52] used a finite state machine to implement the operating mode swapping of the two converters in a hybrid energy storage system. Voltage control, power control and current control of the different sources were used sequentially. Similar work using a finite state machine is found in [88, 89] to swap modes between the battery safe current operation and fuel-cell maximum efficiency power control; and an adaptive control method is proposed for a fuel-cell-battery-powered hybrid system for trams in [90], where eight states (or effectively eight rules) are defined depending on the tram speed, SoC of the battery and super-capacitor and constraints on fuel-cell output power.

A hierarchy of control layers is proposed by some researchers [86]. For example, the author in [16] suggests three layers of energy management: the converter control is at the lower level, operating in the μs time frame, above that the power sharing control between multiple energy storage devices operates in the ms time frame, whilst the top level control is concerned with overall energy management and operates over a time frame of several seconds.

One example of hierarchical methods is in [26], where two levels of control are implemented to manage the power flow in an aircraft electrical system. The higher level determines the total required power to be delivered from the ESS to the bus; the lower level determines the power sharing between the storage units and the load system. Two strategies are proposed for the two levels of control, each contains fuzzy logic. A 3kW test bench shows that the control improves voltage stability, energy efficiency and storage availability. However, the rate-of-change of power drawn from the main power source is not considered and in spite of using an optimized look-up table, the fuzzy logic control requires over 100μs to respond.

A number of authors propose using various combinations of control methods to meet specific requirements, for example, [19] uses a combination of overall loss minimization, combined with a constraint on the maximum permissible rate-of-change of power that may be drawn from the main source. [91] proposes the use of fuzzy logic for state-of-charge management and a filter arrangement to determine the power sharing between sources, whilst in [84], a low-pass filter is used to set the power sharing between sources coupled with a moving average calculation on the main power source to set the state-of-charge control reference.

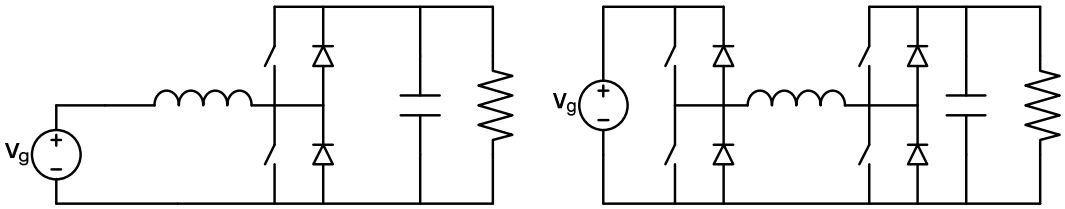
1.2.3 DC-DC converters for energy storage systems

As the core component of an ESS, the power converter provides an interface between the storage device and the electrical bus. The converter manages the power flow, and achieves power conversion between the DC or AC systems. However, in this section, only DC-DC converters are reviewed, since popular storage devices including fuel-cells, batteries and super-capacitors all provide DC voltages, while DC electrical buses (such as IEPNEF) are the target system and are becoming popular because of their weight saving due to the use of only two-wire system rather than three- or four-wire in AC three phase system.

Since a large number of converter topologies is possible [92], only a selection of the main bi-directional DC-DC converters is given, categorised into non-isolated and isolated variants in Sections 1.2.3.1 and 1.2.3.2. A review of common control methods for converters, emerging semiconductor devices and simulation methods then follows.

1.2.3.1 Non-isolated DC-DC converters

Power electronic circuits containing only one switch and one diode have been summarised in [93] where 33 topologies are identified, including the basic buck, boost, buck-boost converters and their derivatives. The basic buck, and boost converters have simple forms and good switch utilisation, which make them widely used [94].



(a) Half bridge converter. **(b) Buck-boost converter.**

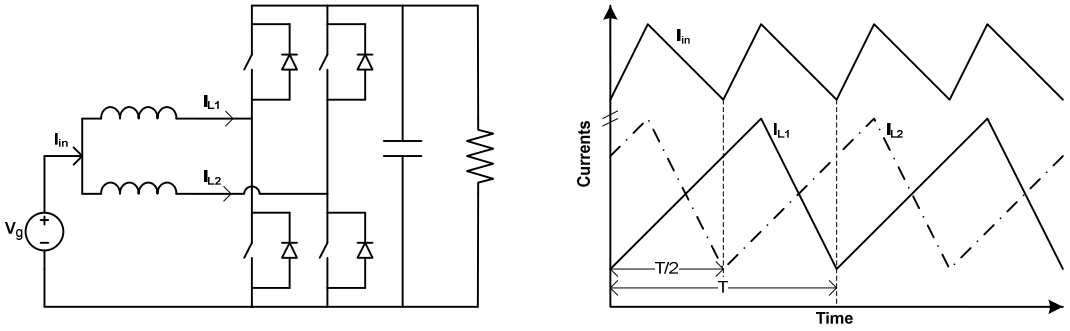
Figure 1.7. Basic non-isolated DC-DC converter topologies.

Nevertheless, the basic buck and boost converters are uni-directional. A bi-directional half-bridge converter combining the buck and boost converters is shown in Figure 1.7c. The half-bridge circuit can work in the same way as the basic boost circuit when the upper switch is permanently off, and as the buck circuit when the bottom switch is off, although to achieve buck operation the source voltage and load resistor must be interchanged.

Due to its simple structure, the half-bridge converter is one of the commonly used converters for energy storage systems (ESS) [22, 28, 58, 68, 95]. For energy storage applications, the storage device may take the place of the load resistor in Figure 1.7c or the source voltage with the DC bus being connected to the other port. The choice of connection depends on whether the storage device voltage is larger or smaller than the bus voltage. The half-bridge converter also forms the basis for a number of other circuits, for example, the buck-boost cascade converter [96, 97], Figure 1.7d.

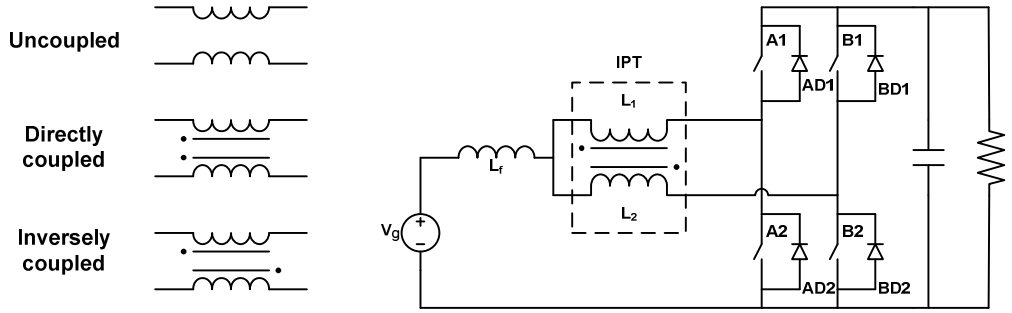
Higher power ratings can be achieved using parallel half-bridges or parallel devices and interleaving techniques, where the latter technique reduces the input and output ripple currents and therefore the size and losses of magnetic components and filter capacitors [98, 99]. An interleaved half-bridge converter circuit comprising two half-bridges sharing the same input and output voltages with individual inductors, is shown in Figure 1.8a. The two half-bridges switch with a 180° phase-shift, which reduces the total input current ripple as shown in the waveform, Figure 1.8b. In [98], both multiple parallel devices and

interleaving techniques are deployed, which effectively reduces the magnetic component size. Further reduction in ripple current can be achieved by increasing the number of phases as in [100, 101] where a three-phase converter is made for 100kW operation, and in [102] and [103] where eight- and 36-phase converters are described respectively.



(a) Bi-directional dual interleaved converter. **(b) Operating waveforms of the converter.**

Figure 1.8. Interleaved bi-directional half-bridge converter and its operating waveforms.



(a) Inductor coupling configurations. **(b) Bi-directional dual interleaved converter with IPT.**

Figure 1.9. Inductor coupling arrangements and the dual interleaved converter with IPT.

To further reduce the size and weight of the magnetic components, several authors have suggested integrating the magnetic components by coupling the input inductors. For the two phase converter, the two inductors in Figure 1.8a can be coupled in two configurations: directly coupled, or inversely coupled, Figure 1.9a. In [104], the two configurations together with the uncoupled version are compared in continuous conduction mode (CCM), where the currents in the inductors are continuous and do not cross zero. The comparison shows that the directly coupled configuration exhibits small-signal dynamic characteristics in which there is an insensitivity to input voltage variations; whilst the inversely coupled version shows a fast response and is insensitive to load variations; whereas the uncoupled inductor configuration shows a medium performance. The inversely coupled inductor arrangement is also referred to an interphase transformer (IPT) [105], which forms the circuit used in this thesis with a further filter inductor added, Figure 1.9b.

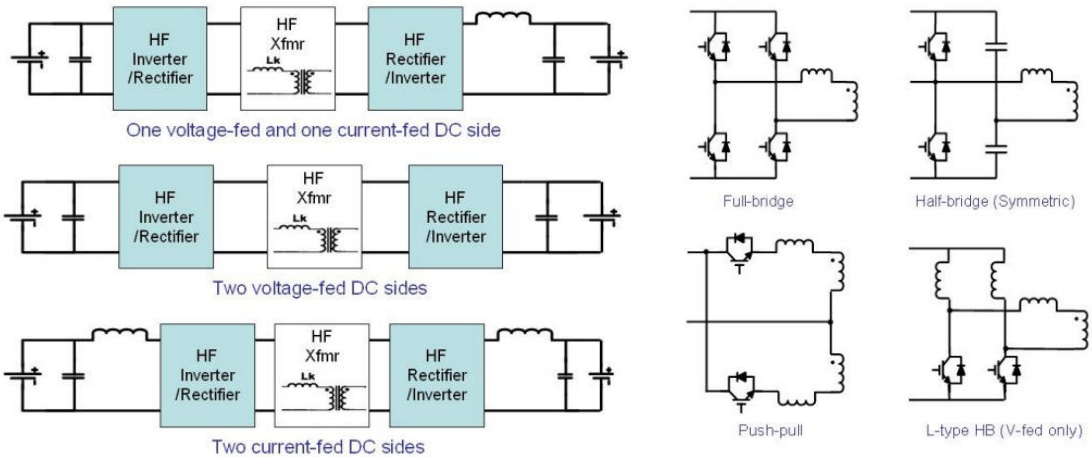
To improve the efficiency of interleaved converters, two simple methods are found in the literature without modifying the circuits. The first uses complementary switching in the half-bridge circuits to achieve zero-voltage-switching (ZVS) when the current flowing in the inductor crosses zero, [100, 101]. However this requires high ripple current, which may increase inductor losses. Another method is to confine the converter to the discontinuous conduction mode (DCM), where the inductor current is zero for a period of time in a switching cycle, and therefore zero transistor turn-on losses and low diode reverse recovery losses can be achieved. However, the DCM operation increases turn-off losses because the peak current in a cycle will be higher if the same average current is to be achieved when compared with CCM operation [100]. Besides, parasitic ringing during the discontinuous part of the cycle may cause extra losses as found in [106], and illustrated in Chapter 2, Section 2.4. As a compromise, some researchers suggest operating the converter in the critical conduction mode (CRM) [107], that is, on the boundary between CCM and DCM.

In many applications described in the literature, the interleaved converter is analysed and designed for only one operating condition, either CCM, CRM or one particular operating pattern in the DCM, furthermore the design is usually optimised for full power conditions. The DCM operation of the uncoupled, directly coupled, and inversely coupled windings are different as described in [108], [99] and [106] respectively. These different DCM operating patterns have also been observed to appear in the converter with IPT and filter inductor in Figure 1.9b, since these three circuits can be transformed into the form shown in Figure 1.9b (transforms given in Appendix A.1). A steady-state analysis applicable to any two-phase interleaved circuit is presented in Chapter 2 to show that seven sub-DCM operating patterns may arise at different input/output voltages and power levels. The analysis is particularly important for super-capacitor applications since the voltage on one side of the converter may vary over a wide-range which can cause the converter operating mode to change between different sub-DCM modes.

1.2.3.2 Isolated DC-DC converters

An isolated DC-DC converter contains an inverting stage (DC-AC), a high frequency transformer (AC-AC), and a rectifying stage (AC-DC) for complete power conversion. Compared to non-isolated converters, the isolated DC-DC converters can provide high step-up/step-down ratio and galvanic isolation through the transformer, which however implies additional cost and losses [109]. Some basic isolated DC-DC converters include the forward, flyback, push-pull, half-bridge and full-bridge topologies [92, 110].

Isolated converters with a bi-directional power flow capability are classified in the review in [109, 111] into voltage-fed or current-fed configurations, Figure 1.10a, depending on whether an inductor is connected at the input or output terminal. Four inverting/rectifying stages for bi-directional converters are identified as shown in Figure 1.10b (here only the inverting stages are shown, since the rectifying stages are a mirror image of the inverting stages). The push-pull and L-type inverter/rectifier circuits tend to impose low current stress and high voltage stress on the switches [111] and therefore tend to find applications in high current and low voltage situations, e.g., 12V to 300V conversion using the L-type circuit in [112], and lower power applications in [113, 114].



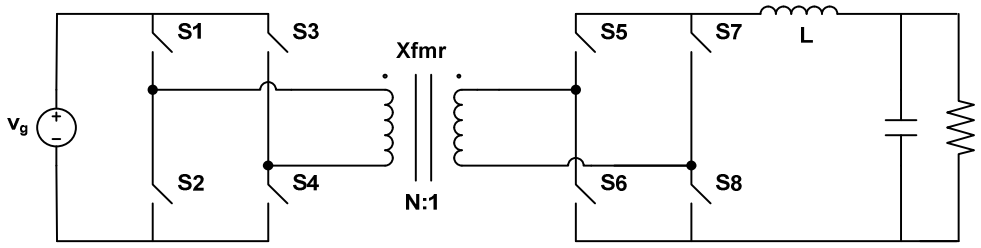
(a) Voltage-fed and current-fed topologies. **(b) Inverting stages.**

Figure 1.10. Topologies of bi-directional DC-DC converters [111].

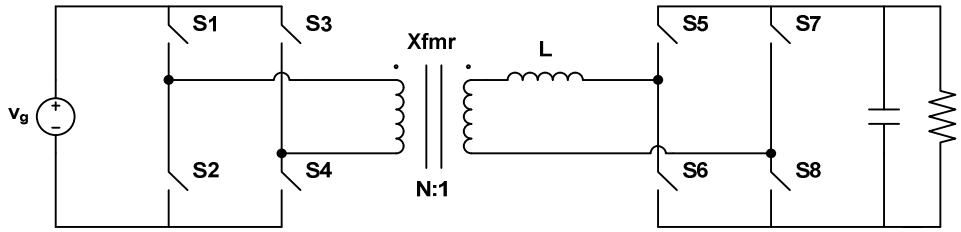
Voltage-fed and current-fed full-bridges and their derivatives are widely used topologies. One example is shown in Figure 1.11a for a 1.5kW prototype [115], which is identified as impractical for high power applications due to the severe voltage transients occurring across the devices on the current-fed side of the circuit caused by circuit parasitic elements

[111]. To address this issue, passive snubber circuits are added in the same circuit in [116], and active clamp circuits are added in [117].

Another widely used topology is the dual-active-bridge (DAB) converter, which is voltage-fed on both sides of the converter. To ensure controllable power transfer, a leakage inductance or external inductor is required in the AC transformer stage, L, Figure 1.11b. The two full-bridges are controlled to generate AC waveforms of the same frequency which are then applied on the transformer and the leakage inductance. By introducing a phase-shift between the AC waveforms, power flow is created between the two full-bridges which is always from the leading bridge to the lagging bridge [118].



(a) Voltage-fed input, current-fed output isolated converter.



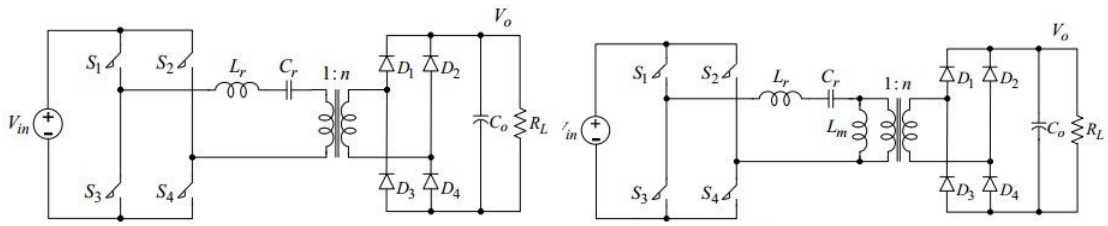
(b) Dual-active-bridge converter.

Figure 1.11. Two isolated converter circuit diagrams.

However, there are a number of technical difficulties with the DAB converter including: high reactive power flow through the transformer, unsuitable for wide voltage range applications, potential transformer saturation, and it also tends to suffer from low efficiency at light load. The work in [119] tries to reduce the reactive power in the transformer so as to reduce conduction losses and switch stresses. The authors in [120-123] propose a multi-phase DAB converter to increase the overall power capability and reduce switch stress. [124] uses 20 DAB converter modules to form a 20kVA solid-state-transformer. To increase converter efficiency, a number of researchers have investigated more advanced modulation techniques, including: traditional phase-shift control plus PWM [125], dual phase-shift control [126, 127], hybrid modulation techniques to improve efficiency and controllability at light load conditions [128, 129], and more complex

modulation techniques designed to achieve optimal efficiency, [130] and [131]. To overcome the potential transformer saturation problems, [132] introduces air gaps in the transformers; [133] uses a dual leakage inductance and variable frequency modulation; whereas [134] proposes an active flux balance control using a 'magnetic ear' to monitor the flux density of the transformer.

As in non-isolated converters, soft-switching can be achieved in isolated converters by using zero voltage switching (ZVS), zero current switching (ZCS), or a combination of both. Some isolated converters naturally exhibit ZVS, for example, the DAB converter due to the leakage inductance in the transformer, but the operating range over which ZVS may be achieved tends to be limited, therefore the work in [135] tries to improve the DAB converter efficiency by extending the ZVS range. An additional resonant LC network, or resonant switch network maybe introduced into the isolated circuits shown in Figure 1.10 for achieving soft switching, but often at the expense of increased conduction loss [92]. Two widely used resonant isolated configurations are the series resonant converter (SRC), and the inductor-inductor-capacitor series resonant converter (LLC-SRC) [136], Figure 1.12, which are shown in uni-directional configurations. The SRC circuit has the main drawback of poor light load efficiency and only buck function, while the LLC-SRC overcomes this problem by utilizing the transformer magnetizing inductance as resonant element as shown in Figure 1.12b.



(a) SRC converter. **(b) LLC-SRC converter.**

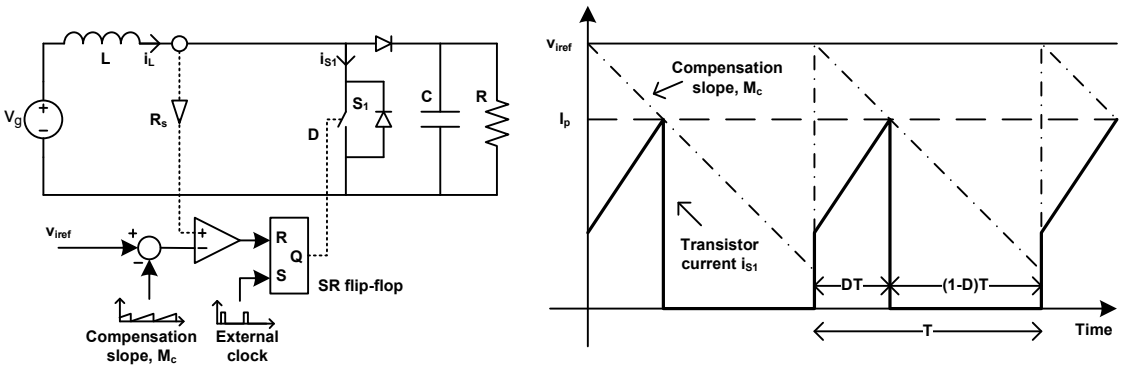
Figure 1.12. SRC and LLC-SRC converters [136].

1.2.3.3 Converter control methods

Direct open-loop control of power electronic converters involves setting the PWM switching signals with the duty ratio as required for a given steady-state operating condition. However, as the conditions vary, for example changes in load or input voltage, the original duty ratio may not provide satisfactory results. A feedback mechanism is

usually introduced to keep the circuit variables at the required levels, and small-signal transfer function analysis is typically undertaken to enable the optimal design of the controller and feedback loop. Among the various control variables, the output voltage is a common regulation target. A PI controller is commonly used for realizing feedback control, generally with satisfactory results, however sometimes a nested, faster, inner loop control is also implemented for improving dynamics.

Current programmed control is a technique that is widely used [137, 138], in which the converter is controlled by setting the peak transistor current [92]. A typical current control circuit for a boost converter is shown in Figure 1.13a, with its operating waveforms shown in Figure 1.13b. At the beginning of every switching cycle, the transistor turns on, triggered by the SR flip-flop due to the rising edge of the external clock signal. The current in the inductor then starts to rise, and this current is sensed through transducer gain R_s, then fed to a comparator circuit where a reference v_{iref} is set which turns off the transistor once the sensed current exceeds this reference. In this way, the peak current of the transistor is controlled by the reference v_{iref}, and the duty ratio is indirectly controlled. For stability purposes, a compensation slope is usually added to the comparator reference [139], as shown in Figure 1.13. This is necessary to prevent the phenomenon of sub-harmonic instability, normally when the duty ratio is greater than 0.5 [140].



(a) Peak current control circuit. **(b) Peak current control waveforms.**

Figure 1.13. Peak current control.

The current control circuit in Figure 1.13 can be extended to multiple phases, with a separate control circuit for each phase but sharing the same reference v_{iref} so as to distribute the current equally among the different phases. For interleaved circuits, the clock signal and compensation slope signals are interleaved as well, as shown in [141].

With the recent advances in microcontrollers and digital signal processors, a growing interest has been developed in using digital controllers for power converter applications. Traditionally analogue controllers have been used for high frequency DC-DC converters due to their inherent speed, however, digital controllers of appropriate speed are now becoming available and offer many advantages over their analogue counterparts, including better noise immunity, reduced sensitivity to parameter variations, and flexibility to realize complex control [142, 143].

1.2.3.4 Emerging semiconductor devices

A new generation of power semiconductor devices is starting to appear which use new materials, the most mature technologies being Silicon Carbide (SiC) and Gallium Nitride (GaN). A recent review [144] compares these technologies, and suggests these devices offer attractive characteristics for high frequency, high voltage, and high temperature applications. A brief summary of these features in comparison with established Silicon (Si) based devices is shown in Figure 1.14.

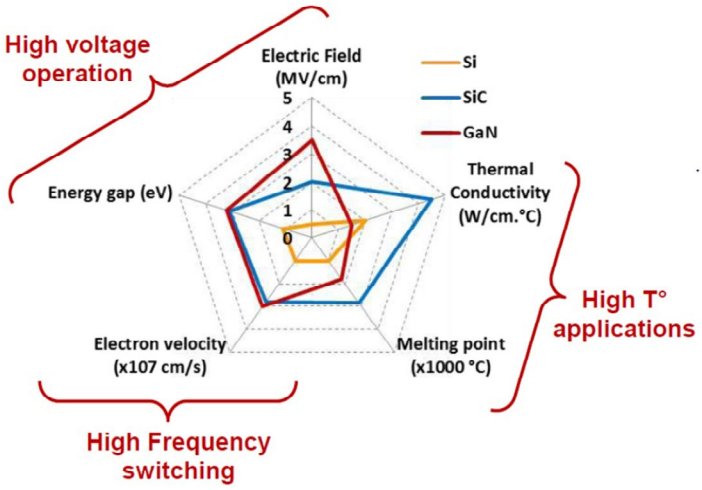


Figure 1.14. Comparison of Si, SiC and GaN semiconductor devices [145].

One example of using these new devices is presented in [146] , where the operation of a 50kW, 75kHz all-SiC converter is compared with that of an IGBT-based silicon converter at 25kHz, each providing 600V output. The results show that the overall losses with SiC devices are 40% less than that of the Si converter and a component weight reduction of 27% is achieved, due to the reduced switching losses, higher switching frequency and reduced inductor size.

1.2.4 Simulation methods

With the recent advances in computing power and memory, the simulation of an electrical circuit or even a complex electrical system has become easier and faster. In this section, the features of several simulation packages including MATLAB, Simulink and Saber are described, while a relatively new simulation concept of Hardware-in-the-loop (HIL) is also discussed.

1.2.4.1 Software simulation

There are many simulation packages on the market, including electronic circuit simulators like Multisim, PLECS, Saber, PSIM, SPICE, PSCAD, each specializing in specific applications. Beyond electrical and electronic circuits, MATLAB and Simulink are widely used for many applications because of their powerful numerical calculation and algebra manipulation capability [147].

In [141], a piece of program is written using MATLAB to evaluate numerically the behaviour of a DC-DC converter, although MATLAB cannot easily be used to model the detailed switching behaviour of a power semiconductor device. Integrated with MATLAB. Simulink is a block diagram environment for multi-domain simulation and model-based design [148] with an important benefit of using Simulink is the additional tool boxes that can be added for facilitating the modelling process.

In constrast, Saber is a powerful specialized circuit simulator for modelling and simulating physical systems, with a focus in power electronics and mechatronics systems [149]. The benefits of Saber are mixed mode system capability (analogue circuitry, digital circuits, magnetic systems) [150], the good convergence characteristic, high accuracy, high speed of simulation, the visualization of circuit structure and the ability to create additional electrical components using MAST or VHDL language. In [151], the author describes a detailed IGBT model which is experimentally verified; research work in [152] experimentally validates a detailed reversely switched dynistor (RSD) model.

The choice of simulation packages is a compromise between simulation accuracy and speed. For the converter simulation, Saber software is appropriate since it can more easily realize detailed converter models for switching cycle waveform analysis. The simulation

work to examine the ESS behaviour and its interaction with the electrical system requires much longer simulation times with a simpler modelling requirement, which makes Simulink an appropriate choice due to its faster simulation time with acceptable accuracy.

1.2.4.2 Hardware-in-the-loop simulation

Originating in the aviation industry around 15 to 20 years ago [153], hardware-in-the-loop (HIL) techniques provide a way of developing and validating a sub-system that forms part of a much larger system, without needing the complete physical system. For example, the development and testing of an engine controller for a large gas engine without requiring the engine itself and all the associated infrastructure and ancillary services which would be needed to run a real engine.

A widely used real-time platform for HIL applications is the dSPACE system, which is a commercial tool for developing electronic control units (ECU) [154] in automotive applications [21, 155] and aerospace applications [26]. Other manufacturers also produce HIL simulation platforms, for example, Applied Dynamics International (ADI) [156], National Instruments (NI) [157] and Opal-RT [158]. For the application in [159], two NI simulation platforms are used, one for the controller, the other for the vehicle and energy storage system, where physical signal cables are connected between the two controllers for control and feedback. Another interesting HIL system made by McLaren [160] provides the complete functionality of an F1 racing car to simulate the running of the car, i.e., engine start, pull away and gear shifting.

One of the most common and straightforward ways to program a HIL system is to use the well supported Simulink embedded system tool box, since ‘drag and drop’ modules can be used for rapidly constructing a model. The constructed model is then automatically compiled into machine language by the embedded system tool box and downloaded to the real-time HIL platform to emulate the behaviour of the target system. In this project, two commercial HIL systems, the ADI system, and the dSPACE system were used, with the former controlling the active loads, and the latter in fast and easy prototyping an energy storage system controller.

1.3 Summary of literature review

The increasing use of electrical technologies within on-board power systems is resulting in complex and highly dynamic networks in which energy storage devices have an important role to play, for example to resolve the instantaneous mismatch between load demand and power availability or to provide the flexibility to optimise overall performance. Among the various energy storage devices, fuel-cells, batteries and super-capacitors are well-suited to on-board applications because of their portability and high power or energy density; however their differing characteristics often result in combinations of dissimilar devices being used within a system.

Regarding the energy management strategies, there is no optimal solution applicable to all events, since each event has different goals. While a great number of strategies focus on improving efficiency, fewer researchers have investigated the availability of energy storage when subject to load variations, and the dynamic performance of the main power source in an electrical system with an ESS. In addition, the highly dynamic load on aircraft electrical systems requires system stability and safe operation to be the first priority instead of efficiency. To realize these goals, a hierarchial two-level control is necessary, with a low level current (or power) control, and a high level rule-based or similar supervisory control method.

The transformer in isolated DC-DC converters implies additional cost and losses, when compared with non-isolated DC-DC converters which often have less number of switches and simpler structures, making them lighter, smaller and more efficient. To minimise system weight, modular DC-DC converters with interleaved topologies are often preferred for interfacing energy storage devices in on-board applications, creating a number of inter-related control challenges: the modelling and control of the individual converters over the wide operating ranges required by energy storage devices, and the management and coordination of storage devices at system level, for example to optimise load sharing, state-of-charge and overall power quality. Current programmed control and feed-forward control are widely used techniques which ensure fast dynamic response, which are implemented in this thesis for low level converter control.

1.4 Scope of this thesis

This chapter has presented the background of the energy storage system (ESS), a brief introduction of the use environment of the ESS, the IEPNEF, together with the objectives of the research and the literature review.

Chapter 2 presents the bi-directional dual-interleaved half-bridge converter, an important interface for an energy storage system. The converter is analysed especially in the discontinuous conduction mode (DCM), to understand the different operating patterns and the overall conversion characteristics. The simulation and experimental validation of the analysis are also provided.

Chapter 3 presents a detailed model of a super-capacitor based energy storage system and associated controller. The design and performance of the controller are examined through simulation and within the IEPNEF lab using an emulated ESS.

In Chapter 4, an advanced ESS controller is proposed, simulated and validated experimentally within the IEPNEF lab. The proposed controller focuses on limiting the rate-of-change in the main source power whilst managing the useable energy of the ESS. A real super-capacitor based ESS was used in the experiments replacing the emulated ESS used in Chapter 3.

Chapter 5 presents the conclusions, contributions of the research and suggestions for further work.

Chapter 2 Dual-interleaved converter with interphase-transformer

2.1 Introduction

This chapter is concerned with the use of the bi-directional dual-interleaved converter (DIC) with an interphase transformer (IPT) as an interface between a super-capacitor energy storage bank and a fixed voltage DC bus.

In particular, a detailed analysis is undertaken to establish the various operating modes which occur under discontinuous current conditions within the IPT and to derive the boundary conditions between the different operating regions. Based on this analysis, general expressions are determined for the average and peak values of the inductor current, and these expressions are used to plot a set of discontinuous mode conversion characteristics.

The discontinuous mode operating patterns and conversion characteristics are validated by Saber simulations and experimental data from high power converters. In the following sections, the boost mode is considered first, then the buck mode.

The dual-interleaved bi-directional converter (Figure 2.1) consists of a filter inductor (L_f), a 1:1 turns ratio interphase transformer (IPT), a full-bridge circuit containing four switching devices (A1, A2, B1, B2) and their anti-parallel diodes (AD1, AD2, BD1, BD2), and filter capacitors C_1 and C_2. The splitting of the filter inductor and the IPT allows different core materials used to reduce core losses, as the filter inductor has a biased DC flux in operation, while the IPT has a large AC flux swing with zero bias[50].

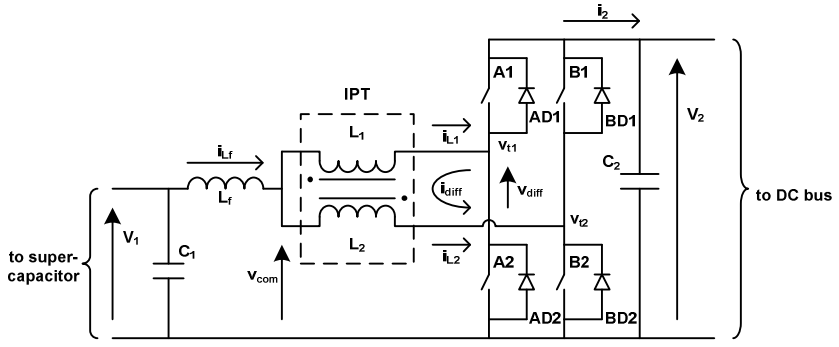


Figure 2.1. Circuit diagram of the converter.

The two half-bridge switches comprise two individual boost/buck cells which operate in an interleaved manner with equal duty ratios (switch on-time to period ratio), i.e., one half-bridge is delayed behind the other by half a cycle.

The IPT is assumed to consist of two perfectly inversely coupled inductors L_1 and L_2 which have equal values. Therefore the total inductance of the IPT between the ends of the windings, points v_{t1} and v_{t2} in Figure 2.1, is $4L_1=4L_2$ (details explained in Appendix A.1) and is denoted L_{diff}, the differential inductance [50].

The filter inductor current i_{Lf} is assumed to divide equally between the two halves of the IPT due to the operation of a current mode controller, which is composed of the common mode component, $i_{Lf}/2$, of the two winding currents. The total phase currents i_{L1} and i_{L2} are given in Equation (2.1).

$$\begin{aligned} i_{L1} &= i_{Lf}/2 - i_{diff} \\ i_{L2} &= i_{Lf}/2 + i_{diff} \end{aligned} \tag{2.1}$$

where i_{diff} is the differential current in the IPT which is produced by voltage v_{diff} across the differential inductance L_{diff}, and $v_{diff}=v_{t1}-v_{t2}$.

The analysis in this chapter assumes lossless components, instantaneous switching, and that the DC terminal voltages are constant across a switching cycle due to the relatively large filter capacitors, C_1 and C_2.

2.2 Boost Mode Operation

In boost mode, V_1 is the low voltage side input voltage and V_2 is the high voltage side output voltage. The top two switches A1 and B1, in Figure 2.1 are permanently off. The bottom two switches A2 and B2 are controlled by two PWM signals of equal duty ratio that are phase-shifted by a half switching cycle, which in practice would be determined by a form of current mode control to ensure equal currents in the two halves of the IPT.

2.2.1 Continuous conduction mode (CCM)

In continuous conduction mode (CCM), none of the currents in the filter inductor or the windings of the IPT drop to zero. This means that at any time, a switching device (or diode) must conduct in each leg. Figure 2.2 summarizes all the possible circuit states in the CCM as follows:

1. both switches (A2 and B2) are on, sub-circuit 1;
2. both switches are off, but both upper diodes are conducting, sub-circuit 2;
3. only one switch is on (A2), and the top right diode (BD1) is conducting, sub-circuit 3;
4. only one switch is on (B2), and the top left diode (AD1) is conducting, sub-circuit 4;

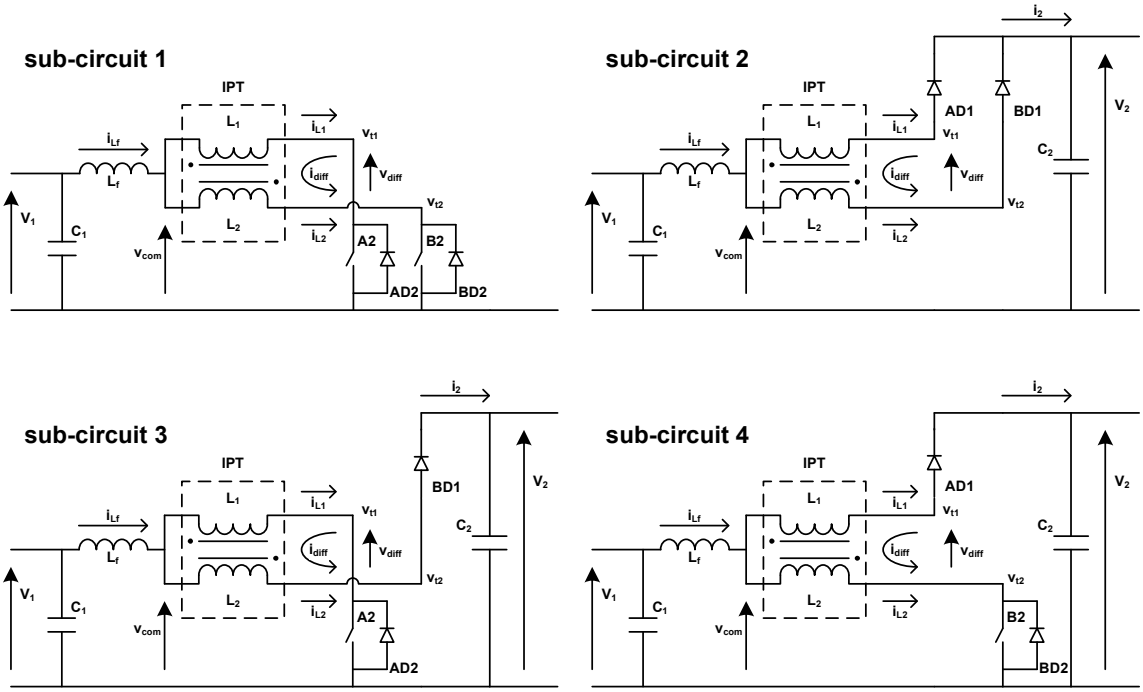


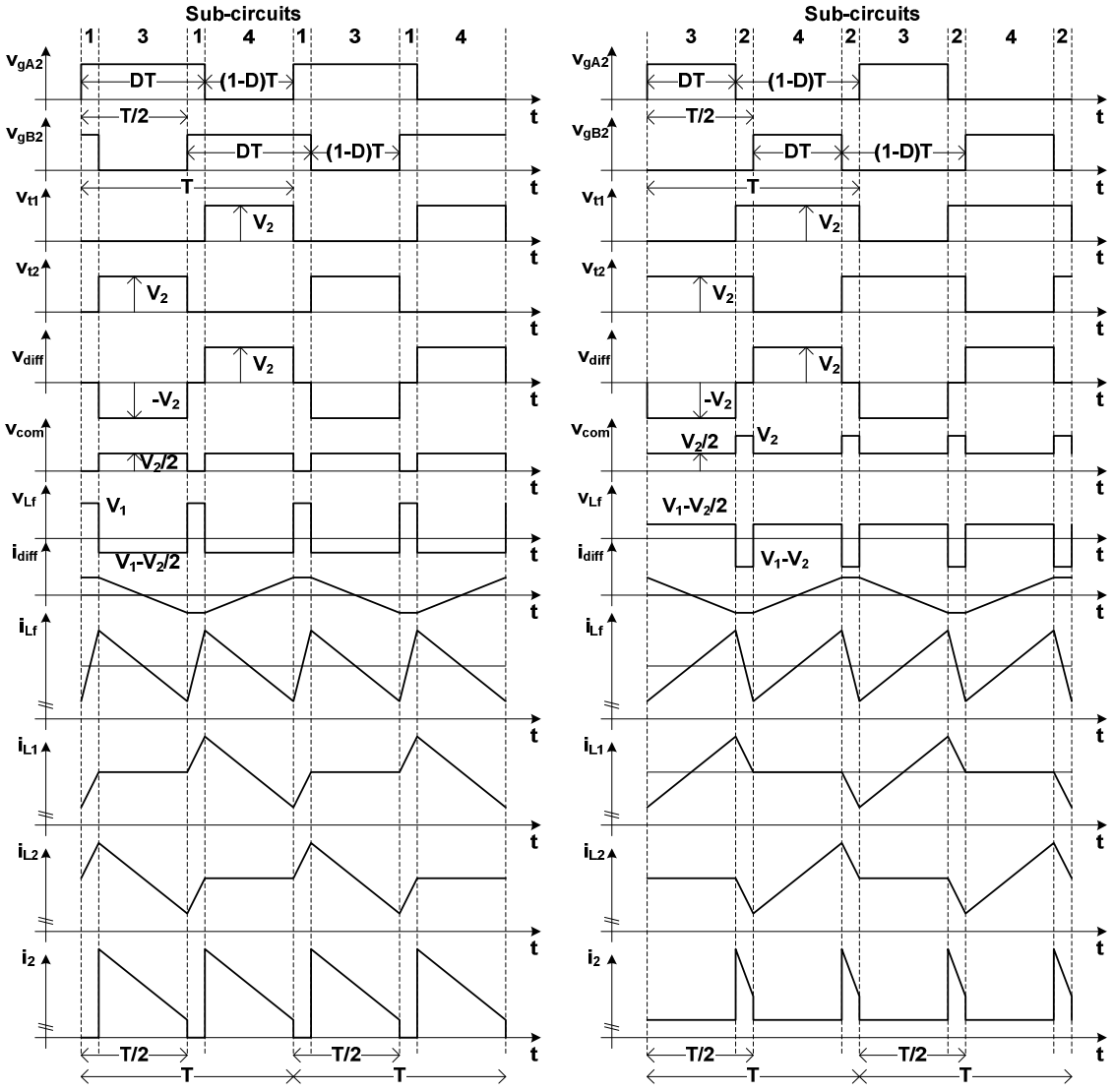
Figure 2.2. Sub-circuits in CCM boost mode.

Depending on the duty ratio D, these sub-circuits may appear in different sequences within a switching cycle, as illustrated in the waveforms in Figure 2.3, which show operation with D>0.5 on the left and D<0.5 on the right. The sub-circuits are marked along the top of the waveforms.

The gate voltage signals are labeld v_{gA2} v_{gB2}, which reflects the duty ratio. The voltages v_{t1} and v_{t2} switch between zero and the output voltage V_2 according to the state of devices A2 and B2, and the differential voltage v_{diff} is a quasi-squarewave of $\pm V_2$. Correspondingly, the voltage v_{com} at the central tap of the interphase transformer will be equal to zero when

both bottom switches are on (sub-circuit 1); equal to V_2 when both upper diodes are conducting (sub-circuit 2); and equal to half of the output voltage $V_2/2$ when only one bottom switch is conducting (sub-circuits 3 and 4), due to the inductive voltage divider formed by the IPT windings.

The voltages applied to the IPT ($v_{diff}=v_{t1}-v_{t2}$) and the filter inductor ($v_{Lf}=V_1-v_{com}$) produce the ripple current in i_{diff} and i_{Lf}. The phase currents of the IPT, i_{L1} and i_{L2}, satisfy Equation (2.1) and have a half cycle shift.



(a) D>0.5. **(b) D<0.5.**

Figure 2.3. Operating waveforms in CCM boost mode.

From Figure 2.3, it is seen that sub-circuit 1 only occurs for D>0.5 and sub-circuit 2 only occurs when D<0.5. A special case occurs when D is exactly 0.5 and neither the sub-circuits 1 or 2 are present. Under these conditions, v_{com} is perfectly smooth and equal to $V_2/2$, the inductor current i_{Lf} is ripple free and only i_{diff} causes a variation in i_{L1} and i_{L2}.

According to the sizes of the filter inductor L_f and the IPT differential inductance L_{diff} and also the value of duty ratio, several patterns of the phase current waveforms are possible as shown in Figure 2.4, with the main noticeable difference being the slopes of the phase currents during sub-circuit 3 (D>0.5) and 4 (D<0.5). Although these waveforms look similar in the CCM, i.e., having the same switching sub-circuit sequences, they give rise to different patterns of operation in the DCM, which shall be discussed in the following sections.

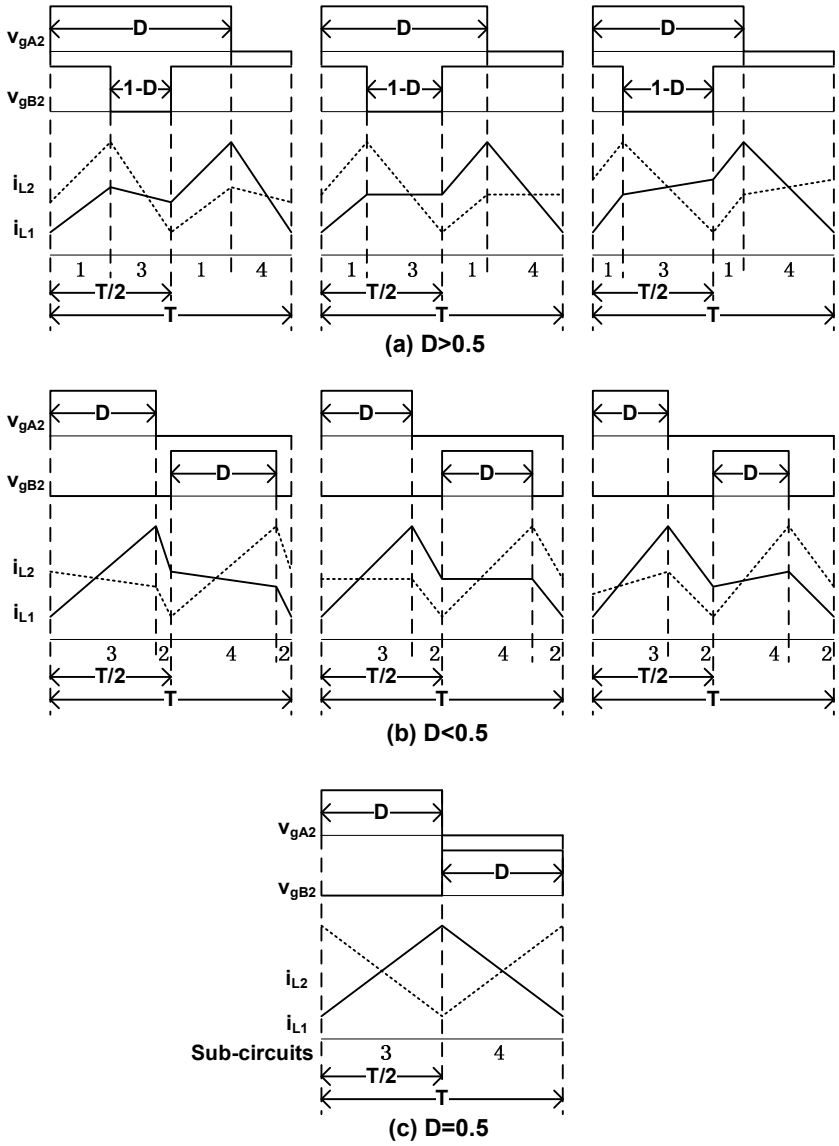


Figure 2.4. Phase currents waveforms in CCM boost mode.

Despite the operating pattern, the voltage ratio $M=V_1/V_2$ can be derived by equating the positive and negative inductor volt-seconds of v_{Lf} for the conditions of $D>0.5$ or $D\leq 0.5$, giving:

$$M = \frac{V_1}{V_2} = 1 - D \tag{2.2}$$

Equation (2.2) is identical to the expression for a single-transistor boost converter operating in continuous conduction mode.

2.2.2 Discontinuous conduction mode (DCM)

The discontinuous conduction mode occurs in the interleaved boost converter when the currents in the windings of the IPT fall to zero and remain at zero for a part of each switching cycle. This normally occurs at lower levels of power throughput since the DC components of the current waveforms are reduced. Although the DCM operation can be avoided by using complimentary switching where current would be negative, this sacrifices the control resolution when using a peak current controller, since a lower average current would be produced with the same peak current reference as used in normal switching.

The conditions for the continuous mode occurring were derived in [50] using a resistive load, and from an analysis of the waveforms in Figure 2.4 may be expressed as:

$$\frac{2L_f}{RT} > \begin{cases} (1-D)D\left(\frac{1}{2} - D + \frac{2}{L_r}\right) & for\ D \leq 0.5 \\ (1-D)^2\left(D - \frac{1}{2} + \frac{2}{L_r}\right) & for\ D > 0.5 \end{cases} \tag{2.3}$$

where R is the effective load resistor connected to the high voltage terminals, voltage V_2, and L_r is the inductor ratio L_{diff}/L_f.

However, the analysis in [50] did not examine the detailed patterns of behaviour in the discontinuous mode and this is the topic of the following sections.

In the discontinuous mode, the four CCM circuit configurations in Figure 2.2 are augmented by the four additional configurations in Figure 2.5 as follows:

5. bottom left branch (A2, AD2) conducting, the other branch current being zero;
6. bottom right branch (B2, BD2) conducting, the other branch current being zero;
7. top left diode (AD1) conducting, the other branch current being zero;
8. top right diode (BD1) conducting, the other branch current being zero.

A further configuration is possible in which there is no current flow in either branch. This sub-circuit is denoted as sub-circuit 0, but is not drawn.

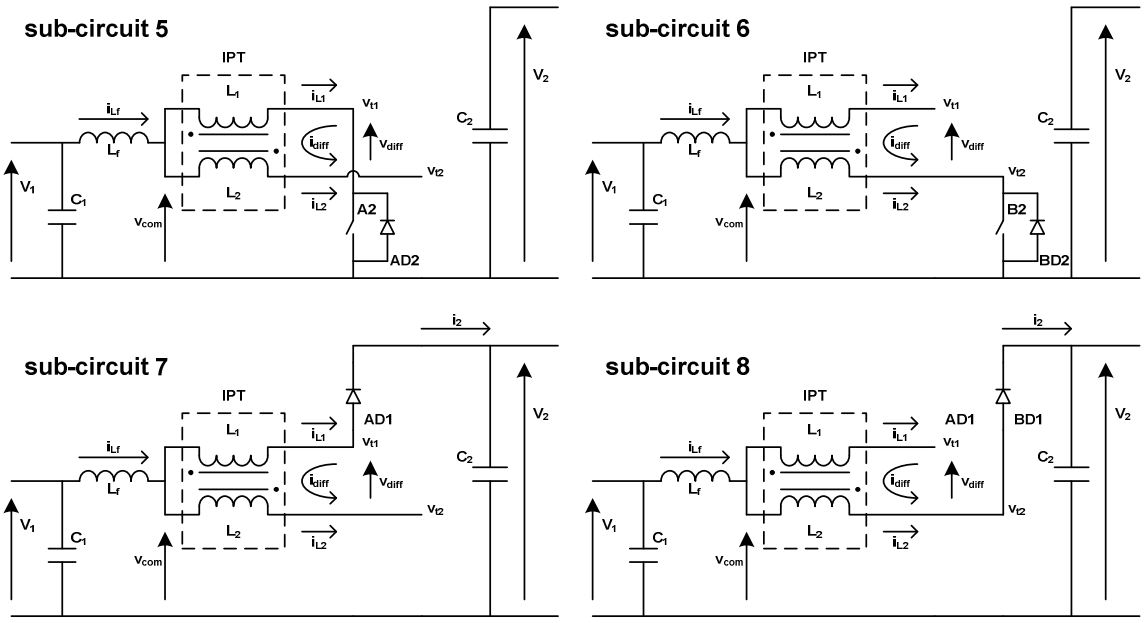


Figure 2.5. Additional four sub-circuits appearing in DCM operation, boost mode.

In order to understand the conditions under which these DCM sub-circuit arise, the voltage on the non-conducting terminal of the IPT (v_{t1} or v_{t2}) is analysed, and the condition for the voltage to fall within the range zero to V_2 is identified. If a solution exists for the IPT terminal voltage within the range of zero to V_2, the associated sub-circuit may occur in the DCM at that operating point, however, if there is no solution for the IPT terminal voltage in the range of zero to V_2, the respective circuit cannot occur.

By considering the conducting half of the IPT and the filter inductor as a voltage divider, an expression may be derived for the voltage on the non-conducting IPT terminal as shown in Table 2.1 (derivation details given in Appendix A.2).

Table 2.1. Terminal voltages v_{t1} and v_{t2} in different DCM sub-circuits

	Sub-circuits			
	5	6	7	8
v_{t1}	0	$\frac{2L_r}{L_r+4}V_1$	V_2	$\frac{2L_rV_1-L_rV_2+4V_2}{L_r+4}$
v_{t2}	$\frac{2L_r}{L_r+4}V_1$	0	$\frac{2L_rV_1-L_rV_2+4V_2}{L_r+4}$	V_2
Existence conditions	M<0.5+2/Lr	M<0.5+2/Lr	M>0.5-2/Lr	M>0.5-2/Lr

The solution for v_{t1} in sub-circuits 5 and 7 are trivial due to the conduction of the transistor A2 and the diode AD1 respectively, and similarly for v_{t2} in sub-circuits 6 and 8. Since the non-trivial solutions for v_{t1} and v_{t2} must lie in the range of zero to V_2 for a particular sub-circuit to exist, this gives rise to a set of necessary but not sufficient conditions for each sub-circuit to occur as listed in Table 2.1.

For example for sub-circuit 5 to occur requires:

$$0 < v_{t2} < V_2 \tag{2.4}$$

Substituting for v_{t2}:

$$0 < \frac{2L_r}{L_r+4}V_1 < V_2 \tag{2.5}$$

Neglecting the lower inequality since it will always be satisfied for positive V_1 results in :

$$\frac{V_1}{V_2} = M < 0.5 + 2/L_r \tag{2.6}$$

The existence conditions in Table 2.1 for the sub-circuits begin to define a number of operating regions in the DCM mode in which a particular sub-circuit sequence will occur. Three regions of voltage ratio M are therefore identified from Table 2.1:

1. 0<M<0.5-2/Lr (sub-circuits 5 and 6 may exist)
2. 0.5-2/Lr<M<0.5+0.5+2/Lr (sub-circuits 5, 6, 7 and 8 may exist)
3. 0.5+2/Lr <M<1 (sub-circuits 7 and 8 may exist)

Through thorough analysis of the waveform patterns in the DCM, the operating regions of the converter may be further broken down as summarised on the M against D graph in Figure 2.6, where each region has the same sub-circuit sequence.

In Figure 2.6, the thick line represents the CCM operation defined by Equation (2.2), whereas the triangular area below that line is the DCM region. However, in practice, the region close to M=0 would not be valid since a inifinte voltage will appear at V_2. Here the analysis only assumes the ideal condition.

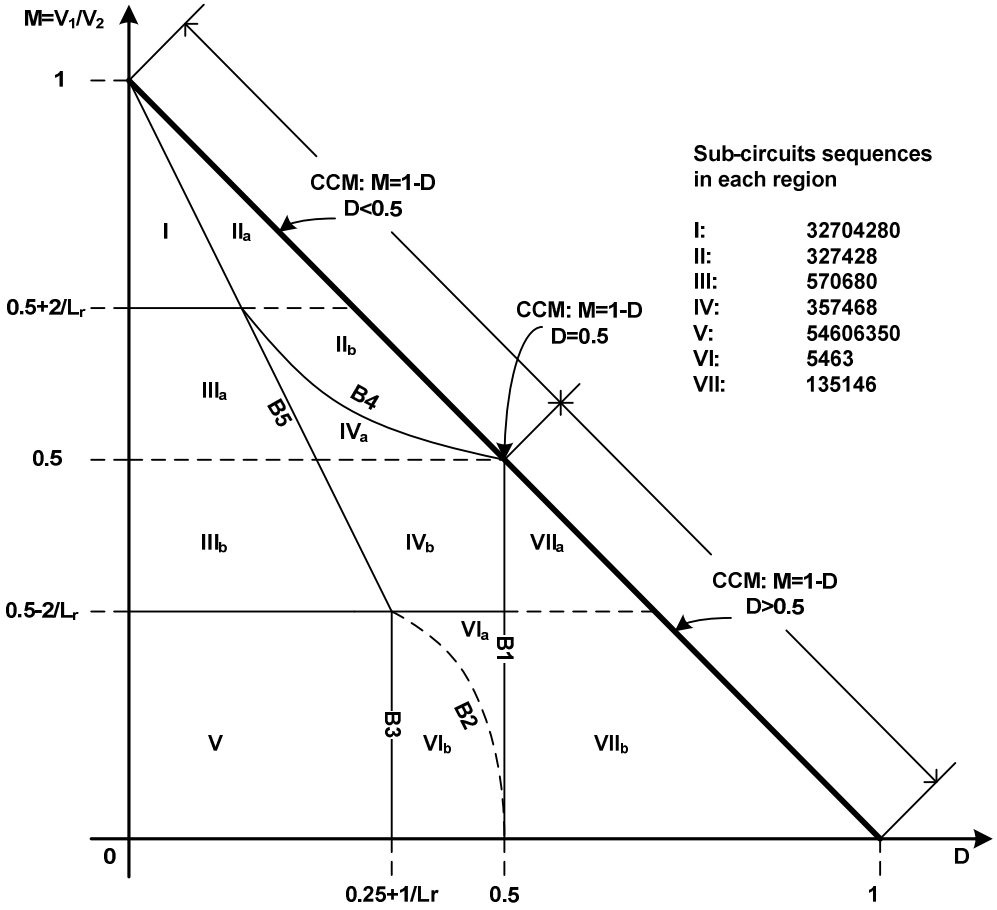


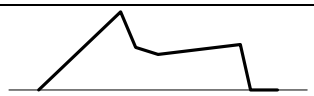
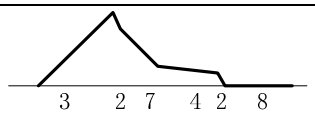
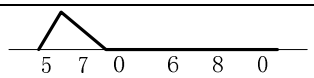
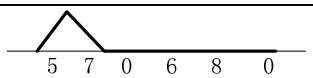
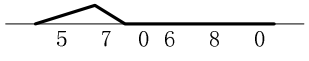
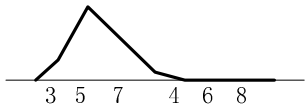
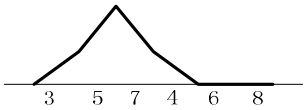
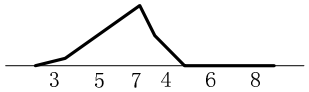
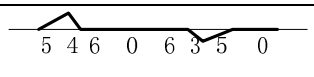
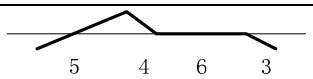
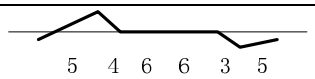
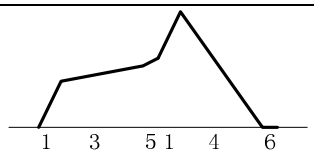
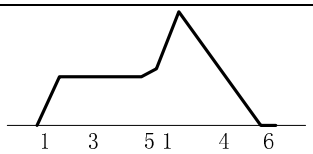
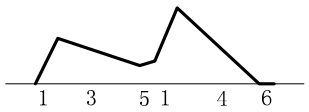
Figure 2.6. DCM operating regions in boost mode.

The DCM operation area in Figure 2.6 is divided into seven major regions labelled as I to VII, represented by the different characteristic waveforms of phase current i_{L1} shown in Table 2.2 which were observed and validated by Saber simulation. Some of these regions are divided into two sub-regions due to slight variations in current slopes, but the sub-circuit sequence is unchanged and the associated waveforms are in the corresponding rows in Table 2.2, denoted by sub-scripts 'a' and 'b'. Table 2.2 also shows the characteristic waveforms on the boundaries between the sub-regions. Moving from a sub-region with

sub-script ‘a’ to the associated sub-script ‘b’ sub-region corresponds to a reduction in voltage ratio M and the variation in waveform shape is indicated by the rows in Table 2.2.

The boundaries between the seven major regions are either the M boundaries previously identified by the existence conditions of sub-circuit 5&6 and 7&8 in Table 2.1, or ones which depend upon duty ratio D.

Table 2.2. DCM waveforms in different regions

Regions	Characteristic phase current waveforms		
	a	Boundary	b
I			
II			
III			
IV			
V			
VI			
VII			

The mathematical expressions for the D-dependent boundaries were determined through detailed analysis of the phase current waveform at the region boundaries and by equating the net increase in phase current in a cycle to zero. This analysis step is summarised by the general expression:

$$\sum_{k=1}^{n} \frac{di_{L1[k]}}{dt} \cdot \Delta t_{[k]} = 0 \tag{2.7}$$

where n is the total number of sub-circuits that the converter goes through within a cycle, $di_{L1[k]}/dt$ is the phase current rate of rise in the k_{th} sub-circuit (derived in Appendix A.3), and $\Delta t_{[k]}$ is the duration of the k_{th} sub-circuit (which can be expressed as a function of D).

The detail of the analysis is included in Appendix A.4 and the final expressions for the boundaries are listed in Table 2.3 and are drawn in Figure 2.6.

Table 2.3. Summary of DCM boundary duty ratios in boost mode

Boundary duty ratios				
B1	B2	B3	B4	B5
$D = 0.5$	$D = \frac{(2M-1)(4+L_r)}{2(2L_rM - L_r - 4)}$	$D = 0.25 + 1/L_r$	$D = \frac{4(1-M)}{2L_rM - L_r + 4}$	$D = \frac{1-M}{2}$

The operating regions in Figure 2.6 and the boundaries in Table 2.3 are based on the assumption that the inductance ratio L_r is larger than 4, since the vertical ($0.25+1/L_r$) and horizontal boundaries ($0.5 \pm 2/L_r$) labelled in the figure have to be within the limit of (0,1). However, as L_r reduces below 4, the horizontal region boundaries in the M:D plane of Figure 2.6 move towards and pass the limits of M=0 and 1. Under these conditions, the DCM operation is simpler and there are only three regions, III, IV and VII_a.

2.2.3 Saber simulation validation

The analysis of the DCM mode patterns has been confirmed by extensive simulation using Saber with different circuit parameters covering all regions. Two examples are presented, Figure 2.7 and Figure 2.8, showing the transistor gate drive signals for A2 and B2, the IPT terminal voltages v_{t1} and v_{t2} (which are also the transistor collector-emitter voltages), the phase currents i_{L1} and i_{L2}, and the filter inductor current i_{Lf}.

The simulation model used idealised components with virtually no conduction loss and very rapid switching times. The circuit parameters are listed in the figure title and are based on the practical converter that is used in Section 4.6. Capacitors C_1 and C_2 were omitted from the simulations since the terminal voltages V_1 and V_2 were set by ideal voltage source/sink elements. The converter model contains a peak current mode controller (Figure 1.13) to ensure equal current sharing between the two halves of the IPT. The detailed Saber circuit diagram is given in Appendix A.5.

In Figure 2.7, the input voltage is V_1=200V, the voltage ratio M is 200/540=0.37 and the duty ratio is 0.6. The horizontal M boundaries in Figure 2.6 are then 0.5+2/L_r=0.53 and 0.5-2/L_r=0.47, therefore with D=0.6 and M=0.37, the converter will be working in region VII_b of the DCM region map in Figure 2.6. Correspondingly, the waveform shape and the sub-circuit sequence (135146) in Figure 2.7 match the expectation for region VII_b according to the summary in Table 2.2. The terminal voltages v_{t1} and v_{t2} exhibit periods when the voltage settles to an intermediate level between zero and V_2=540V, 378.55V in this case, due to the non-conducting IPT winding in sub-circuit 5 or 6. The predicted values of v_{t1} and v_{t2} in the discontinuous sub-circuits, listed in Table 2.1, accurately predict the values observed in simulation, which is $2L_rV_1/(L_r+4)$=378.86V compared with 378.55V in the simulation.

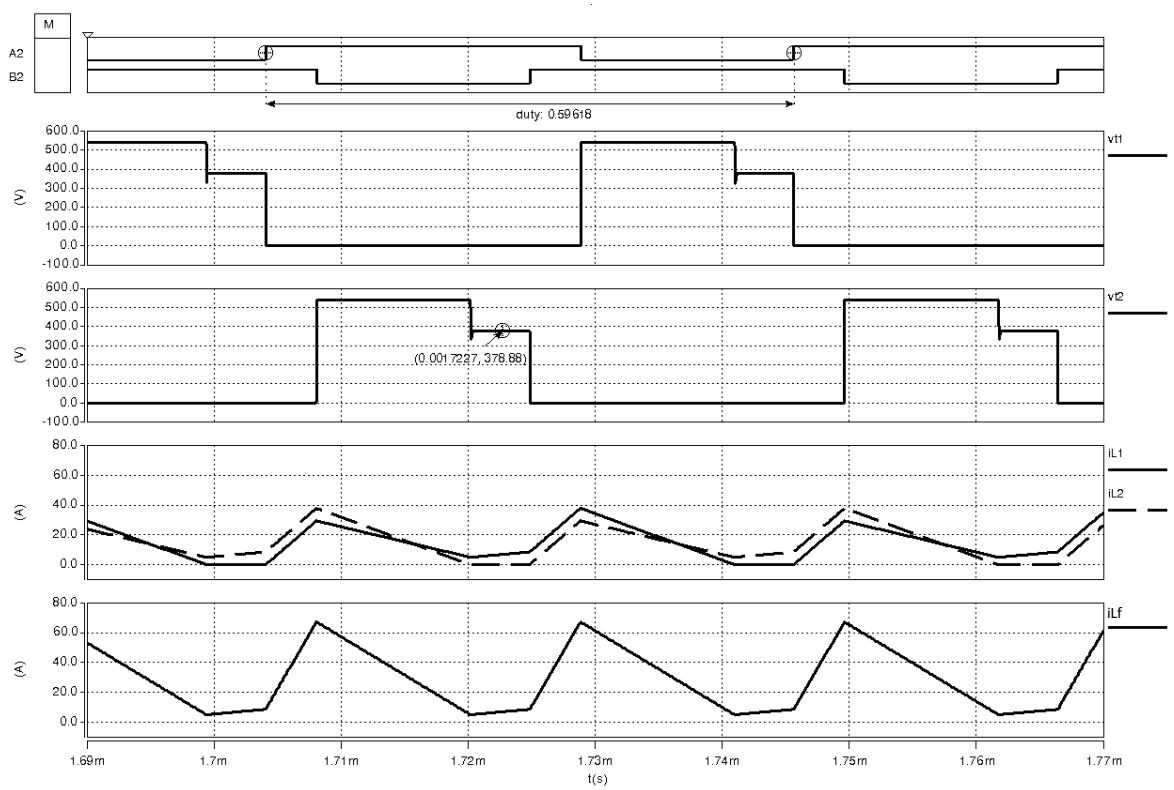


Figure 2.7. Saber simulation waveforms in boost mode, V_1=200V, V_2=540V, M=0.37, D=0.6, f=24kHz L_r=71.7, L_f=13.6uH, region VII_b.

Figure 2.8 shows the simulated operating waveforms, with M=0.509, D=0.34. Since the duty ratios on boundaries B5 and B4 in Figure 2.6 are (1-M)/2=0.246 and 4(1-M)/(2L_rM-L_r+4)=0.371 respectively (when M=0.509, Table 2.3), the converter will be working in region IV_a with the sub-circuit sequence of 357468. The v_{t2} voltages of 520.5V and 38.422V labelled in the figure occur during the discontinuous sub-circuits 5 and 7 respectively. This further confirms the operating pattern analysis of the converter in the DCM. Similar correspondence with Saber simulation has been observed over a wide range of conditions.

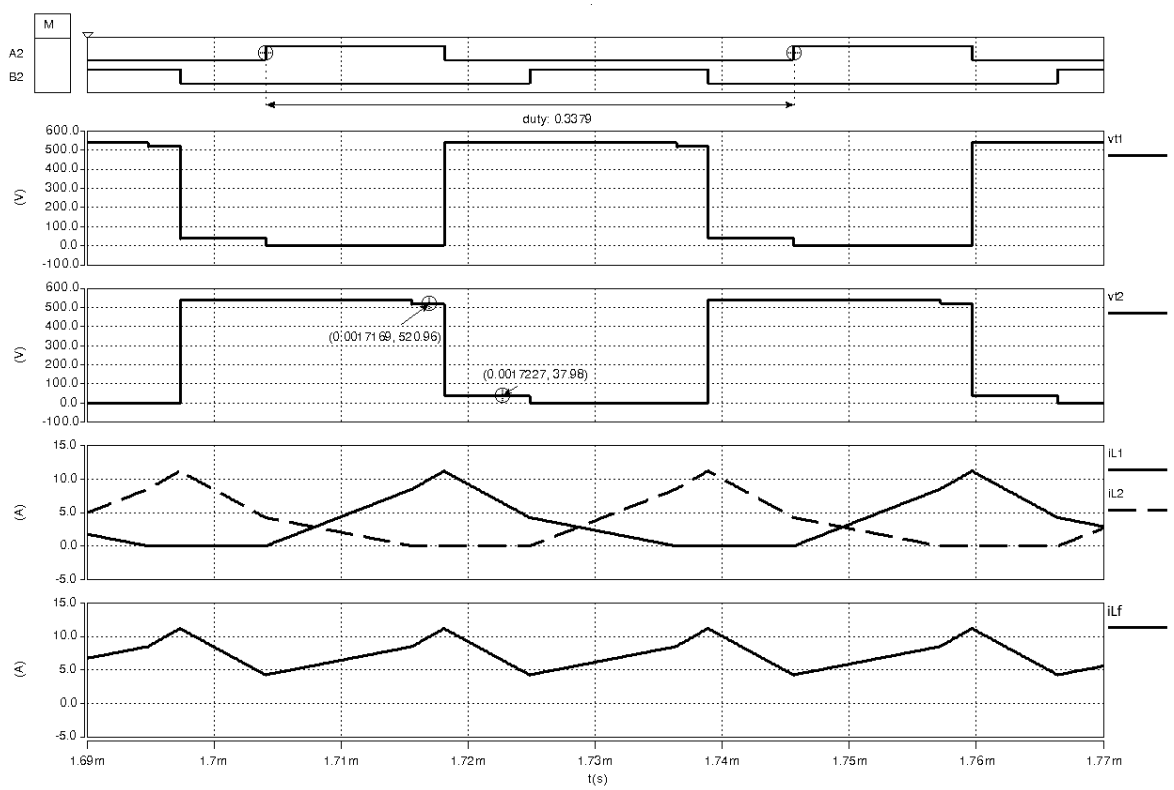


Figure 2.8. Saber simulation waveforms in boost mode, V_1=275V, V_2=540V, M=0.509, D=0.3, f=24kHz, L_r=71.7, L_f=13.6uH, region IV_a.

In both of the simulation examples, the inductor current i_{Lf} is seen to remain continuous even though the IPT phase currents are discontinuous; but compared with the CCM pattern in Figure 2.3, the current has a more complex shape.

However, the inductor current will become discontinuous when the operating pattern includes sub-circuit 0, which is when the two phases of the IPT currents i_{L1} and i_{L2} are simultaneously zero.

2.2.4 Peak phase current and average inductor current

By undertaking detailed analysis of the characteristic phase current waveform in each of the discontinuous operating regions, expressions may be derived for the peak values of the phase current $I_{L1\text{-}peak}$ or $I_{L2\text{-}peak}$, and the average filter inductor current $I_{Lf\text{-}avg}$, which is also the converter average input current in boost mode. The analysis is based on the generalised sketch of phase current i_{L1} shown in Figure 2.9.

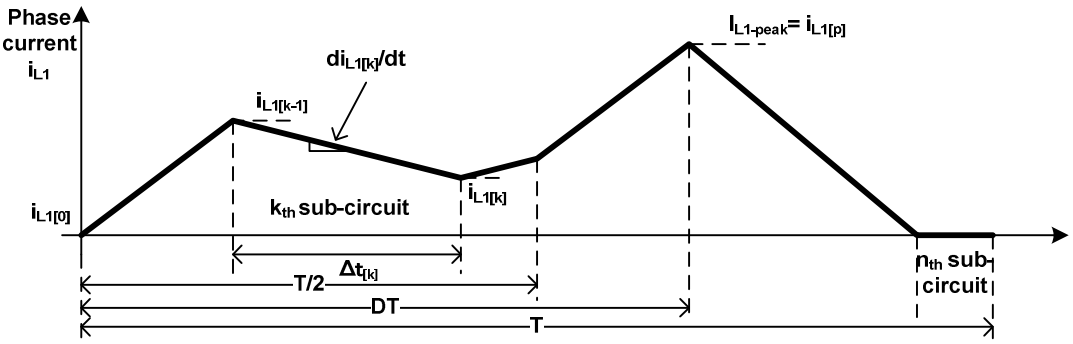


Figure 2.9. Illustration of defined variables, $i_{L1[k]}$, $\Delta t_{[k]}$.

The full expressions are listed in Appendix A.6 and the analysis procedure for each case may be summarised by starting from the general set of expressions for the values of the phase current i_{L1} at the end of the k_{th} sub-circuit stage $i_{L1[k]}$ within the switching cycle, Figure 2.9, Equation (2.8).

$$i_{L1[k]} = \begin{cases} 0 & k = 0 \\ \sum_{m=1}^{k} \frac{di_{L1[m]}}{dt} \cdot \Delta t_{[m]} & k \geq 1 \end{cases} \tag{2.8}$$

$i_{L1[0]}$ is the initial current and will be zero in discontinuous conduction mode except in region VI, whilst $\Delta t_{[k]}$ is the duration of the k_{th} configuration in a particular operating pattern.

The peak phase current $I_{L1\text{-}peak}$ is calculated as:

$$I_{L1-peak} = i_{L1}\Big|_{A2\,turns\,off} = i_{L1[k]}\Big|_{k=p} \tag{2.9}$$

where from inspection of Table 2.2, p=1 in regions I, II, III, V and VI_b, p=2 in region IV and VI_a, and p=4 in region VII.

The average input current $I_{Lf\text{-}avg}$ may be determined by doubling the average value of one of the IPT phase currents calculated across a switching period. Equation (2.10) provides a general expression for the calculation and the detail is summarised in Appendix A.6.

$$I_{Lf-avg} = 2 \cdot \frac{1}{T} \sum_{k=1}^{n} \frac{(i_{L1[k-1]} + i_{L1[k]})}{2} \Delta t_k \tag{2.10}$$

After obtaining the average inductor current expressions for each region using Equation (2.10), the characteristics of $I_{Lf\text{-}avg}$ against duty ratio D can be generated for a specific value of voltage ratio $M=V_1/V_2$. By considering a horizontal line in Figure 2.6 and collecting the average inductor current expressions for the regions that this horizontal line crosses, a piece-wise function is obtained taking the form of Equation (2.11). A similar approach may be used to obtain an expression for the peak current, Equation (2.12).

$$I_{Lf-avg}(V_1, V_2, D) = \begin{cases} I_{Lf-avg}\Big|_{region\ x_1} & (0 \le D < db_1) \\ \ldots & \\ I_{Lf-avg}\Big|_{region\ x_l} & (db_{l-1} \le D \le db_l) \end{cases} \tag{2.11}$$

$$I_{L1-peak}(V_1, V_2, D) = \begin{cases} I_{L1-peak}\Big|_{region\ x_1} & (0 \le D < db_1) \\ \ldots & \\ I_{L1-peak}\Big|_{region\ x_l} & (db_{l-1} \le D \le db_l) \end{cases} \tag{2.12}$$

where region x_1 to region x_l denote the DCM regions that the converter passes through as the duty ratio increases from zero to the CCM boundary (D=1-M). The range of D for each region, i.e. the values of boundaries db_1 to db_l may be determined through Figure 2.6 and Table 2.3.

In this way, altogether four piecewise functions are derived (Appendix A.6), representing the M ranges, (0 to 0.5-2/Lr), (0.5-2/Lr to 0.5), (0.5 to 0.5+2/Lr) and (0.5+2/Lr to 1).

Figure 2.10 shows the generalized current characteristics against duty ratio, where each curve is for a fixed value of voltage ratio M. The inductor current is normalized by using the base current $I_{base}=V_1T/L_f$ and the normalized current is defined as $I_{Lf\text{-}avg}'=I_{Lf\text{-}avg}/I_{base}$. The inductance ratio L_r is assumed to be larger than 4.

Three special cases are shown, which correspond to M=0.5-2/Lr, M=0.5 and M=0.5+2/L_r. Due to the form of Equation (2.11), each curve is split into sections by round dots to discriminate the different operating modes, which correspond to the DCM sub-regions previously defined in Figure 2.6. The vertical part of the curves indicate the CCM operation (in shadow) where any inductor current value above the minimum set by the DCM boundary may be achieved for a given value of D and M. The curved sections of the plots are parabolas due to the squared D terms in the average current expressions.

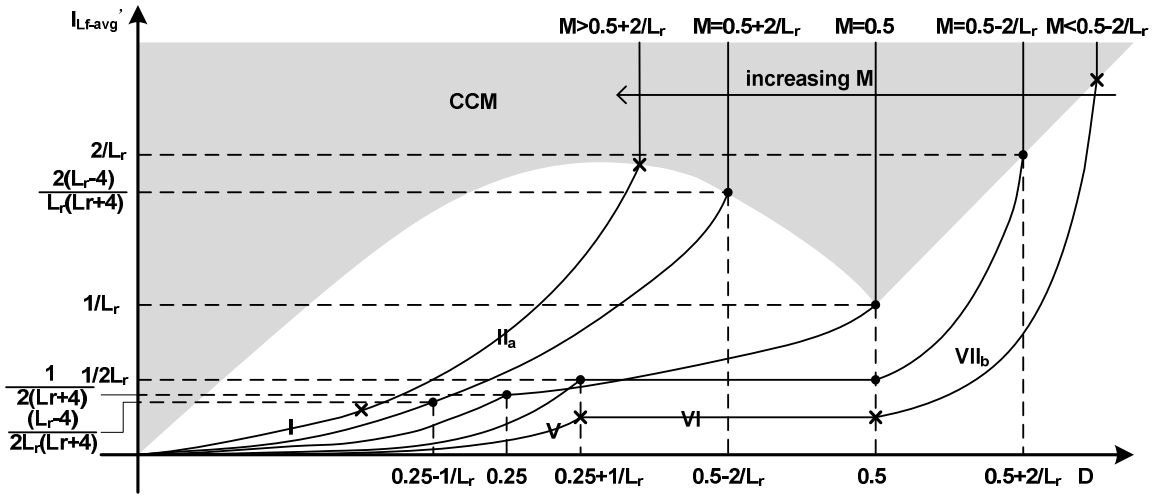


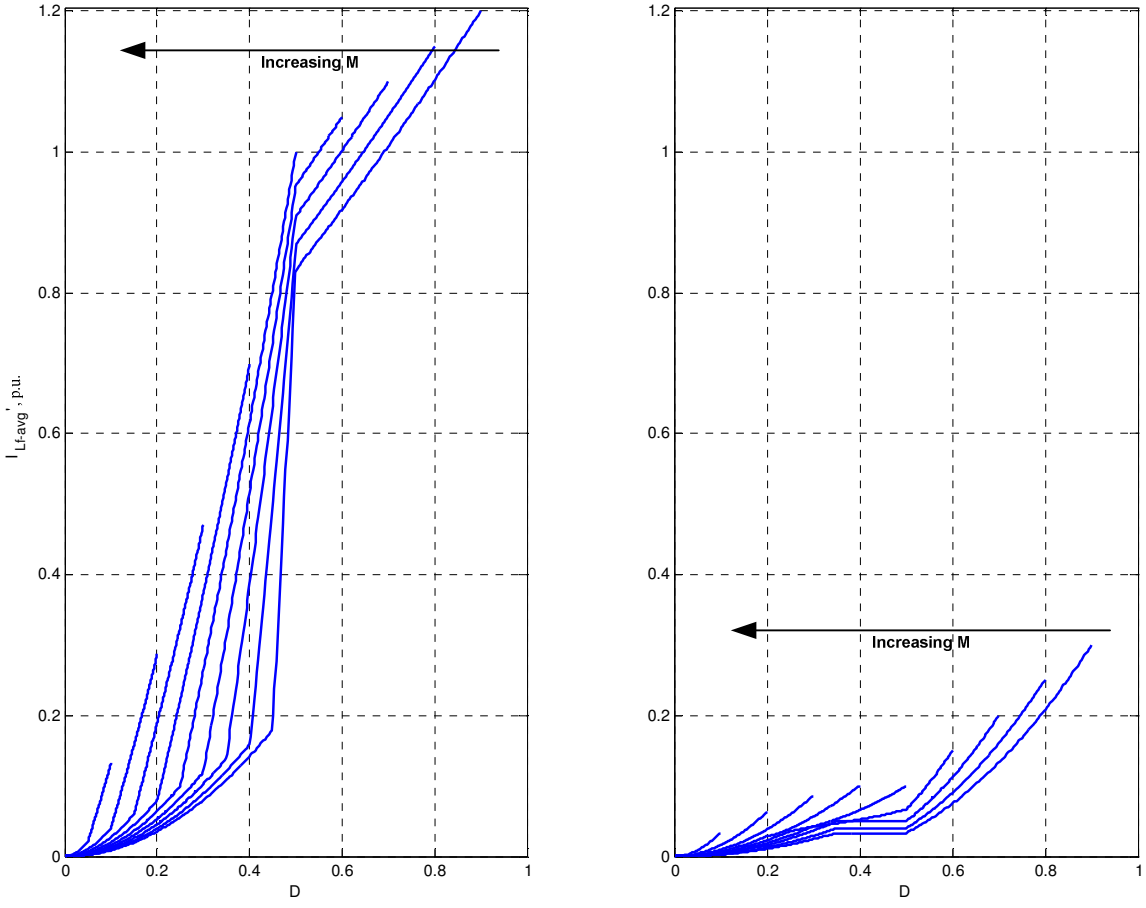
Figure 2.10. Characteristics of normalized average inductor current $I_{Lf\text{-}avg}'$ against D for different M, L_r>4, boost mode.

Two more general curves representing typical characteristics for M∈(0,0.5-2/L_r) and M∈(0.5+2/L_r,1) are also presented. The cross signs indicate the boundary points between different operating modes, which are labelled with the region numbers. In a similar way, characteristic curves can be obtained in the M region of (0.5-2/Lr, 0.5+2/Lr), however these are not shown to avoid overcrowding the diagram.

The equations derived for the average current and the peak current in region I and region II are found to be the same. Therefore, the curve for M>0.5+2/L_r (including M=0.5+2/L_r) is actually a single parabola, although different operating modes do occur in these regions with varying duty ratio.

Also, the relative position of the curves and the region boundary points in Figure 2.10 will change depending on the L_r value, as indicated on the axes of the plot. In some circumstances the curves may cross over each other as seen in one place in Figure 2.10, which may indicate a potential problem in a closed loop system. Furthermore, the horizontal sections of the characteristics (when $M \leq 0.5\text{-}2/L_r$) may also be problematic from a control perspective, indicating regions of D over which the current is insensitive to the value of D. For this reason, a feedforward current controller is implemented instead of using closed-loop control, which will be described in Section 4.6.2.

To illustrate the variation of the average current against duty ratio characteristic as L_r changes, Figure 2.11 illustrates the current characteristic when L_r takes the values 1 and 10, where different patterns of the current characteristic occur. The values of M increase from 0.1 to 0.9 in steps of 0.1.



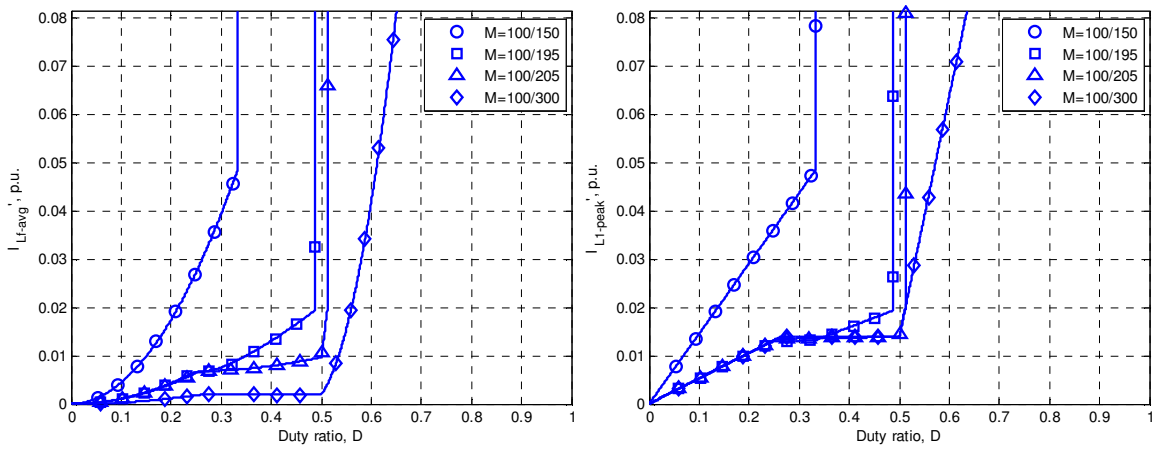
(a) L_r=1. **(b) L_r=10.**

Figure 2.11.Characteristics of normalized average inductor current $I_{Lf\text{-}avg}$' against duty ratio D, boost mode, M increasing from 0.1 to 0.9 in steps of 0.1.

In Figure 2.11, only the average current in the DCM operation is shown, the end of each line denotes the boundary between the DCM and CCM where a vertical line may be added

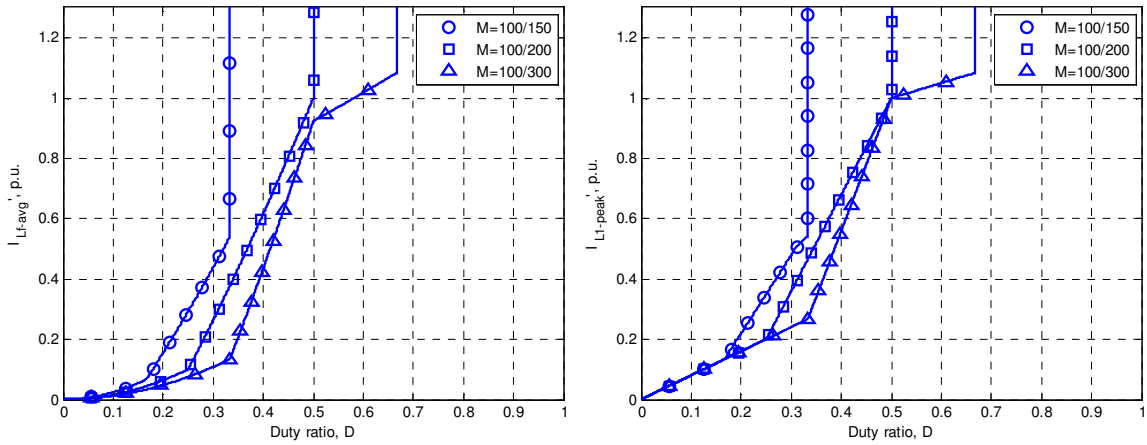
to extend to the CCM operation. When L_r=1 (Figure 2.11a), the number of DCM regions is reduced since the M-dependent mode boundaries in Figure 2.6 (M=0.5-2/L_r and M=0.5+2/L_r move outside the range zero to one. The overall pattern of the average current against D characteristic therefore differs between the cases of L_r=1 and L_r=10, with no constant current sections appearing in the L_r=10 characteristics, Figure 2.11b.

The average inductor current characteristic has been validated using the same Saber model as previously described for examining the waveform patterns, Section 2.2.3, in which the inductance ratio L_r was 71.7 and the filter inductor was 13.6μH whilst the switching frequency was 24kHz. Additionally, the inductance ratio was also changed to L_r=1 to provide further validation of the analytical results. Figure 2.12a and Figure 2.13a show the comparison between the theoretically calculated average filter inductor current using Equation (2.11) in this section and Equation (A.23) in Appendix A.6 (solid lines) and the Saber simulation results (discrete markers) for L_r=71.7 and L_r=1 respectively. A constant input voltage V_1=100V was used and the output voltage V_2 was set at the required level by a second voltage source/sink. An excellent match is seen between the theory and simulation over all conditions. The differences are typically less than 1% and were attributed to rounding errors in the calculations and simulation results processing. A similar validation exercise was undertaken for the peak phase current expression Equation (2.9) in this section and Equation (A.24) in Appendix A.6, and very close agreement was again found with the Saber simulation. The results are shown in Figure 2.12b and Figure 2.13b.



(a) Average filter inductor current. **(b) Peak phase current.**

Figure 2.12. Comparison of average inductor current between the calculated values (solid lines) and Saber simulation results (markers), V_1=100V, V_2=150V/195V/205V/300V, L_f=13.6uH, L_r=71.7, T=24kHz, boost mode, rated current I_{base}=306A.



(a) Average filter inductor current. **(b) Peak phase current.**

Figure 2.13. Comparison of peak phase current between the calculated values (solid lines) and Saber simulation results (markers), V_1=100V, V_2=150V/200V/300V, L_f=13.6uH, L_r=1, T=24kHz, boost mode, rated current I_{base}=306A.

2.3 Buck Mode Operation

The operation and analysis of the converter discontinuous conduction behaviour in the buck (step-down) mode is a mirror image of the boost mode operation and is therefore described relatively briefly in this section.

2.3.1 Simplified analysis using symmetry characteristics

In buck mode, the bottom two switches A2 and B2 in Figure 2.1 are permanently off. The top two switches A1 and B1 are controlled by two PWM signals of equal duty ratio that are phase-shifted by a half switching cycle.

The eight sub-circuits for buck mode operation are displayed in Figure 2.14, where the top four configurations show the CCM sub-circuits while the bottom four only appear in DCM operation. The directions of the currents in these eight sub-circuits are defined from right to left, and the sub-circuit numbers are re-allocated and underlined to distinguish them from those in the boost mode. The re-numbering of the sub-circuits in the buck mode enables the symmetry in the circuit waveforms to be exploited as explained later in this section.

To simplify the analysis, the symmetry in the rate of current rise in the boost and buck modes is utilized, and this is briefly explained as follows.

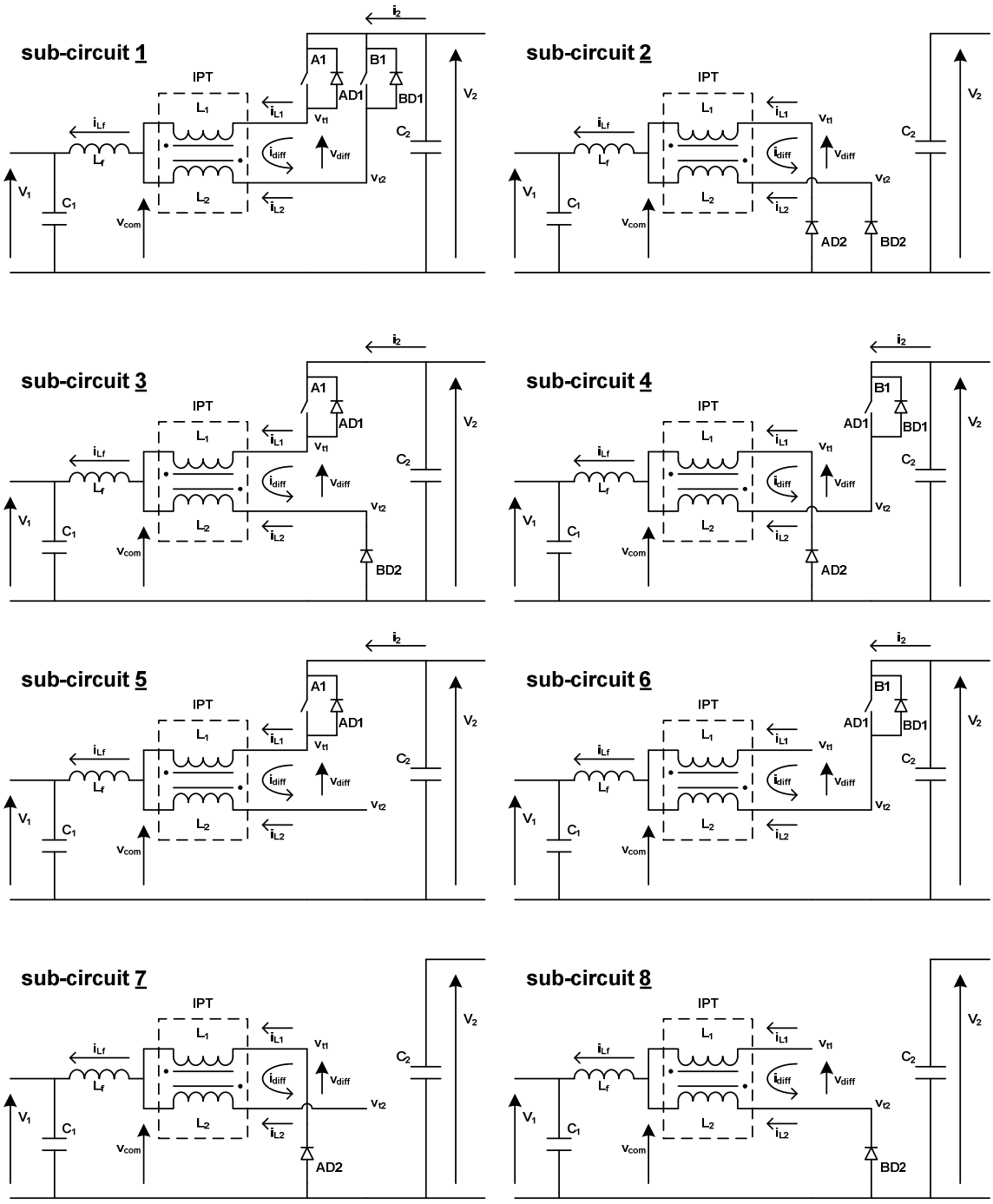


Figure 2.14. Summary of sub-circuits in buck mode.

By considering di_{L1}/dt as a function of M and V_2, Equation (2.13) can be obtained for all the sub-circuits:

$$f_n(M,V_2)=\frac{di_{L1}}{dt}=(A\cdot M+B)\cdot\frac{V_2}{L_f} \tag{2.13}$$

where A and B depend on L_r and can be identified from the results derived in Appendix A.3, Table A.2 (boost mode) and Table A.3 (buck mode). The function subscript n in Equation (2.13) is the sub-circuit number which can be either boost mode 1 to 8 or buck mode 1 to 8.

The normalized functions $f_n'(M)=AM+B$ using the base of V_2/L_f are linear functions, and the plots for the cases of n=1 to 5 and 7 (boost mode) are shown in Figure 2.15. By inspection, a symmetry exists amongst these functions whereby equal and opposite values are obtained from pairs of functions by replacing M by 1-M.

This may be expressed mathematically by the following sets of equations:

$$\begin{aligned} f_1(M,V_2) &= f_1'(M)\frac{V_2}{L_f} = -f_2'(1-M)\frac{V_2}{L_f} = -f_2(1-M,V_2) \\ f_3(M,V_2) &= f_3'(M)\frac{V_2}{L_f} = -f_4'(1-M)\frac{V_2}{L_f} = -f_4(1-M,V_2) \\ f_5(M,V_2) &= f_5'(M)\frac{V_2}{L_f} = -f_7'(1-M)\frac{V_2}{L_f} = -f_7(1-M,V_2) \end{aligned} \tag{2.14}$$

The cases for n=6 and 8, i.e., f_6 f_8 are zeros due to the non-conducting phase.

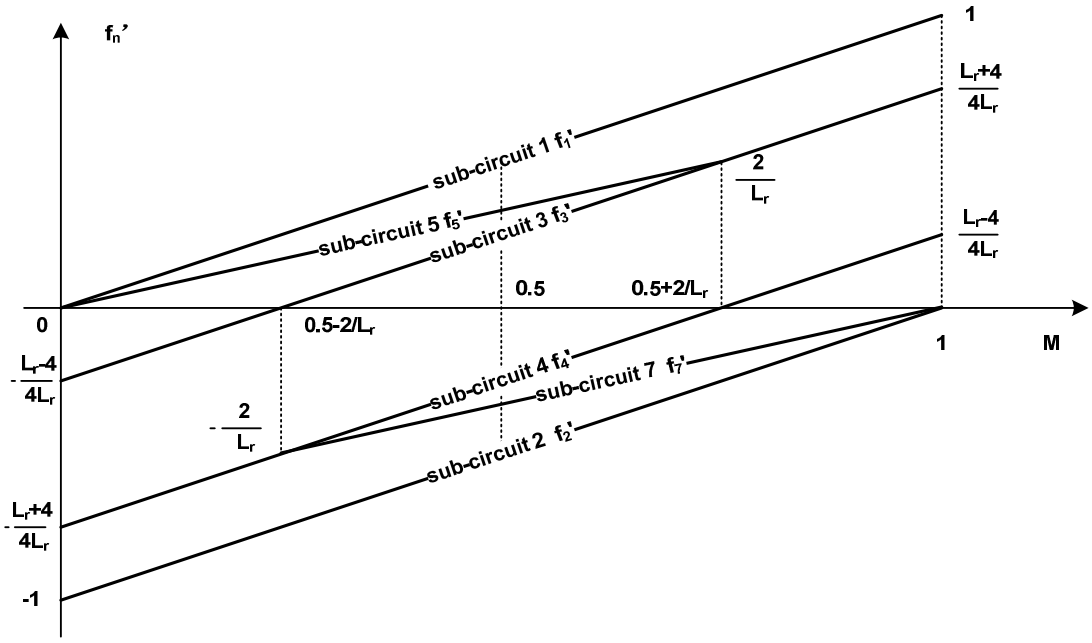


Figure 2.15. Normalized rate of rise in phase current di_{L1}/dt against voltage ratio M for boost mode.

The buck mode functions $f_{\underline{1}}$ to $f_{\underline{8}}$ have a mapping relationship with the boost functions f_1 to f_8 due to the sub-circuit pairs which have the same current path, for example, sub-circuits $\underline{1}$ and 2. The complete set of mappings is listed in Equation (2.15), where the minus signs are due to the reversed current direction defined for buck mode.

$$\begin{aligned} f_{\underline{1}} &= -f_2 \quad & f_{\underline{2}} &= -f_1 \quad & f_{\underline{3}} &= -f_4 \quad & f_{\underline{4}} &= -f_3 \\ f_{\underline{5}} &= -f_7 \quad & f_{\underline{6}} &= -f_8 = 0 \quad & f_{\underline{7}} &= -f_5 \quad & f_{\underline{8}} &= -f_6 = 0 \end{aligned} \tag{2.15}$$

By substituting Equation (2.14) into Equation(2.15), the pattern of symmetry between the current waveforms is revealed:

$$\begin{aligned} f_{\underline{1}}(M,V_2) &= f_1(1-M,V_2) & f_{\underline{2}}(M,V_2) &= f_2(1-M,V_2) \\ f_{\underline{3}}(M,V_2) &= f_3(1-M,V_2) & f_{\underline{4}}(M,V_2) &= f_4(1-M,V_2) \\ f_{\underline{5}}(M,V_2) &= f_5(1-M,V_2) & f_{\underline{7}}(M,V_2) &= f_7(1-M,V_2) \\ f_{\underline{6}}(M,V_2) &= f_6(1-M,V_2)=0 & f_{\underline{8}}(M,V_2) &= f_8(1-M,V_2)=0 \end{aligned} \tag{2.16}$$

According to Equation (2.16), a series of sub-circuits appearing in buck mode with voltage ratio M is equivalent to the corresponding set of boost mode sub-circuits with a voltage ratio of (1-M). For example, the converter working in boost mode region I with M=0.9 will have sub-circuit sequence 32704280, which will have the same operating pattern as in the buck mode having the sub-circuit sequence of <u>32704280</u> with 1-M=0.1, assuming that the two converters have the same value of V_2; that is, the current waveforms will be equal, but opposite in direction. As a result, the equations in the form of f(M, V_2) in the analysis of the boost mode can be applied to the buck mode by replacing M with (1-M).

2.3.2 Analysis of Buck mode CCM and DCM operation

The buck mode CCM and DCM operating patterns are identified as follows using the method described in Section 2.3.1 and are validated through Saber simulations.

The CCM operation follows the characteristic conversion Equation (2.17):

$$M = \frac{V_1}{V_2} = D \tag{2.17}$$

which can be derived by equating the positive and negative inductor volt-seconds of V_{Lf}, or simply by replacing M with 1-M in Equation (2.2) and can also be obtained by considering the fact that the duty ratio D of the top switch results in a duty ratio of (1-D) for the bottom diode in CCM, so that Equation (2.2) is applicable with D replaced by (1-D). Therefore, the current waveforms in CCM with a particular duty ratio D in buck mode are exactly the same as those with duty ratio (1-D) in boost mode in Figure 2.3.

A summary of the DCM operating regions for the buck mode is shown in Figure 2.16. As expected, the same divisions of the DCM operating regions for boost mode in Figure 2.6

are obtained but in inverse form due to the symmetry around M=0.5. The thick line represents the CCM operation while the triangular area above the line bounded by M=1 is the DCM operating region. The DCM phase current waveforms for boost mode in Table 2.2 still apply to the labelled regions for buck mode in Figure 2.16, although different sub-circuits occur within the cycle, as accounted for by the re-numbering of the sub-circuits in the buck mode.

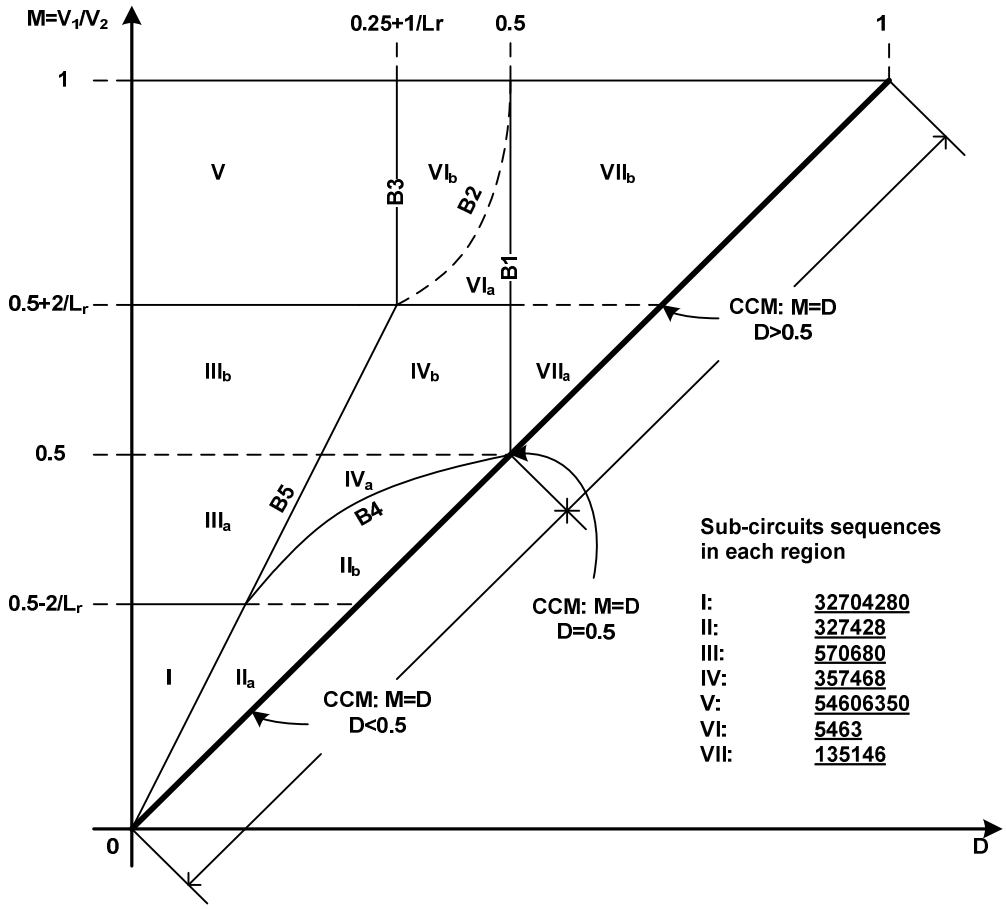


Figure 2.16. DCM operating regions in buck mode.

The boundaries B1 to B5 in Figure 2.16 are given in Table 2.4 which can be obtained by replacing M with 1-M in the expressions derived for boost mode in Table 2.3.

Table 2.4. Summary of DCM boundary duty ratios in buck mode

Boundary duty ratios				
B1	B2	B3	B4	B5
$D=0.5$	$D=\frac{(2M-1)(4+L_r)}{2(2L_rM-L_r+4)}$	$D=0.25+1/L_r$	$D=\frac{4M}{L_r-2L_rM+4}$	$D=\frac{M}{2}$

The average filter inductor current and peak phase current for the buck mode can be derived using Equation (2.8), (2.9) and (2.10), or can also be obtained by replacing M with 1-M in the expressions derived for the boost mode. The full expressions are given in Appendix A.6. The normalized average filter inductor current against duty ratio characteristic is generally summarised in Figure 2.17 where as before the shaded region indicates CCM. The DCM operating regions are marked on the corresponding sections of the characteristics, and the characteristics become vertical in the CCM. Numerical examples of the characteristics are plotted in Figure 2.18 for L_r=1 and 10, the values of M increasing from 0.1 to 0.9 in steps of 0.1.

Validation of the expressions for average inductor current and peak phase current was undertaken using an idealised Saber simulation and the results are plotted in Figure 2.19 and Figure 2.20. The same parameters were used as for the boost mode validation in Figure 2.12 and Figure 2.13, namely: V_1=100V, L_f=13.6uH, L_r=1 or 71.7. The results show excellent correspondence, confirming the correctness of the theoretical predictions.

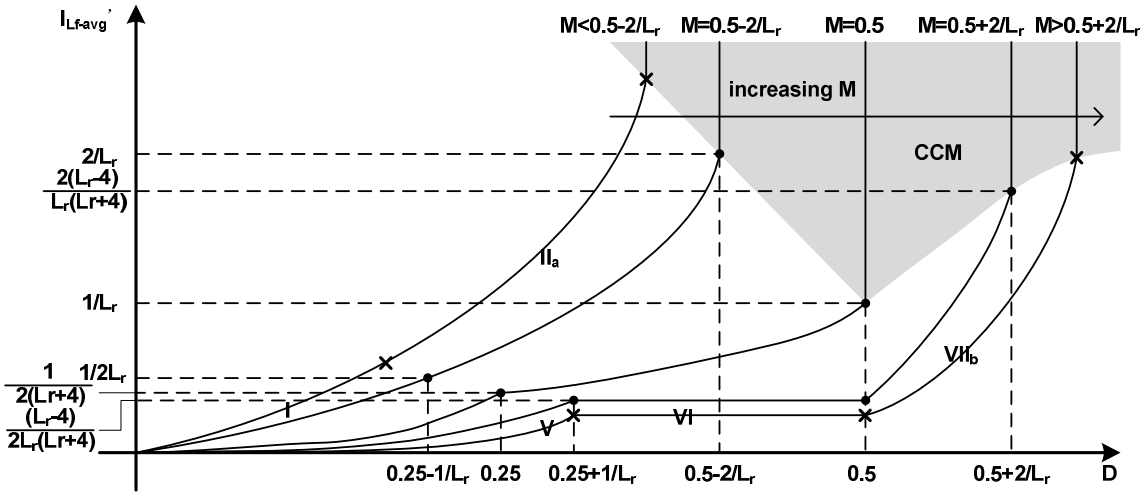
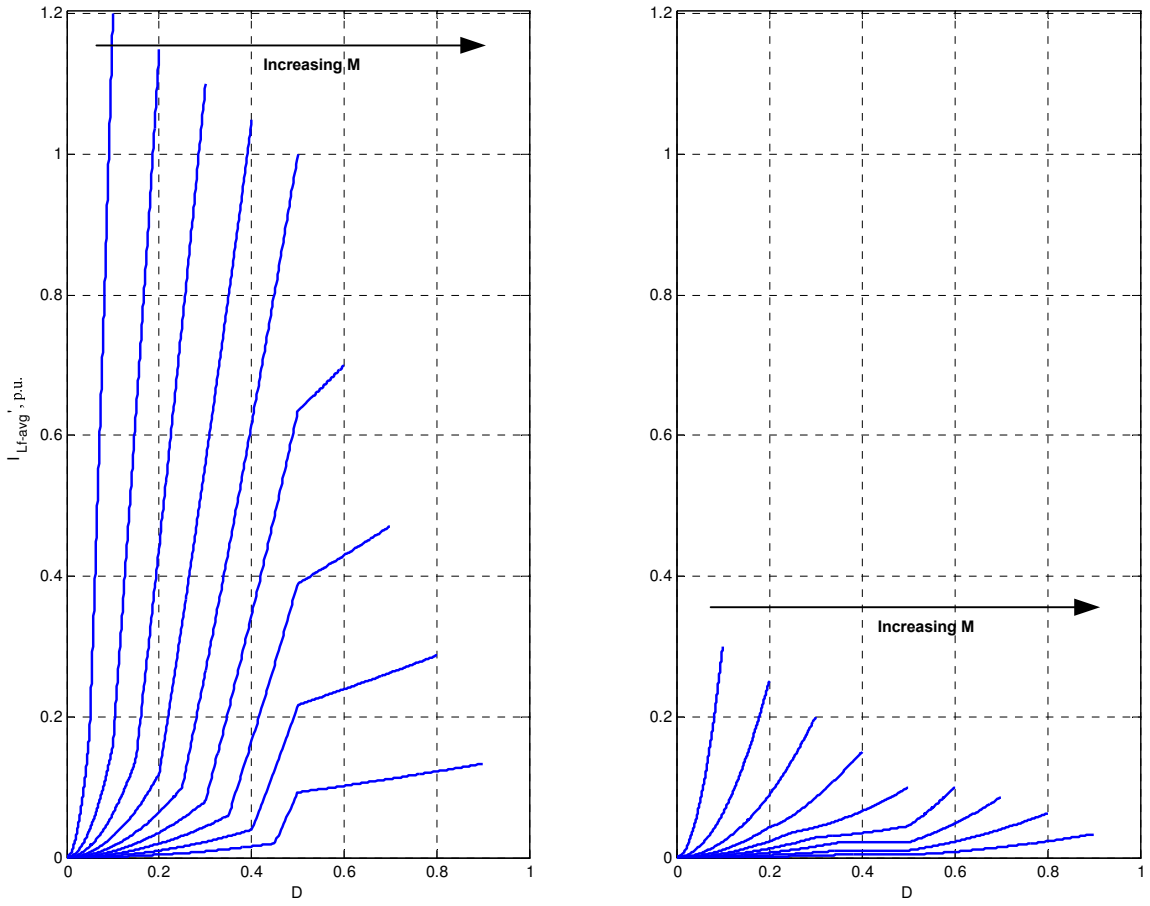
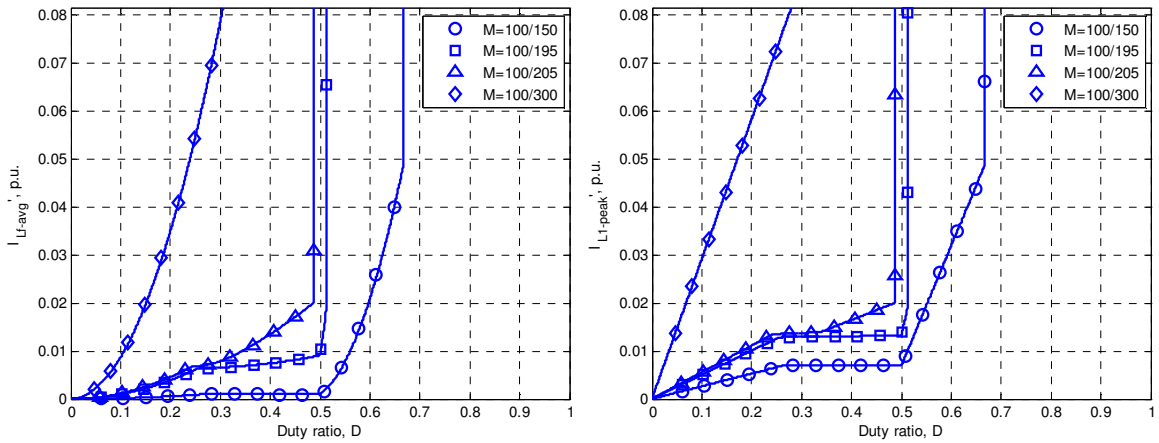


Figure 2.17. Characteristics of average inductor current $I_{Lf\text{-}avg}$' against D for different M, L_r>4, buck mode.



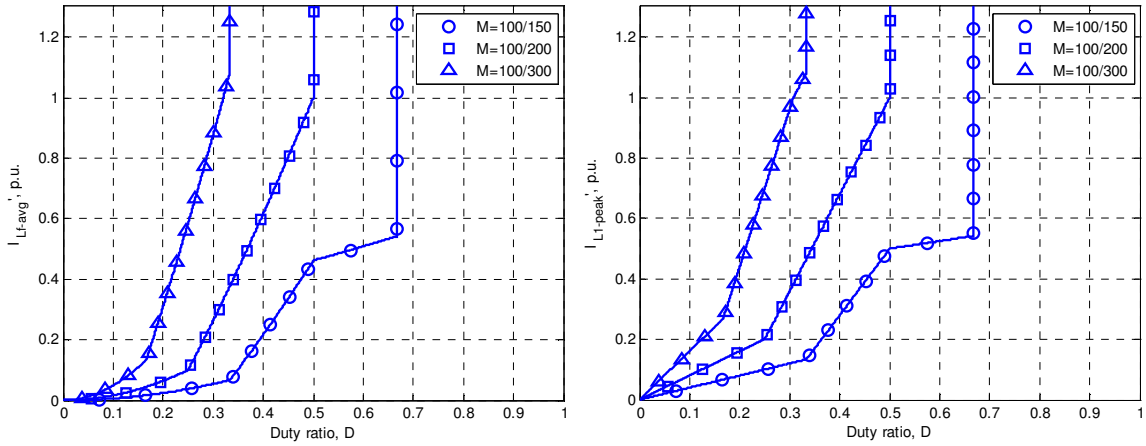
(a) L_r=1. **(b) L_r=10.**

Figure 2.18. Characteristics of normalized average inductor current $I_{Lf\text{-}avg}$' against D, buck mode, M increasing from 0.1 to 0.9 in steps of 0.1.



(a) Average filter inductor current. **(b) Peak phase current.**

Figure 2.19. Comparison of average inductor current between the calculated values and Saber simulation results, V_1=100V, V_2=150V/195V/205V/300V, L_f=13.6uH, L_r=71.7, T=24kHz, buck mode, rated current I_{base}=306A.



(a) Average filter inductor current. **(b) Peak phase current.**

Figure 2.20. Comparison of peak phase current between the calculated values and Saber simulation results, V_1=100V, V_2=150V/200V/300V, L_f=13.6uH, L_r=1, T=24kHz, buck mode, rated current I_{base}=306A.

2.4 Experimental validation

The DCM operating modes have been validated by practical experiments using two dual-interleaved converter prototypes. The parameters of the two converters are given in Table 2.5, one of which (converter A) is the origin of the parameters used in the Saber simulations, which were reported earlier in this chapter. The converters were designed and constructed by Dr Gerardo Calderon-Lopez as part of a separate research project, however, all the experimental measurements reported here were made by the author. The converters used a peak current mode controller to ensure equal current sharing between the two halves of the IPT. The minimum low voltage port voltage V_1 in the table is the threshold where the nominal output power will be achieved due to the current limits, however, with a V_1 voltage lower than this, the converter can still operate but with less output power capability.

Table 2.5. Converter details in experiments

Parameter (units)	Converter A	Converter B
Switching frequency (kHz)	24.0	24.7
Filter inductor L_f (μH)	13.6	15.4
Differential inductance of the IPT L_{diff} (μH)	976	540
Mutual inductance ans self-inductance of the IPT L_M=L_1=L_2 (μH) *	244	135
Inductance ratio L_r=L_{diff}/L_f (-)	71.7	35.1
Minimum low voltage port voltage V_1 (V)	190	220
Nominal high voltage port voltage V_2 (V)	600	600
Nominal filter inductor current $I_{Lf\text{-}avg}$ (A)	170	260
Nominal output power (kW)	50	58

*The IPT is tightly coupled with coupling coefficient higher than 0.998

Figure 2.21 to Figure 2.27 show a selection of the DCM operating waveforms both in simulation and experiment to illustrate the operating regions analysed in this chapter. The simulation results for comparison purposes were obtained from an idealised Saber model which used lossless components (Appendix A.5). The waveforms in the DCM operating regions II and VII have been validated in boost mode using converter A, Figure 2.21 and Figure 2.23, which have a relatively high current and the key features are therefore easier to identify; while regions I, V, VI are demonstrated in buck mode with converter B, Figure 2.24 to Figure 2.27. In contrast to the idealised predictions, the operating patterns in regions III and IV were obscured in the experiments by parasitic ringing and were also difficult to observe due to the narrow region of M over which the operating patterns occur, namely, $M=0.5-2/L_r$ to $0.5+2/L_r$. This will be explained in more detail in the following section.

2.4.1 Boost DCM operation

The boost mode operation uses the converter A in Table 2.5, a DC power supply at the low voltage side V_1, and a resistor bank of $R=120\Omega$ at the high voltage side V_2. The high resistance value ensures a light load condition so that DCM mode can be easily observed. The results presented here have the same output voltage V_2 of 530V, whereas the input power supply voltage is varied to achieve the different conversion ratios.

Figure 2.21 shows the waveforms when the converter is operating in region VII_b, and operates with the sub-circuit sequence of 135146. From top to bottom are the gate drive signals v_{gA2} and v_{gB2} of the bottom two switches A2 and B2, the filter inductor voltage v_{Lf}, the differential voltage across the IPT v_{diff}, one of the IPT phase currents i_{L1},and the filter inductor current i_{Lf}. The currents were measured using Rogowski coils which can only observe the AC component of the measured waveform. However, the average input current i_{Lf} was read from the power supply's control panel (TopCon, 0.025% measurement resolution [161]), and enabled the complete waveforms to be re-constructed by adding the measured DC component of i_{Lf} to the measured AC component, and half the measured DC component of i_{Lf} to the measured AC component of i_{L1}.

The average filter inductor current $I_{Lf\text{-}avg}$ is predicted using the equation in Table A.5 for comparison with the corresponding values from the simulation and experimental

measurements. The values are shown in the figure title under each set of results. In this case, they are 13.6A, 13.4A and 12.5A for the theoretical calculation, simulation and experimental measurement. The agreement is generally very good with the experimental value being slightly lower due to the effects of circuit losses.

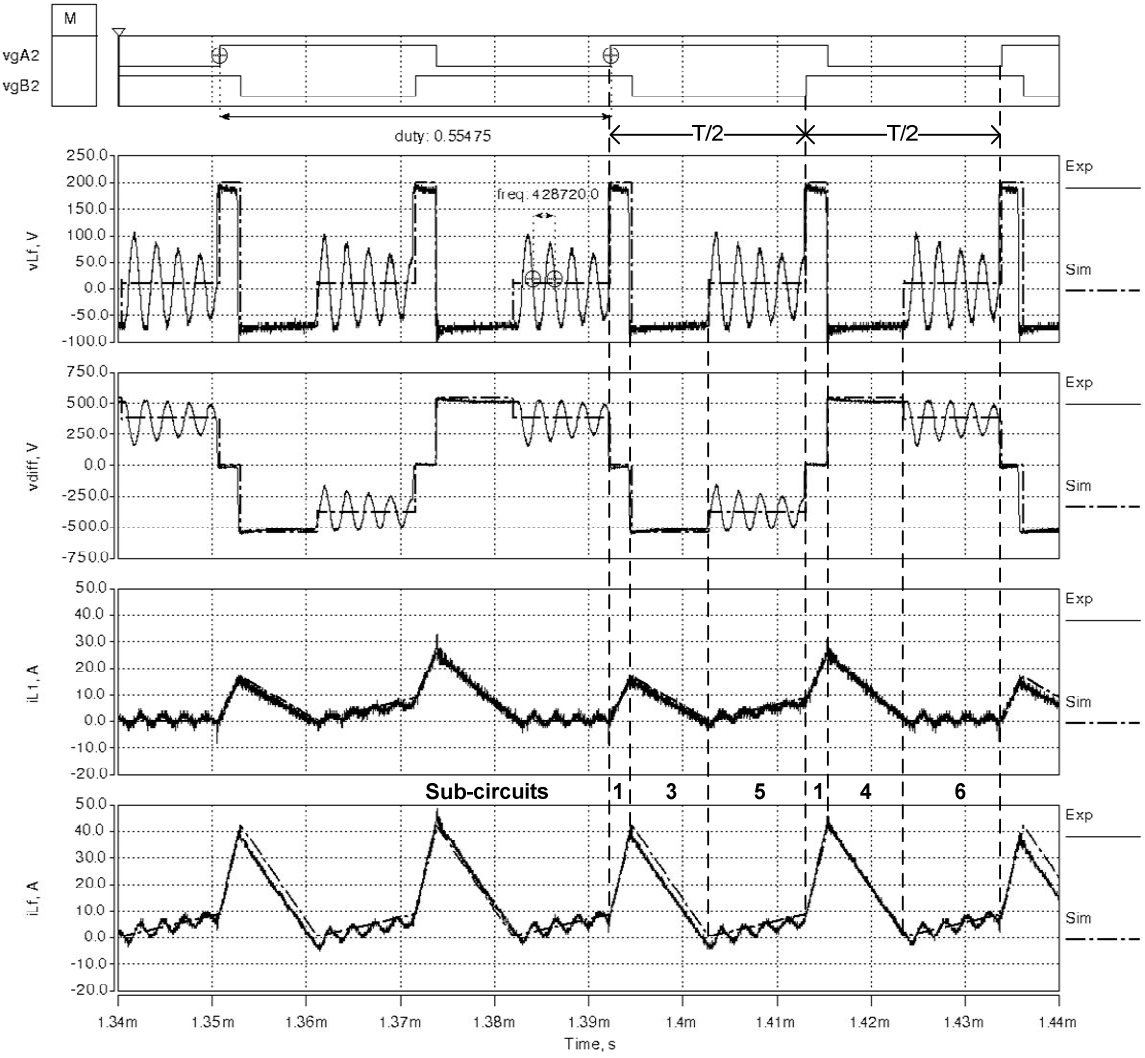
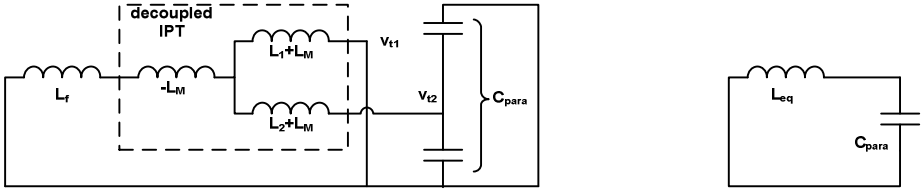


Figure 2.21. Boost mode, region VII$_b$, converter A, D=55.4%, V_1=200V, V_2=530V, $I_{Lf\text{-}avg}$=13.6A, 13.4A, 12.5A (from theoretical, simulation and measurement respectively) , R=120Ω

The two measured voltages v_{Lf} and v_{diff} match well with those from simulation except in the intermediate voltage levels where a parasitic ringing effect is present. The oscillation occurs in the DCM sub-circuits (5 and 6) when one of the IPT windings ceases conduction and is due to the interaction between the device parasitic capacitances and the inductance in the circuit (both the IPT and the filter inductor). The simulation shows that the phase current i_{L1} is virtually zero in sub-circuit 6 between 1.423ms and 1.433ms, which accompanies the oscillation in the experimental results. The same effect happens in the other half cycle when the other phase current i_{L2} is zero, that is, sub-circuit 5. However a

small current oscillation of the same frequency as the voltage oscillation is observed in the filter inductor and IPT currents.

The parasitic oscillation can be analysed by using an equivalent circuit, Figure 2.22a, where in this case the conducting terminal of the IPT is v_{t1}, and v_{t2} is floating. The equivalent circuit comprises the filter inductor L_f, the de-coupled IPT with winding self-inductance L_1, L_2 and the mutual inductance L_M (L_M=L_1=L_2)[162], and the equivalent parasitic capacitance C_{para} which is the sum of the upper and lower switching devices' output capacitances.



(a) Full circuit. **(b) Simplified circuit.**

Figure 2.22. Equivalent circuit for the parasitic ringing analysis.

The whole circuit can be simplified into an LC resonant circuit as shown in Figure 2.22b, where L_{eq} is the equivalent inductance derived from the circuit on the left, Equation (2.18), and is equal to 52uH according to the values given in Table 2.5 for converter A. The parameter C_{para} is composed of the device output capacitances which are non-linear and decrease sharply as the device voltages increase. From the IGBT module datasheet (CM600DU-24NFH[163]), the total parasitic capacitance was estimated to be C_{para}=1.39nF+0.82nF=2.21nF for the applied voltages of 151V and 530-151=379V obtained in the simulation.

$$L_{eq} = L_2 + L_M + (L_f - L_M) // (L_1 + L_M) \tag{2.18}$$

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{eq} C_{para}}} \tag{2.19}$$

The combination of L_{eq}=52uH and C_{para}=2.21nF suggests a natural oscillation frequency f_{osc}=470kHz according to Equation (2.19). However, the oscillation frequency is 429kHz in the measured waveform in Figure 2.21. The discrepancy was attributed to the additional stray capacitance and parasitic inductance in the circuit, for example the inter-winding capacitance of the magnetic components and the inductance of the circuit layout.

Also, Figure 2.21 shows a slight asymmetry in the experimental IPT winding current and this was attributed to an imbalance in the current sharing between two halves of the IPT.

Figure 2.23 shows the results when the operating mode is in region II_a, with a sub-circuit sequence of 327428 as labelled in the figure. Similar to the results in Figure 2.21, the voltages and currents have oscillations during the DCM sub-circuit periods. The ringing frequency has changed to 398kHz in this case, which is thought to be due to the change of voltage level on the devices and the associated change in the capacitance C_{para}. Because of the varying C_{para}, using fixed value capacitors across switches in a converter model to represent the parasitic capacitance is not suitable. By using snubber capacitors much larger than C_{para}, the varying parasitic capacitance can be neglected, which however introduces unnecessary circulating energy within the converter that may lead to extra losses.

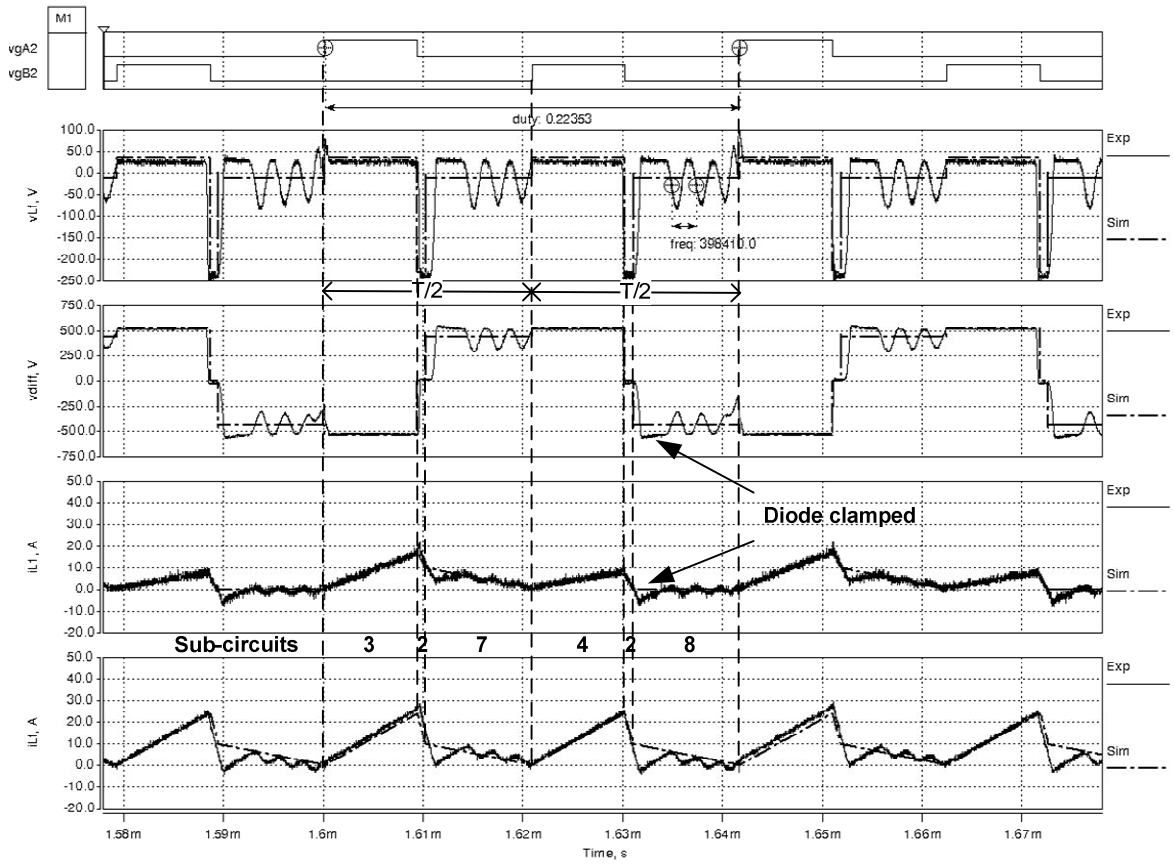


Figure 2.23. Boost mode, region II_a, converter A, D=22.3%, V_1=300V, V_2=530V, $I_{Lf\text{-}avg}$=8.7A, 8.7A, 8.2A (from theoretical, simulation and measurement respectively), R=120Ω.

A noticeable discrepancy was observed between the simulation and experimental results at t=1.632ms in the third and fourth plots, i_{L1} and i_{Lf}, which is thought to be due to the turn-off of diode AD1 at the end of sub-circuit 2 followed by the resonant charging/discharging of the leg output capacitance producing a negative value of i_{L1}, which brings diode AD2 into conduction. This contributes to the lower average current in the experiment (8.2A) compared with the simulation and prediction (8.7A). The same phenomenon is observed in other operating modes, which will be described in the following section for the buck mode.

2.4.2 Buck DCM operation

The buck mode operation uses the converter B, Table 2.5, a DC power supply at the high voltage side to provide a constant voltage of V_2=100V, and resistors connected at the output voltage V_1 side as the load. The currents are measured using current probes (LeCroy, CP150, CP500 [164]).

Figure 2.24 shows the case when the duty ratio is very low, D=10.8%, and the converter is working in buck mode region I with sub-circuit sequence of 32704280. From top to bottom are the gate drive signal of the left top switch v_{gA1}, the switch voltage v_{A1}, the phase current i_{L1} and the filter inductor current i_{Lf}. Due to the existence of sub-circuit 0, the current levels of i_{L1} and i_{Lf} are both zero for a period of time; however, the parasitic ringing still exists in this case. The average current $I_{Lf\text{-}avg}$ from the theoretical calculation shows very closed agreement with the simulation results and measurement, the values being 1.06A, 1.07A, and 1.09A respectively.

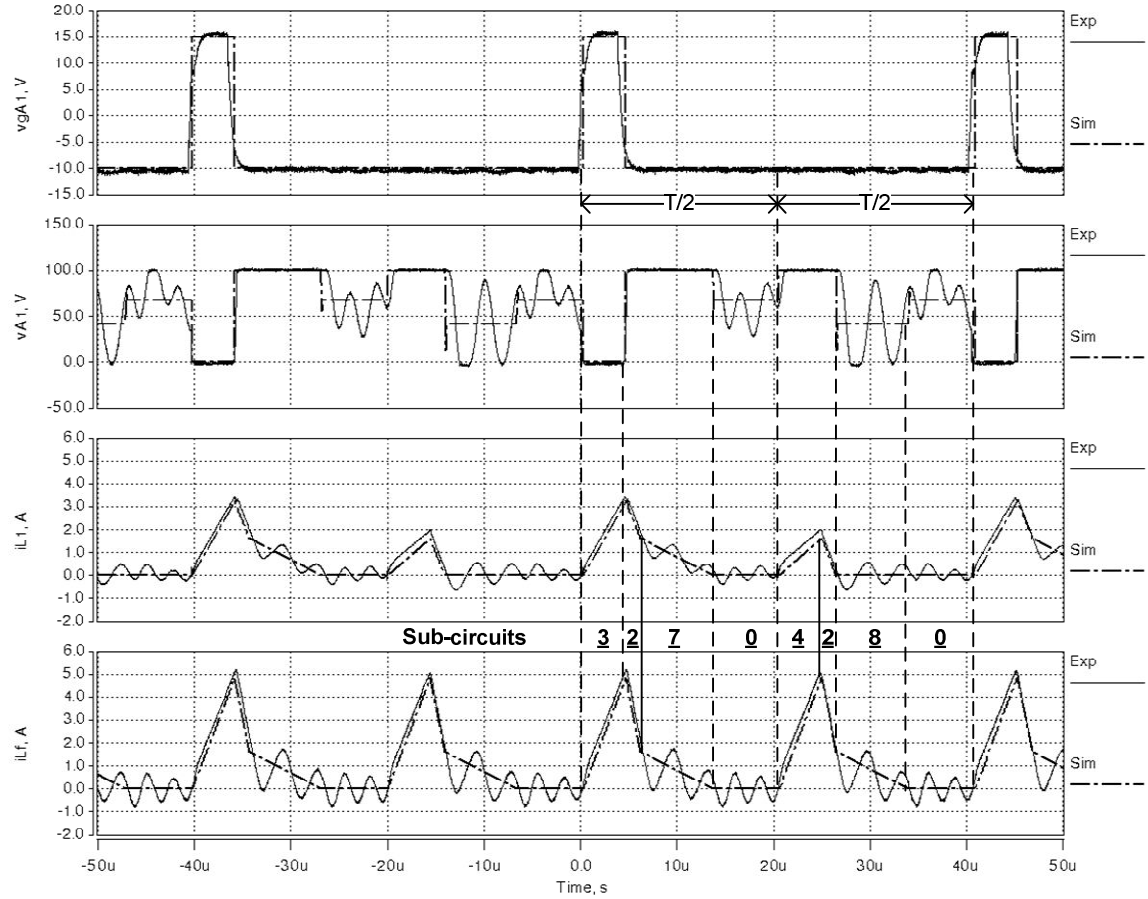


Figure 2.24. Buck mode, converter B, D=10.8%, V_1=32.9V, V_2=100V, $I_{Lf\text{-}avg}$=1.06A, 1.07A, 1.09A (from theoretical, simulation and measurement respectively), R=30Ω, region I.

Figure 2.25 shows the result when the duty ratio is 19.3%, and the converter is working in region V with a sub-circuit sequence of 54606350. The currents i_{L1} and i_{Lf} have negative parts and match fairly well with the simulation except for the ringing. The transistor voltage v_{A1} in the second plot is heavily distorted by the parasitic oscillations, and there are periods when one of the anti-parallel diodes is brought into conduction by the oscillations resulting in the voltage being clamped to zero or the input level of 100V.

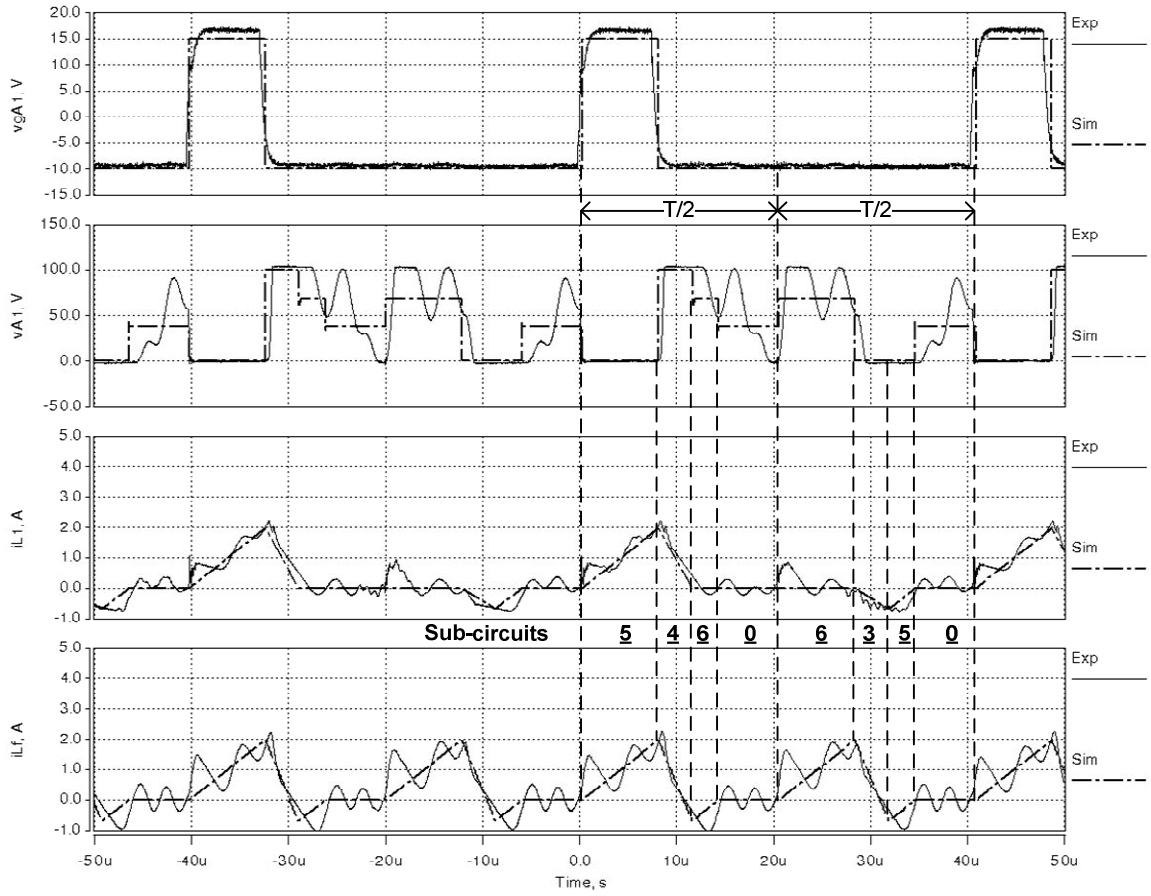


Figure 2.25. Buck mode, converter B, D=19.3%, V_1=62V,V_2=100V, $I_{Lf\text{-}avg}$=0.44A, 0.44A, 0.52A (from theoretical, simulation and measurement respectively), R=120Ω, region V.

In the first half cycle from t=0s to t=20μs, sub-circuit sequence 5460 should be present since four voltage levels in v_{A1} appear in the simulation, but this is not clearly shown in the experiments result due to the ringing effect during the third and fourth sub-circuits 6 and 0. However, the parasitic ringing appears to be superimposed around the expected intermediated voltage levels as indicated in the simulation, although the voltage is transiently clamped at zero due to anti-parallel diode conduction. In the second half cycle from 20μs to 40μs, sub-circuit sequence 6350 appears, but only three voltage levels appear because sub-circuits 3 and 5 have either the transistor or the associated anti-parallel diode in conduction; nevertheless, the current behaviour in these two sub-circuits are different.

Figure 2.26 shows the result for buck mode region VI operation, where excellent correspondence is achieved between the prediction and measurement since the duty ratio and the current have increased and the parasitic oscillation does not obscure the transistor voltage v_{A1} waveform so severely. An important feature of this operating mode is that the switch anti-parallel diode is in conduction before the switch itself is signalled to turn-on. For example, at t=-8μs, a negative current flows through the transistor's anti-parallel diode AD1 and the transistor voltage v_{A1} in the second plot is zero after t=-8μs.

A current imbalance exists between the IPT windings since the filter inductor current does not have half-cycle symmetry. This results in the average current being lower than expected, giving 0.52A instead of 0.9A as predicted from the theoretical calculation.

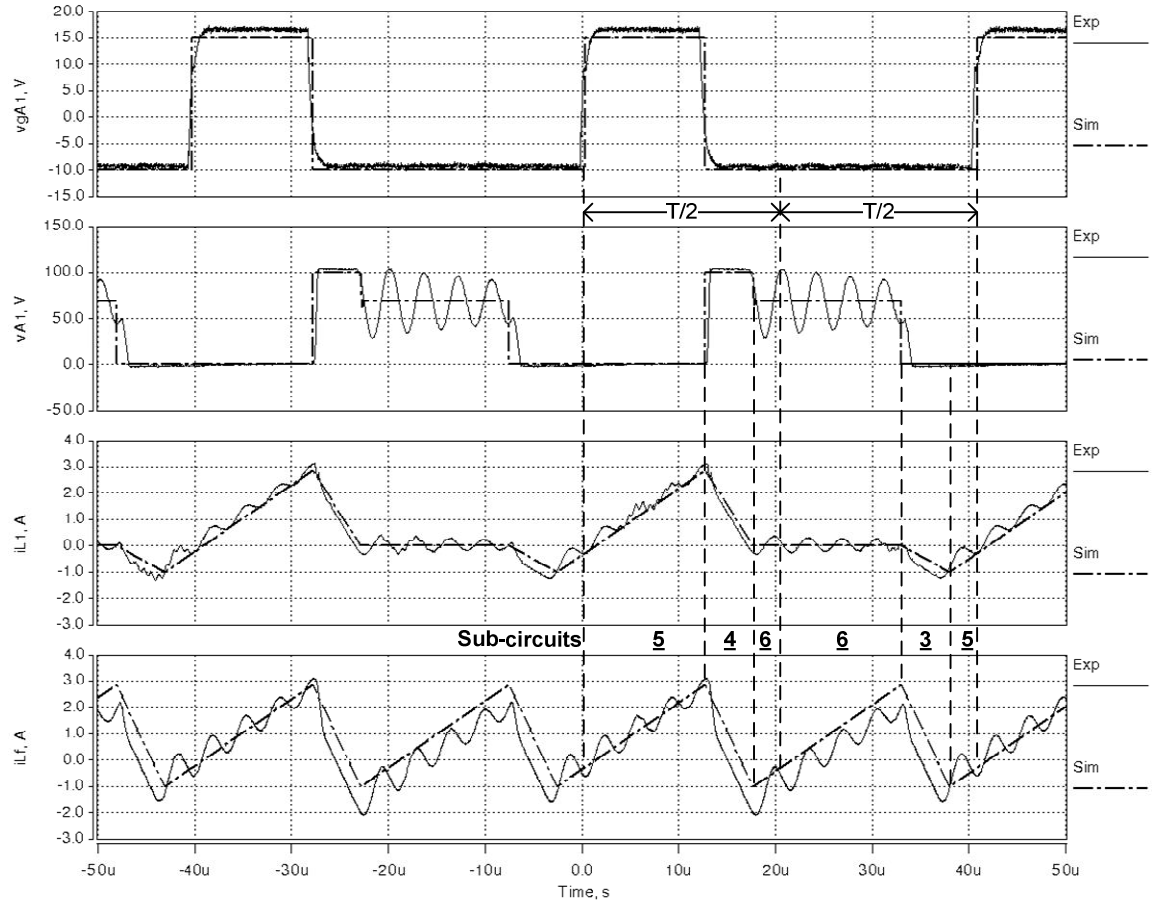


Figure 2.26. Buck mode, converter B, D=31%, V_1=62V, V_2=100V, $I_{Lf\text{-}avg}$=0.91, 0.90, 0.52A (from theoretical, simulation and measurement respectively), R=120Ω, region VI.

The duty ratio and output voltage combination in Figure 2.27 should give region IV_b operation with a sub-circuit sequence of 357468. However, a discrepancy is found between the experimental results and the simulation. An unexpected negative current in the phase current i_{L1} appears between t=37μs and 41μs, again caused by resonant charge/discharge of

the leg capacitance as previously shown in Figure 2.23. A large difference can be noticed in the filter inductor current in the fourth row, due to the imbalance in current sharing and the effect of unexpected negative current. It is thought that the duty ratio of transistor B1 does not match that of the transistor A1 due to a number of factors: noise, difference in driving signal delays and control reference bias in the two interleaved channels. Due to the reduced phase current i_{L2}, the average filter inductor current is 1.7A, 0.5A less than the predicted value.

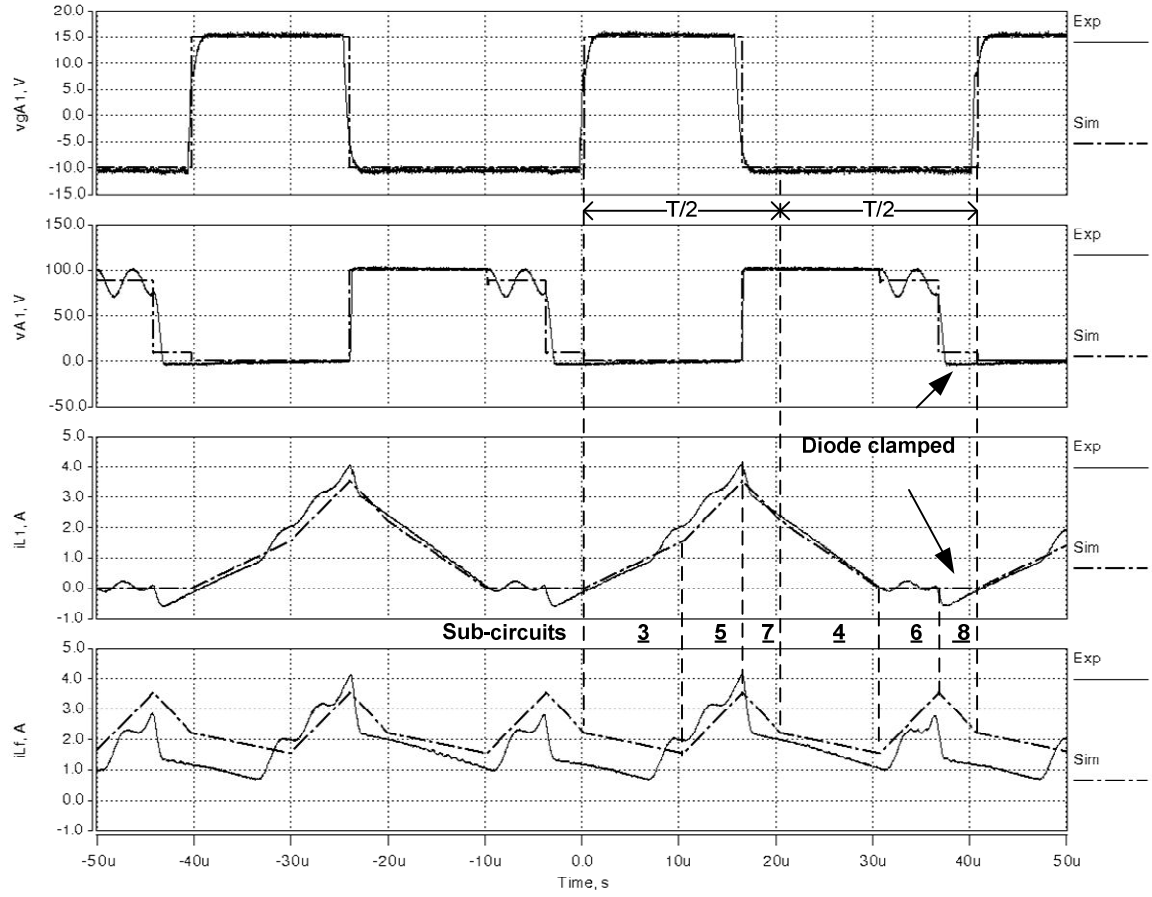


Figure 2.27. Buck mode, converter B, D=40.1%, V_1=51V, V_2=100V, $I_{Lf\text{-}avg}$=2.28A, 2.28A, 1.7A (from theoretical, simulation and measurement respectively), R=30Ω, region IV_b.

The same effect is observed in region III where negative current and current imbalance appear again. Another difficulty is that the inductance ratios L_r are high in both converters, which leads to a narrow band of voltage for these two modes to exist, i.e., $M=0.5-2/L_r$ to $M=0.5+2/L_r$. With smaller L_r values, the band will be increased so that the two regions may be easier to identify. For example, the work reported in [99] shows the waveforms corresponding to region IV with a directly coupled transformer of coupling coefficient 0.91 (with effectively $L_r=L_{diff}/L_f$= 22μH/115μH=0.19).

2.5 Conclusion

For the purpose of controlling a dual-interleaved converter with interphase transformer, all the possible operating patterns have been summarised in this chapter. Due to the nature of wide range of converter operating condition (voltages, currents and power), the converter may enter different operating modes. Therefore, not only the continuous conduction mode (CCM) but also the discontinuous conduction mode (DCM) have been analyzed thoroughly, which has not previously been documented in the literature. Since the DCM operation is much more complicated than CCM operation, closed-loop current control for DCM is also complex and beyond the scope of this research, which has been identified as a subject for future work in Section 5.4.1.

Seven operating patterns are identified in the DCM, and the condition for these patterns to appear is presented as seven regions in a voltage ratio M against duty ratio D map. The boundary conditions for each region are also derived. The average current and peak current equations for each operating pattern are derived, showing non-linear characteristics as the duty ratio changes.

The boost mode and buck modes are shown to be similar and the symmetry patterns between the operating modes are identified and used to simplify the analysis.

The observed DCM operating patterns and the equations derived for the average and peak currents are validated through extensive Saber simulation of an idealised converter where excellent agreement is achieved for both boost and buck modes with errors less than 1%. Furthermore, the boost and buck mode operation waveforms are validated by experiments using two different converter prototypes, although parasitic ringing between the device output capacitances and circuit inductances were seen to modify the waveforms in same circuit configurations. For the application in this thesis, the theoretical anaylsis regardless of the parasitic elements will be deployed, as will be described in Chapter 4 for an energy storage system which is based on using a dual-interleaved converter.

Chapter 3 Control of emulated energy storage system

3.1 Introduction

In this chapter, a simple method is examined for the control of a super-capacitor based energy storage system within a small DC electrical system. The super-capacitor is linked to the DC system through a bi-directional DC-DC converter. The goal of the control is to resolve the instantaneous mismatch between load demand and power availability, and to manage the energy within the ESS depending on the load conditions.

The design and characteristics of the system controller are studied by means of a Simulink simulation and the results are validated using hardware-in-the-loop (HIL) emulation of a super-capacitor system coupled to a real generator and load equipment.

The contents of this chapter formed the basis of a paper presented at the 2010 IEEE APEC conference [12].

3.2 ESS system description

This chapter describes a method of control for an energy storage system (ESS) that may be used in a small on-board electrical system such as a vehicle, aircraft or ship. Many of the electrical loads in these systems are highly dynamic and there is a risk that rapid load changes may adversely affect the primary electrical power source, which would typically be a rotating generator driven by a prime mover, a battery or fuel-cell. For example, rapid load changes could place an excessive stress on the power source, which may cause high losses, limit lifetime, or even result in malfunction. Designing the primary power source to withstand these transients would result in an increase in cost, weight and maintenance requirements.

The system under consideration is shown in Figure 3.1. A single power source is connected to several load elements through a DC electrical circuit, however multiple power sources may also be present. The super-capacitor, which can be replaced by other energy storage sources, serves as an energy buffer and is connected to the bus through a DC-DC converter. The DC-DC converter ensures an orderly flow of power in or out of the super-capacitor.

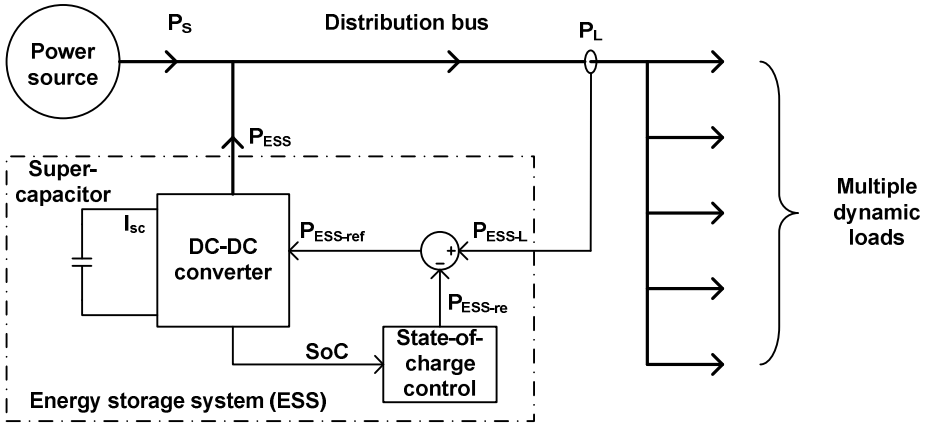


Figure 3.1. System diagram of the ESS and the DC distribution network.

The purpose of the energy storage system is to shield the primary power source from sudden load changes. To achieve this, the energy storage system responds rapidly to load changes, by injecting power into the electrical system to meet load increases, or drawing power from the system when the load suddenly falls as illustrated in Figure 3.2.

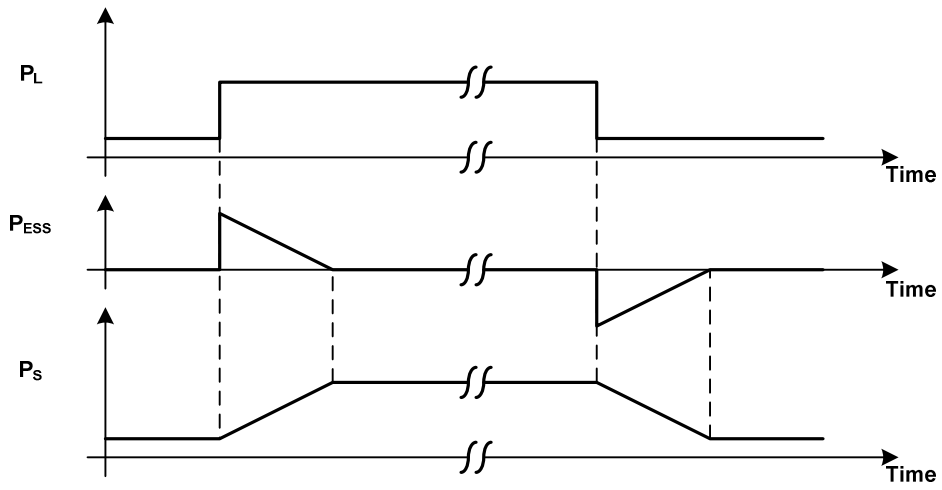


Figure 3.2. Power flow characteristics.

Following the transient in load power P_L in Figure 3.2, either an increase or decrease, the output power of the energy storage system P_{ESS} changes almost instantaneously to match

the load transient, then gradually reduces to zero; in this way, the primary power source P_S adapts to the new load conditions in a gentle, well-controlled manner.

However, whilst providing this operation, the system controller must also manage the state-of-charge (SoC) of the storage system, preventing under or over charging. The system diagram in Figure 3.1 shows the two control actions in simplified form: one based on the load power, $P_{ESS\text{-}L}$, and the second based on the state-of-charge, $P_{ESS\text{-}re}$.

The work in this chapter is based on the electrical system in IEPNEF (as described in Chapter 1, Section 1.1.3), where the power sources are two generators and the emulated dynamic loads include actuators, landing gear, avionic's systems, etc. In the following sections, a super-capacitor based energy storage system is designed and modelled for this system, followed by an explanation of the control, including parameter selection, and finally the system performance is evaluated using a hardware-in-the-loop (HIL) emulator.

3.2.1 ESS system modelling

Figure 3.3 shows the power circuit of the ESS, a super-capacitor bank and a DC-DC converter, which are connected to a DC distribution network comprising the load and the power source.

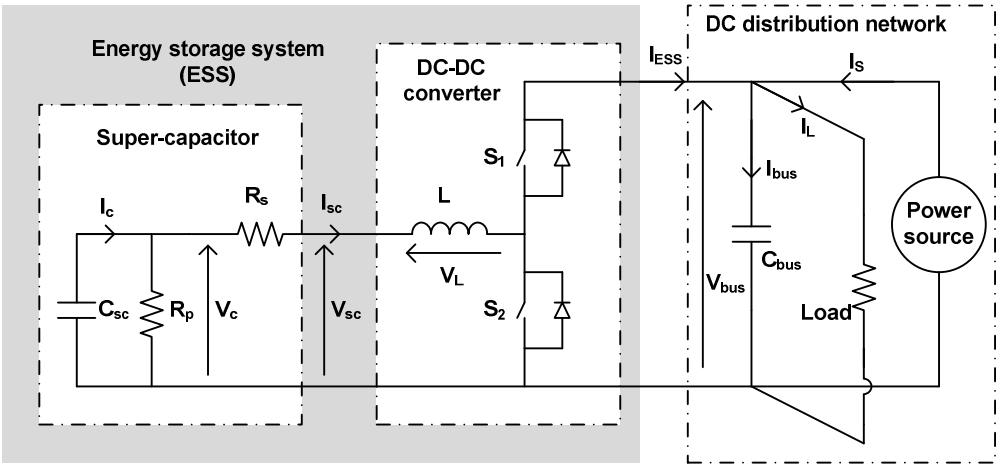


Figure 3.3. Model of the energy storage system in the DC distribution network.

For simplicity, a single-leg topology is assumed for the DC-DC converter, however an interleaved circuit as discussed in Chapter 2 could well be used to reduce the input and output ripple currents and the individual device currents. The DC bus voltage V_{bus} is regulated by the power source, for example a generator control unit. The bus filter capacitor C_{bus} represents the total capacitance on the DC bus.

3.2.1.1 Super-capacitor modelling

The super-capacitor is modelled using the simple equivalent circuit [165] comprising series resistance R_s and leakage resistance R_p as shown in Figure 3.3, which provides a good compromise between accuracy, complexity and simulation time for system level studies [166]. Through some derivation, the super-capacitor can be represented by the state-space Equation (3.1).

$$\begin{aligned} \dot{V}_c &= -\frac{1}{R_p C_{sc}} V_c - \frac{1}{C_{sc}} I_{sc} \\ V_{sc} &= V_c - R_s I_{sc} \end{aligned} \tag{3.1}$$

where V_c is the state variable, the voltage on the ideal capacitor, C_{sc} is the super-capacitor capacitance, and V_{sc} is the terminal voltage of the super-capacitor, Figure 3.3. The parameters of super-capacitor, R_p, R_s, and C_{sc} are assumed to be constants.

3.2.1.2 DC-DC Converter modelling

A half-bridge bi-directional DC-DC converter is used as shown in Figure 3.3, in which the switches of the half-bridge are assumed to operate in a complementary pattern. By denoting the duty ratio of the bottom switch S_2 as D and assuming ideal switches and lossless conversion, the averaged voltage applied across the inductor is derived as (Appendix B.1):

$$V_L = L\frac{dI_{sc}}{dt} = V_{sc} - V_{bus}(1-D) \tag{3.2}$$

On the bus side, the current I_{bus} can be derived as:

$$I_{bus} = C_{bus}\frac{dV_{bus}}{dt} = I_{ESS} + I_S - I_L \tag{3.3}$$

where I_{ESS} is the energy storage system output current, I_L is the total load current, and I_S is the power source current as labelled in Figure 3.3.

By assuming zero initial conditions and taking Laplace transforms, Equation (3.2) and (3.3) become:

$$I_{sc} = \frac{V_{sc} - V_{bus}(1-D)}{sL} \tag{3.4}$$

$$V_{bus} = \frac{I_{ESS} + I_S - I_L}{sC_{bus}} \tag{3.5}$$

where s is the Laplace operator.

Equation (3.4) and (3.5) describe the averaged dynamic characteristics of the converter for frequencies well below the switching frequency and are used as the basis of the current controller design in the next section.

3.2.1.3 Current controller for the converter

The control of the converter is based on a current feedback loop to regulate the inductor current, (I_{sc} in this case, Figure 3.3), since the inductor current is one of the system state variables and plays an important role in determining the converter input and output currents. The closed-loop current control system, assuming the use of a simple PI controller, is shown in Figure 3.4.

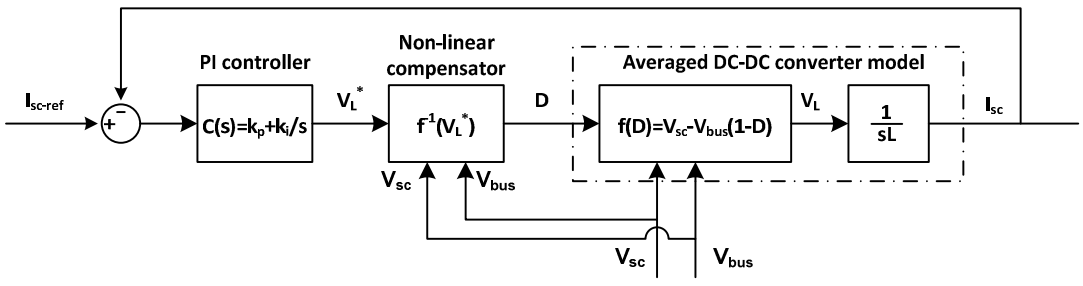


Figure 3.4. Super-capacitor current controller using the non-linear compensator.

In Figure 3.4, the DC-DC converter is represented by the non-linear system described by Equation (3.4), in which the input is duty ratio D and the output is the super-capacitor current I_{sc}. To linearize the system, a compensator is added in the loop to cancel the non-linearity [128].

By denoting the average inductor voltage V_L as a function of D, f(D):

$$V_L = f(D) = V_{sc} - V_{bus}(1-D) \tag{3.6}$$

the compensator function $f^{-1}(V_L^*)$ is then the inverse of Equation (3.6), and can be determined as:

$$D = f^{-1}(V_L^*) = 1 - \frac{V_{sc} - V_L^*}{V_{bus}} \tag{3.7}$$

where V_L* is the output signal from the PI controller.

A linear system transfer function P(s) relating I_{sc} and V_L^* can then be determined from Figure 3.4 and Equation (3.7) as:

$$P(s) = \frac{I_{sc}}{V_L^*} = \frac{f(f^{-1}(V_L^*)) \cdot \frac{1}{sL}}{V_L^*} = \frac{1}{sL} \tag{3.8}$$

The inclusion of the non-linear compensator in P(s) enables Equation (3.8) to have a simple first order characteristic.

The PI controller denoted C(s) takes the following form:

$$C(s) = k_p + k_i / s \tag{3.9}$$

where k_p and k_i are the proportional and integral constants.

The open-loop and closed-loop transfer functions L(s) and T(s) of the current control loop can be derived from Equation (3.8) and (3.9) as:

$$L(s) = C(s) \cdot P(s) = (k_p + \frac{k_i}{s}) \cdot \frac{1}{sL} \tag{3.10}$$

$$\frac{I_{sc}}{I_{sc-ref}} = T(s) = \frac{C(s) \cdot P(s)}{1 + C(s) \cdot P(s)} = \frac{\frac{k_p(s + \frac{k_i}{k_p})}{L(s^2 + \frac{k_p}{L}s + \frac{k_i}{L})}}{} \tag{3.11}$$

The unity gain cross-over frequency ω_c in L(s) can be determined as, $\omega_c = k_p/L$, by substituting $s = j\omega_c$ into Equation (3.10) and assuming ω_c is large. The denominator of the closed loop transfer function T(s) in Equation (3.11) can be compared to the classic second

order differential equation [92] to enable k_p and k_i to be calculated using Equation (3.12) and (3.13) for a specific natural frequency ω_n and damping ratio ζ, giving:

$$2\zeta\omega_n = k_p / L \tag{3.12}$$

$$\omega_n^2 = k_i / L \tag{3.13}$$

To avoid any switching frequency related instabilities, ω_c would typically be chosen to be well below half of the switching frequency of the DC-DC converter. The damping ratio ζ would be chosen to be between 0.7 and 1 as a compromise between the speed of response to errors in I_{sc} and limiting the potential overshoot in I_{sc}. The k_p and k_i values can then be calculated based on ω_c and ζ values.

3.2.2 ESS system controller

Arising from the ESS requirements of following instantaneous load changes and managing super-capacitor state-of-charge, the reference signal $I_{sc\text{-}ref}$ for the current controller in Figure 3.4 has two components, $I_{sc\text{-}L}$ and $I_{sc\text{-}re}$ in Figure 3.5 which form $I_{sc\text{-}ref}=I_{sc\text{-}L}-I_{sc\text{-}re}$.

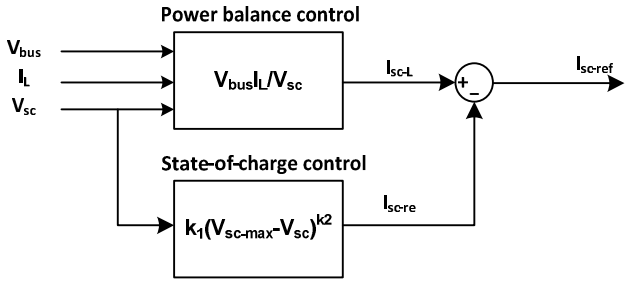


Figure 3.5. Two components of the super-capacitor current reference.

The first component $I_{sc\text{-}L}$ is determined based on the power balance calculation shown in Equation (3.14). Assuming lossless conversion [167], this will ensure that any instantaneous load changes are immediately compensated by a corresponding power flow to/from the super-capacitor bank. Measured values of bus voltage V_{bus}, super-capacitor voltage V_{sc} and the load current I_L are used to determine the $I_{sc\text{-}L}$ current reference component.

$$I_{sc-L} = \frac{V_{bus} \cdot I_L}{V_{sc}} \tag{3.14}$$

The second component $I_{sc\text{-}re}$ regulates the recharge power and is intended to vary much more slowly to manage the state-of-charge of the super-capacitor. Intuitively speaking, the recharge current shall increase as the super-capacitor voltage drops, and this is indicated by an error between actual super-capacitor voltage and the fully charged value. The form of the proposed function is shown in Equation (3.15) with two additional control parameters k_1 and k_2 which gives more control flexibility.

$$I_{sc-re} = k_1(V_{sc-\max} - V_{sc})^{k_2} \tag{3.15}$$

where $V_{sc\text{-}max}$ is a fixed reference voltage and is the full super-capacitor voltage, k_1 and k_2 are two parameters (both above zero) which affect the rate of charge of the super-capacitor.

In the case when a load is applied so $I_{sc\text{-}L}>0$ and the super-capacitor is fully charged, i.e., $V_{sc}=V_{scmax}$, so $I_{sc\text{-}re}=0$, the resultant $I_{sc\text{-}ref}=I_{sc\text{-}L}-I_{sc\text{-}re}$ will give a positive command to the converter to discharge the super-capacitor. As the super-capacitor voltage V_{sc} gradually decreases due to the discharging process, the component $I_{sc\text{-}re}$ will increase because of the increasing error, $V_{sc\text{-}max}-V_{sc}$, which reduces the super-capacitor current reference $I_{sc\text{-}ref}$. If the load is kept unchanged, $I_{sc\text{-}re}$ will eventually match the load current component $I_{sc\text{-}L}$ in steady-state, Equation (3.16), producing a zero current reference $I_{sc\text{-}ref}$, and command no further current from the super-capacitor:

$$I_{sc-L} = \frac{V_{bus} \cdot I_L}{V_{sc}} = k_1(V_{sc-\max} - V_{sc})^{k_2} = I_{sc-re} \tag{3.16}$$

Equivalent powers, $P_{sc\text{-}L}$, $P_{sc\text{-}re}$ and $P_{sc\text{-}ref}$, corresponding to $I_{sc\text{-}L}$, $I_{sc\text{-}re}$ and $I_{sc\text{-}ref}$ respectively can be defined as:

$$P_{sc-L} = V_{sc} \cdot I_{sc-L} = V_{bus} \cdot I_L = P_L \tag{3.17}$$

$$P_{sc-re} = V_{sc} \cdot I_{sc-re} = V_{sc} \cdot k_1(V_{sc-\max} - V_{sc})^{k_2} \tag{3.18}$$

$$P_{sc-ref} = V_{sc} \cdot I_{sc-ref} = V_{sc} \cdot (I_{sc-L} - I_{sc-re}) = P_{sc-L} - P_{sc-re} \tag{3.19}$$

Using Equations (3.17) to (3.19), Equation (3.16) can be rewritten in the following form by multiplying through by V_{sc}:

$$P_{sc-L} = P_L = k_1 V_{sc}(V_{sc-\max} - V_{sc})^{k_2} = P_{sc-re} \tag{3.20}$$

Equations (3.16) and (3.20) show the steady-state condition when the two current or power reference components are equal. The equations show that the super-capacitor will be fully charged in steady-state at no load, i.e., P_L=0, V_{sc}=$V_{sc\text{-}max}$ and therefore sufficient energy will be available to meet any rapid load turn-on transient. Furthermore, under equilibrium conditions, the super-capacitor will be heavily discharged when the DC bus is fully loaded, ensuring that maximum energy storage capacity is available to absorb the source current transiently should the load current suddenly decrease.

The parameters k_1 and k_2 should therefore be suitably chosen to achieve this goal without exceeding the super-capacitor working voltage limits. The simplest parameter choice is to set k_2=1, giving $I_{sc\text{-}re}$=k_1($V_{sc\text{-}max}$-V_{sc}) or equivalently $P_{sc\text{-}re}$=k_1V_{sc}($V_{sc\text{-}max}$-V_{sc}); however, other combinations of k_1 and k_2 are possible.

One consideration when choosing suitable k_1 and k_2 parameters is that the maximum recharge power component in Equation (3.18) should not be below the maximum load power, max{$P_{sc\text{-}re}$}≥$P_{L\text{-}max}$. Otherwise an equilibrium condition will not be reached, leading to the energy storage unit being completely emptied, since the power balance of $P_{sc\text{-}re}$=$P_{L\text{-}max}$ could never occur.

By setting the derivatives of Equation (3.18) to zero, the maximum of $P_{sc\text{-}re}$ can be found to occur when V_{sc}=$V_{sc\text{-}max}$/(1+k_2) and the maximum value as a function of k_1 k_2 and $V_{sc\text{-}max}$ is given by Equation (3.21).

$$\max\{P_{sc-re}\} = \frac{k_1 k_2^{\,k_2} V_{sc-\max}^{\,(1+k_2)}}{(1+k_2)^{1+k_2}} > P_{L-\max} \tag{3.21}$$

Figure 3.6 shows a sample curve of recharge power $P_{sc\text{-}re}$ against super-capacitor voltage V_{sc}, Equation (3.18), with the featured local maximum point described by Equation (3.21). Assuming that a load P_L is applied such that $P_{sc\text{-}L}=P_L$, Equation (3.17), two equilibrium operating points exist as shown in Figure 3.6 where the horizontal line $P_{sc\text{-}L}$ intersects with the $P_{sc\text{-}re}$ curve. The power reference $P_{sc\text{-}ref}=P_{sc\text{-}L}-P_{sc\text{-}re}$, Equation (3.19), is positive if $P_{sc\text{-}L}>P_{sc\text{-}re}$, commanding the super-capacitor to supply power, which would result in V_{sc} falling towards an equilibrium point where $P_{sc\text{-}L}=P_{sc\text{-}re}$. Alternatively, the super-capacitor voltage will increase when $P_{sc\text{-}L}<P_{sc\text{-}re}$, which in turn would tend to reduce $P_{sc\text{-}re}$ so as to reach the equilibrium point. This gives rise to a stable operating region with a given load, illustrated in Figure 3.6. The section beyond the left intersection point is an unstable region, and the super-capacitor energy will be depleted completely should the system enter this zone.

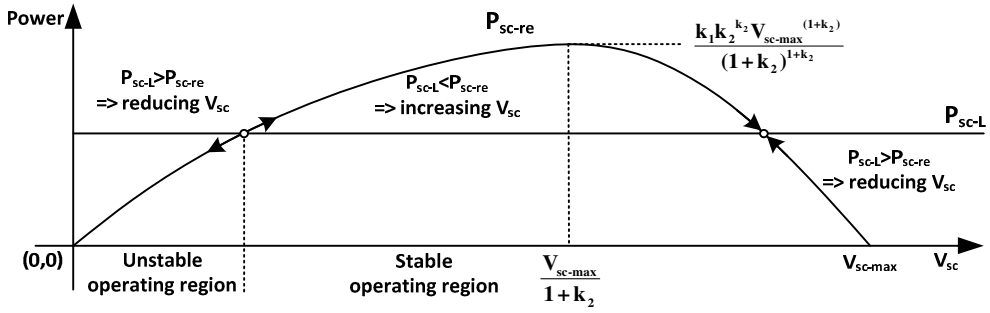


Figure 3.6. Characteristic of $P_{sc\text{-}re}$ against V_{sc}, Equation (3.18).

In pratical, when ESS losses are taken into account, the relationship in Figure 3.6 still applies. However, the losses indicate less energy is effectively used mitigating load transient while discharing, and longer charge time will be required for a specific super-capacitor voltage target in a charge process.

The function of $P_{sc\text{-}re}$ is not restricted by the form of Equation (3.18), any form of $P_{sc\text{-}re}=f(V_{sc})$ can be used giving the characteristics of targeted super-capacitor voltage for a specific power. A more general analysis of the energy storage system state-of-charge control is described in Chapter 4.

3.3 ESS simulation in DC electrical system

A Simulink model was created for the energy storage system shown in Figure 3.3, based on the modelling of the ESS and its controller described in Section 3.2, to examine the ESS performance in relieving the impact of a load disturbance in the DC electrical system on the main power source.

3.3.1 Simulation configuration

A schematic of the Simulink model diagram is given in Appendix B.2 consisting of an ESS, a generator, a load, and a DC bus where they are connected as shown in Figure 3.1. The parameters of the devices are given in Table 3.1, and they are all based on real devices either in the IEPNEF lab or in reported literature which will be described later.

Table 3.1. Simulation parameters

ESS hardware	Super-capacitor	R_s	3x7.5mΩ=22.5mΩ			
		R_p	3x10kΩ=30kΩ			
		C_{sc}	165F/3=55F			
		$V_{sc\text{-}max}$	135V			
		$V_{sc\text{-}min}$	60V			
	DC-DC converter	L	100μH			
		f_s	30kHz			
		D	range: 0.05 to 0.95			
ESS control	Current controller	ω_c	2π·8000rad/s			
		k_p	5.03			
		k_i	80k			
		P_m	73.2°			
	SoC controller	k_1	5.56	0.64	0.0741	8.55m
		k_2	1	1.5	2	2.5
DC bus		V_{bus}	540V			
		C_{bus}	800μF			
Power source		-	five phase PMG, 70kW			
Load		$P_{L\text{-}max}$	25kW DC load			
Simulation model		Time step	10μs			
		Solver	ode1			

Three 48V super-capacitor modules are assumed to be connected in series to form a bank with a total energy of 0.57MJ. The total energy is approximately rated for an aircraft gas-engine start [168], however energy is only one consideration when sizing the module with other factors, such as terminal voltage, peak power, volume and weight together with the

design of the DC-DC converter, needing to be carefully evaluated. Optimising the super-capacitor bank for a specific application is outside the scope of this thesis. The total equivalent R_s, R_p and C_{sc} are obtained from manufacturer's data sheet (Maxwell, BMOD0165 [169]). The maximum working voltage $V_{sc\text{-}max}$ is set at 135V, considering the absolute maximum voltage is 48x3=144V. The minimum voltage $V_{sc\text{-}min}$ is set at 60V, which is chosen to be approximately half of the maximum working voltage as a compromise between usable energy and the capacitor and converter current level when the super-capacitor voltage is low [48]. The DC-DC converter is assumed to have a switching frequency of 30kHz, an inductor of 100μH [170] and its duty ratio is limited to be within the range of 0.05 to 0.95.

The current controller is designed for a cross-over frequency of ω_c=8kHz, well below half of the DC-DC converter switching frequency, and a damping ratio of 0.889. k_p and k_i which set the closed-loop response can be calculated from this information according to Equation (3.12) and (3.13), and are listed in Table 3.1 and give a phase margin of P_m=73.2°.

The k_1 and k_2 parameters of the state-of-charge controller are chosen such that the super-capacitor voltage will be 60V ($V_{sc\text{-}min}$) at full load power $P_{L\text{-}max}$=25kW as defined in Table 3.1. By substituting $V_{sc\text{-}max}$=135V, $V_{sc\text{-}min}$=60V and $P_{L\text{-}max}$=25kW into Equation (3.20), the following equations can be obtained to determine k_1 and k_2 which satisfy the stated condition:

$$25 = k_1 \cdot 60 \cdot (135 - 60)^{k_2} \tag{3.22}$$

k_2 values of 1, 1.5, 2, and 2.5 are considered and the associated k_1 values can be calculated according to Equation (3.22) and are listed in Table 3.1.

In addition to the ESS model, a power source and load are also modelled to form the full DC electrical system as shown in Figure 3.1. The power source was represented by a five phase permanent magnet generator (PMG) and a converter system which provides a regulated 540V DC output. This generator model (containing the converter system) was developed as part of a related research programme [9]. The load network was modelled as a single load element, either a defined resistance value or an ideal constant power load.

The simulation is run with a fixed time-step of 10μs using the Simulink built-in first-order ordinary differential equation (ODE) solver, 'ode1', which gives both acceptable accuracy and computational speed.

3.3.2 Simulation results

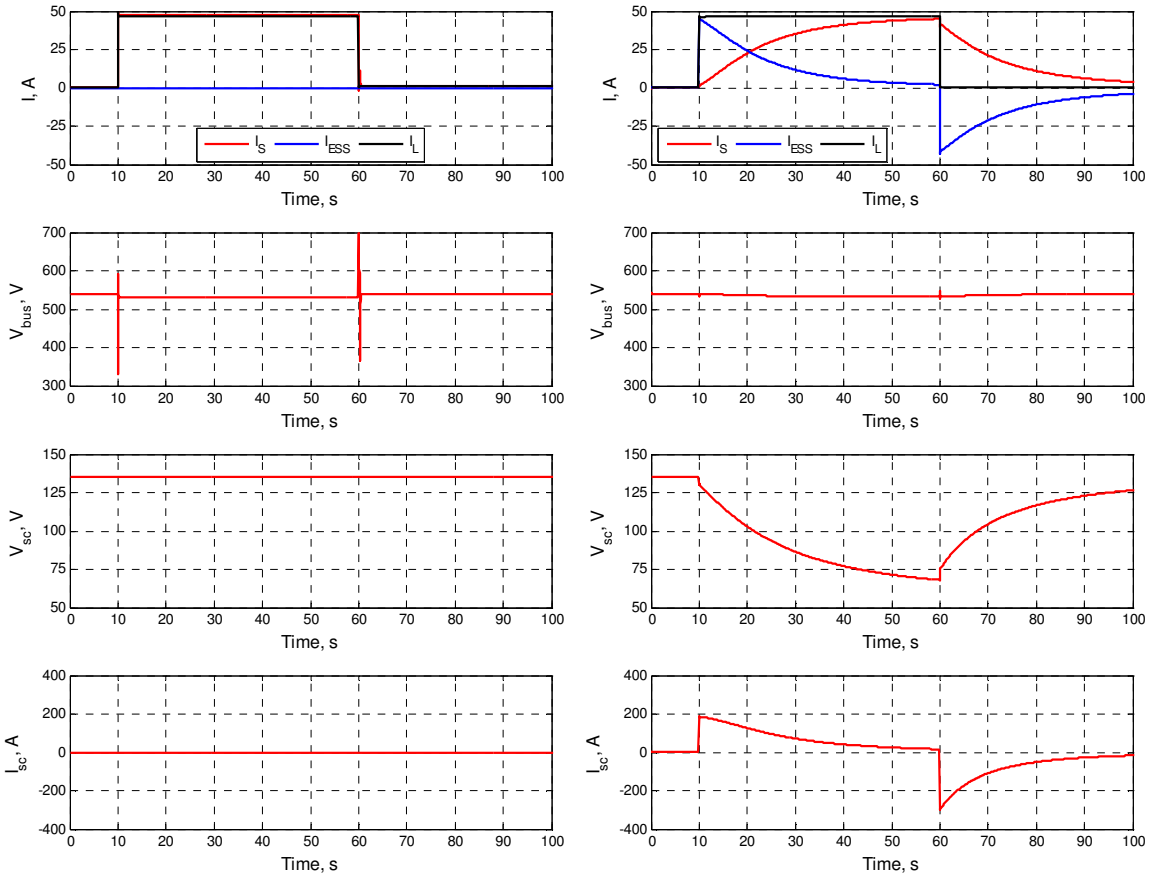
The simulation model was tested for different load profiles. Constant power loads were used in the simulation as these are becoming increasingly common in aircraft [171] and other DC networks; resistive loads were also simulated but are not presented here, since the results were almost the same. The simulation results presented in this section are for a full power load (zero to 25kW) step, with the power increase occurring at t=10s and decreasing at t=60s. The generator control was regulating the DC bus to 540V and the generator droop control was active which provides a linear, 20V drop in bus voltage as the generator power increases from zero to maximum [9].

3.3.2.1 Simulation results using k_1=0.64 and k_2=1.5

Figure 3.7 shows the system simulation without the ESS on the left, and with the ESS using the recharge parameters of k_1=0.64 and k_2=1.5 on the right.

The first set of waveforms in Figure 3.7 show the load current I_L (black), the ESS current I_{ESS} (blue) and the resultant source or generator current I_S (red) where $I_S=I_L-I_{ESS}$. The bus voltage V_{bus}, super-capacitor voltage V_{sc} and current I_{sc} are shown in the second, third and fourth plots respectively.

The load current switches from zero to 47A (25kW) at a time of 10s, then switches back to zero at 60s. In Figure 3.7a where the ESS is inactive, the ESS current is always zero and the PMG provides all the load which results in the severe bus voltage transients (100ms) due to the slow dynamics of the generator. The steady-state difference in bus voltage is due to the action of the generator droop control [9].



(a) ESS inactive. **(b) ESS active.**

Figure 3.7. Simulation results of full power step load, k_1=0.64, k_2=1.5.

In Figure 3.7b, the severe generator transients are moderated by the action of the ESS. As the load current rises at time 10s, the ESS responds almost instantaneously to provide the additional load current, but then gradually falls back to zero, resulting in a gradual increase in generator current. There is a corresponding flow of current from the super-capacitor and the super-capacitor voltage falls. When the load current falls, the reverse process occurs. Only small transients are noticeable in the bus voltage when the load current changes and the bus voltage is again seen to fall slightly during the period of increased load due to the action of the droop controller [9] in the generator system. The instantaneous steps in super-capacitor voltage V_{sc} at t=10s and 60s are due to the voltage drop across the super-capacitor equivalent series resistance.

3.3.2.2 Simulation results using different k_1, k_2

To illustrate the effect of different controller parameters k_1 and k_2, the simulation in Figure 3.7 was repeated with the different pairs of values for k_1 and k_2 listed in Table 3.1. Figure 3.8 shows $P_{sc\text{-}re}$, the super-capacitor recharge power against the super-capacitor voltage V_{sc}, calculated from Equation (3.20), for the k_1 and k_2 combinations from Table 3.1.

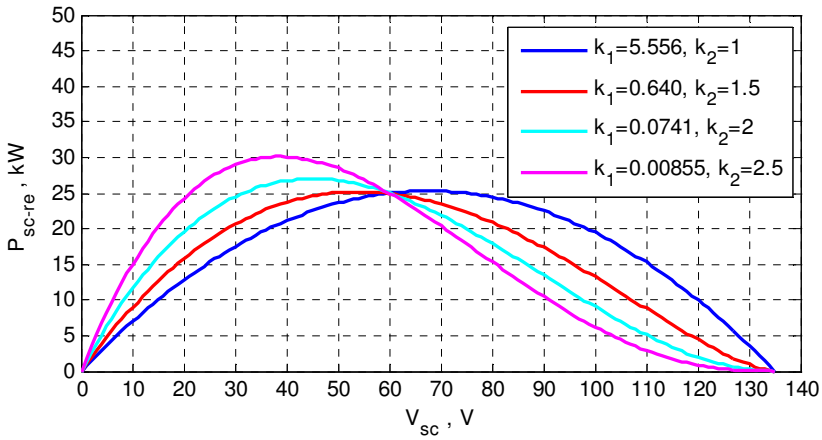


Figure 3.8. Characteristics of $P_{sc\text{-}re}$ against V_{sc} with different k_1 and k_2 parameters.

According to the common design constraints, all the curves in Figure 3.8 show zero super-capacitor recharge power $P_{sc\text{-}re}$ when V_{sc}=135V, corresponding to the fully charged condition, and the recharge power is 25kW when V_{sc}=60V, corresponding to the maximum load condition.

As discussed in Section 3.2.2, each curve in Figure 3.8 has a maximum recharge power which sets the maximum possible steady-state load level. For example, an equilibrium would not be reached when a 30kW load was applied except with k_1=0.00855, k_2=2.5 in Figure 3.8.

Another noticeable feature in Figure 3.8 is that with increasing k_2 the super-capacitor voltage will settle to a lower steady-state voltage with a given load power. For example, when a 15kW load is applied, the curve of k_2=1 has the highest steady-state super-capacitor voltage at around 110V, while the k_2=2.5 curve shows that V_{sc} falls to 81V.

The simulation results in Figure 3.9 show the same simulation conditions, generator control and load profile as in Figure 3.7, but with the different pairs of controller parameters k_1 and k_2 listed in Table 3.1. The results in the figure have an identical initial super-capacitor voltage of 135V. For larger values of k_2, the energy storage system

responds more strongly to the initial load step resulting in a more gradual load increase on the generator and a deeper discharge of the super-capacitor.

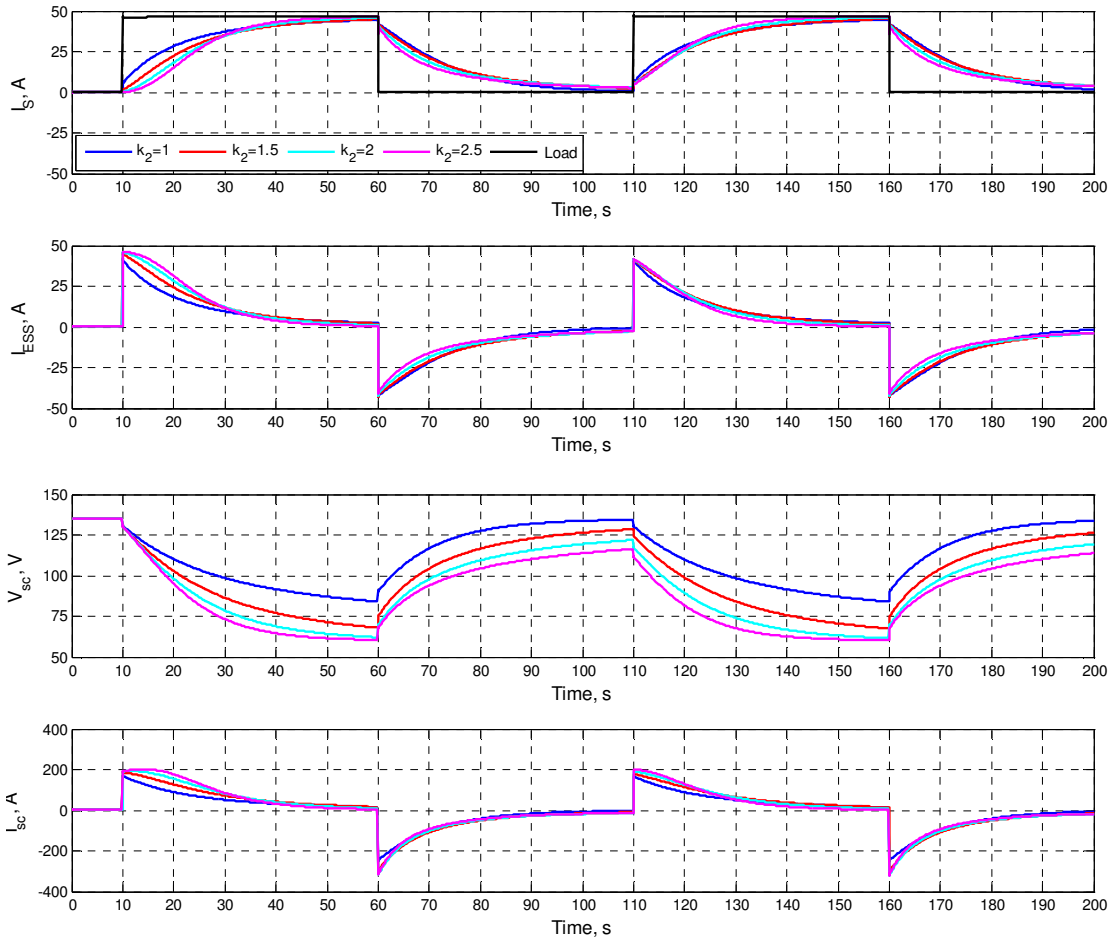


Figure 3.9. Simulation results for full power step load with different k_1 k_2, initial V_{sc} = 135V, $V_{sc\text{-}max}$=135V.

According to the prediction in Figure 3.8, the super-capacitor voltage in Figure 3.9 should drop to 60V in the steady-state since the applied load is the maximum power level of 25kW. At t=60s, only the result with parameter k_2=2.5 reaches the steady-state voltage of 60V. The control parameter combinations with k_2<2.5 have a slower response and so are yet to reach a steady-state value at t=60s; however in each case, the trajectory of the super-capacitor voltage is on target for 60V. The same phenomenon is observed at t=110s, when the expected super-capacitor voltage should be the maximum (135V) since the load is zero. The current charging the super-capacitor for k_2=2.5 is -12A at t=110s, resulting in the slow charging of the super-capacitor.

After t=60s, the generator power transients using different k_1 k_2 combinations become much more similar, and the waveforms tend to repeat over each cycle. The system is approaching a dynamic steady-state in which the super-capacitor voltage varies

periodically around an average level, which is set by the average load power. In this case with 25kW load pulses of 50% duty ratio, the average power is 12.5kW and the average super-capacitor voltage will tend to the steady-state values that arise from the control parameter values k_1 and k_2 as predicted in Figure 3.8.

To illustrate further the manner in which the super-capacitor voltage settles to a steady-state average level, the simulation in Figure 3.9 was repeated with the initial super-capacitor voltage set to 100V as shown in Figure 3.10.

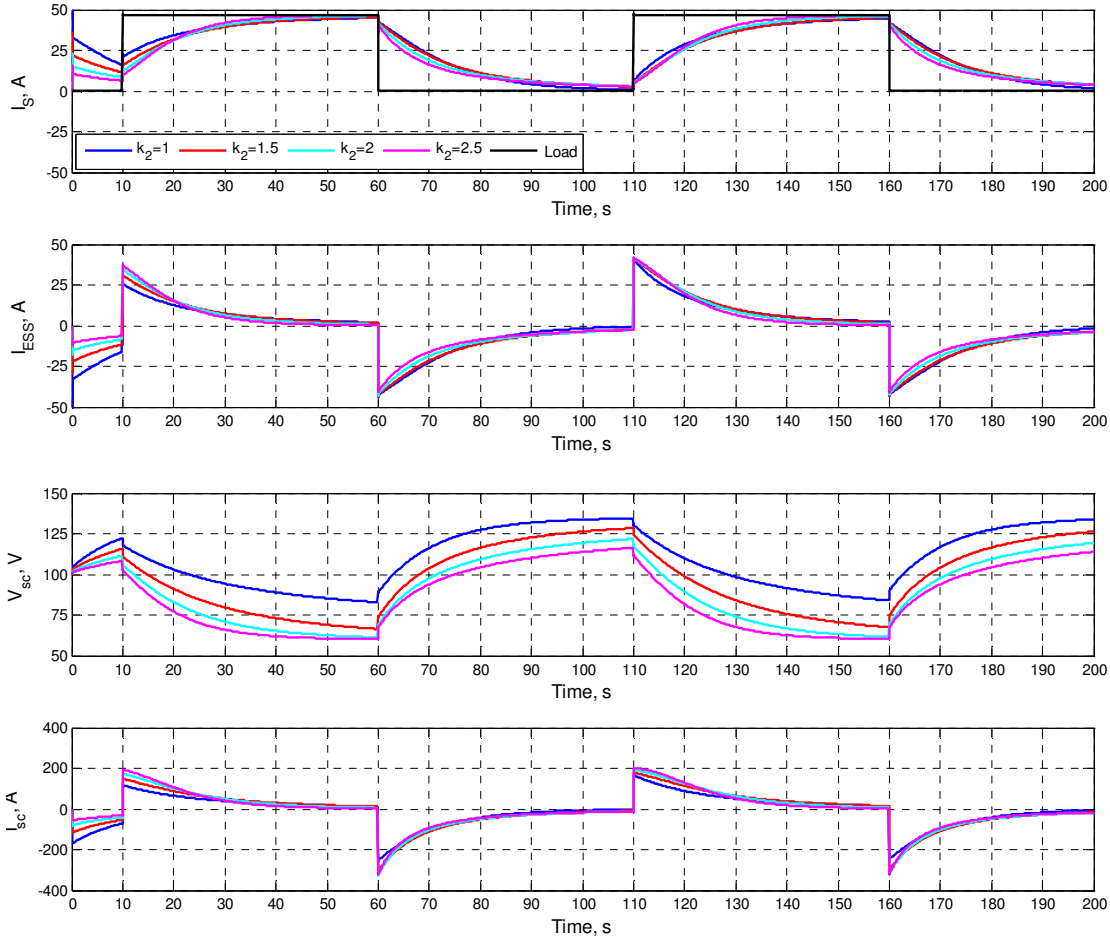


Figure 3.10. Simulation results for full power step load with different k_1 k_2, initial V_{sc}=100V, $V_{sc\text{-}max}$=135V.

The key difference between Figure 3.9 and Figure 3.10 is that during the first 10 seconds in Figure 3.10, the generator current is positive even when the load is zero, which charges the super-capacitor and its voltage rises as shown in the third plot. The charging current is commanded by the $I_{sc\text{-}re}$ component, and since $I_{sc\text{-}re}=k_1(V_{sc\text{-}max}-V_{sc})^{k2}>0$, the current reference $I_{sc\text{-}ref}=I_{sc\text{-}L}-I_{sc\text{-}re}<0$ which causes the super-capacitor to be charged.

The voltage and current responses in Figure 3.10 are identical to those in Figure 3.9 after t=60s showing that the control drives the average super-capacitor voltage to the predicted steady-state levels in Figure 3.8.

A final simulation is presented to highlight the relationship between ESS energy and source (generator) response. The available energy in the super-capacitor is limited by lowering $V_{sc\text{-}max}$ in Figure 3.8 while keeping the same $V_{sc\text{-}min}$; which is similar to having a reduced number of super-capacitor modules. In the simulation results in Figure 3.11, $V_{sc\text{-}max}$ is set at 100V while $V_{sc\text{-}min}$ is again at 60V, giving a 56% reduction in energy compared with the higher $V_{sc\text{-}max}$ configuration. The ESS response to a load change in Figure 3.11 is still instantaneous, however the control rapidly reduces the output power of the ESS to zero since less energy is available. The more rapid reduction in ESS power causes a more rapid change in source power. All the control profiles except k_2=1 reach a steady-state super-capacitor voltage of 60V during the high load period, while during the zero load period, only the result with k_2=1 enters steady-state with a super-capacitor voltage of 100V due to the small current charging the super-capacitors.

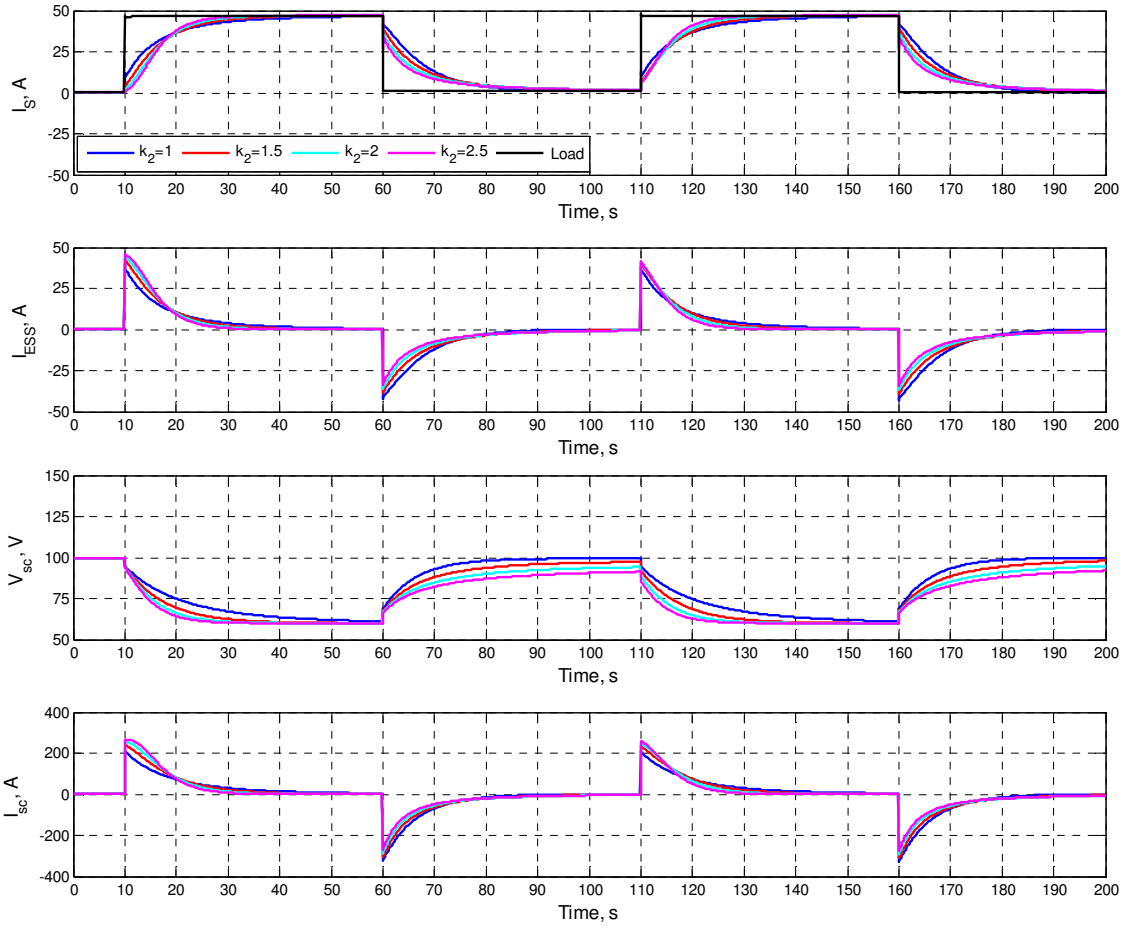


Figure 3.11. Simulation results for full power step load with different k_1 k_2, initial V_{sc}=100V, $V_{sc\text{-}max}$=100V.

3.4 ESS emulation in the IEPNEF DC electrical system

To illustrate the operation of the energy storage system controller and the effect that the device has on a practical electrical system, the energy storage system was emulated in the IEPNEF system using one of the programmable bi-directional active load units.

3.4.1 Experiment configuration

The overall system diagram for the experiments is shown in Figure 3.12, where the DC electrical bus and the connected devices are on the right. The 70kW permanent magnet generator (PMG) located in IEPNEF is used as the main power source. The two active load systems on the DC bus act as the dynamic electrical load and the ESS respectively. A resistive bank is connected to the bus as the background load.

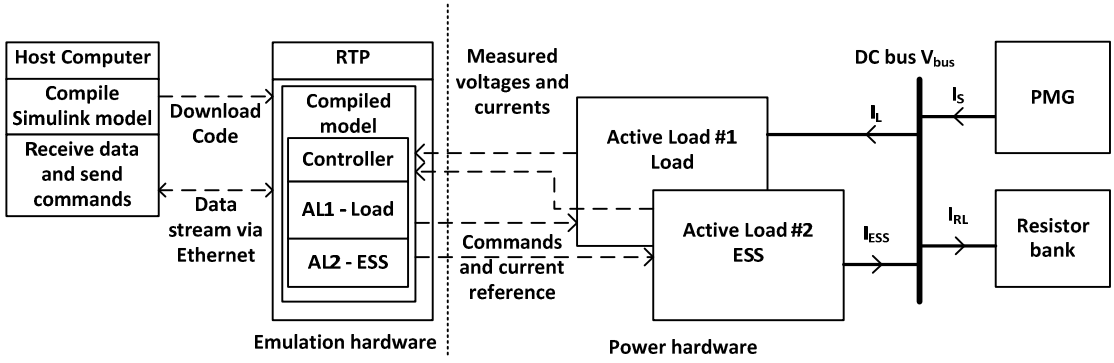


Figure 3.12. Structure of ADI RTP and the IEPNEF DC network.

The two active loads are controlled to produce the required DC bus currents I_L and I_{ESS} by a real-time platform (RTP), Figure 3.12 (manufactured by Applied Dynamics International (ADI)). The RTP is programmed by the host computer, and the program code for the active load units is compiled in the host computer from a Simulink model and then downloaded to the RTP. The signals measured by the RTP are transmitted through Ethernet to the host computer for data storage and post-analysis.

To facilitate easy communication with the RTP system, a graphical user interface (GUI) (Appendix B.4) was created on the host computer using LabView, enabling simple commands for high level control to be sent through an Ethernet connection, including ESS enable/disable, or setting power levels for the active loads, and the monitoring of model variables. The LabView GUI is then mapped to the Simulink model variables in the RTP.

This approach enables load profiles and ESS modes to be changed in a single test without modifying, compiling and re-downloading the program.

To emulate the ESS using one of the active loads (Active Load #2), the Simulink model in Section 3.3 was used to form the code to command the active load unit. The measured bus voltage and current were used as input signals to the RTP for the ESS control and the resultant simulated current that the ESS draws or delivers from or to the DC bus was used to command the output current of the active load. The real-time model ran with a cycle time of 10μs. The emulation technique allows interactions between the ESS and the electrical network and generator to be examined.

The simulation program to emulate the dynamic load using another active load (Active Load #1) was built using the State-flow block in Simulink, which commands repeating cycles of load steps with variable duration and power level, as illustrated in Figure 3.13. The State-flow code is given in Appendix B.3.

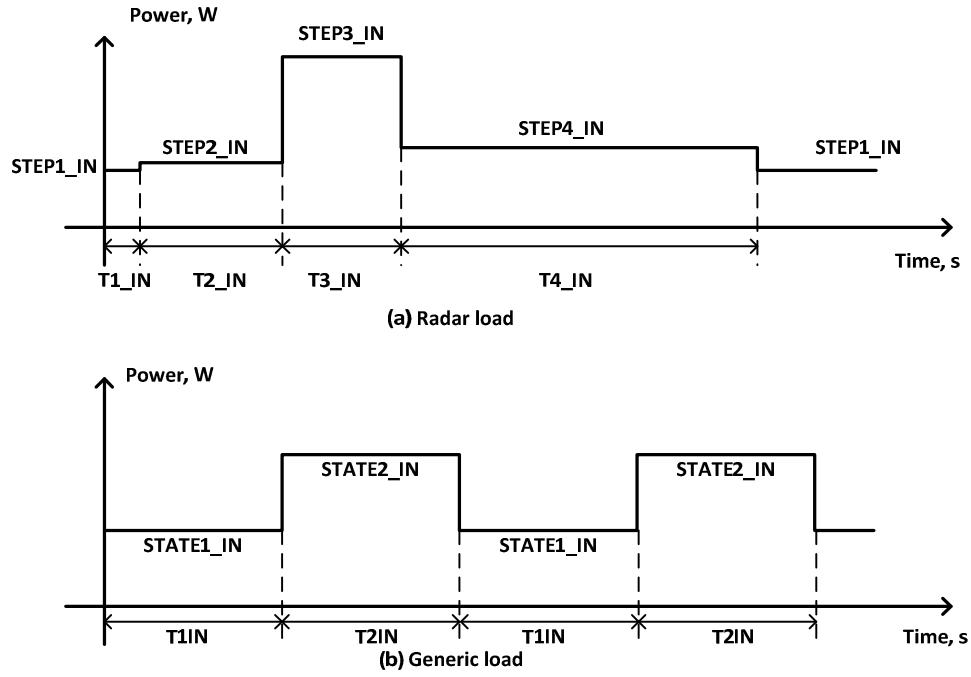


Figure 3.13. Programmable load profiles.

The load profiles in Figure 3.13 show two types of on-board electrical loads. The first load represents a hypothetical model of a multi-functional radar load profile which was provided through industrial contacts at Rolls-Royce. The time and power parameters of the load profiles used for the experiments are provided in Table 3.2. The second load has a

simple generic profile switching between two power levels. In the test results presented in the following section, active load steps between 1kW to 10kW are used together with a 22kW resistive load. In each case, the active load is commanded by a current reference which is calculated in real-time by dividing the required power by the measured bus voltage, thereby providing a constant power type of characteristic.

Table 3.2. Parameters of the load profiles

Radar load				Generic load			
Time interval	Time interval duration	Power step	Power step value	Time interval	Time interval duration	Power step	Power step value
T1_IN	5s	STEP1_IN	4kW	T1IN	1s	STATE1_IN	1kW
T2_IN	25s	STEP2_IN	5kW	T2IN	1s	STATE2_IN	10kW
T3_IN	20s	STEP3_IN	21kW				
T4_IN	60s	STEP4_IN	7kW				

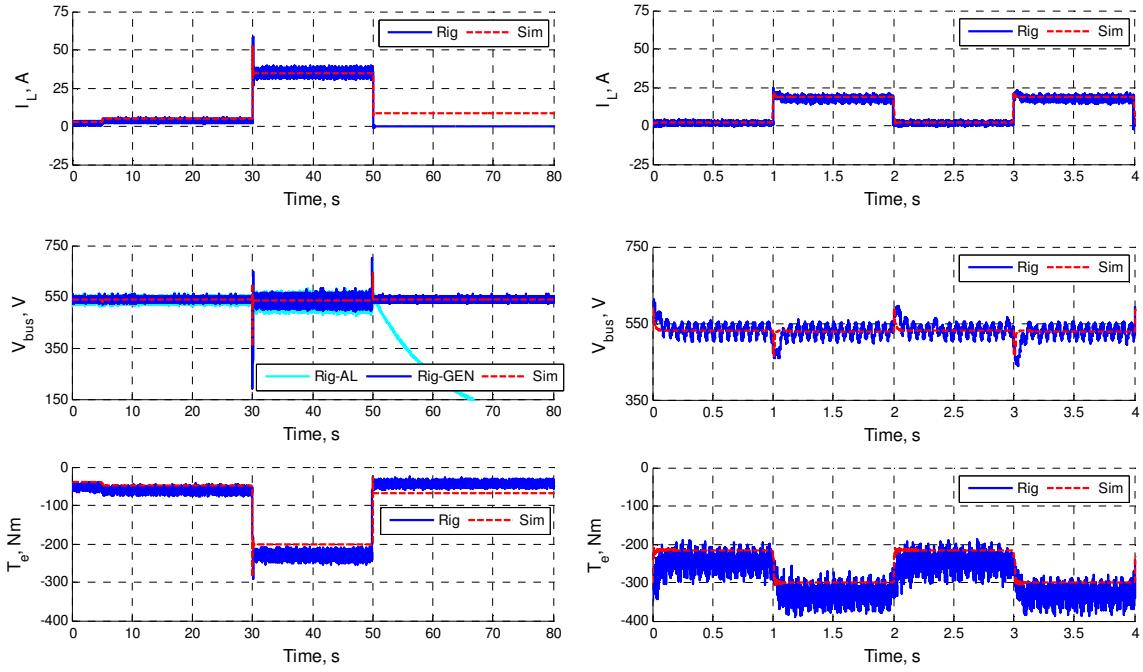
3.4.2 Experimental validation

This section presents the results obtained using the active loads to emulate the ESS and impose load profiles on the DC bus. The measured data is compared with simulation results from the model described in Section 3.3 where good agreement is found.

3.4.2.1 Emulation results with ESS inactive

The emulated radar load and pulse load in Table 3.2 were applied in turn to observe the bus voltage transients and torque changes of the generator and compare the responses with and without the ESS. The generator controller regulates the DC bus to 540V. Since the generator is driven at constant speed of 1006rpm [12], the torque is proportional to the output power of the generator. The transient torque also indicates the stress that the generator and the prime mover may have to withstand.

Figure 3.14a shows the measured test results (in blue) together with simulation results (in red) for a radar profile with a 2.4kW background resistive load when the ESS is inactive. The use of additional background resistive load ensures bus voltage stability, due to the requirement of generator control unit. A large voltage deviation can be seen due to the load change at t=30s and t=50s, which is reflected in the torque change shown in the third plot. The bus voltage reaches a minimum of 189V at t=30s when the power increases from 5kW to 21kW and a maximum of 680V at t=50s when the power drops from 21kW to 7kW, which is due to the relatively small capacitance of the DC bus of 800μF.



(a) Radar load. **(b) Pulse load.**

Figure 3.14. Experimental results with ESS inactive.

The simulation data matches well with the measured results until the active load system tripped and was then disconnected from the DC network due to the over-voltage at t=50s, which explains why the measured test results (cyan trace) differ from the simulation beyond 50s. However the generator was still online.

A second load profile with higher frequency load transients was also tested. The active load switches between 1kW and 10kW with a 0.5 duty ratio at 0.5Hz, as shown in Figure 3.14b. A 22kW resistive background load is connected in parallel with the active load which causes an approximately 214Nm constant load on the generator. I_L in Figure 3.14b only relates to the active load profile current and not total load current in this

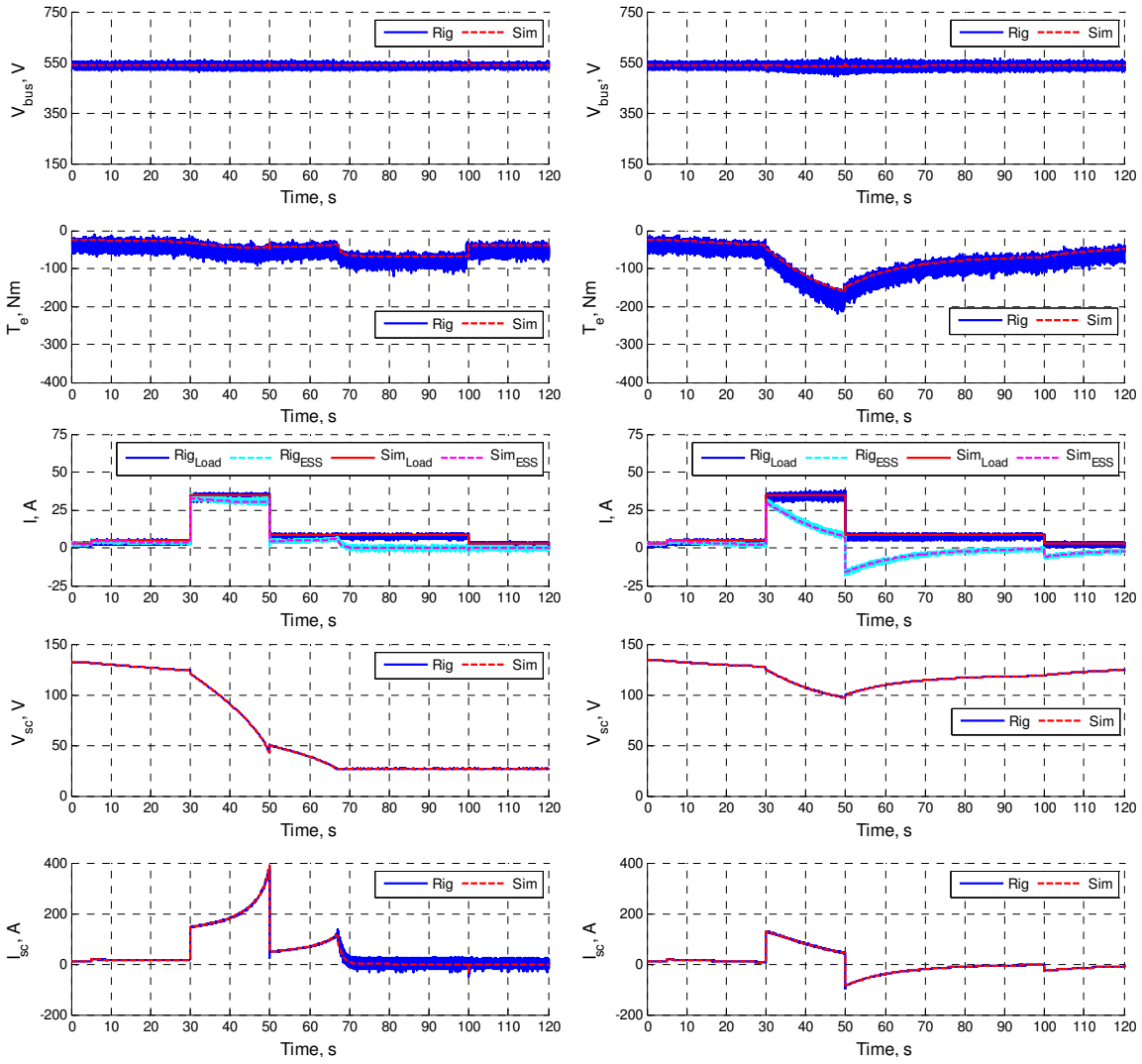
implementation. Similar to the results in Figure 3.14a, significant DC bus voltage deviations are seen in Figure 3.14b at the instants when the load changes, with a maximum of 612V (t=0, 2s) and a minimum of 440V (t=1, 3s), although the recovery time of the transients is 0.1s. The load change is reflected in the measured torque (Figure 3.14b), and imposes an 85Nm torque step on the constant 214Nm load, which may affect the gas turbine or prime mover and its associated controller. The comparison between test-rig data and simulation shows a good correlation for V_{bus} and a slight difference in the torque T_e due to the omission of losses from the simulation model, including both mechanical losses from friction and electrical losses in generator power converter.

3.4.2.2 Emulation results with ESS active

To demonstrate the ESS performance, two sets of parameters were used for the recharge current component $I_{sc\text{-}re}$ as described in Section 3.3.1. Figure 3.15a shows the test results using k_1=0.5, k_2=1, which gives a linear function of $I_{sc\text{-}re}=0.5(V_{sc\text{-}max}-V_{sc})$, where $V_{sc\text{-}max}$ is 135V; whereas Figure 3.15b shows the results using k_1=0.64, k_2=1.5, giving a non-linear function of $I_{sc\text{-}re}=0.64(V_{sc\text{-}max}-V_{sc})^{1.5}$, again $V_{sc\text{-}max}$ is 135V.

In Figure 3.15a (k_1=0.5, k_2=1, radar load), the super-capacitor runs out of energy after t=67s, and the super-capacitor voltage V_{sc} then remains at 27V as the converter control is inactive when the duty ratio reaches the limit of 0.95. From Equation (3.21), the maximum load power for k_1=0.5, k_2=1 is 2.3kW and so the ESS cannot regulate the state-of-charge if the load is maintained above 2.3kW for a significant time as in the radar load profile between t=25s to t=50s.

Due to the operation of the ESS, the generator torque in Figure 3.15a is very smooth until the super-capacitor energy is depleted at t=67s. Before this, the generator was shielded from the load transients, providing less than 100Nm torque during the high power load period (t=30s to t=50s), when, without the ESS, the torque was in excess of 200Nm (Figure 3.14a).



(a) k_1=0.5, k_2=1. **(b) k_1=0.64, k_2=1.5.**

Figure 3.15. Experimental results with ESS active for radar load.

Figure 3.15b shows the result using k_1=0.64 and k_2=1.5, which gives a larger recharge component $P_{sc\text{-}re}$ and the maximum load power from Equation (3.21) is 25.24kW. Consequently there is a lower super-capacitor current reference and a higher generator output power in Figure 3.15b compared to Figure 3.15a. A significant, but gradually increasing torque is seen during t=30s to 50s, due to the lower power contribution from the ESS. However, the torque transient is much less severe than in the initial test without the ESS operational, Figure 3.14a. The super-capacitor voltage drops down to around 100V during the high power step, and at t=50s, the ESS output current is approaching zero, which means the generator is providing the majority of the power required by the load. Again the correlation between the experimental and simulation data in Figure 3.15 is good.

Test and simulation results when the ESS is active with the parameters of k_1=0.64 and k_2=1.5 are shown in Figure 3.16 in response to the 0.5Hz load as used in Figure 3.14b.

The DC bus voltage in the first plot is well smoothed and no obvious voltage deviations can be found when comparing Figure 3.16 to Figure 3.14b when the ESS was inactive. The torque in the second plot is maintained constant around 240Nm. The ESS is actively working to balance the power as the super-capacitor voltage rises and drops as shown in the third plot, due to the repetitive charging and discharging process. The steps in the super-capacitor voltage V_{sc}, for example at t=1s and 3s, are due to the voltage drop across the equivalent series resistance of the super-capacitor, which is a function of the super-capacitor current.

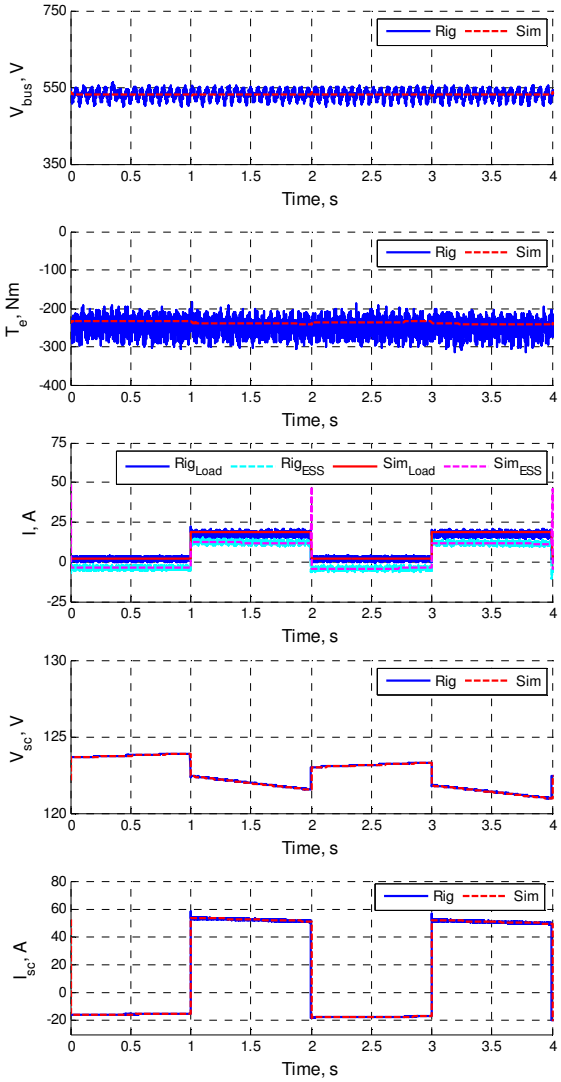


Figure 3.16. Experimental results with ESS active for high frequency load.

The super-capacitor voltage in Figure 3.16 is decreasing slightly over time as the ESS recharge control is transitioning to the $P_{sc\text{-}re}$ value appropriate for this pulse load. The intentionally slower response of the state-of-charge control means this transition takes

approximately 23 cycles (or 46s). Simulation shows that (Chapter 4, Figure 4.15, p117) for this pulse load with an average 5.5kW power, the ESS will enter a dynamic steady-state condition centred on 117V which corresponds to a 5.5kW $P_{sc\text{-}re}$ from Figure 3.8.

3.5 Conclusion

A control method for a super-capacitor based energy storage system (ESS) has been shown to manage the state-of-charge and protect the primary power source from sudden load changes on a DC distribution network. A power based control component is commanded to the ESS to ensure any instantaneous load changes can be followed by the ESS, therefore smoothing the load seen by the power source and virtually eliminating voltage transients from the DC bus. A slower-acting control loop actively manages the ESS state-of-charge, ensuring the super-capacitor voltage remains within the working range and at a suitable level, ready to be discharged or charged. The effectiveness of the control method has been validated in simulation using a selection of state-of-charge control parameters. The use of the exponent k_2 in the state-of-charge controller in addition to the proportional parameter k_1 is seen to provide the flexibility to use the super-capacitor more aggressively under certain states-of-charge.

The hardware-in-the-loop technique was deployed to investigate the system level performance of the ESS experimentally. Two bi-directional active load units controlled by a real-time simulation platform emulated the ESS and the electric loads, allowing the effects of parameter changes to be readily examined. With the emulated ESS and load, a radar load profile and a generic higher frequency load were tested to demonstrate the system performance, which shows the effectiveness of the ESS and its control. The ESS significantly mitigated bus voltage transients for both load types investigated. The generator torque steps in response to load steps were also much gentler when the ESS was active. However, as demonstrated by the simulation and experiments results, as the rate-of-change in source power (or torque) is unmanaged, this causes long charge or discharge times in some cases. Besides, the similar behaviours in source power or energy variations using k_1 k_2 paramters indicate there can be a more flexible form of defining the recharge component $P_{sc\text{-}re}$. A more general analysis of ESS system and its control is provided in Chapter 4.

Chapter 4 Advanced control for an energy storage system

4.1 Introduction

To provide improved control of the source power within a small electrical system such as that described in Chapter 3, this chapter describes the development and demonstration of a control method for the energy storage device which focuses on the rate-of-change of source power. The principle is first introduced through a simple analysis of energy flows within the system.

Results from a simple, generic simulation model are used to illustrate the macro level behaviour of this control technique, comparing several different rate-of-change limits. The system level performance is then presented using both simulation results and experimental results from a real super-capacitor based energy storage system within the IEPNEF rig.

4.2 General analysis of an ESS

The energy management control developed in this chapter has two functions, managing the available energy in the ESS and regulating the rate-of-change of source power. These two aspects of the ESS behaviour are examined in detail in Sections 4.2.1 and 4.2.2 respectively as this analysis forms the theoretical basis for the energy management control.

4.2.1 Steady-state analysis

In Chapter 3, a recharge profile (of the form $P_{sc\text{-}re}=k_1 V_{sc}(V_{sc\text{-}max}-V_{sc})^{k2}$, Equation (3.18)) was examined where the steady-state super-capacitor voltage V_{sc} is dependent on the load power P_L. The recharge profile effectively determines the energy according to the load condition, with the storage device having a high energy at low load and low energy at high load. To examine the relationship between energy on load power, alternative recharge functions are investigated which are not restricted to the form of Equation (3.18).

Figure 4.1 shows three profiles of stored energy versus load power, labelled L, C and H.

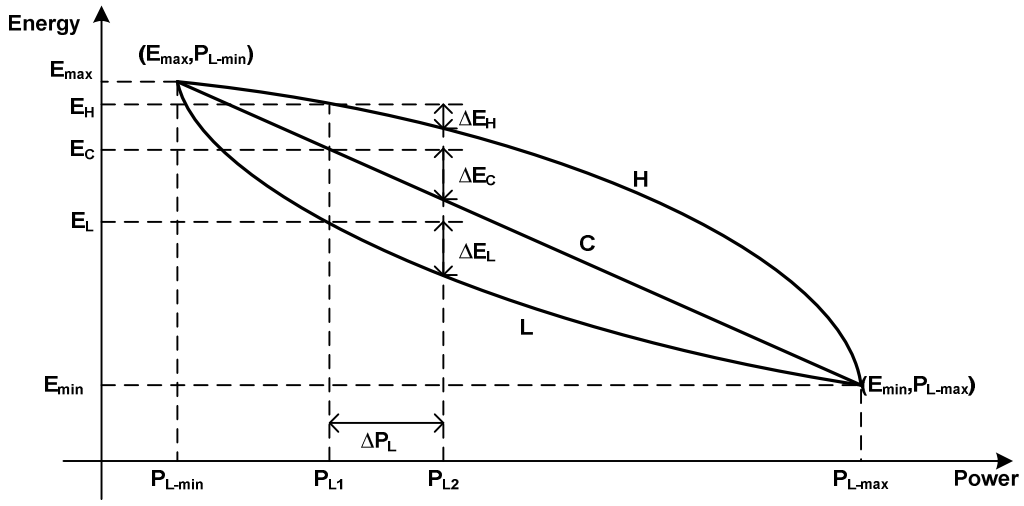


Figure 4.1. Sample stored energy against load power profiles.

All of the curves in Figure 4.1 pass the same two points, E_{max}, $P_{L\text{-}min}$ where the energy storage unit is full and the load is at its minimum, and E_{min}, $P_{L\text{-}max}$ where the energy storage unit is at its minimum and the maximum load is applied within the system. In the analysis in this section, the minimum load power $P_{L\text{-}min}$ is assumed to be zero.

For a specific load, P_{L1}, in Figure 4.1, each profile has a different steady-state energy with profile L having the lowest stored energy, E_L, and profile H having the highest remaining stored energy, E_H, for the profiles examined. The general expression for this is:

$$E = f_{ss}(P_L) \tag{4.1}$$

where the function $f_{ss}()$ defines the shape of the curve and should be monotonically decreasing so that it satisfies the general ESS rule of high stored energy at low load, and low stored energy at high load. Other alternative profiles are valid providing they pass the two points, E_{max}, P_{min} and E_{min}, P_{max} as these define the limits of device and system operation.

The main difference amongst the curves in Figure 4.1 is the different energy flow for a specific load step at different levels of load power, which is reflected in the slope of each curve. Curve L has a high dE/dP at low load power and low dE/dP at high load power, indicating that at low load powers the storage system will respond more strongly, that is, the low power region is prioritised; curve H works in the opposite way and so prioritises the high power region, and curve C has a constant dE/dP and so the storage system will

respond in a similar manner at all load levels. As an example, a load step ΔP_L from P_{L1} to P_{L2} is shown in Figure 4.1. Each curve, H, C and L, has a different change in energy due to the load step ΔP_L, with curve H using an energy of ΔE_H, curve C using ΔE_C, and curve L using ΔE_L. As the load step occurs at relatively low power, ΔE_L is larger than both ΔE_H and ΔE_C. If the ESS uses curve L then the impact of the load step on the power source will be more gradual. For a load step in the high power region, curve H would use more energy in response to the step than either curve C or L.

Determining the best energy against power profile for a specific application would depend on the characteristics of the loads, source/generator and prime mover, and is beyond the scope of this thesis.

4.2.2 Dynamic response analysis

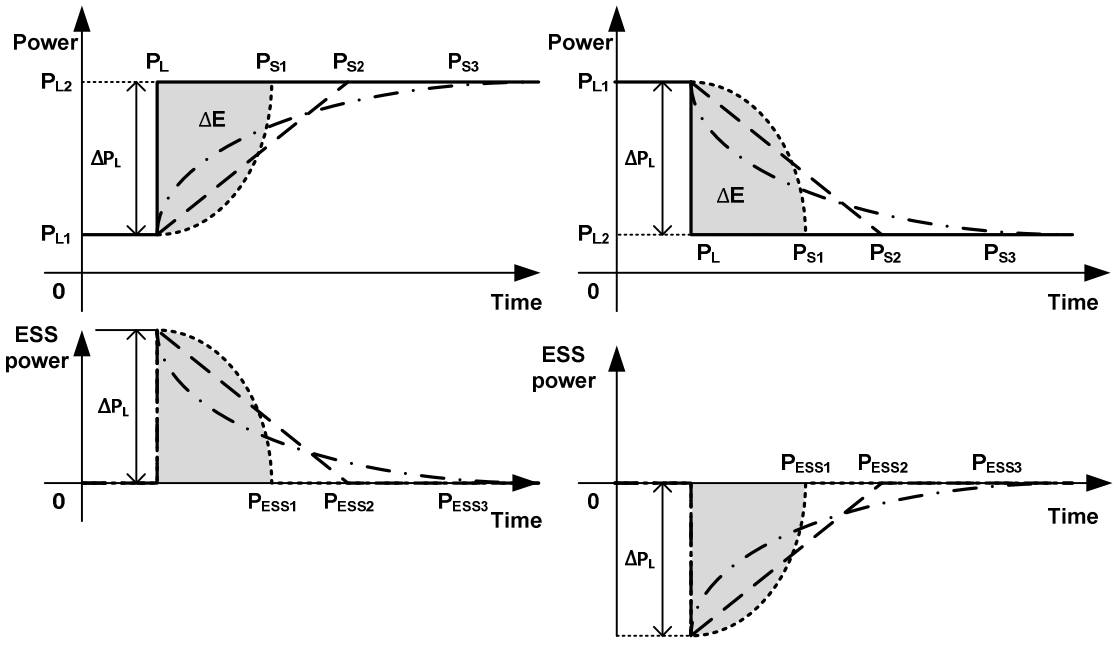
The profiles shown in Figure 4.1 determine the steady-state stored energy for a specific load power, $E=f_{ss}(P_L)$. If there is a load step between two steady-state loads, such as the load change from P_{L1} to P_{L2} in Figure 4.1, the stored energy will change from $E_1=f_{ss}(P_{L1})$ to $E_2=f_{ss}(P_{L2})$. However, an infinite number of transitions from E_1 to E_2 exist, each with different characteristics, but all with identical energy usage levels. The remainder of this section examines different energy transitions.

A sample load power step is shown in Figure 4.2 to illustrate the analysis for a system consisting of a single power source and a single ESS. The consumed/stored energy from/to the ESS in response to the load change, is the integral of the difference between the load and source powers with time, Equation (4.2). Taking P_{S1} as an example gives the shaded area in Figure 4.2.

$$\Delta E = \int (P_L - P_S)dt = \int P_{ESS}\,dt \tag{4.2}$$

where ΔE is the consumed/stored energy from/to the ESS, P_L, P_S and P_{ESS} are the instantaneous load, source and ESS powers respectively.

Three response profiles P_{S1}, P_{S2} and P_{S3} are shown in Figure 4.2 and all are assumed to result in the same amount of energy being consumed/stored so that the profiles can be compared fairly.



(a) Load step increase. **(b) Load step decrease.**

Figure 4.2. Three different power source response profiles.

In all cases in Figure 4.2a, the ESS responds instantaneously to the change in load (profiles P_{ESS1}, P_{ESS2}, P_{ESS3}), and the power source has a zero instantaneous response and then gradually the generator output P_{S1}, P_{S2}, P_{S3} increases to match the load power. Throughout the profile, P_S plus P_{ESS} is equal to P_L. Similar behaviour is shown in Figure 4.2b for a load decrease, however, the ESS absorbs power in this case so as to allow the source power to reduce gradually.

For profile P_{S1} in Figure 4.2, the source power has a gentle initial response (low dP_S/dt) but encounters a high rate-of-change in power as P_{ESS1} approaches zero. Profile P_{S3} is the opposite of profile P_{S1}, with a high initial dP_S/dt and a much reduced dP_S/dt as P_{ESS3} approaches zero. Profile P_{S3} exhibits a similar response to a simple low-pass filter. Profile P_{S2} has a constant rate-of-change in power and so has the lowest peak dP_S/dt when compared to P_{S1} and P_{S3}, for the same energy usage. However, under some load conditions, it may be beneficial to use the other two profiles. For example, with a high frequency stepped part load, the slow initial response from profile P_{S1} may mean the power source does not encounter the high dP_S/dt region before the transition is completed.

By using the constant dP_S/dt rate profile P_{S2} and denoting dP_S/dt equal to k_c, the energy used during the transition of P_{L1} to P_{L2} ($\Delta P_L=P_{L2}-P_{L1}$) in Figure 4.2 can be worked out using Equation (4.2) so:

$$\Delta E = \frac{1}{2}\Delta P_L \cdot \Delta t = \frac{1}{2}\Delta P_L \cdot \frac{\Delta P_L}{k_c} = \frac{1}{2}\frac{\Delta P_L^2}{k_c} \tag{4.3}$$

The rate-of-change in power source output $dP_S/dt=k_c$, can be determined from Equation (4.3) as:

$$\frac{dP_s}{dt} = k_c = \frac{\Delta P_L^2}{2\Delta E} \tag{4.4}$$

Equation (4.4) shows that the rate-of-change in power k_c will increase as the load change ΔP_L increases or as the available energy ΔE decreases. This reflects the simple fact that the dynamic response of the power source will be more gentle if exposed to a small load change with a large stored energy. The k_c value also indicates the minimum possible rate-of-change in power throughout the load transition given a known ΔP_L and ΔE, since using any other non-constant dP_S/dt profile will result in a larger peak rate-of-change in power as illustrated in Figure 4.2.

By considering the extreme case when the load changes from $P_{L\text{-}min}$ to $P_{L\text{-}max}$ (or vice versa), and all the available energy is used (or stored), i.e., $\Delta E=E_{max}-E_{min}$, $\Delta P_L=P_{L\text{-}max}-P_{L\text{-}min}$, the rate-of-change in power for this condition is $k_{c\text{-}max}$ and can be determined from Equation (4.4) as:

$$k_{c-\max} = \frac{(P_{L-\max} - P_{L-\min})^2}{2(E_{\max} - E_{\min})} \tag{4.5}$$

Since this dP_S/dt rate is fixed for the known total storage capacity $\Delta E=E_{max}-E_{min}$ and maximum and minimum load power $P_{L\text{-}max}$ and $P_{L\text{-}min}$, the control strategy objective is to make sure that the dP_S/dt rate for other load steps is equal to or less than $k_{c\text{-}max}$ during the resulting charge or discharge process, therefore

$$k_c = \frac{\Delta P_L^2}{2\Delta E} \le k_{c-\max} = \frac{(P_{L-\max} - P_{L-\min})^2}{2(E_{\max} - E_{\min})} \tag{4.6}$$

To achieve this objective together with the energy usage from Section 4.2.1, a control method is proposed and is described in Section 4.3.

4.3 Proposed control method

The proposed ESS control method has a similar structure to the control presented in Chapter 3, as the power reference $P_{ESS\text{-}ref}$ which commands the ESS to provide the required power, consists of two components given in Equation (4.7):

$$P_{ESS-ref} = P_{ESS-L} - P_{ESS-re} = P_L - P_{ESS-re} \tag{4.7}$$

where the load power balance control component $P_{ESS\text{-}L}$ is measured from and is equal to the load power P_L, and $P_{ESS\text{-}re}$ is the recharge component which manages the ESS energy.

Assuming a lossless system, and that the ESS accurately follows the reference value, so P_{ESS}=$P_{ESS\text{-}ref}$, the ESS output power is given by:

$$P_{ESS} = P_{ESS-ref} = P_L - P_S \tag{4.8}$$

From Equations (4.7) and (4.8), it can be deduced that:

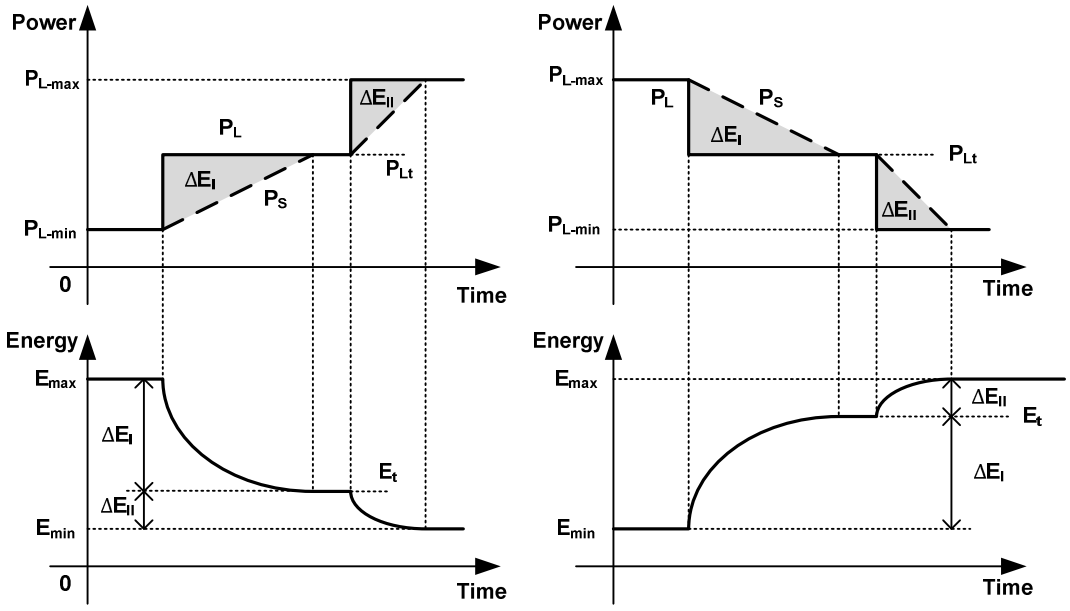
$$P_S = P_{ESS-re} \tag{4.9}$$

Equation (4.9) shows that the power source output P_S is indirectly controlled by $P_{ESS\text{-}re}$. Therefore the proposed control method is to set $P_{ESS\text{-}re}$ so as to manage the dynamic power performance of the power source and also the energy level (or SoC) of the ESS. The proposed method is applicable to a generic electrical system with any ESS, and the controller design is given in Section 4.3.1 and 4.3.2.

4.3.1 Proposed steady-state SoC control

The finite energy capacity of the ESS means that the usage of energy must be carefully managed as outlined in Section 4.2.1. The process for managing energy is developed by considering the charge and discharge of the ESS.

A discharge cycle is shown in Figure 4.3a, where the load power P_L (solid line) changes in steps from $P_{L\text{-}min}$ to P_{Lt} and then to $P_{L\text{-}max}$ and the power source output P_S (dashed line) changes with a fixed rate k_c given by Equation (4.4) which respects the $k_{c\text{-}max}$ constraint over the full load profile. The energy consumption in response to the two steps are labelled as ΔE_I and ΔE_{II} in the lower plot in Figure 4.3a, and E_t is the corresponding total remaining stored energy at load power P_{Lt}.



(a) Discharge cycle. **(b) Charge cycle.**

Figure 4.3. Full discharge and charge cycle of the ESS.

For any intermediate load power level P_{Lt}, sufficient energy $\Delta E_{II}=E_t-E_{min}$ has to be reserved to ensure that the ESS is able to respond to a load increase from P_{Lt} to the full load power $P_{L\text{-}max}$, while imposing the calculated dP_S/dt rate k_c from Equation (4.4).

The energy required $\Delta E=\Delta E_{II}=E_t-E_{min}$ for any intermediate load level P_{Lt} can be solved by substituting $\Delta E=E_t-E_{min}$, and $\Delta P_L=P_{L\text{-}max}-P_{Lt}$ into Equation (4.6), so:

$$k_c = \frac{(P_{L-\max} - P_{Lt})^2}{2(E_t - E_{\min})} \le k_{c-\max} = \frac{(P_{L-\max} - P_{L-\min})^2}{2(E_{\max} - E_{\min})} \tag{4.10}$$

which can be rearranged as:

$$E_t \ge \frac{(P_{L-\max} - P_{Lt})^2}{(P_{L-\max} - P_{L-\min})^2}(E_{\max} - E_{\min}) + E_{\min} \tag{4.11}$$

Similarly, for a charge process, Figure 4.3b, a sufficient energy margin $\Delta E=\Delta E_{II}=E_{max}-E_t$ has to be reserved for a potential power decrease from the load power P_{Lt} to the minimum

load power $P_{L\text{-}min}$, the solution is to substitute $\Delta E=\Delta E_{II}=E_{max}-E_t$, and $\Delta P_L=P_{Lt}-P_{L\text{-}min}$ into Equation (4.6), so:

$$k_c = \frac{(P_{Lt} - P_{L-\min})^2}{2(E_{\max} - E_t)} \le k_{c-\max} = \frac{(P_{L-\max} - P_{L-\min})^2}{2(E_{\max} - E_{\min})} \tag{4.12}$$

which gives:

$$E_t \le E_{\max} - \frac{(P_{Lt} - P_{L-\min})^2}{(P_{L-\max} - P_{L-\min})^2}(E_{\max} - E_{\min}) \tag{4.13}$$

Equations (4.11) and (4.13) are parabolas in the form of $E_t = a(P_{Lt} - b)^2 + c$, where a, b, and c are constants depending on E_{max}, E_{min}, $P_{L\text{-}max}$ and $P_{L\text{-}min}$. The two equations define two steady-state profiles of energy against load power, i.e., $E_t=f_{ss}(P_{Lt})$ in the form of Equation (4.1), so that the target energy E_t obtained from the profile ensures $k_c \le k_{c\text{-}max}$ for a discharge process from any load power P_{Lt} to maximum load power $P_{L\text{-}max}$ or a charge process from any power P_{Lt} to minimum power $P_{L\text{-}min}$ respectively.

By defining $E_t'=E_t-E_{min}$, and $P_L'=P_{Lt}-P_{L\text{-}min}$, Equations (4.11) and (4.13) can be generalised as:

$$\begin{aligned} \frac{E_t'}{E_{\max} - E_{\min}} &\ge (1 - \frac{P_L'}{P_{L-\max} - P_{L-\min}})^2 \qquad \text{for} \quad \text{discharging} \\ \frac{E_t'}{E_{\max} - E_{\min}} &\le 1 - (\frac{P_L'}{P_{L-\max} - P_{L-\min}})^2 \qquad \text{for} \quad \text{charging} \end{aligned} \tag{4.14}$$

Equation (4.14) can be rewritten in per unit terms by defining $E_{base}=E_{max}-E_{min}$, $P_{L\text{-}base}=P_{L\text{-}max}-P_{L\text{-}min}$, and by setting $E_{t\text{-}pu}=E_t'/E_{base}$, $P_{L\text{-}pu}=P_L'/P_{L\text{-}base}$:

$$E_{t-pu} \ge (1 - P_{L-pu})^2 \qquad \text{for} \quad \text{discharging} \tag{4.15}$$

$$E_{t-pu} \le 1 - P_{L-pu}{}^2 \qquad \text{for} \quad \text{charging} \tag{4.16}$$

Equation (4.15) is the form of curve L in Figure 4.1, either reflected from the equation itself or from illustration in Figure 4.3a. The state-of-charge at a particular load power is the lowest amongst the three profiles, indicating that more energy will be transferred in response to transients at low load levels, whilst the minimum possible energy is reserved to meet potential load increases up to full power at a dP_S/dt rate of $k_{c\text{-}max}$. In contrast profile H works in the opposite way and provides the highest state-of-charge at any load level, just reserving enough storage capacity to respond to a load decrease to zero at a dP_S/dt rate of $k_{c\text{-}max}$. The two parabolas of these two equations enclose an area in which the two

inequalities, Equations (4.15) and (4.16), are always satisfied, and include the linear profile C in Figure 4.1, which is given by:

$$E_{t-pu} = 1 - P_{L-pu} \tag{4.17}$$

According to the requirements of an application, any one, or a blended combination of these profiles could be used, for example blending the L and H profiles together according to the predicted future use of power within the network.

4.3.2 Proposed dynamic response control

The dynamic response of the ESS can be used to impose a limit on the rate-of-change of source power. In this control method, the dP_S/dt rate of the power source is set at a constant k_c in contrast to Chapter 3, where the power source output is determined by super-capacitor voltage and so the dP_S/dt rate is uncontrolled.

The steady-state energy profile in Section 4.3.1 determines a target energy $E_t=f_{ss}(P_L)$ for a given load power P_L. If the source power P_S is not equal to the load power P_L then the ESS must source or sink power to balance the system until P_S is equal to P_L. The energy which may be used in response to a load change is the the current available energy, E, minus the target energy, $E_t=f_{ss}(P_L)$, so:

$$\Delta E = E - E_t = E - f_{ss}(P_L) \tag{4.18}$$

where $f_{ss}(P_L)$ is either Equation (4.15), (4.16) or (4.17), although other forms may apply.

The power difference between the load power P_L and the power source output P_S is given by:

$$\Delta P_L = P_L - P_S = P_{ESS} \tag{4.19}$$

By substituting Equation (4.18) and (4.19) into Equation (4.4), the rate-of-change of source power is therefore:

$$k_c = \frac{{P_{ESS}}^2}{2(E - f_{ss}(P_L))} \tag{4.20}$$

which gives the most gradual, constant, rate-of-change in the power source output for a specific load step.

For the purposes of a practical implementation, Equation (4.20) would be utilized in a real-time controller, where a rate limit function set by k_c is constantly updated, and this process is illustrated in Figure 4.4. The denominator of Equation (4.20) determines the useable energy, given by the difference between the current and target energy; whereas the numerator P_{ESS} is the difference between source and load powers. The implementation of this control is described in the following sections.

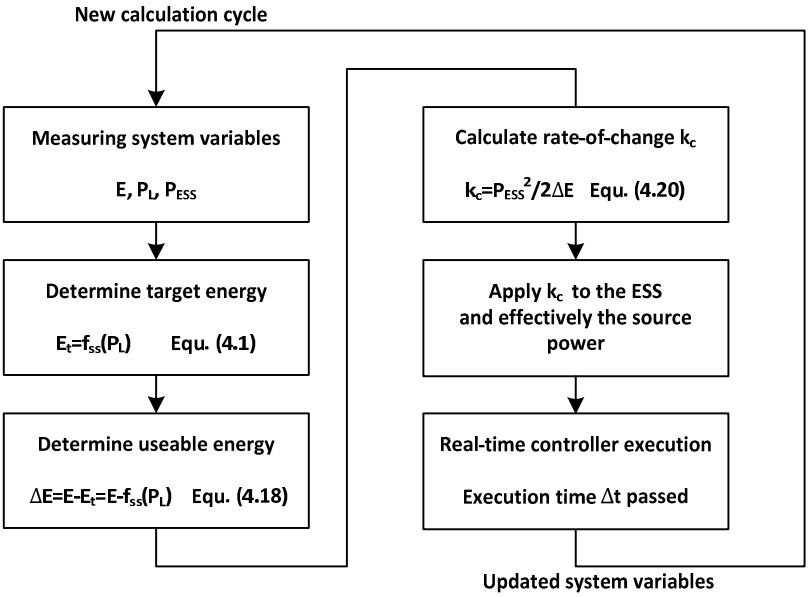


Figure 4.4. Flow chart of the k_c calculation.

4.4 Generic ESS simulation

The mathematical equations derived in Section 4.3 can be used to form a simple generic ESS simulation model to investigate the ESS and system behaviour. This model omits the main power source controller dynamics and the ESS inner control dynamics, however the core behaviour of the ESS is preserved, enabling the proposed ESS control method to be assessed without the influence of other system dynamics. The performance of three steady-state energy profiles L, C, H as described in Section 4.3.1 are examined by simulation using the dynamic response profile described in Section 4.3.2.

4.4.1 Simulation model

An ideal ESS can be modelled assuming that the power flow to/from the storage device, P_{ESS}, can perfectly track the power reference $P_{ESS\text{-}ref}$, so that $P_{ESS}=P_{ESS\text{-}ref}$. Then, the rate-of-change in stored energy E is equal to the charging power to the ESS ($dE/dt=P_{ESS}$, negative

when being discharged), and as $P_{ESS\text{-}ref}=P_L-P_{ESS\text{-}re}$, Equation (4.7), a differential equation to describe the ESS behaviour can be written:

$$\dot{E} = P_{ESS} = P_{ESS-ref} = P_L - P_{ESS-re} \tag{4.21}$$

Figure 4.5 shows the block diagram of the simplified Simulink model for a generic ESS based on Equation (4.21). An integrator is used to relate P_{ESS} and E, and the summation block reflects the power balance in the electrical system, $P_{ESS}=P_L-P_S$. The source power P_S is effectively controlled by the recharge power signal $P_{ESS\text{-}re}$ which is set to be equal to the rate limited variable load power. The rate limiter actively controls the rate-of-change of $P_{ESS\text{-}re}$ to k_c from Equation (4.20) and so effectively limits the rate-of-change of the source power P_S. Determining k_c requires the measurement of several system variables including P_L, P_{ESS} and E, which increases the complexity of the control.

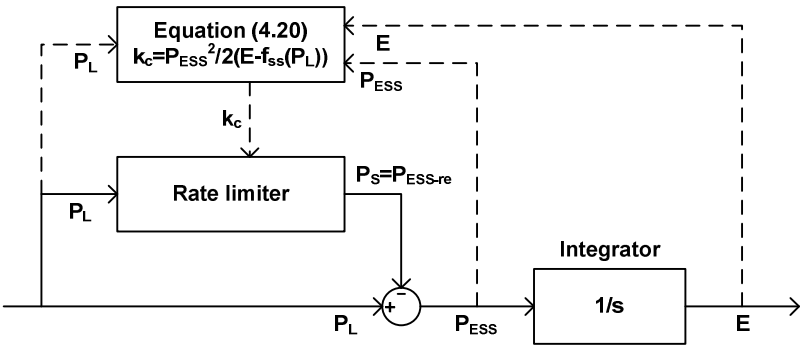


Figure 4.5. $P_{ESS\text{-}re}$ control using rate limiter.

For simplicity, the model uses the per unit system, and is generic to any system providing the variables are correctly scaled. In addition to the base values defined previously ($E_{base}=E_{max}-E_{min}$, $P_{L\text{-}base}=P_{L\text{-}max}-P_{L\text{-}min}$), the dP_S/dt base $k_{c\text{-}base}$ and the time base T_{base} are defined as:

$$k_{c-base} = \frac{P_{L-base}^{\ 2}}{E_{base}} \tag{4.22}$$

$$T_{base} = \frac{E_{base}}{P_{L-base}} \tag{4.23}$$

The maximum rate-of-change of source power in per unit $k_{c\text{-}max\text{-}pu}$ is therefore :

$$k_{c-\max-pu} = \frac{k_{c-\max}}{k_{c-base}} = \frac{(P_{L-\max} - P_{L-\min})^2}{2(E_{\max} - E_{\min})} / \frac{P_{L-base}^{\ 2}}{E_{base}} = 0.5\,p.u. \tag{4.24}$$

and is the rate that would occur in response to a load step from minimum to maximum.

4.4.2 Control design

Three control variations are examined, namely, L, C and H, as previously described in Section 4.3.1. Figure 4.6 illustrates these three profiles in per unit form based on Equation (4.15), (4.16) and (4.17) respectively. As shown in the figure, with profile L, the storage system will respond more strongly at lower load powers. In contrast, with curve H, the energy storage system will respond more strongly at lighter load powers.

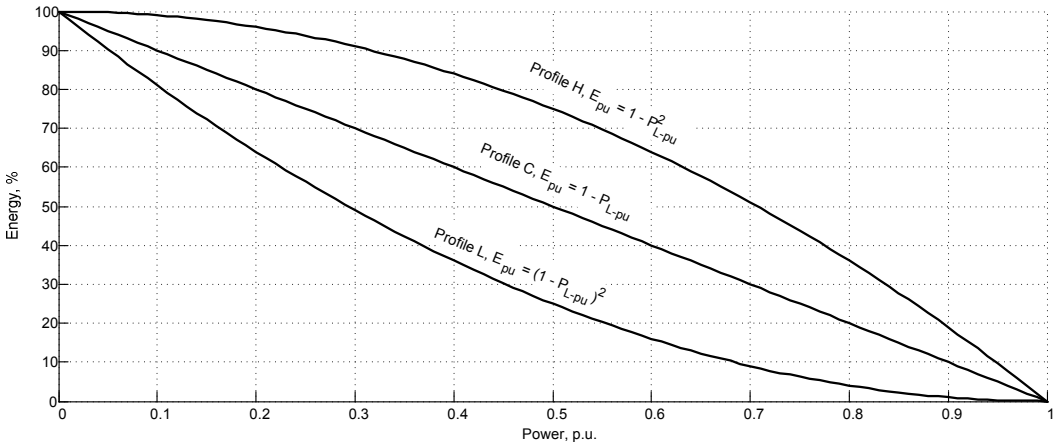
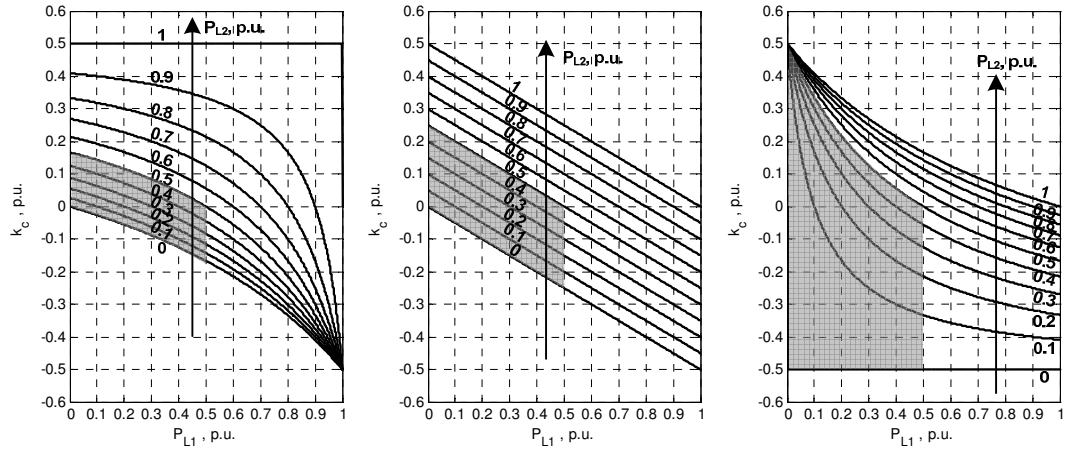


Figure 4.6. Three control profiles used in simulation, L, C and H.

For the steady-state energy profiles shown in Figure 4.6, the optimal rate-of-change in power value k_c can be calculated using Equation (4.4) for any load transition from P_{L1} and P_{L2} ($\Delta P=P_{L2}-P_{L1}$) since the useable energy is known to be $\Delta E=f_{ss}(P_{L1})-f_{ss}(P_{L2})$. Figure 4.7 shows the calculated k_c per unit values for different P_{L1} and P_{L2} combinations using the three energy profiles. Each curve in the figure gives k_c for a load transition from P_{L1} to P_{L2}. For example, a load transition from P_{L1}=0.2p.u. to P_{L2}=0.3p.u. using profile L will give k_c=0.03p.u. as read from the P_{L2}=0.3p.u. curve in Figure 4.7a. A negative k_c indicates a step decrease in load power, that is, when $P_{L1}>P_{L2}$.

In Figure 4.7, the shaded areas are when both P_{L1} and P_{L2} are less than 0.5p.u., representing the low load region. In Figure 4.7a where profile L is used, the low load area is compressed towards the zero line compared to the other two profiles, indicating the dP_S/dt rate k_c is reduced and confirming that the storage system will respond more strongly in the low load region as predicted in Section 4.2.1. However, this sacrifices the performance at high loads, as the P_{L2} curves above 0.5p.u. in Figure 4.7a indicate much larger values of k_c, but less than the maximum of 0.5. In Figure 4.7c using profile H, the situation is reversed with the storage system responding more strongly at higher loads. A neutral profile is exhibited in

Figure 4.7b using profile C, where the rate-of-change in power changes linearly with the load step magnitude.



(a) Profile L **(b) Profile C** **(c) Profile H**

Figure 4.7. k_c values calculated for transition from P_{L1} to P_{L2}.

All the profiles in Figure 4.7 show that the maximum rate-of-change in source power k_c is lower than $k_{c\text{-}max\text{-}pu}$=0.5p.u. as calculated in the design stage in Section 4.4.1. However, when losses are taken into consideration, a higher rate-of-change in source power k_c will appear in a load increase transition, since less energy is effectively usable. It is either required to increase the storage capacity of the ESS to achieve the same maximum $k_{c\text{-}max\text{-}pu}$=0.5, or to have a power source capable to tolerate the higher rate due to the losses.

4.4.3 Simulation results

A selection of different load profiles, including small and large power changes with different rise/fall rates, is presented and discussed in this section to demonstrate the system operation with the power rate limited control presented in Section 4.3. The simulation model used is the ideal ESS structure given in Figure 4.5, and all three control profiles, shown in Figure 4.6, have been implemented to examine the ESS performance. A time base of T_{base}=1s is assumed, so that the time in the results is all expressed in seconds.

4.4.3.1 Small load steps simulation

Figure 4.8 shows the main power source and ESS response for small load steps over the full power range of the load. The load power increases from no-load to 1p.u. and then back to no-load in 0.1p.u. steps occurring every 5s; each step has a 1ms rise/fall time. All plots in Figure 4.8 show results for each of the control profiles, profile L is indicated by the green traces, profile C by the blue traces and profile H by the red traces.

The load power and source power P_S are shown in the top plot in Figure 4.8a; the ESS power is not shown in the plot for clarity, but is the difference between the load and source power. The middle plot in Figure 4.8 is the rate-of-change in main source power dP_S/dt and the bottom plot is the ESS energy E.

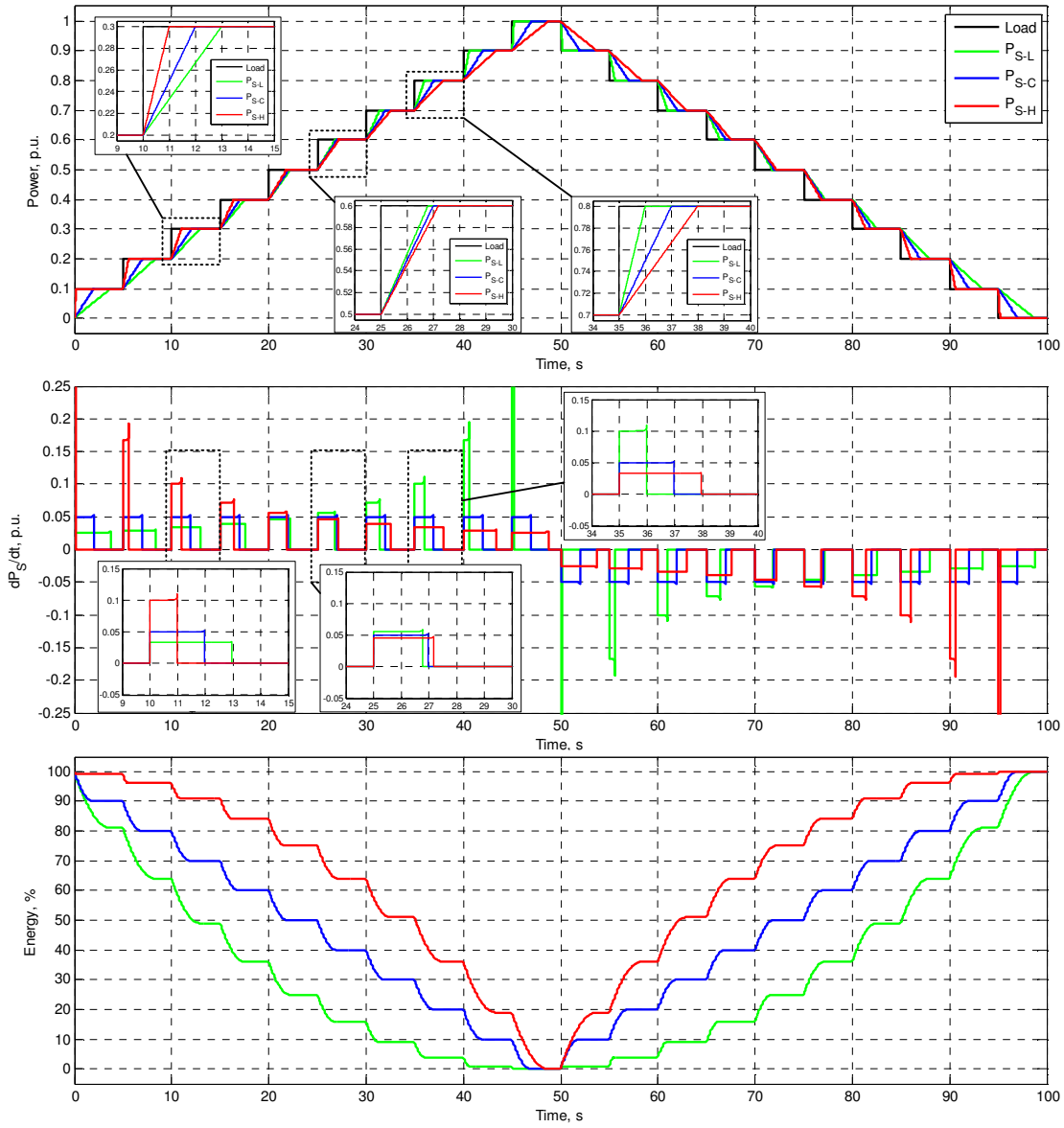


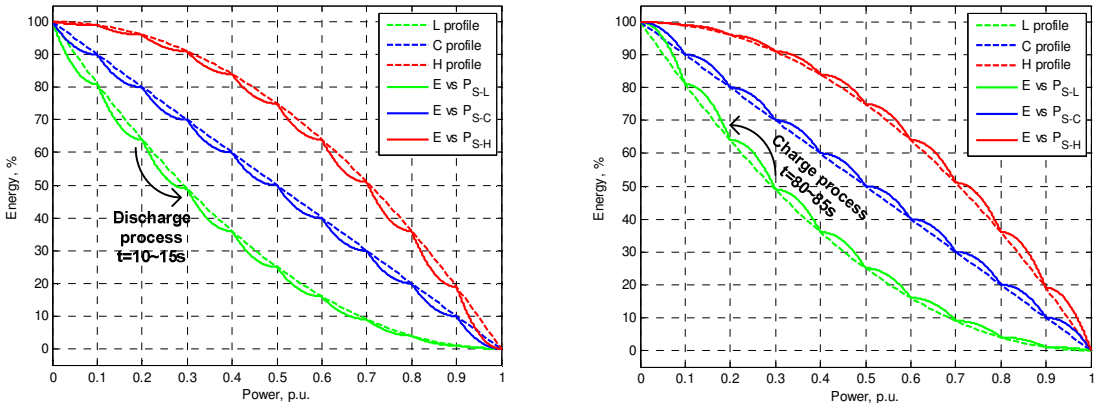
Figure 4.8. Small load steps responses.

For each small load step, the main source power in Figure 4.8 does not respond instantaneously but has a gradual increase/decrease until it is equal to the load power. During each load transition, the three control profiles cause different system peformance which is deteremined by the energy used. For the load step from 0.2p.u. to 0.3p.u. (t=10-15s), profile L, offers the most gradual power source change dP_S/dt=0.03p.u., whereas the dP_S/dt for profile C and H are higher at 0.05p.u. and 0.1p.u. respectively; all values match the predicted value from Figure 4.7. The energy usage for profile L is more during this load transition at 15%, compared with 10% for profile C and 5% for profile H, which

results in the lowest steady-state energy of 64%. When the initial load value is 0.5p.u., the energy usage from of the three profiles is similar at approximately 10% giving a dP_S/dt value of near 0.05p.u as shown in Figure 4.8. During the load transition from 0.7p.u. to 0.8p.u., the profile H results in the lowest dP_S/dt since more energy is available for use, and the profile H is designed to use more energy in this load region.

From zero to full power, the dP_S/dt using the profile L increases as the initial values of the 0.1p.u. load steps increase, illustrated in Figure 4.8, second row, where the dP_S/dt gradually increases from 0.026p.u. at low load to 0.5p.u. at high load (cropped in Figure 4.8), validating the low load oriented design. Profile H exhibits the opposite effect since it tends to use the stored energy more strongly at lighter load levels, while the dP_S/dt for profile C is constant at 0.05p.u. for a 0.1p.u. step with a constant 10% energy consumption across the full load range. Similar behaviour for the three control profiles can be observed during the load decrease stage from t=50s to 100s.

The steady-state energy values in Figure 4.8 match the design data in Figure 4.6 for a specific load P_L, satisfying both $E=f_{ss}(P_L)$ and also $E=f_{ss}(P_S)$ since $P_S=P_L$ in the steady-state. However, Figure 4.9a and b demonstrate that when the ESS discharges or charges, the energy E against power source output P_S trajectory deviates from the ideal control profile, $E \neq f_{ss}(P_S)$ during a load transition. A mathematical derviatiation is given in Appendix B.5 proving that the energy against power trajectory from one steady-state condition to another is a parabola of the form of Equation (4.15) (discharge) or (4.16) (charge). If the profile is closely tracked then k_c would vary during the load transition and so the constant rate k_c condition would not be met. This has been confirmed by simulation, however the results are not included here.



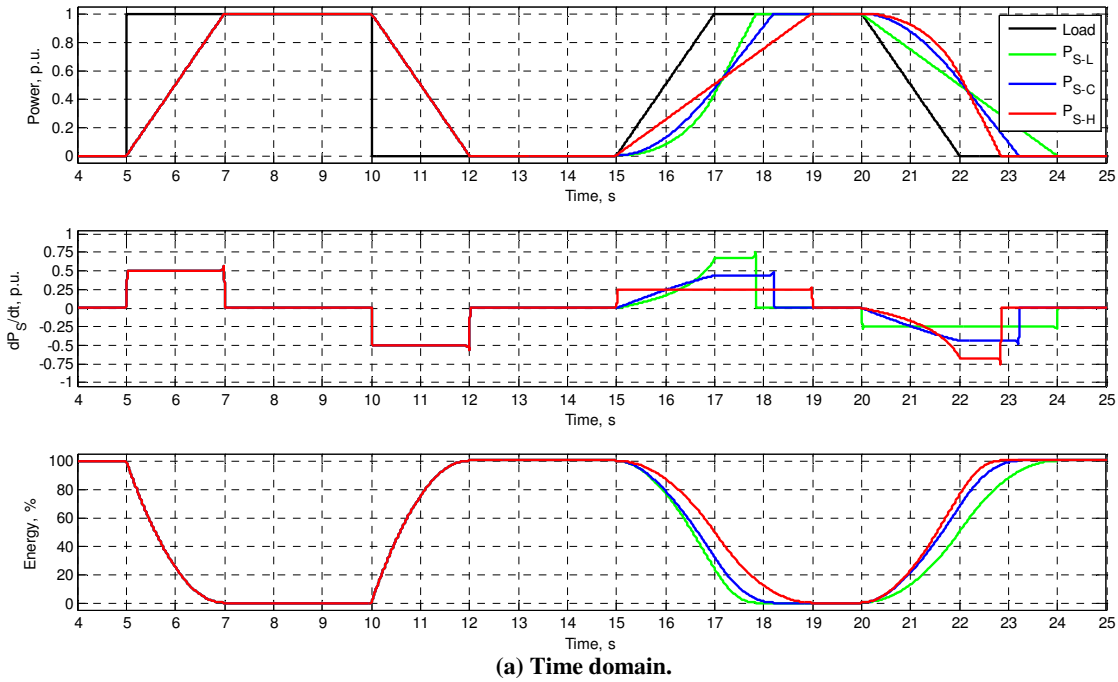
(a) Load increase, discharge **(b) Load decrease, charge**

Figure 4.9. Energy E against power source output P_S trajectories.

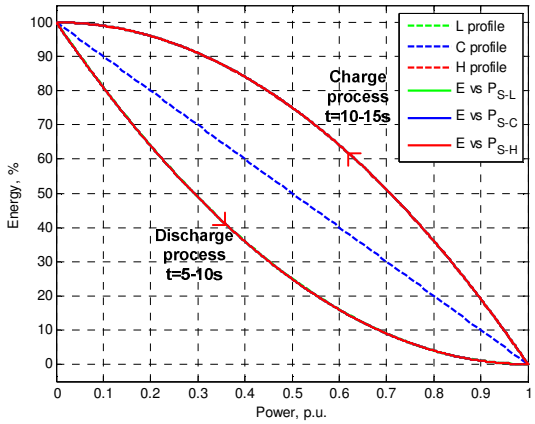
4.4.3.2 Full power load steps and ramps simulation

Two large load profiles are shown in Figure 4.10, the first is a full power step, which has a 1ms rise/fall time and increases at time 5s and reduces at time 10s, and the second is a full power ramp with a 2s rise/fall time which starts to increase at time 15s and starts to decrease at time 20s. The detailed control performance was explained in the discussion relating to Figure 4.8 and so is not repeated here; the discussion in this section focuses on features specific to large power steps/ramps.

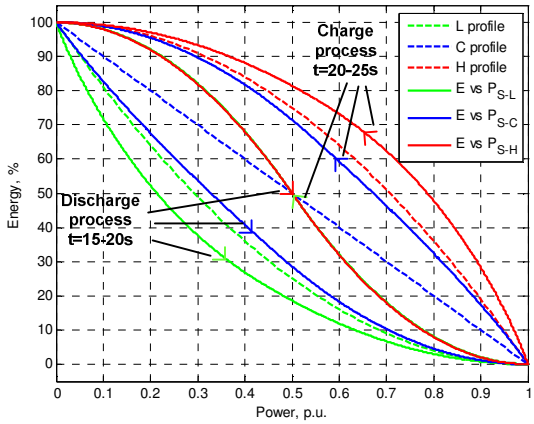
Only the profile H traces are visible in the plots in Figure 4.10a during the full load step increase and decrease because, from Figure 4.6 and Figure 4.7, all three profiles tested are using all of the available energy and so have identical dP_S/dt values which are equal to the $k_{c\text{-}max}$ of 0.5p.u. from Equation (4.24). The main power source supplies the full load 2s after the load change due to the dP_S/dt of 0.5p.u.



(a) Time domain.



(b) Energy versus P_S, step load.



(c) Energy versus P_S, ramp load.

Figure 4.10. Large load step responses.

The actual energy versus source power for the three profiles tested are all identical and map perfectly to profile L in Figure 4.10b during the discharge process as all profiles have identical dP_S/dt values which are equal to $k_{c\text{-}max}$. Similarly, for the full charging cycle all profiles tested perfectly follow the profile H in Figure 4.6 due to the identical dP_S/dt values which are again equal to $k_{c\text{-}max}$. The identical charge/discharge profiles for the ESS only occur for a full charge or discharge cycle, if a part load step is tested then the system behaviour will be a modified version of Figure 4.9.

The system response to the ramp load varies in Figure 4.10 with each control profile tested. Considering the ramp increase in power for profile L, during the low load region the dP_S/dt in Figure 4.10a is the lowest of the profiles tested, resulting in the gentlest increase in source power and the highest use of energy. The target energy E_t changes during the load transition given by $E_t=f_{ss}(P_L)$, since the load P_L is always changing until it settles at full power at 17s. This results in an overconsumption of energy in the initial several seconds after the load change, and only 24% energy is remaining when the load settles compared to 32% in the theoretical prediction, Figure 4.5. Consequently, the dP_S/dt at the end of the transient is 0.67p.u., higher than the limit $k_{c\text{-}max}=0.5$ due to the energy overconsumption. The sustained overconsumption of profile L is also noticeable in Figure 4.10c where the is energy is always lower than the theoretical profile L. Profile H achieves a linear increase in main source power during the ramp load increase as dP_S/dt is constant at 0.25p.u. This is due to a combination of the ramp duration and magnitude, and the prioritisation of high power loads with profile H. The situation is reversed during the ramp decrease in load, with profile L providing a linear change in main source power and profile H exceeding the dP_S/dt limit of $k_{c\text{-}max}$ for some of the transition.

The initial and final energy and main source power values in Figure 4.10a match the theoretical prediction in Figure 4.6 and so even with the overconsumption of energy during the load power ramp the ESS still remains online to respond to future transients.

The full load power transitions in Figure 4.10 demonstrate some worst case scenarios which could be experienced by the system. In a practical system, it is likely that multiple load systems would be active on the power network and so the likelihood of a full power transition is relatively low.

4.5 Super-capacitor based ESS simulation

The detailed performance of the advanced energy management control, developed in Section 4.3, was illustrated in the results presented in Section 4.4, but the generic simulation omitted the models of the individual sub-systems such as the energy device, the DC/DC converter and the low level converter controller. This section examines the behaviour of the advanced energy management controller on a simplified simulation model of a super-capacitor based ESS.

4.5.1 Simulation model

The super-capacitor based ESS model, presented in Section 3.2, consists of a simple super-capacitor model, an averaged DC/DC converter model and a basic controller. The controller has a low level super-capacitor current control with a non-linear function, and supervisory power balance and recharge control. Figure 4.11 shows an overview of the Simulink ESS model from Chapter 3, with the addition of the advanced energy management controller that determines the current command signal $I_{sc\text{-}ref}$, which is then sent to the low level super-capacitor current controller described in Section 3.2.1 to determine the converter duty cycle D. The command signal $I_{sc\text{-}ref}$ is calculated by dividing the ESS power reference $P_{ESS\text{-}ref}$ by the actual super-capacitor voltage V_{sc}. The reference $P_{ESS\text{-}ref}$ is composed of two components, a power balance component $P_{ESS\text{-}L}$ from the measured load power P_L, and $P_{ESS\text{-}re}$ from the SoC control in Section 4.3.

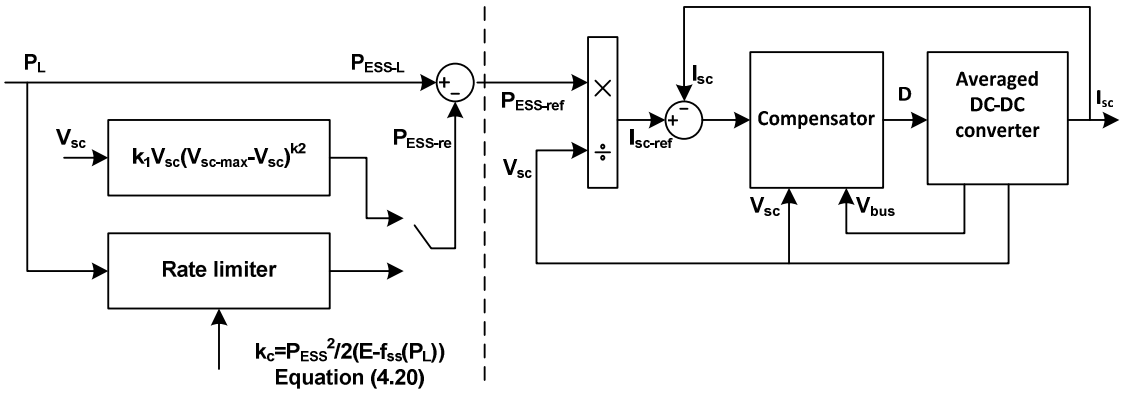


Figure 4.11. Simulation model overview of the ESS with the advanced energy management controller.

For comparison purposes, the model incorporates two different control methods to determine the SoC component $P_{ESS\text{-}re}$ as shown in Figure 4.11. The first SoC controller method is that described in Chapter 3, $P_{ESS\text{-}re}=k_1V_{sc}(V_{sc\text{-}max}-V_{sc})^{k2}$, where k_1 and k_2 are 0.64

and 1.5 respectively. The second method, proposed in Section 4.3, uses a rate limiter, whose rate is controlled by an external signal k_c determined by Equation (4.20).

4.5.2 Control design

The generic controller must be configured according to the system characteristics. Super-capacitors are used as the energy storage medium and so the energy can be determined as a function of super-capacitor voltage; maximum, minimum, target and actual super-capacitor voltages are $V_{sc\text{-}max}$, $V_{sc\text{-}min}$, $V_{sc\text{-}t}$, and V_{sc} respectively and are defined by the following equations:

$$\begin{aligned} E_{\max} &= \frac{1}{2} C_{sc} V_{sc-\max}^2 \\ E_{\min} &= \frac{1}{2} C_{sc} V_{sc-\min}^2 \\ E_t &= \frac{1}{2} C_{sc} V_{sc-t}^2 \\ E &= \frac{1}{2} C_{sc} V_{sc}^2 \end{aligned} \tag{4.25}$$

By substituting Equation (4.25) into Equations (4.11), (4.13) and (4.17), the steady-state super-capacitor voltage profiles L, C, H are obtained. The target super-capacitor voltage $V_{sc\text{-}t}$ can be calculated as Equation (4.26) for profile L, Equation (4.27) for profile C and Equation (4.28) for profile H, for a minimum load power $P_{L\text{-}min}$ of zero which enables the super-capacitors to be fully charged at no-load, as in Section 3.3 to enable a fair comparison of the control methods.

Profile L
$$V_{sc-t} = \sqrt{(V_{sc-\max}^2 - V_{sc-\min}^2) \cdot (1 - P_L / P_{L-\max})^2 + V_{sc-\min}^2} \tag{4.26}$$

Profile C
$$V_{sc-t} = \sqrt{(V_{sc-\max}^2 - V_{sc-\min}^2) \cdot (1 - P_L / P_{L-\max}) + V_{sc-\min}^2} \tag{4.27}$$

Profile H
$$V_{sc-t} = \sqrt{(V_{sc-\max}^2 - V_{sc-\min}^2) \cdot (1 - (P_L / P_{L-\max})^2) + V_{sc-\min}^2} \tag{4.28}$$

Three 48V 165F super-capacitor modules (BMOD0165, Maxwell [169]) are used providing a useable super-capacitor voltage range of $V_{sc\text{-}min}$=60V, $V_{sc\text{-}max}$=135V, with a maximum load of 25kW; identical to the configuration in Section 3.3. Figure 4.12 shows graphically the profiles L, C and H, determined by Equation (4.26) to (4.28), together with the k_1 k_2 profile from Section 3.3. Super-capacitor voltage is used as the indication of energy against load power.

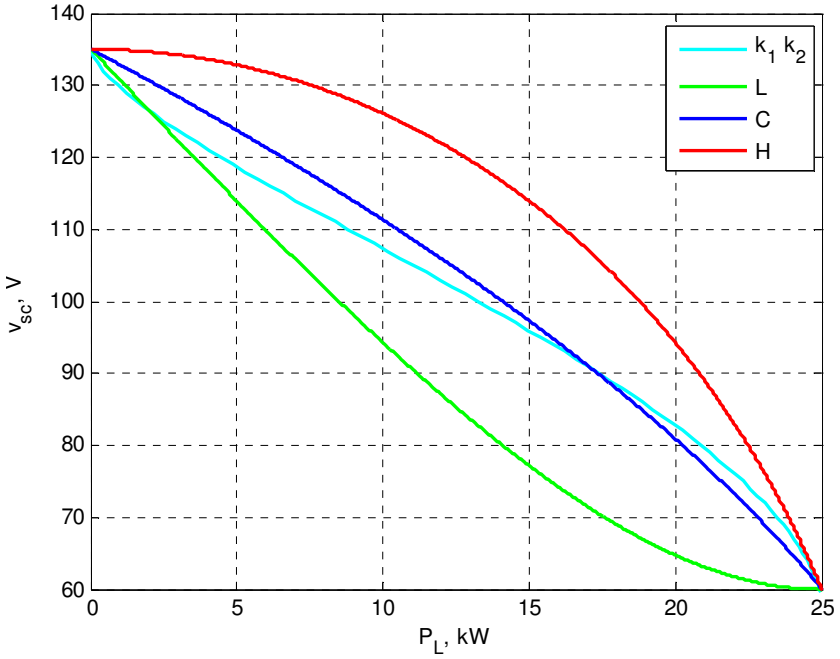


Figure 4.12. Comparison of controller profiles for the super-capacitor based ESS.

The profiles in Figure 4.12 demonstrate the same characteristic variation with load as in Section 4.2.1. Profile L heavily uses the available energy in the low power region to give a low dP_S/dt, when compared to the other profiles, at the expense of having less available energy at higher load levels; whereas profile H enables transients in the high power region to be suppressed more strongly, resulting in a lower dP_S/dt than in the low power region. Profile C offers a constant rate-of-change in power dP_S/dt over the full load region, which results in a non-linear trace in Figure 4.12 due to the non-linear relationship between super-capacitor voltage and energy. The control profile k_1 k_2 discussed in Chapter 3 offers a similar energy use to profile C with marginally more energy usage in both the low power and high power load regions.

The maximum rate-of-change in source power $k_{c\text{-}max}$ can be calculated using Equation (4.5) with $P_{L\text{-}min}$=0 to give Equation (4.29):

$$k_{c-\max} = \frac{P_{L-\max}^2}{C_{sc}(V_{sc-\max}^2 - V_{sc-\min}^2)} \tag{4.29}$$

The optimal rate-of-change in power for a specific load variation can be calculated using Equation (4.20) to give:

$$k_c = \frac{{P_{ESS}}^2}{C_{sc}(V_{sc}^2 - V_{sc-t}^2)} \tag{4.30}$$

where $V_{sc\text{-}t}$ is given by Equation (4.26) to (4.28).

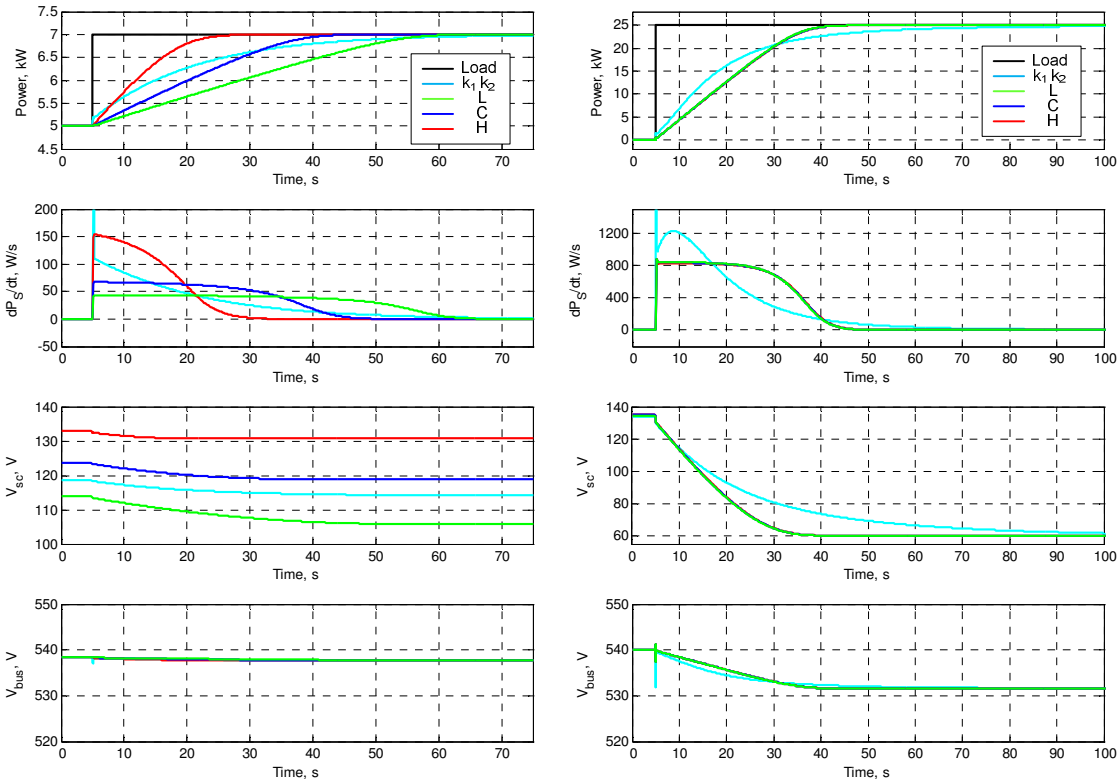
4.5.3 Simulation results

The system level simulation model developed in Section 3.2.1 is used to evaluate the performance of the advanced energy management control when applied to a non-ideal ESS for several different load profiles. The model consists of the ESS, shown in Figure 4.11, multiple load systems, and a permanent magnet generator [172] which is the main power source in the system. The generator control regulates the DC bus voltage to nominally 540V.

Section 4.4 discussed the key features of the advanced energy management control using an ideal ESS model and a simplified system. This discussion is not repeated in this section for brevity, only differences between the results from the ideal model, Section 4.4 and the non-ideal model are discussed.

4.5.3.1 Small and large load steps

Simulation results for two load steps are shown in Figure 4.13, when the ESS is commanded using profile L (green trace), C (blue trace) and H (red trace) from the advanced energy management control, and the control from Section 3.3 (cyan trace) for k_1=0.64 and k_2=1.5. In Figure 4.13, the top plot shows the load and generator power, the second plot is the rate-of-change in generator power dP_S/dt, the third plot is super-capacitor voltage, and the bottom plot is bus voltage.



(a) Small load step, 5kW to 7kW. **(b) Large load step, zero to 25kW.**

Figure 4.13. Load steps simulation results.

The general characteristics in Figure 4.13 correspond well with the system behaviour with an ideal ESS in Section 4.4. For the 5kW to 7kW load step in Figure 4.13 which is in the low power region of the 25kW system, profile L enables a gentle and generally linear generator response compared to the other three methods tested. The bus voltage shows no significant transients, and the the steady-state super-capacitor values in Figure 4.13 are in good agreement with the theoretical profiles in Figure 4.12.

A slight non-linearity is noticeable in the generator output power in Figure 4.13 when the generator is approaching the full load value which was not apparent in the ideal ESS simulation results in Figure 4.8. The non-linearity is a result of the voltage drop across the super-capacitor's internal series resistance, due to the simple electrical model used for the super-capacitor, shown in Figure 3.3. When the load increases the super-capacitor is discharging and the terminal voltage is lower than the internal voltage across the capacitor and so the usable energy viewed by the SoC control is slightly less than the value in Figure 4.12. Therefore the SoC controller imposes a higher rate-of-change in ESS power, calculated by Equation (4.30), and so slightly less energy is used than predicted. As the ESS power approaches zero, the super-capacitor terminal voltage equals the internal

voltage and the available energy is slightly higher than the value in Figure 4.12. The opposite effect is observed when the load decreases as less storage capacity is available due to the increased super-capacitor terminal voltage.

The dP_S/dt for profile L and C in Figure 4.13a are generally constant, corresponding to Equation (4.30), with a reducing dP_S/dt reflecting the non-linear part of the generator response. The generator response for the k_1 k_2 profile exhibits an instantaneous power change at the moment the load changes as the voltage drop across the super-capacitor series resistance is passed directly to the ESS power reference, causing a very large spike in dP_S/dt which does not appear with profile L, C or H. In addition, the generator power response for the k_1 k_2 profile is similar to profile C, since they use similar SoC profiles as shown in Figure 4.12. However, the dP_S/dt shows less variation for profile C, than with the k_1 k_2 method. In contrast, profile H has the largest dP_S/dt rate; nevertheless, the generator response is still gentler than if the ESS is offline.

A full power load step is shown in Figure 4.13b, and as in the ideal ESS results in Section 4.4, the generator response for all three ESS control profiles L, C, H overlap, since they have the same, limited dP_S/dt. Again, the non-linearity in generator power is apparent as the ESS approaches zero output, and the voltage drop on the super-capacitor causes an increase in the initial dP_S/dt. From Equation (4.29) or (4.30), the expected dP_S/dt for a full load transition should be $k_c=k_{c\text{-}max}$=777W/s, however, the simulation result shows 843W/s due to the super-capacitor voltage drop of 5V at t=5s, which causes a 9% reduction in the measured energy. As a result of the effect of the non-linearity, the generator is supplying the full load power approximately 40s after the load transient, which is slightly longer than the 32s prediction for the rate of 777W/s.

The generator power response when the k_1 k_2 method is used initially has a higher dP_S/dt which slowly reduces; 100s after the load transition, the ESS still has not reached the steady-state target of 60V as can be noticed in the third plot in Figure 4.13b.

4.5.3.2 Radar load

Figure 4.14 shows simulation results for two 100s cycles of the hypothetical radar load profile from Chapter 3, for the ESS profiles L, C and H, together with the k_1 k_2 profile. The super-capacitor voltage is initialised at 135V, which, due to the initial 5kW load is incorrect for all profiles from Figure 4.12 and so the ESS control must rebalance super-capacitor voltage with load. The ESS rebalances after approximately 50s in Figure 4.14 with the steady-state super-capacitor voltages at 100s approaching the theoretical values in Figure 4.12. All rate-limited profiles provide a relatively constant dP_S/dt for the step load changes in Figure 4.14, whereas the k_1 k_2 profile causes a triangular dP_S/dt response which has a similar average dP_S/dt as the other control profiles but a higher initial dP_S/dt. The rate-limited profiles dP_S/dt are quite constant during the high power step and so the generator response is linear; the non-linear behaviour from Figure 4.13 is not apparent during this step as the load changes again before the generator reaches a steady-state. The bus voltage is stable and varies due to the generator's droop control. Slight transient spikes are present at every load transition using the k_1 k_2 method due to the step changes in generator output power caused by the error in ESS output power.

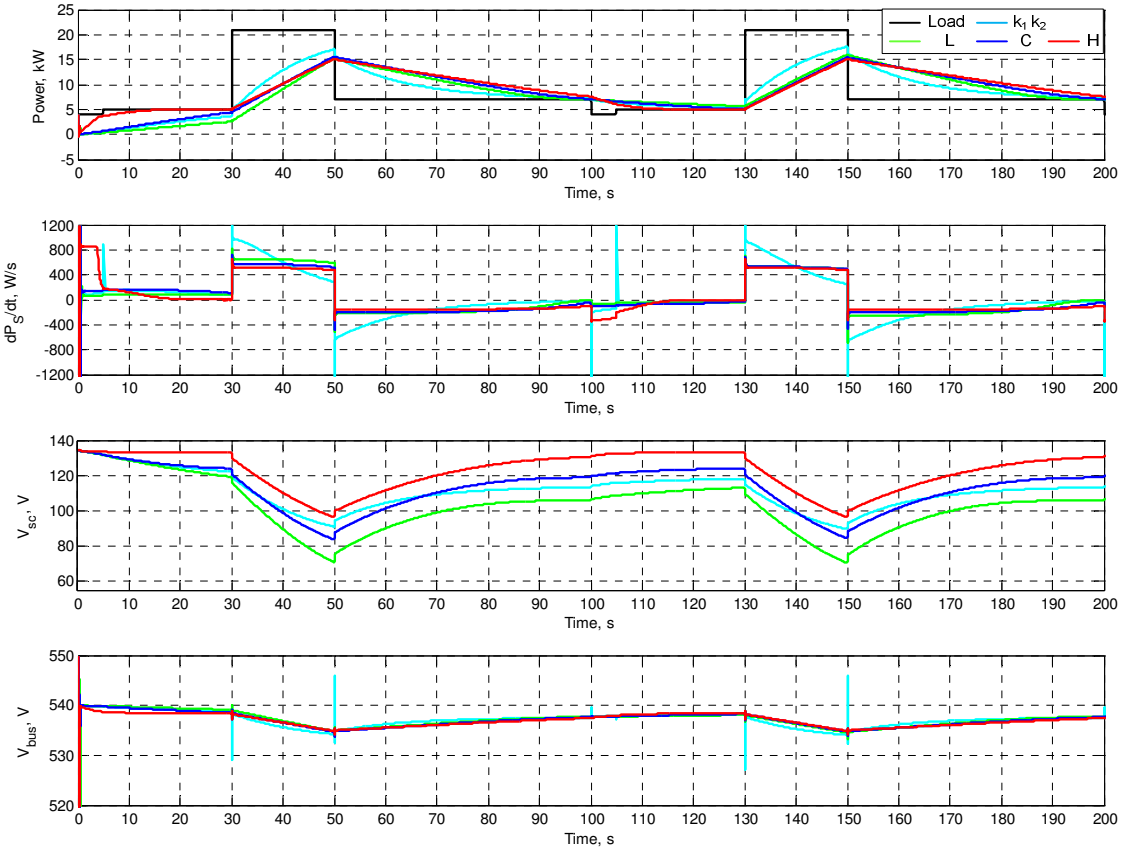
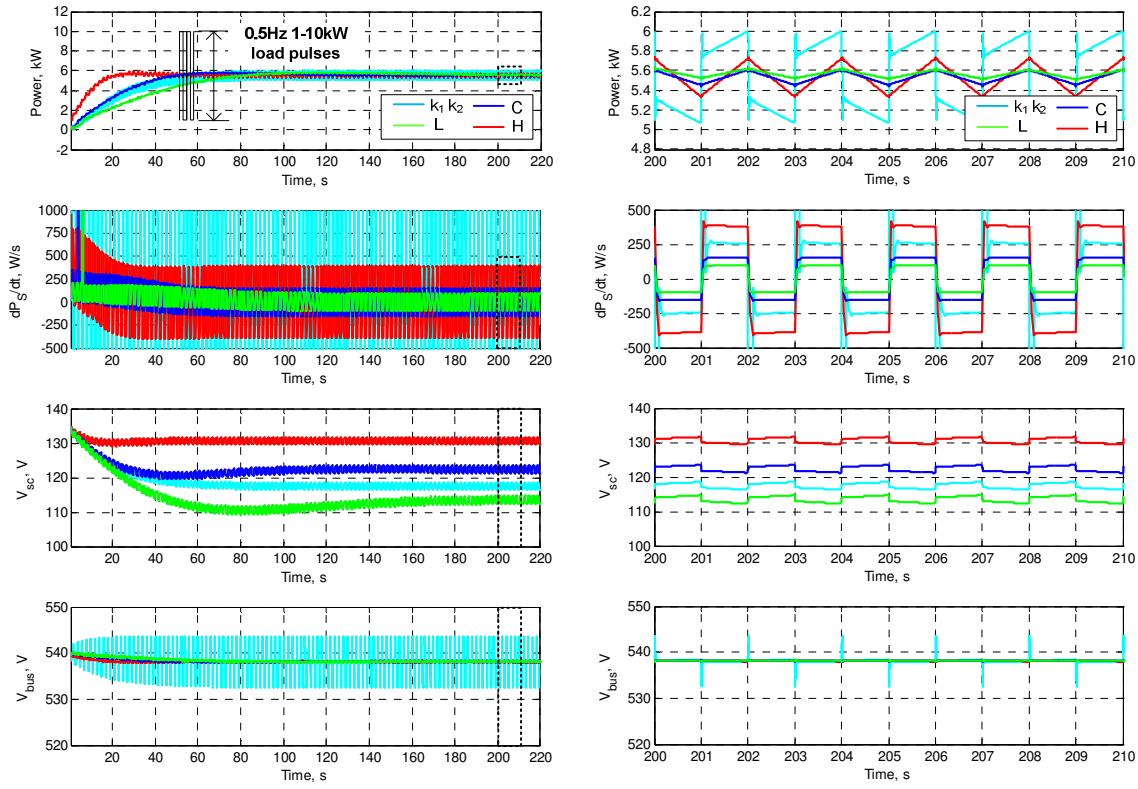


Figure 4.14. Radar load simulation results.

4.5.3.3 Pulse load

The same pulse load of 0.5Hz varying between 1kW to 10kW used in Chapter 3 has also been simulated, with the results in Figure 4.15a showing several load cycles. The super-capacitor voltage is again initialised at 135V and so the ESS control must rebalance super-capacitor voltage to the load power. The time for the ESS to rebalance is dependent on dP_S/dt, with the profile using least energy from Figure 4.12 achieving the rebalance fastest and so from Figure 4.15a, profile H (red) rises fastest, profile L (green) rises slowest with C and k_1 k_2 profiles being in between. All profiles reach the same steady-state power of 5.5kW, which is the average power of the 1-10kW pulse load, protecting the generator from the pulse load.



(a) Pulsed load, 1kW to 10kW, 0.5Hz. **(b) Magnified view from Figure 4.15a.**

Figure 4.15. Pulsed load simulation results.

Figure 4.15b shows a magnified view for a short time period from Figure 4.15a at time 200s to show the detailed behaviour. A slight power ripple is apparent in Figure 4.15b, with profile L exhibiting the smallest peak to peak ripple power of 0.1kW since the average load power of 5.5kW is within the low power region, while profile H has the largest ripple. Similar to Figure 4.13 and Figure 4.14, the k_1 k_2 method (cyan) has a noticeable step in power at every load transition, and corresponding spikes in dP_S/dt.

Several load profiles have been used in this section to compare the performance of the advanced energy management with that presented in Chapter 3. The advanced energy management control profile L offered the most gentle power source response for the load profiles in Figure 4.14 and Figure 4.15 since they fell within the low power region of the 25kW system. Had the overall power level been higher, profile H would have offered the gentlest generator power response.

4.6 Practical implementation and experimental test results

This section presents results from a real 1.14MJ energy storage system within the IEPNEF lab which is controlled using the advanced energy management technique, demonstrating the practical implementation of the control. The ESS was designed and constructed by Dr Frank Bryan as part of a related research project, however the author was responsible for the programming of the advanced energy management controller and some of the associated signal interfacing. All the experimental testing reported here was undertaken by the author. The experimental results demonstrate the ESS performance focusing on reducing the rate-of-change in generator power, mitigating bus voltage transients, and managing the state-of-charge of the ESS.

4.6.1 Experimental test system

Figure 4.16 shows a subset of the aircraft electrical system demonstrator facility [8], which contains a switched reluctance starter/generator (SRSG) [173], an active load (AL), an energy storage system (ESS), and a background resistive load.

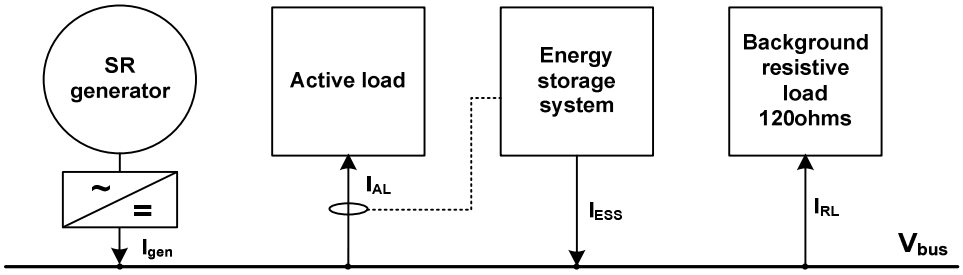
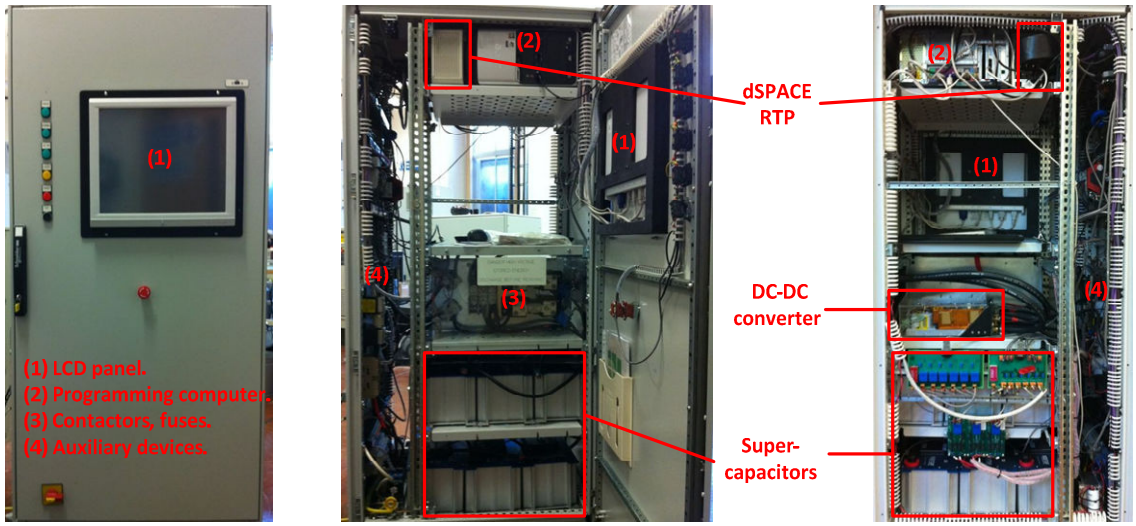


Figure 4.16. ESS system diagram for the test.

Due to the equipment restriction, a SRSG was used as opposed to the PMG in Chapter 3 which operates as the main power source and regulates the DC bus to be nominally 540V. The active load is used to emulate the dynamic electrical load profiles used in the test program, and a 120Ω resistive load provides a fixed background load level. The active load current I_{AL} is measured in real-time and used as part of the ESS reference $P_{ESS\text{-}L}$ as described in Section 4.5; in these demonstration results the background load current is not sensed by the ESS.

4.6.2 Energy storage system design and control

The ESS hardware is shown in the pictures in Figure 4.17. The ESS consists of three main components, all labelled in Figure 4.17c, which are the super-capacitor bank which serves as the storage medium, the bi-directional DC-DC converter which interfaces the super-capacitors with the DC bus, and the dSPACE real-time platform (RTP) which is in charge of the overall system. Additional auxiliary systems are labelled numerically in Figure 4.17. The ESS cabinet was designed and assembled as part of a separate project funded by Rolls-Royce; the advanced energy management control and practical implementation were developed solely as a part of this project and so are detailed in this chapter.



(a) Front view, front door closed. **(b) Internal front view.** **(c) Internal rear view.**

Figure 4.17. Energy storage system cabinet.

An overall schematic of the ESS is shown in Figure 4.18 to show the integration of the main components. The RTP (dSPACE, RT1103 [174]) is on the left, while the power hardware including the DC-DC converter (Chapter 2, Table 2.5, converter A) together with the peak current controller and the super-capacitors is shown on the right.

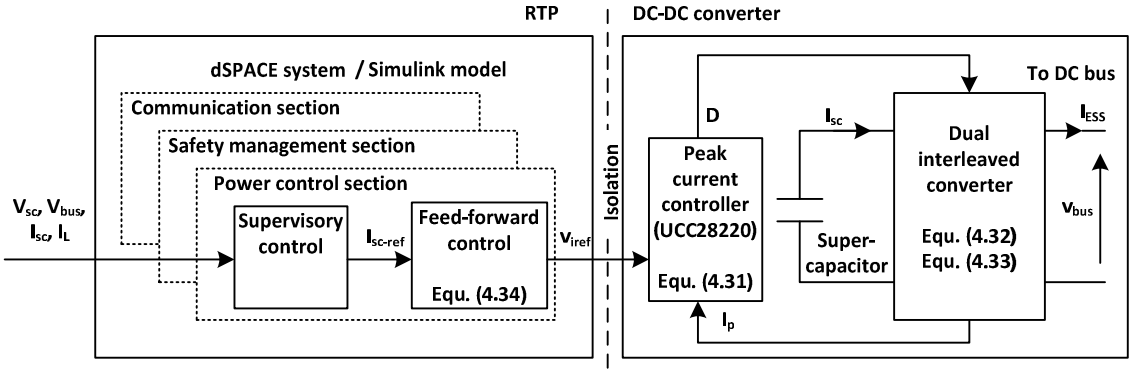


Figure 4.18. ESS dSPACE RTP and its connection to the power hardware.

The dSPACE RTP is programmed using a Simulink model, and implements the supervisory advanced energy management power and state-of-charge (SoC) control, plus the additional protection/communication functions. The supervisory control determines the super-capacitor current reference $I_{sc\text{-}ref}$ depending on the load level and SoC, which is based on the method described in Section 4.5. However, the converter cannot be directly commanded using $I_{sc\text{-}ref}$ as the peak current controller (which is part of the converter design [105]) requires a scaled voltage equivalent to $I_{sc\text{-}ref}$, labelled as v_{iref} in Figure 4.18. The mapping of super-capacitor current $I_{sc\text{-}ref}$ to the scaled control reference v_{iref} is implemented using an inverse-model-based feed-forward current controller [175], which requires accurate modelling of the peak current controller and the DC-DC converter. The following sub-sections give an overview of the development of the feed-forward control equation and the implementation and validation on the practical system; the full equations are omitted and reference is made to the appropriate equations developed in Chapter 2.

Peak current controller IC

The peak current controller is implemented in the test system by an analogue dual-channel integrated PWM generation circuit (UCC28220 [176]) with a programmable peak current capability. The mechanism of peak current control for a boost converter has been explained in the literature review, Section 1.2.3. For a two-phase converter with a peak current controller (detailed diagram given in Appendix A.5), each phase works in the same way as a single-phase converter, that is, the transistor in each phase is turned off with a duty ratio D when the measured current from the associated inductor exceeds the scaled reference v_{iref}, giving a peak transistor current I_p. The relationship between D, I_p and v_{iref}, is summarised in Equation (4.31) as given in [50],

$$v_{iref} = f_c(D, I_p) = (M_c \cdot D \cdot T + R_{cs} \cdot I_p + v_{bias}) / k_{pwm} \tag{4.31}$$

where k_{pwm} is the gain of the control reference v_{iref}, M_c is the slope compensation rate, T is the converter switching period, R_{cs} is the current sensor ratio, and v_{bias} is the bias voltage in the PWM chip. These parameters are set by the resistors in controller chip peripheral circuits. However, to ensure accuracy, the parameters are experimentally obtained by setting different v_{iref} and I_p values and measuring the output duty ratio D, and are shown in Table 4.1.

Table 4.1. Parameters of peak current controller

Parameter	k_{pwm} (-)	M_c (V/s)	v_{bias} (V)	T (s)	R_{cs} (Ω)
Measured value	0.624	33314	0.723	41.56μ	5.6m

Dual-interleaved converter

The dual-interleaved DC-DC converter has been analysed in detail in Chapter 2, and two equations, Equations (4.32) and (4.33), are required to describe the steady-state behaviour relevant to the feed-forward control.

$$I_p = f_p(V_{sc}, V_{bus}, D) \tag{4.32}$$

$$I_{sc} = f_{sc}(V_{sc}, V_{bus}, D) \tag{4.33}$$

In Equation (4.32) and (4.33), I_p and I_{sc} correspond to the peak current $I_{L1\text{-}peak}$ of phase L_1 and the average filter inductor current $I_{Lf\text{-}avg}$ as defined in Chapter 2, while V_{sc} and V_{bus} correspond to the low and high side voltages (V_1 and V_2) respectively of the dual-interleaved converter. Therefore, Equation (4.32) and (4.33) can be determined from Equation (A.24) and (A.25), Appendix A.6.

Feed-forward current controller and linearization

The three equations, Equation (4.31) to (4.33), fully describe the steady-state behaviour of the dual-interleaved converter with a peak current controller as required to develop the feed-forward controller. The equations have six variables, therefore, if any three are known, then the remaining variables can be determined mathematically; this approach is used to implement the inverse-model-based feed-forward controller.

By combining Equation (4.31), (4.32) and (4.33) and eliminating D and I_p, a mapping relationship between the control reference v_{iref} and the super-capacitor current I_{sc} can be determined, denoted as a function $f_{ref}()$, as:

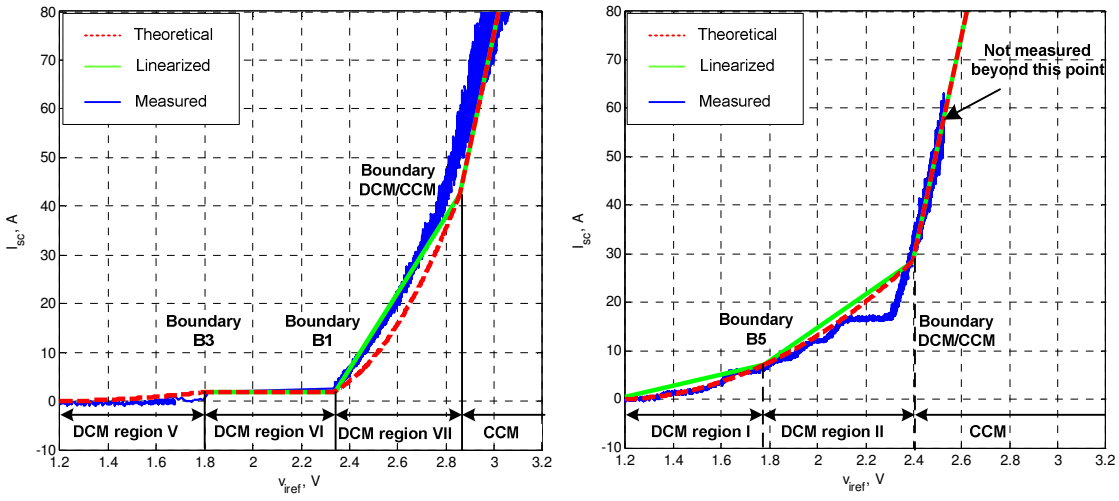
$$v_{iref} = f_{ref}(V_{sc}, V_{bus}, I_{sc}) \tag{4.34}$$

As the supervisory control determines the reference super-capacitor current $I_{sc\text{-}ref}$, this reference as opposed to the actual super-capacitor current I_{sc} is used in Equation (4.34). Equation (4.34) then enables the control reference v_{iref} to be calculated for the specific reference super-capacitor current $I_{sc\text{-}ref}$, provided that the voltages V_{sc} and V_{bus} are

measured in real-time. The feed-forward current controller has been designed based on Equation (4.34), and was implemented on the dSPACE real-time platform as shown in Figure 4.18.

Equation (4.34) is difficult to solve and incurs a high computation time since it is non-linear due to the squared D terms which appear in Equation (4.33); shown in full in Table A.5 and Table A.6 in Appendix A.6. As a compromise between accuracy and processing time, a piece-wise linearization of Equation (4.33) is performed to make the mapping between v_{iref} and $I_{sc\text{-}ref}$ piece-wise linear (the other two equations, $v_{iref}=f_c(D, I_p)$, $I_p=f_p(V_{sc}, V_{bus}, D)$ are linear, since $\partial v_{iref}/\partial D$, $\partial v_{iref}/\partial I_p$, and $\partial I_p/\partial D$ are piece-wise constant if V_{sc} and V_{bus} are fixed).

The accuracy of the piece-wise linearization of Equation (4.34) is demonstrated experimentally for two values of V_{sc} (200V and 290V) for a V_{bus} of 530V in Figure 4.19.



(a) V_{sc}= 200V, V_{bus}=530V(average), boost mode. **(b) V_{sc}=290V, V_{bus}=530V(average), boost mode.**

Figure 4.19. Comparison between theoretical, linearized and measured characteristic of I_{sc} versus v_{iref}.

To ensure V_{sc} is constant a DC power supply is used in this test as opposed to the super-capacitor modules. The bus side voltage is held approximately constant by the generator voltage control. The measured results, shown in blue, were obtained by gradually increasing $I_{sc\text{-}ref}$ in Figure 4.18 using a ramp profile. The theoretical predictions of super-capacitor current for a specific v_{iref} are shown in red and are piece-wise because of the different sub-DCM operating modes identified in Chapter 2 and reflected in the converter characteristics, Equation (4.32) and (4.33). The green line is a linearized version of the theoretical prediction (red) where the linearization takes place between the various DCM

region boundary points (labelled in the figure). To locate the boundary points in Figure 4.19, the boundary duty ratio D was calculated using the equations provided in Table A.5 (boost) and Table A.6 (buck) in Appendix A.6 and then I_{sc} and v_{iref} can both be calculated for the calculated D using Equation (4.31) to (4.33). A piece of software code was written to implement this function and a detailed flow-chart is given in Appendix B.6. The code is converted into an executable block in Simulink using the built-in 'S-function builder', and is executed every 50μs with updated measurement. The bus and super-capacitor voltages signals are filtered with a first-order filter with a time constant of 10ms.

The results in Figure 4.19 show the theoretical/linearized results generally have a good correlation with the measured data, only minor errors exist which are inevitable since the feed-forward control needs perfect modelling of the system to achieve zero error. Additional tests, not shown here, have been undertaken over the full operating range of the super-capacitors up to the voltage limit of 290V and the error between the measured and piece-wise linear prediction of I_{sc} is bounded by -10A to 5A.

A noticeable error can be observed in Figure 4.19b where the measured I_{sc} is constant for an increasing v_{iref} around 2.2V, causing a maximum error of 6A. The constant I_{sc} is due to the parasitic ringing which effectively causes a shift in the DCM/CCM boundary changing the operating mode. An example of this behaviour was illustrated in Figure 2.23 and Figure 2.27 in Chapter 2, where the average input current is reduced by the parasitic ringing and so the circuit behaves as if the CCM region is extended beyond the expected DCM/CCM boundary point as shown in Figure 4.19b.

The piece-wise linear form of Equation (4.34) exhibits a satisfactory correlation with the measured value over the full super-capacitor operating range. Therefore the piece-wise linear equation is used to form the feed-forward control in the test system to map between the reference super-capacitor current $I_{sc\text{-}ref}$ determined by the supervisory controller and the v_{iref} required by the peak current controller.

Supervisory control design

The supervisory control developed in Section 4.5.2 is used to determine the super-capacitor current reference, which is then converted to v_{iref} by the feed-forward current controller. However, the converter in the real ESS requires a higher voltage super-capacitor bank configuration and so the control parameters of the supervisory control are redesigned.

The dual-interleaved half-bridge converter used in the experimental system has a 170A current limit on the low voltage (super-capacitor) side to prevent the filter inductor saturating and can operate at this maximum current between 180V to 350V on the low voltage side [50] for 30kW operation. Lower voltages are permitted, however the power capability is reduced to prevent the filter inductor saturating.

The super-capacitor bank used in the experimental system comprises six 48V 165F super-capacitor modules connected in series (BMOD0165, Maxwell [169]), providing a maximum energy of 1.14MJ and a total voltage of 288V. This configuration is selected as a compromise between usable energy to demonstrate the ESS control and super-capacitor bank voltage required on the low voltage side of the dual-interleaved converter. The maximum super-capacitor voltage $V_{sc\text{-}max}$ in the experimental system is set at 250V as opposed to the absolute maximum of 288V as some system interaction effects exist if the voltage is above 264V (which are discussed in the experimental results, Section 4.6.3.1). The minimum super-capacitor voltage $V_{sc\text{-}min}$ is set at 140V and so the useable energy is 0.59MJ.

In Section 4.5.3 the simulation results demonstrated that profile L offered the gentlest rate-of-change in main power source demand for the small aircraft load profiles which were examined, since the average load power is a small proportion of the system capacity. As the ESS in the test configuration in Figure 4.16 only uses the measured current from a single active load system and the tested load power are relatively low, it is appropriate to undertake experimental tests using only profile L. The maximum load power $P_{L\text{-}max}$ is set to 30kW for the controller, however, for the dual-interleaved converter used in the test system full power operation at the minimum super-capacitor voltage will result in the super-capacitor current slightly exceeding the converter continuous current rating; in these demonstration results the load power is limited to 23kW to prevent input inductor

saturation. The steady-state SoC profile L for a six 48V super-capacitor module configuration with a maximum load power $P_{L\text{-}max}$ of 30kW is defined from Equation (4.26) as:

$$V_{sc-t} = \sqrt{(250^2 - 140^2) \cdot (1 - P_L / 30000)^2 + 140^2} \tag{4.35}$$

which is plotted in Figure 4.20, showing that the super-capacitor shall be charged to 250V at no load and discharged to 140V at full load of 30kW.

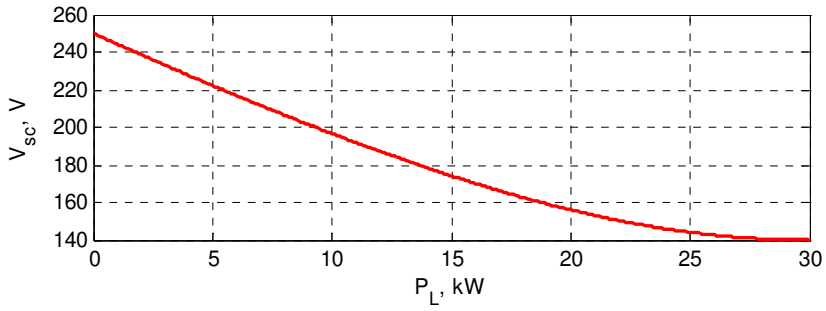


Figure 4.20. Steady-state super-capacitor voltage against load power P_L

With the steady-state profile L given by Equation (4.35) and Figure 4.20, the variable rate-of-change in power k_c can be determined from Equation (4.30), and for a full load transition from zero gives $k_{c\text{-}max}$=762W/s.

4.6.3 Experimental Validation

Results from the test system, shown in Figure 4.16, are presented in this section. The SRSG is used to regulate the DC bus to a nominal 540V at zero generator load, with a linear droop voltage of 20V at maximum generator power [173]. A combination of active and resistive load systems were used in each test and the specific conditions are listed in each section. The ESS, active load and generator current, and the super-capacitor voltage, were measured using an oscilloscope, while the other signals were measured by current/voltage sensors, transmitted to, and recorded by the dSPACE RTP. The test results are split into two sections, the first experiments demonstrate the effectiveness of the feed-forward control outlined in Section 4.6.2 whereas the second set of results show the performance of the supervisory ESS control.

4.6.3.1 Feed-forward controller tests

Two separate tests have been undertaken to demonstrate the performance of the feed-forward controller, which maps $I_{sc\text{-}ref}$ to v_{iref}, outlined in Section 4.6.1.

$I_{sc\text{-}ref}$ tracking performance

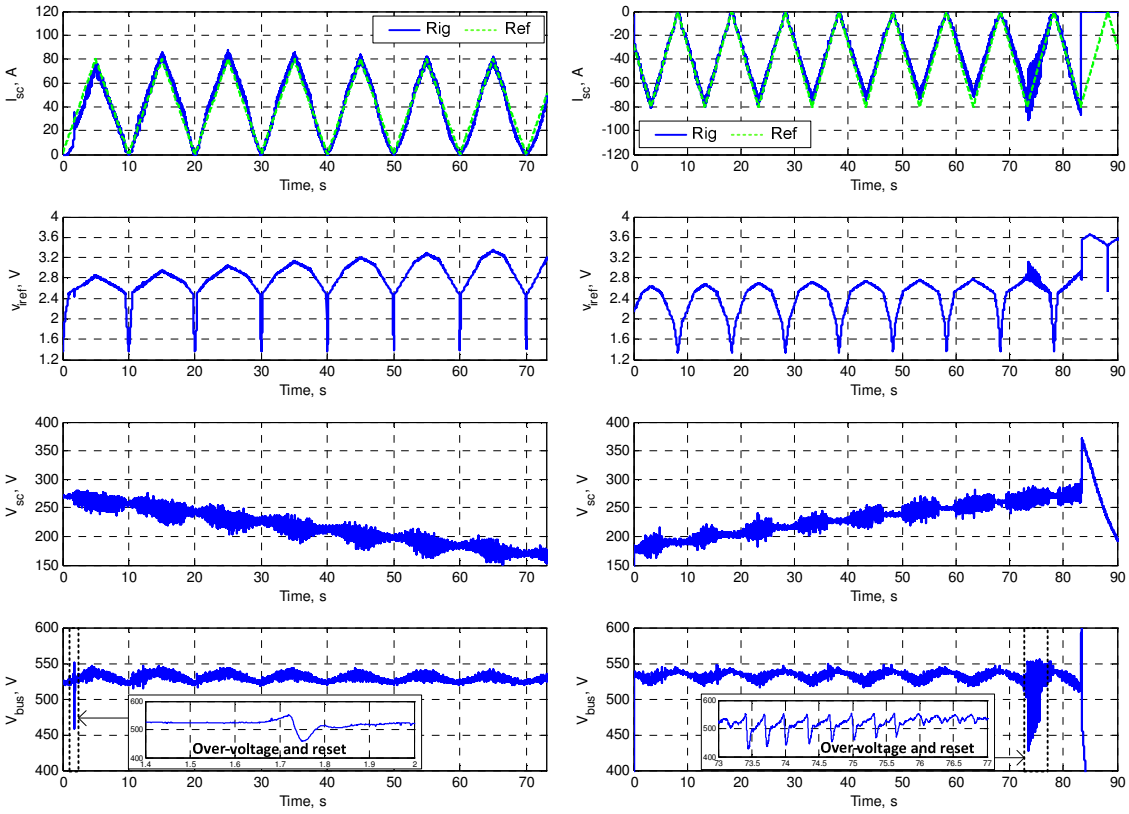
In the first test scenario, the supervisory ESS control in Figure 4.18 is disabled, and an ideal current reference $I_{sc\text{-}ref}$ commands the feed-forward current controller. Both charge and discharge performance is evaluated: for the ESS discharge test a constant 30kW resistive load is applied to the bus and there is zero load connected for the ESS charge test.

Figure 4.21 shows the results using the feed-forward controller, where an ideal triangular current $I_{sc\text{-}ref}$ (green) is the input to the feed-forward controller which produces the reference v_{iref} shown in the second row.

The current reference is set as a repetitive triangular current of zero to +80A (for boost mode, Figure 4.21a), or -80A (for buck mode, Figure 4.21b) and back to zero with a 10s cycle. Although the current reference varies linearly with time, the feed-forward controller output v_{iref} shown in the second row is only piece-wise linear reflecting the different operating modes of the converter and the varying magnitude of super-capacitor voltage V_{sc} (third row). The bus voltage V_{bus} in the fourth row varies due to the droop profile in the generator control and is a minimum when the generator is heavily loaded, and a maximum at light load.

In general the actual super-capacitor current I_{sc} (blue) follows the triangular current reference $I_{sc\text{-}ref}$ (green) well which validates the $I_{sc\text{-}ref}$ to v_{iref} function. A slight error is apparent between $I_{sc\text{-}ref}$ and I_{sc} at low current levels in Figure 4.21a (this is most noticeable at $t<3s$) which is attributed to the error between the linearized feed-forward control function and the actual I_{sc} to v_{iref} response, similar to that shown in Figure 4.19b.

The transient in I_{sc} in Figure 4.21b after t=73s is due to interactions between the feed-forward control function and the generator control unit. At t=73s, bus voltage V_{bus} in the fourth plot exceeds the generator control integral reset limit of 558V [173] which then disables the voltage regulation, causing V_{bus} to suddenly decrease until the control is re-enabled when the bus voltage drops below the generator reference voltage. The details of the transients are shown in the boxes in Figure 4.21. The exact origin of the over-voltage on V_{bus} at t=73s is not completely clear and is an area for future work.



(a) Boost mode operation (discharge). **(b) Buck mode operation (charge).**

Figure 4.21. Detailed ESS response for triangular $I_{sc\text{-}ref}$.

At t=83s, both the generator the ESS trip offline due to the significant over-voltage on V_{bus}. The super-capacitor voltage after 83s is due to the residual voltage on the converter, since a contactor disconnects the super-capacitors and the converter when the ESS is offline. The high super-capacitor voltage and the collapsed bus voltage cause the error in v_{iref}.

The results in Figure 4.21 show the feed-forward control tracks the current reference well for a wide range of super-capacitor voltages, however, the maximum super-capacitor voltage will be limited to 250V to avoid the transient behaviour shown in Figure 4.21.

Large step load

In this test the supervisory ESS control is partly enabled; the power flow balance is enabled in response to a load step, whereas the state-of-charge management is disabled initially until the load decreases and the ESS energy is low. A constant 120Ω resistive load is applied to the bus and the active load (AL) is programmed to impose a 2.7kW base load with a 20kW power step for 20s with rise/fall times of 14ms. The bus voltage is regulated by the generator control unit.

The results in Figure 4.22 show AL and ESS currents I_{AL} and I_{ESS}, generator current I_{gen}, super-capacitor current I_{sc} and voltage V_{sc}, and bus voltage V_{bus} from top to bottom.

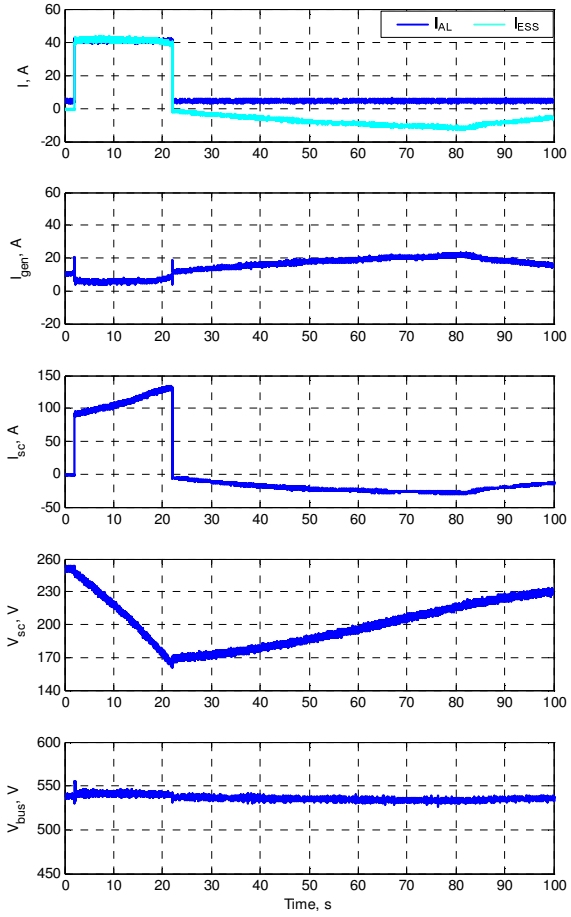


Figure 4.22. System response to large step load.

The ESS is offline for the first 2s in Figure 4.22 and so the generator supplies both the resistive load and active load base level. At t=2s the active load is increased to 22.7kW for 20s and the ESS is enabled to fully supply the active load power since the ESS power control uses the measured active load current as the reference. Consequently, the generator current I_{gen} is reduced to 5A as it is only supplying the resistive load, as shown in the second row. The good correlation between ESS current and active load current again

confirms the good performance of the feed-forward controller over a wide super-capacitor voltage range as in this process the super-capacitor voltage V_{sc} changes from 252V to 165V (fourth row in Figure 4.22). The bus voltage V_{bus} in the fifth plot is increased slightly when the generator is unloaded as the droop voltage component reduces with reduced generator power. The active load power is switched back to 2.7kW at t=22s and a simple PI based recharge function is activated in the ESS.

The results in this section confirm the performance of the feed-forward controller which will be used in the following section where the full supervisory ESS control from Section 4.6.2 will be enabled to determine the super-capacitor current reference $I_{sc\text{-}ref}$.

4.6.3.2 Supervisory control tests

Two different types of load profile have been programmed in the active loads in this section to demonstrate the system level performance of the ESS. The advanced energy management control from Section 4.5 is used with profile L implemented.

Hypothetical multi-functional radar load profile

Figure 4.23 shows simulation and test results for the ESS and generator when the active load is programmed to follow the hypothetical radar load profile used in Section 3.4.2, which is paralleled with a 120Ω resistive load. The radar profile contains four power steps which are 4kW, 5kW, 21kW and 7kW. The SRSG regulates the DC bus and the droop control is active. The full supervisory ESS control, shown in Figure 4.18, is enabled.

The simulation results are obtained from a model using the averaged DC-DC converter model with the simple low level super-capacitor current control from Section 3.2.1, the supervisory ESS control of Section 4.5.2, and a model of the SRSG developed by Virgilio Valdivia using a behavioural modelling technique [173] to ensure a fast run-time. The detailed ESS simulation behaviour will differ from the experimental ESS, however the effect of the different converter and low level control will be negligible on the system level behaviour as it is the supervisory control which determines the system level operation.

The results in Figure 4.23 show two consecutive radar load cycles; the first plot is the AL and ESS currents I_{AL} and I_{ESS}, the second plot is the generator current I_{gen}, the third and fourth plots are the super-capacitor current I_{sc} and voltage V_{sc}, respectively and the last plot

is the bus voltage V_{bus}. The super-capacitor current reference $I_{sc\text{-}ref}$, produced by the supervisory controller is also plotted, shown in green in the third plot (recorded by dSPACE RTP). The experimental data and simulation results are overlaid to demonstrate the close match between the data sets. The general characteristics of the results in Figure 4.23a for the radar load are similar to those in Section 4.5.3.2 and so the discussion here focuses on the differences between the results.

The generator current response exhibits different constant rates-of-change in current during each load power level in Figure 4.23. The state-of-charge control determines the specific rate-of-change in generator power for each load according to the available ESS energy. This is most visible in Figure 4.23 during the high power step when the dP_S/dt from the experimental results is 385W/s (average over the load step) which is in good agreement with the simulation of 331W/s and 337W/s from theoretical calculation.

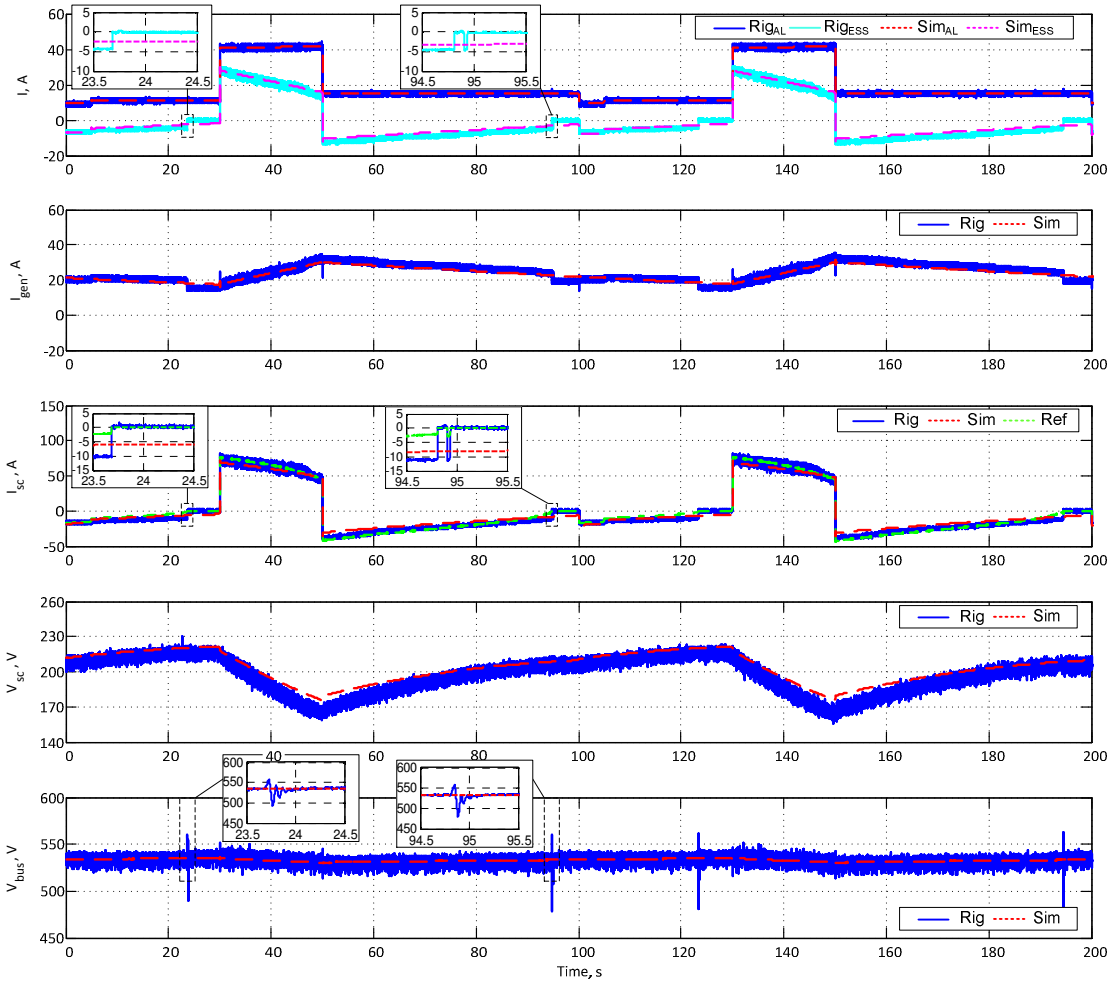


Figure 4.23. Overall system response due to hypothetical radar load.

The low rate-of-change in generator power imposed by the supervisory ESS control causes the ESS to never reach a steady-state value in Figure 4.23, though the ESS output is

approaching zero for all load powers. For example, considering the peak power of 21kW from 30s to 50s, the super-capacitor voltage should be 153V in the steady-state, however the measured voltage is 163V at 50s in Figure 4.23; if the load does not change at 50s then the super-capacitor would continue discharging until the voltage settles around the target voltage of 153V. The system enters a dynamic steady-state where the measured voltage or current waveforms are repetitive for the 100s cycle load profile.

In Figure 4.23 there are two noticeable voltage transients per load cycle, with magnified plots being shown in the boxes in Figure 4.23, which are caused by the sudden decrease in ESS current. At t=23.7s, the super-capacitor current reference $I_{sc\text{-}ref}$ (third row, green) reaches the ESS dead-band (Appendix B.6) threshold of $\pm$2A, during which the ESS is disabled to avoid sudden changes in power flow direction; however, the actual super-capacitor current is -10A and the ESS output current is -4A (charging), with the error in reference and actual I_{sc} being caused by the inaccuracy of the feed-forward control. Disabling the ESS when the output is -4A and not zero causes a step load decrease on the generator, which increases the bus voltage, triggering the resetting of the integral component in the generator voltage control. In addition, the bus voltage transient at t=94.5s interacts with ESS controller which sets a small pulse in $I_{sc\text{-}ref}$ at t=95s.

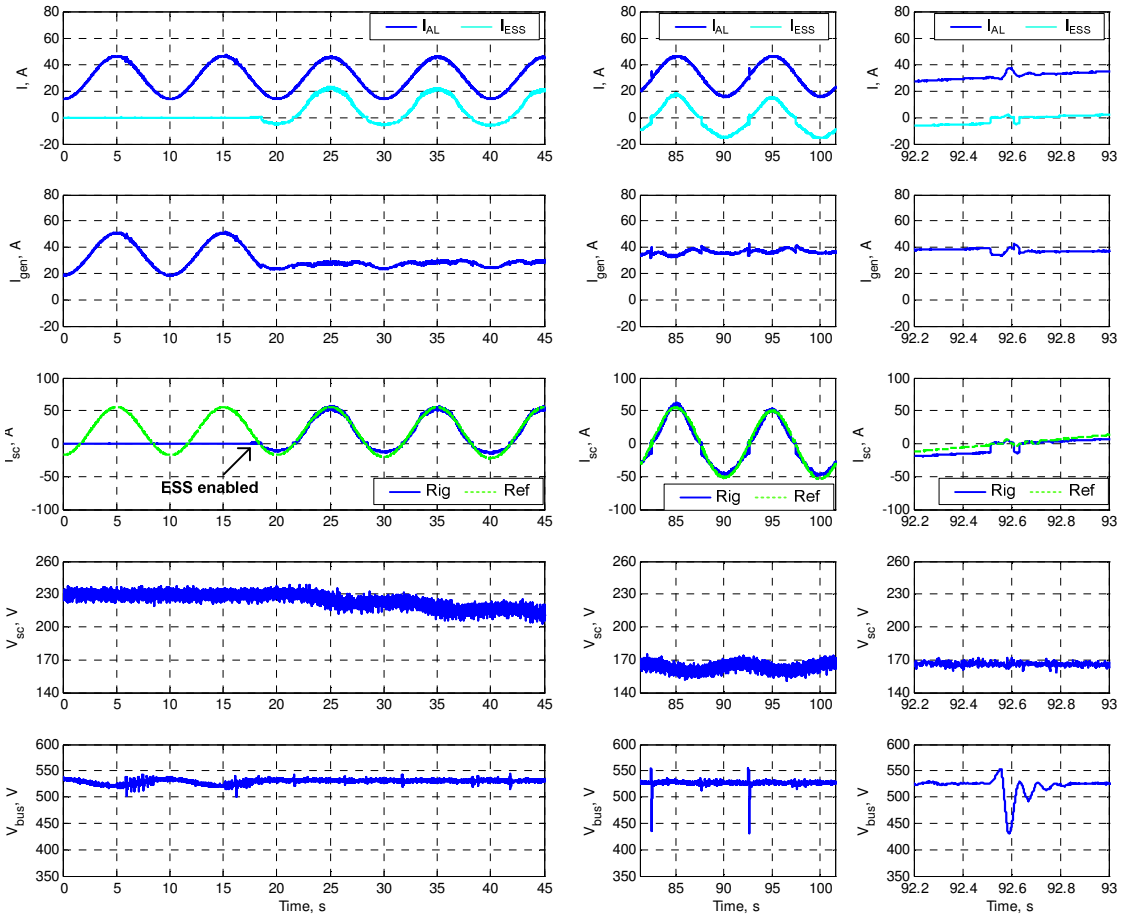
In general, the results from the simulation correlate well with the test data, with the exception of the transients resulting from the deactivation of the ESS, and that the super-capacitor voltage in the simulation is always higher than the experimental value. A number of issues may contribute to the difference in super-capacitor voltages, including converter efficiency, feed-forward control inaccuracy and measurement errors, and it is not completely clear which effect is most significant in determining the ESS behaviour. The effect of converter losses are apparent during the high power period from 30s to 50s, where the super-capacitor current from the experiment is higher than the simulation result, causing deeper super-capacitor discharge, while achieving the same ESS current.

Sinusoidal load profile

A set of experimental tests for a variable frequency sinusoidal load emulated by the active load system (with a high bandwidth current control loop around 3kHz[173]) indicate the effective bandwidth of the ESS. All the emulated sinusoidal loads consist of a base 15kW

load plus a ±8kW peak sinusoidal element of 0.1Hz to 150Hz. The 120Ω resistive load is connected as a background load; the SRSG regulates the DC bus voltage and the droop control is active; the full supervisory ESS control is enabled.

The results in Figure 4.24 to Figure 4.27 show the AL, ESS and generator currents together with the super-capacitor current and voltage, and the bus voltage. The generator currents are measured at the bus side, which also include bus filter capacitor current. The results in this section show the system performance with the ESS disabled for approximately the first 50% of time, then the ESS is enabled and is active for the remaining time period.



(a) Operating waveforms. **(b) Steady-state.** **(c) Transients.**

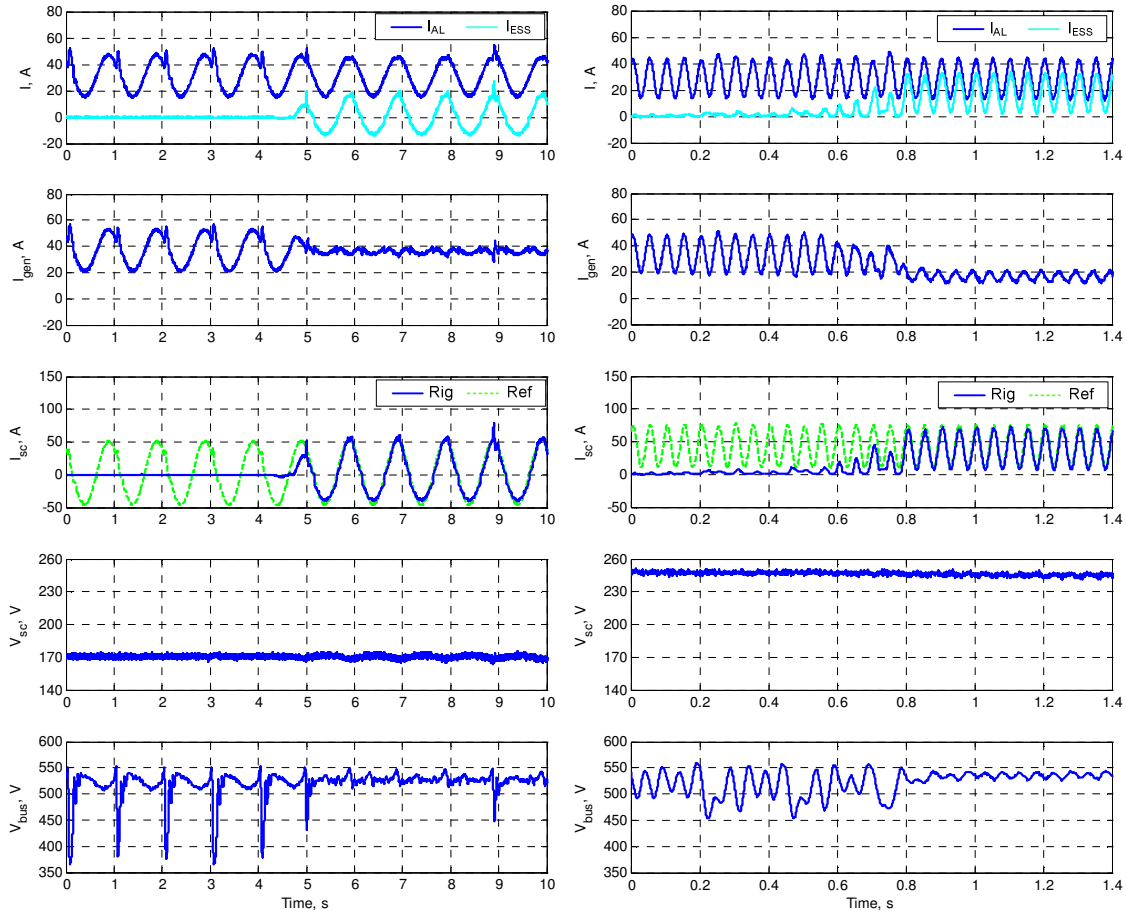
Figure 4.24. Overall system response due to 0.1Hz sinusoidal load variation.

In Figure 4.24a the active load is imposing a 0.1Hz sinusoidal load current which is solely supplied by the generator in the first 18s and so the bus voltage varies in a similar manner due to the effect of the droop control (520V to 535V). The ESS is enabled at approximately 18s in Figure 4.24a and the ESS supplies the ripple component of the sinusoidal load. Consequently, the generator current ripple is significantly reduced, which reduces the bus voltage ripple. The super-capacitor voltage is gradually falling in Figure

4.24a, towards a steady-state value of 174V for a 15kW load (average load power) according to Equation (4.35). Figure 4.24b shows data for when the ESS has reached steady-state operation for the 0.1Hz load and the super-capacitor voltage is approximately 168V which shows a small error compared to the theoretical value.

The super-capacitor current I_{sc} in the third row correctly tracks the reference $I_{sc\text{-}ref}$ with the exception of the zero-crossing region which causes the bus voltage transients in Figure 4.24b (shown in detail in Figure 4.24c) and is consistent with Figure 4.23. Should the accuracy be improved at low current region, the sudden switch of the converter may not cause voltage transients when the converter control input enters the deadband .

In the test results shown in Figure 4.25 and Figure 4.26, the active load is programmed to impose 1Hz, 20Hz, 100Hz and 150Hz sinusoidal loads with a 15kW base load plus a ±8kW peak sinusoidal element.



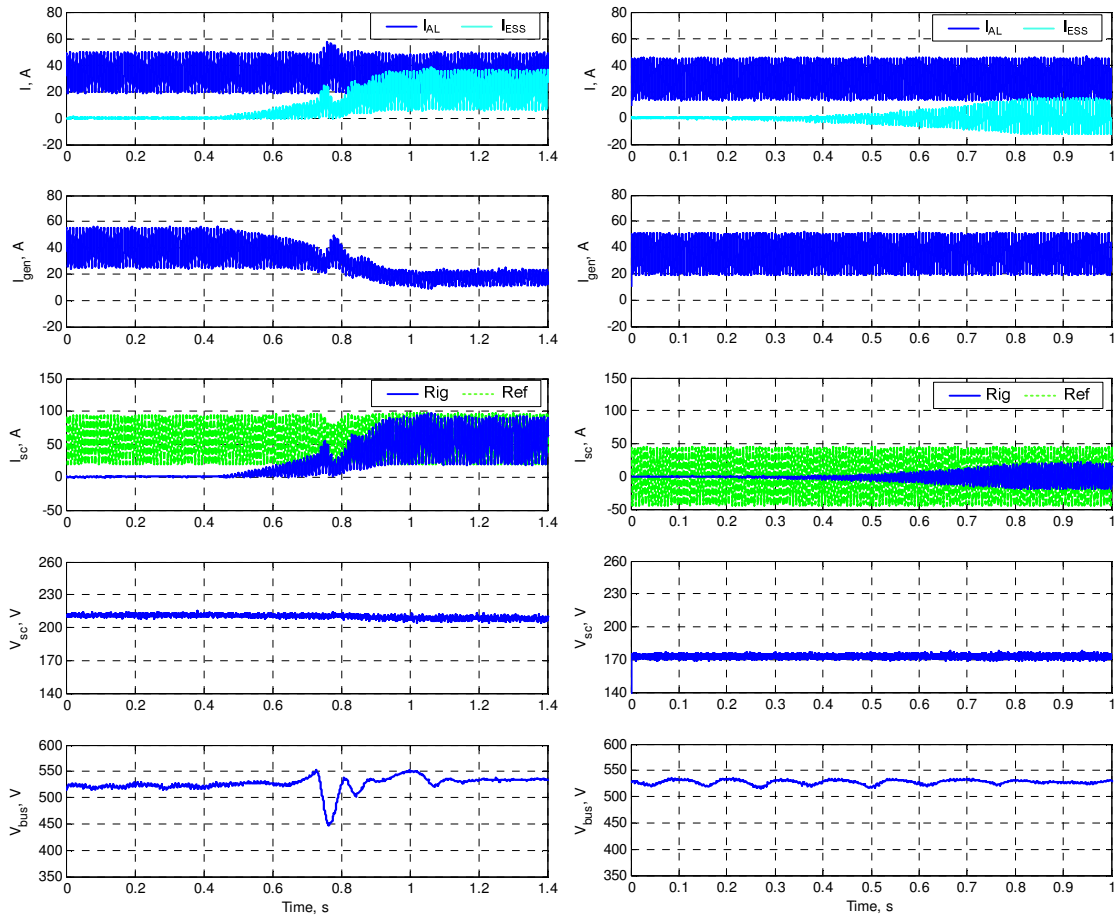
(a) 1Hz load. **(b) 20Hz load.**

Figure 4.25. Overall system response due to low frequency sinusoidal loads.

The results in Figure 4.25a (1Hz) and Figure 4.25b (20Hz) show significant bus voltage transients reaching down to 365V and 450V due to the generator control reset during the

first half of the test data with the ESS inactive. When the ESS is enabled after t=4.6s in Figure 4.25a and t=0.5s in Figure 4.25b, the generator current is significantly smoother as the ESS is supplying the sinusoidal element of the load variation. The bus voltage is more stable when the ESS is active, however, there is still one smaller voltage transient in Figure 4.25a for the 1Hz load.

When the load frequency increases to 100Hz, Figure 4.26a, the ESS still significantly reduces the load variation experienced by the generator, resulting in a reduced ripple in I_{gen}. There is little ripple voltage on bus whether the ESS is enabled or disabled as the generator output capacitor absorbs the ripple current.



(a) 100Hz load. **(b) 150Hz load.**

Figure 4.26. Overall system response due to high frequency sinusoidal loads.

When the load frequency increases to 150Hz in Figure 4.26b, the generator current contains a significant ripple component even with the ESS active. This is due to the slow converter dynamics and the zero crossing delay of 2.5ms which results in the ESS current being distorted (Figure 4.27) and so only offering partial compensation of the load variation. No severe voltage transients can be observed on the DC bus voltage in Figure

4.26b; however a slight ripple voltage at approximately 10Hz is apparent when the ESS is disabled which is suppressed when the ESS is enabled.

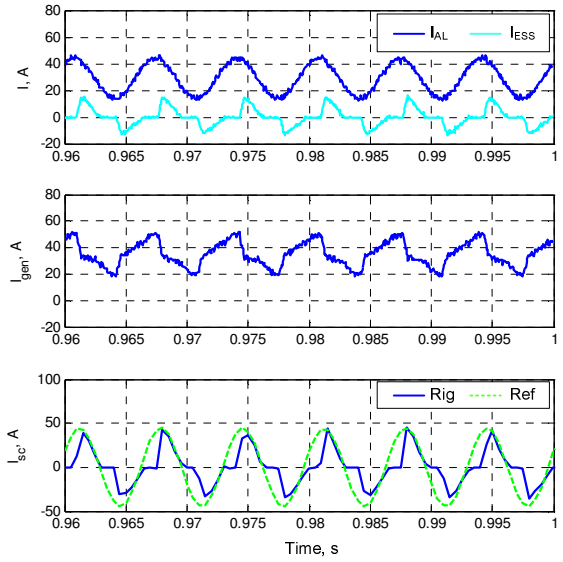


Figure 4.27. Magnified view of Figure 4.25d from 0.9s to 1s.

The test results in Figure 4.25 and Figure 4.26 are the summary of several separate tests which were performed with different initial values of super-capacitor voltage. The super-capacitor voltage in Figure 4.25a and Figure 4.26b was at approximately the correct value of 174V for the 15kW average load value and so the ESS quickly enters steady-state operation signified by the I_{ESS} having zero DC component. In Figure 4.25b and Figure 4.26a the super-capacitor voltage was higher than the theoretical value of 174V from Figure 4.20, and so when the ESS is enabled I_{ESS} has a positive component which causes the super-capacitor voltage to decrease until the ESS reaches a steady-state condition.

The set of test results in Figure 4.24 to Figure 4.27 demonstrate the ESS can effectively shield the generator from the load frequency variation if the frequency is 100Hz or less. The actual upper limit for this ESS is likely to be slightly higher than 100Hz but less than 150Hz.

4.7 Conclusions

An advanced energy management control with an integrated variable rate-limit function is proposed and analysed in this chapter for an energy storage system. The variable rate-limit enables the rate-of-change in source power to be constrained within acceptable levels inspite of instantaneous load changes. Analysis shows that the smallest peak rate-of-change in source power can be achieved when this rate is constant throughout a load transition, with the specific rate being dependent on the amount of useable energy and the load variation. The energy management controller can be designed to use the available energy more aggressively during load changes in the low or high power regions, profile L Equation (4.15) or profile H Equation (4.17) respectively, while offering the lowest possible rate-of-change of generator power, or offering a fixed minimum rate-of-change in power for a given total load and amount of energy, profile C Equation (4.16).

The performance of the advanced energy management control using all three control profiles is examined using two simulation models to validate the concept. The first simulation uses an ideal generic ESS model and the control profiles enable different performance depending on the load region; all simulation results perfectly match the theoretical prediction and validate the concept of a constant rate-of-change k_c in demanded main power source output, which depends on both the load change and available energy ($k_c=\Delta P_L^2/2\Delta E$) while managing the state-of-charge. A second simulation provides further validation of the advanced control concept using a more realistic model of an electrical system with a generator, converter, super-capacitors and electrical loads. The results show similar performance as in the generic ESS model, although some slight non-linearity is apparent in the actual rate-of-change which differs from the expected k_c values due to SoC measurement errors. However, when compared with the control method described in Chapter 3, there is significant improvement in exploiting the energy and managing the source transients.

The proposed advanced control method is implemented in a real energy storage system in the IEPNEF test environment, where the ESS consists of a dual-interleaved converter with a peak current controller and super-capacitor bank. An inverse-model based feed-forward controller which maps the current reference $I_{sc\text{-}ref}$ determined by the advanced ESS control to the scaled voltage equivalent required by the peak current control is proposed and

experimentally validated over the full super-capacitor operating range. The performance of the proposed advanced control method using profile L is experimentally validated for a hypothetical radar load and the results show a well controlled rates-of-change in the generator power. Slight differences are apparent between the experimental and simulation results relating to the assumption of a lossless converter, measurement errors and limited performance of the feed-forward control at low current levels. A series of sinusoidal load tests indicate the converter and control have a dynamic performance limit of approximately 100Hz.

Chapter 5 Conclusions and further work

5.1 Introduction

This chapter summarises the main areas of work in the thesis, the contribution of the research, and suggestions for further work.

5.2 Summary of the thesis

This thesis describes the modelling, simulation, emulation and experimental validation of a super-capacitor based energy storage system for a small electrical system, covering topics on the converter, the converter controller, the energy storage system controller and energy management strategies. The summary of the thesis will be described in this section in the order of each chapter.

5.2.1 DCM converter analysis

When using a super-capacitor for storage, the interface converter has to operate over wide ranges of voltage and power, which includes the discontinuous conduction mode. A detailed analysis is undertaken of the dual-interleaved converter with an interphase transformer, which has been identified as a candidate topology for the super-capacitor based ESS. The analysis focuses on the discontinuous conduction mode where at least one of the phase currents is zero for a period of time. Depending on the sub-circuit sequences that appear in a switching cycle, seven different discontinuous conduction operating modes have been identified for the converter. Correspondingly, seven operating regions in the M:D plane (voltage ratio against duty ratio) are obtained, representing where these discontinuous patterns occur. The operating patterns have been validated by Saber simulation and experimentally using two converters with different inductance ratio (L_r=71.7 and 35.1), though ringing between parasitic circuit elements obscures some of the waveforms. The equations for peak and average inductor current have been derived from the detailed operating waveforms, and are utilized in Chapter 4 to implement a feedforward super-capacitor current controller.

5.2.2 ESS simulation and emulation

The load smoothing and bus voltage stabilising performance of an energy storage system within a small DC electrical system was examined through Simulink modelling and simulation. The energy storage system model consists of a three super-capacitor modules connected in series (165F, 48V each), a virtually lossless averaged DC-DC converter model with an inner average current control loop and a supervisory controller. The supervisory controller performs two functions, commonding the ESS output current to track load transients by means of a power balance calculation, and secondly managing the super-capacitor state-of-charge by adding a recharge power component to the overall power flow of the storage system. The recharge power is a function of the super-capacitor voltage and uses two control parameters k_1 and k_2, $P_{sc\text{-}re}=k_1(V_{sc\text{-}max}-V_{sc})^{k2}$. The effect of k_1 and k_2 on the overall system performance when subjected to a pulsating and intermitent load was investigated, in particular with regard to the source power profile. The investigation indicates the potential for more sophisiticated control methods to manage the power flow and super-capacitor state-of-charge, i.e., the function may not be restricted by the equation form using only two parameters k_1 and k_2.

The controller's performance is examined in experiments by using the hardware-in-the-loop technique, where a programmable active load is configured to emulate the ESS behaviour, and is tested within the IEPNEF lab, with a real generator and emulated loads of a radar load (21kW at peak) and a pulsating load (switching between 1kW and 10kW). The emulation results show excellent agreement with the simulation, illustrating the effectiveness of the ESS in smoothing the generator power profile and eliminating bus voltage transients. This is reflected in the generator torque which is vastly reduced using ESS from 200Nm to less than 100Nm at peak with the radar load, and kept constant at 240Nm with the pulsating load. Also, the bus voltage transients is stabilized at nominal voltage of 540V, while without the ESS, the bus voltage reaches a minimum of 189V in a 5kW to 21kW load transition.

5.2.3 Advanced ESS control

An advanced control method is proposed in Chapter 4 for the ESS, where more flexible profiles of steady-state energy against load power are investigated, and also an emphasis is

placed on controlling the rate-of-change in source power. A general form of steady-state energy, E, against load, P_L, is developed, expressed as: $E=f_{ss}(P_L)$, where $f_{ss}()$ can take various forms and is a curve on an E against P_L map. The shape of the curve $f_{ss}()$ determines the amount of energy transferred by the ESS for a particular load change, suggesting that the generator power profile may be tailored according to operational requirements. Three SoC against load profiles are suggested, L, H and C, providing stronger ESS support in the low load region, the high load region or an even performance across the whole load range respectively. However each profile ensures that the maximum rate-of-change in source power is never greater than a defined maximum, $k_{c\text{-}max}$. For a given SoC profile, an operating strategy is proposed whereby $f_{ss}()$, the planned energy use ΔE for a load transition ΔP_L is determined, and the ESS power transfer is commanded to change at a rate $k_c=\Delta P_L^2/2\Delta E$, since this will impose the smallest achievable dP/dt on the power source.

The proposed control profiles and strategies are first examined in a Simulink simulation with a generic lossless ESS model which only represents the power flows and stored energy. Small and large step loads, a ramp load and a more complicated avionic load profile are tested and exhibit well-controlled rates-of-change in source power. However, when the control is migrated to a more realistic IEPNEF model, non-ideal behaviour such as slight non-linearities in the rate-of-change of power were observed due to the internal resistance voltage drops on the super-capacitor providing an erroneous indication of available energy (9% in one simulation example). Nevertheless there is significant improvement in the generator power profile when compared to the results in Chapter 3, for example, the peak rate-of-change of generator power has been reduced to almost a half in the high power period (30-50s) radar load, Figure 4.14.

A real super-capacitor energy storage system was tested within in the IEPNEF, together with a real generator and emulated loads to examine the controller's performance. A dual-interleaved DC-DC converter with IPT as described in Chapter 2, was used as the interface between six super-capacitor modules (Maxwell, 165F, 48V each) and the 540V DC bus. An inverse-model based feedforward controller was implemented to command the super-capacitor current, using the analysis of the converter in Chapter 2, and demonstrated close matching of the current reference and actual output with a -10A to 5A error observed in the

experiments. A supervisory controller for SoC management deploying the L profile was used and showed well-controlled rates-of-change in source power, which matched closely with the simulation. However, due to the limitation of the converter current control and the absence of losses in the simulation, some small differences were observed, particularly in the super-capacitor voltages with a maximum error of 10V, which could form a topic for further investigation. Finally sinusoidal load test revealed that the storage system may achieve effective compensation for load frequencies up to 100Hz.

5.3 Contributions of this research

The contributions of this research may be summarised as follows.

5.3.1 DCM converter analysis

All the discontinuous conduction operating patterns of the dual-interleaved converter with an IPT for both boost and buck modes have been thoroughly analysed and examined in simulation and experimentally. In addition, the boundary conditions between the operating patterns have also been derived, which have not been reported in the literature. In constrast with the analysis in literature specific to a certain converter topology, the analysis in this thesis is also widely applicable to a group of similar converters, the dual-interleaved converter with uncoupled, and directly coupled inductors, by transforming the circuit as illustrated in Appendix A.1. The symmetry characteristics between boost and buck mode operation were identified and exploited to simplify the analysis, furthermore this analysis may have applications in other bi-directional converter topologies, for example, interleaved circuits with higher phase numbers. The average filter inductor current equation $I_{Lf\text{-}avg}(V_1, V_2, D)$ is derived in Appendix A.6, and a cross-over feature has been identified as illustrated in Figure 2.10 which may indicate a potential control problem which should be overcome or avoided in closed-loop control designs. The current equation can be used to predict input/output current when the converter voltages V_1 and V_2 are fixed and known, but can also be used to predict output voltage if a resistor R is connected at the output port by solving an output equation, $V_1/R=I_{Lf\text{-}avg}(V_1, V_2, D)$ for buck mode or $V_2^2/RV_1= I_{Lf\text{-}avg}(V_1, V_2, D)$ for boost mode, given that one of the voltages V_1 or V_2 is known.

5.3.2 ESS simulation and emulation

While a great number of ESS strategies focus on the system efficiency, fewer researchers have investigated the SoC management of the ESS, or limiting the rate-of-change of power drawn from the primary source in an electrical system. An ESS controller is proposed in this thesis, which manages SoC and rate-of-change of source power by using a power balance control loop and a SoC control loop, which generate a super-capacitor current reference. To provide flexibility to use the super-capacitor more aggressively under certain states-of-charge, a super-capacitor recharge current of the form $I_{sc\text{-}re}=k_1(V_{sc\text{-}max}-V_{sc})^{k2}$ is introduced in the SoC control loop, and the impact of parameters k_1 and k_2 on the overall system operation has been explored and understood.

A hardware-in-the-loop technique was used to study the system level performance of the energy storage system which successfully demonstrates the ESS behaviour, smoothing load transients and eliminating voltage transients.

5.3.3 Advanced ESS control

The work in Chapter 4 investigates a steady-state profile of energy, E, against load, P_L, in a general form $E=f_{ss}(P_L)$, which is widely applicable to any storage system. The effects of different definitions of $E=f_{ss}(P_L)$ have been analysed in terms of the local load smoothing performance. Three special cases L, H and C are proposed, in which the SoC is kept at a minimum, a maximum or an intermediate level, which results in more aggressive operation of the storage system at different load levels. Nevertheless, the function $E=f_{ss}(P_L)$ can take other forms, and the analysis gives an insight into choosing a suitable $E=f_{ss}(P_L)$ function depending on the load conditions. For example, if both the low load and the high load appear more frequently, then it is reasonable to prioritise using energy in these two regions, while the mid load region will then be weakened, with the $E=f_{ss}(P_L)$ function looking like a 'S' curve.

A control on the rate-of-change of the source power is proposed in this thesis, given by $k_c=\Delta P_L/2\Delta E^2$, which is the smallest achievable rate-of-change in source power subject to a load change ΔP_L, and useable energy ΔE. The dP_S/dt value gives a guide in choosing the

energy storage system capacity based on the need to satisfy a limit on the rate-of-change of power drawn from the primary source to avoid its sub-optimal operation or malfunction.

5.4 Suggestions for future work

The energy storage system together with the wider electrical network comprise a large system which poses many research topics. In addition to further work on the ESS itself, research on the interaction between the ESS and the electrical system requires further investigation, some potential areas of which are suggested in this section.

5.4.1 More advanced converter control

The feedforward super-capacitor current controller used in Chapter 4 exhibits some limitation in control accuracy, which may be overcome by using a feedback current controller. To implement the feedback control, a small-signal analysis of the system is needed to determine the controller's parameters, but this is likely to be difficult due to the complexity and non-linearity of the system, especially in the discontinuous conduction mode since up to seven operating modes may appear. In addition, the converter controller used in this work was based around a simple analogue integrated circuit which is inflexible and has numerous non-ideal features such as delays and offsets. Furthermore the converter itself has highly non-linear characteristics at low load. It is thought that a combination of both feedforward and feedback control may be helpful to achieve better accuracy without losing the dynamic performance brought by the feedforward controller used in Chapter 4 and a digital implementation of the controller may give more flexibility.

5.4.2 DC-DC converter for ESS

A non-isolated DC-DC converter described in Chapter 2 was used in the thesis, which is limited in its conversion ratio. To increase the step up/down ratio and allow greater flexibility over the choice of super-capacitor voltage, an isolated converter may be adopted, which would also provide the benefit of galvanic isolation. One possible isolated converter topology is the dual-active-bridge, which however does not work efficiently over a wide range due to the limited ZVS characteristics and the huge reactive power flowing in the isolation transformer. To achieve better performance, potential work may include using

advanced modulation techniques, modifying the circuit topology, and using modular dual-active-bridge converters.

5.4.3 More advanced energy management strategies

An alternative to the control method proposed in Chapter 4 would be to set maximising the system efficiency globally as an objective. However this would require accurate loss and efficiency models for the system components such as the generator, prime mover and key loads. This would pose major challenges, requiring deep investigation and multi-disciplinary knowledge, as well as the capability to determine accurately the global optimum in real-time.

5.4.4 Fault ride through capability of the ESS

DC bus voltage transients caused by electrical faults in the network may result in undesirable operation of the storage system, for example potentially increasing the fault current level or creating an instability in which the bus voltage may collapse completely. Additional control functions must be devised and validated for storage systems to ensure safe and orderly operation of the network under the range of faults that may occur.

5.5 Conclusions

Energy storage systems are being used more actively due to the great benefits they provide, confronting the challenges of dynamic loads, and leading to a more robust electrical system. As one of the key components in the ESS, the converter plays an important role in transferring energy between the storage device and the electrical system. The detailed analysis of one particular but widely deployed DC-DC converter is given in this thesis, with all the operating modes identified including the DCM modes which are complex and usually occur at low power. The analysis is therefore crucial to the design of the converter and its control for realizing wide power range operation and ensuring the ESS is working properly. Beyond the ESS application, the converter analysis is applicable to uni-directional power conversion applications, fuel-cell converter in hybrid electrical vehicles for example, where DCM operation is commonly seen due to the zero circulating energy at zero output power that leads to higher efficiency at low power.

At a higher level, the analysis of ESS energy management given in this thesis concerns a system with a weak power source, where the rate-of-change in source power needs to be carefully regulated to shield it from load transients with the aid of an ESS. In a pratical electrical system, the weak power source can be a generator, or a generator driven by a weak prime mover, like a gas turbine, where care should be taken to prevent thermal stress in the generator, increased vibration and wear in the mechanical drivetrain, less efficient operation of the gas turbine to ensure it stays within its surge margin. A generic analysis of the rate-of-change control and ESS energy management is given, and validated using one particular super-capacitor based ESS for an aircraft electrical system, which may possibly extend to other systems, including those on road vehicles, trams, or ships where their generators, drivetrains and prime movers may have similar issues.

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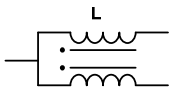
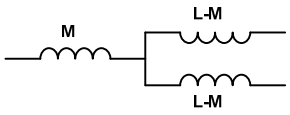
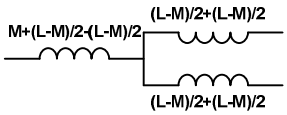
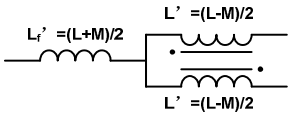
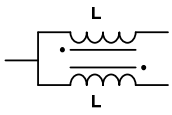
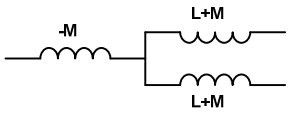
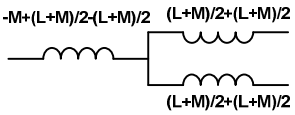
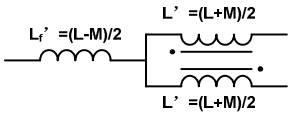
Appendices

A Dual-interleaved converter with IPT

A.1 Transform of coupled inductors into an IPT

The transform of two directly coupled or inversely coupled inductors into the configuration of a tightly coupled IPT plus an extra filter inductor is illustrated in Table A.1, with an assumption that the self-inductance of the two inductor windings are equal, i.e., $L_1=L_2=L$.

Table A.1. Transform of coupled inductors

Original circuits	Decoupled circuits	Circuits manipulation	Equivalent circuits
			
			

The decoupled circuits of the directly coupled (top) and inversely coupled (bottom) inductors are shown in the second column [162]. In the inversely coupled configuration, the differential inductance across the right two terminals can therefore be deduced as $L_{diff}=2(L+M)$. If tight coupling is achieved such that L=M, then the differential inductance is four times the self-inductance, $L_{diff}=2(L+M)=4L=4L_1=4L_2$.

By manipulating the decoupled circuits as shown in the third column and reversing the decoupling process of inversely coupled inductors, a tightly coupled IPT ($L'=L_1'=L_2'=M'$) with a filter inductor L_f' can be obtained as illustrated in the fourth column. An equivalent circuit can also be obtained for uncoupled inductors, where M=0 and therefore $L_f'=L'=L/2$; in addition, since the differential inductance L_{diff}' is 4L', the inductance ratio is $L_r'=L_{diff}'/L_f'=4L'/L'=4$. For any coupled inductors where M>0, this results in the inductance ratio being above four (inversely coupled) or below four (directly coupled) as can be easily calculated from the circuits from the fourth column in Table A.1.

A.2 Calculation of terminal voltage for the IPT

The non-conducting terminal voltage can be determined by considering two facts. Firstly, the terminal voltages v_{t1} and v_{t2}, and the IPT central tap voltage v_{com} always satisfy the following equation:

$$v_{com} = \frac{v_{t1} + v_{t2}}{2} \tag{A.1}$$

Secondly, the non-conducting IPT phase can be regarded as in open circuit. Therefore, the inductance seen by the external circuit in the conducting phase is only the self-inductance of that phase.

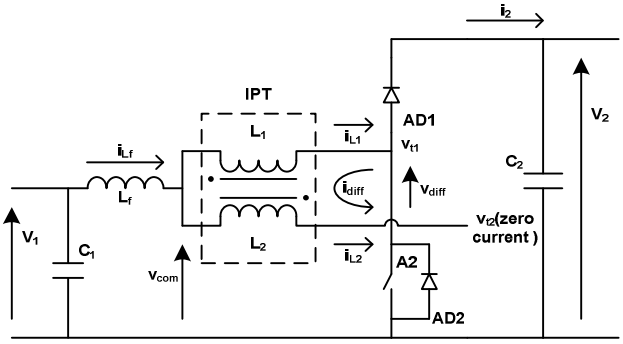


Figure A.1. Circuit diagram when v_{t2} is floating.

Considering the case when the phase current i_{L2} is zero for example, Figure A.1. The non-conducting IPT phase (L_2) can be regarded as open circuit. Therefore, the inductance seen by the external circuit in the conducting phase is the self-inductance of that winding (L_1). By using an inductive voltage divider circuit containing the input inductance L_f and the self-inductance L_1 between the input voltage V_1 and v_{t1}, the central tap voltage v_{com} can be obtained using Equation (A.2).

$$v_{com} = V_1 \cdot \frac{L_1}{L_1 + L_f} + v_{t1} \cdot \frac{L_f}{L_1 + L_f} \tag{A.2}$$

Since v_{t1} can be either zero (in sub-circuit 5) or the output voltage V_2 (in sub-circuit 7), this gives:

$$v_{com} = V_1 \cdot \frac{L_1}{L_1 + L_f} \qquad for\ sub-circuit\ 5 \tag{A.3}$$

$$v_{com} = V_1 \cdot \frac{L_1}{L_1 + L_f} + V_2 \cdot \frac{L_f}{L_1 + L_f} \qquad for\ sub-circuit\ 7 \tag{A.4}$$

Assuming the transformer is tightly coupled so that there is no leakage inductance, the differential inductance, L_{diff} is then four times L_1, $L_{diff}=4L_1$ [50]. Replacing L_1 with $L_{diff}/4$ in Equations (A.3) and (A.4):

$$v_{com} = V_1 \cdot \frac{L_{diff}/4}{L_{diff}/4 + L_f} = \frac{L_r}{L_r + 4} V_1 \qquad for\ sub-circuit\ 5 \tag{A.5}$$

$$V_{com} = V_1 \cdot \frac{L_1}{L_1 + L_f} + V_2 \cdot \frac{L_f}{L_1 + L_f} = \frac{L_r \cdot V_1 + 4V_2}{L_r + 4} \qquad for\ sub-circuit\ 7 \tag{A.6}$$

where the inductance ratio L_r is defined as $L_r=L_{diff}/L_f$.

By combining Equations (A.1) and (A.5) the floating phase terminal voltage v_{t2} may be obtained for sub-circuit 5:

$$v_{t2} = 2v_{com} - v_{t1} = 2\frac{L_r}{L_r + 4} V_1 - 0 = \frac{2L_r}{L_r + 4} V_1 \tag{A.7}$$

and using Equation (A.1) and (A.6) for sub-circuit 7:

$$v_{t2} = 2v_{com} - v_{t1} = 2\frac{L_r V_1 + 4V_2}{L_r + 4} - V_2 = \frac{2L_r V_1 + 4V_2 - L_r V_2}{L_r + 4} \tag{A.8}$$

The non-conducting phase voltage v_{t1} for sub-circuits 6 and 8 can also be obtained using the same method, since they have similar topologies. As a matter of fact, Equation (A.7) applies to v_{t1} for sub-circuit 6, and Equation (A.8) applies to sub-circuit 8.

The results of this analysis are summarised in Table 2.1 in Section 2.2.2 of Chapter 2.

A.3 di_{L1}/dt and di_{L2}/dt calculation

The di/dt of currents for each boost mode sub-circuit together with the values of v_{Lf} and v_{diff} are listed in Table A.2 using the following equations, where Equation (A.13) and (A.14) can be obtained by taking derivatives on both sides of Equation (2.1).

$$v_{Lf} = V_1 - v_{com} \tag{A.9}$$

$$v_{diff} = v_{t1} - v_{t2} \tag{A.10}$$

$$\frac{di_{Lf}}{dt} = \frac{v_{Lf}}{L_f} \tag{A.11}$$

$$\frac{di_{diff}}{dt} = \frac{v_{diff}}{L_{diff}} = \frac{v_{diff}}{L_r \cdot L_f} \tag{A.12}$$

$$\frac{di_{L1}}{dt} = \frac{1}{2} \cdot \frac{di_{Lf}}{dt} - \frac{di_{diff}}{dt} \tag{A.13}$$

$$\frac{di_{L2}}{dt} = \frac{1}{2} \cdot \frac{di_{Lf}}{dt} + \frac{di_{diff}}{dt} \tag{A.14}$$

Equations (A.11), (A.13), (A.14) and (A.14) are redefined with a negative sign for buck mode due to the current direction change, and the derived results are shown in Table A.3.

Table A.2 Voltages and di/dt of circuit elements in boost mode

Sub-circuits	1	2	3	4	5	6	7	8
v_{Lf}	V_1	$V_1 - V_2$	$V_1 - \frac{V_2}{2}$	$V_1 - \frac{V_2}{2}$	$\frac{4V_1}{L_r + 4}$	$\frac{4V_1}{L_r + 4}$	$\frac{4(V_1 - V_2)}{L_r + 4}$	$\frac{4(V_1 - V_2)}{L_r + 4}$
v_{diff}	0	0	$-V_2$	V_2	$-\frac{2L_rV_1}{L_r + 4}$	$\frac{2L_rV_1}{L_r + 4}$	$-\frac{2L_r(V_1 - V_2)}{L_r + 4}$	$\frac{2L_r(V_1 - V_2)}{L_r + 4}$
$\frac{di_{Lf}}{dt}$	$\frac{V_1}{L_f}$	$\frac{V_1 - V_2}{L_f}$	$\frac{V_1 - V_2/2}{L_f}$	$\frac{V_1 - V_2/2}{L_f}$	$\frac{4V_1}{(L_r + 4)L_f}$	$\frac{4V_1}{(L_r + 4)L_f}$	$\frac{4(V_1 - V_2)}{(L_r + 4)L_f}$	$\frac{4(V_1 - V_2)}{(L_r + 4)L_f}$
$\frac{di_{diff}}{dt}$	0	0	$-\frac{V_2}{L_rL_f}$	$\frac{V_2}{L_rL_f}$	$-\frac{2V_1}{(L_r + 4)L_f}$	$\frac{2V_1}{(L_r + 4)L_f}$	$-\frac{2(V_1 - V_2)}{(L_r + 4)L_f}$	$\frac{2(V_1 - V_2)}{(L_r + 4)L_f}$
$\frac{di_{L1}}{dt}$	$\frac{V_1}{2L_f}$	$\frac{V_1 - V_2}{2L_f}$	$\frac{2L_rV_1 - L_rV_2 + 4V_2}{4L_rL_f}$	$\frac{2L_rV_1 - L_rV_2 - 4V_2}{4L_rL_f}$	$\frac{4V_1}{(L_r + 4)L_f}$	0	$\frac{4(V_1 - V_2)}{(L_r + 4)L_f}$	0
$\frac{di_{L2}}{dt}$	$\frac{V_1}{2L_f}$	$\frac{V_1 - V_2}{2L_f}$	$\frac{2L_rV_1 - L_rV_2 - 4V_2}{4L_rL_f}$	$\frac{2L_rV_1 - L_rV_2 + 4V_2}{4L_rL_f}$	0	$\frac{4V_1}{(L_r + 4)L_f}$	0	$\frac{4(V_1 - V_2)}{(L_r + 4)L_f}$

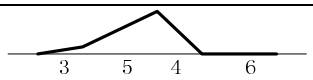
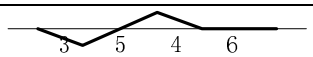
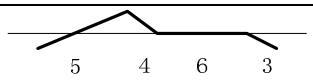
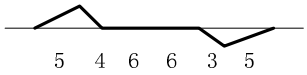
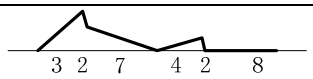
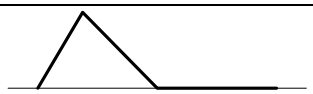
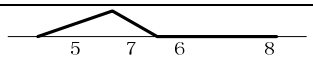
Table A.3. Voltages and di/dt of circuit elements in buck mode

Sub-circuits	1	2	3	4	5	6	7	8
v_{Lf}	$V_1 - V_2$	V_1	$V_1 - \frac{V_2}{2}$	$V_1 - \frac{V_2}{2}$	$\frac{4(V_1 - V_2)}{L_r + 4}$	$\frac{4(V_1 - V_2)}{L_r + 4}$	$\frac{4V_1}{L_r + 4}$	$\frac{4V_1}{L_r + 4}$
v_{diff}	0	0	V_2	$-V_2$	$-\frac{2L_r(V_1 - V_2)}{L_r + 4}$	$\frac{2L_r(V_1 - V_2)}{L_r + 4}$	$-\frac{2L_rV_1}{L_r + 4}$	$\frac{2L_rV_1}{L_r + 4}$
$\frac{di_{Lf}}{dt}$	$-\frac{V_1 - V_2}{L_f}$	$-\frac{V_1}{L_f}$	$-\frac{V_1 - V_2/2}{L_f}$	$-\frac{V_1 - V_2/2}{L_f}$	$-\frac{4(V_1 - V_2)}{(L_r + 4)L_f}$	$-\frac{4(V_1 - V_2)}{(L_r + 4)L_f}$	$-\frac{4V_1}{(L_r + 4)L_f}$	$-\frac{4V_1}{(L_r + 4)L_f}$
$\frac{di_{diff}}{dt}$	0	0	$\frac{V_2}{L_rL_f}$	$-\frac{V_2}{L_rL_f}$	$-\frac{2(V_1 - V_2)}{(L_r + 4)L_f}$	$\frac{2(V_1 - V_2)}{(L_r + 4)L_f}$	$-\frac{2V_1}{(L_r + 4)L_f}$	$\frac{2V_1}{(L_r + 4)L_f}$
$\frac{di_{L1}}{dt}$	$-\frac{V_1 - V_2}{2L_f}$	$-\frac{V_1}{2L_f}$	$-\frac{2L_rV_1 - L_rV_2 - 4V_2}{4L_rL_f}$	$-\frac{2L_rV_1 - L_rV_2 + 4V_2}{4L_rL_f}$	$-\frac{4(V_1 - V_2)}{(L_r + 4)L_f}$	0	$-\frac{4V_1}{(L_r + 4)L_f}$	0
$\frac{di_{L2}}{dt}$	$-\frac{V_1 - V_2}{2L_f}$	$-\frac{V_1}{2L_f}$	$-\frac{2L_rV_1 - L_rV_2 + 4V_2}{4L_rL_f}$	$-\frac{2L_rV_1 - L_rV_2 - 4V_2}{4L_rL_f}$	0	$-\frac{4(V_1 - V_2)}{(L_r + 4)L_f}$	0	$-\frac{4V_1}{(L_r + 4)L_f}$

A.4 Boundary conditions of the DCM modes

A full list of boundary phase current waveforms is shown in Table A.4. The waveforms and sub-circuit numbers labelled below the waveforms are applicable to both boost mode and buck mode, although different sub-circuits are present.

Table A.4. Phase current waveforms at boundary

Boundary	Region transition	Waveform at boundary
B1	$IV_b \Leftrightarrow VII_a$	
	$VI_a \Leftrightarrow VII_b$	
B2	$VI_a \Leftrightarrow VI_b$	
B3	$V \Leftrightarrow VI_b$	
B4	$IV_a \Leftrightarrow II_b$	
B5	$I \Leftrightarrow II_a$	
	$III_a \Leftrightarrow IV_a$	
	$III_b \Leftrightarrow IV_b$	

The duty ratios for each boundary are unique and can be determined by Equation (2.4), recalled here:

$$\sum_{k=1}^{n} \frac{di_{L1[k]}}{dt} \cdot \Delta t_{[k]} = 0 \tag{A.15}$$

where di_{L1}/dt is listed in Table A.2 and Table A.3 for each possible circuit configuration in terms of V_1, V_2, L_r and L_f. $\Delta t_{[k]}$ can be expressed as function of DT and therefore, D can be solved using Equation (A.15) for given V_1 and V_2 and circuit parameters of L_r, L_f and T.

However, additional equations are required to find out the expressions for Δt_k, which can be derived from the following equations:

$$\sum_{k=1}^{n} \Delta t_{[k]} = T \tag{A.16}$$

$$\sum_{k=1}^{p} \Delta t_{[k]} = D \cdot T \tag{A.17}$$

$$\Delta t_{[k]} = \Delta t_{[n/2+k]} \qquad for\ k \in [1, n/2] \tag{A.18}$$

which state the facts that:

1. the sum of the all sub-periods is a whole switching cycle, Equation (A.16) ;
2. the sum of the first p sub-periods is DT, Equation (A.17);
3. the k_{th} sub-circuit has the same duration of the $(n/2+k)_{th}$ sub-circuit due to waveform half-cycle symmetry, Equation (A.18).

Since there are altogether 1+1+n/2 equations and n unknown variables (Δt_k, k=1 to n), the equation set can be solved when 1+1+n/2≥n, i.e., n≤4, which applies to most boundary conditions in Table A.4. However, for the cases when n=6, an additional equation can be acquired since the current at the half cycle is zero according to Table A.4, and thus the equations can be solved.

With the obtained sub-period duration as a function of D, Equation (A.15) can be solved and the result for the boundary duty ratios is summarised for the boost mode and the buck mode in Table 2.3 and Table 2.4 respectively.

The following shows an example of the calculation for boundary duty ratio B2. The sub-circuit sequence is 5463 (n=4) according to Table A.4.

Equation (A.16) to (A.18) then become:

$$\begin{cases} \Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_4 = T \\ \Delta t_1 = DT \\ \Delta t_1 = \Delta t_3, \quad \Delta t_2 = \Delta t_4 \end{cases} \tag{A.19}$$

Therefore Δt_1 to Δt_4 can be obtained:

$$\begin{cases} \Delta t_1 = DT \\ \Delta t_2 = (1-2D)T/2 \\ \Delta t_3 = DT \\ \Delta t_4 = (1-2D)T/2 \end{cases} \tag{A.20}$$

Substituting Equation (A.20) into Equation (A.15) gives:

$$\begin{aligned} \sum_{k=1}^{4} \frac{di_{L1[k]}}{dt} \cdot \Delta t_{[k]} &= \frac{di_{L1[1]}}{dt} DT + \frac{di_{L1[2]}}{dt}(1-2D)T/2 + \frac{di_{L1[3]}}{dt} DT + \frac{di_{L1[4]}}{dt}(1-2D)T/2 \\ &= (\frac{di_{L1[1]}}{dt} - \frac{di_{L1[2]}}{dt} + \frac{di_{L1[3]}}{dt} - \frac{di_{L1[4]}}{dt})DT + (\frac{di_{L1[2]}}{dt} + \frac{di_{L1[4]}}{dt})T/2 \\ &= [\frac{4V_1}{(L_r+4)L_f} - \frac{2L_rV_1 - L_rV_2 - 4V_2}{4L_rL_f} + 0 - \frac{2L_rV_1 - L_rV_2 + 4V_2}{4L_rL_f}]DT \\ &\quad + (\frac{2L_rV_1 - L_rV_2 - 4V_2}{4L_rL_f} + \frac{2L_rV_1 - L_rV_2 + 4V_2}{4L_rL_f})T/2 \\ &= [\frac{4V_1}{(L_r+4)L_f} - 2\frac{2L_rV_1 - L_rV_2}{4L_rL_f}]DT + 2\frac{2L_rV_1 - L_rV_2}{4L_rL_f}T/2 = 0 \end{aligned} \tag{A.21}$$

where $di_{L1}[1]/dt$ to $di_{L1}[4]/dt$ are the rate-of-change in current i_{L1} in sub-circuit 5, 4, 6, 3 respectively, whose expressions are provided in Table A.2 (boost mode).

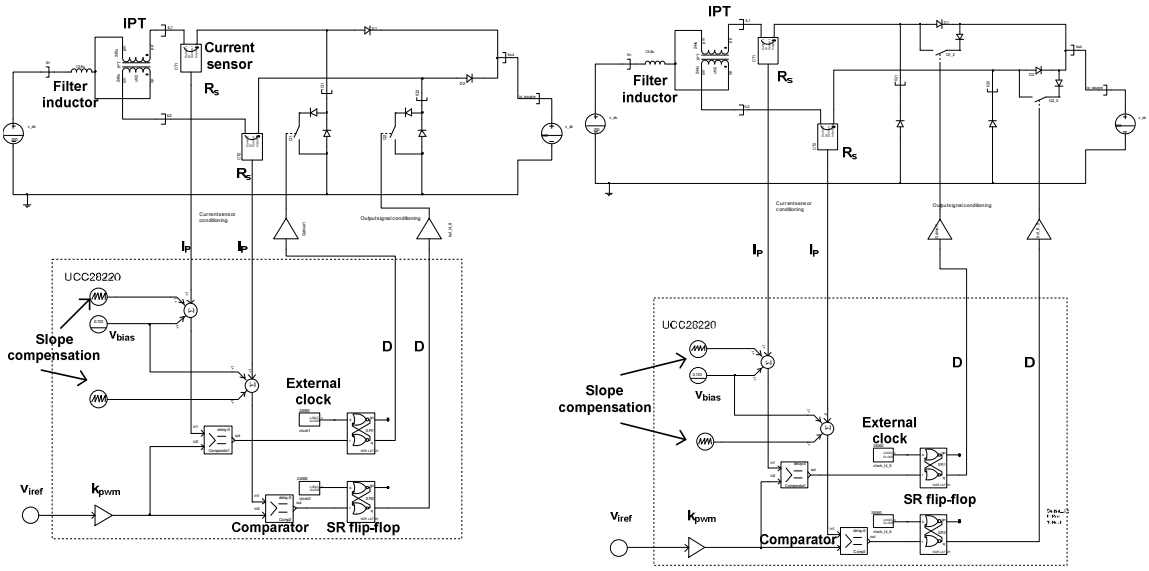
Solving Equation (A.21) then gives:

$$D = \frac{(2V_1 - V_2)(L_r+4)}{2(2V_1L_r - L_rV_2 - 4V_2)} = \frac{(2V_1/V_2 - 1)(L_r+4)}{2(2L_rV_1/V_2 - L_r - 4)} = \frac{(2M-1)(L_r+4)}{2(2L_rM - L_r - 4)} \tag{A.22}$$

which is the boundary duty ratio for boundary B2.

A.5 Saber circuit diagram of the dual-interleaved converter

The circuit diagram of the dual-interleaved converter circuit with a peak current controller is shown in Figure A.2a and b for boost mode and buck mode respectively. The same components as described in literature review, Section 1.2.2.3 for a peak current controller are used, including: slope compensation, external clocks, comparators and SR flip-flops.



(a) Boost mode **(b) Buck mode**

Figure A.2. DC-DC converter circuit diagram with peak current controller in Saber

In experiments, the above functionality is achieved by using a two-channel PWM controller UCC28220, in which an additional gain k_{pwm}, and an internal bias v_{bias} are added as shown in Figure A.3.

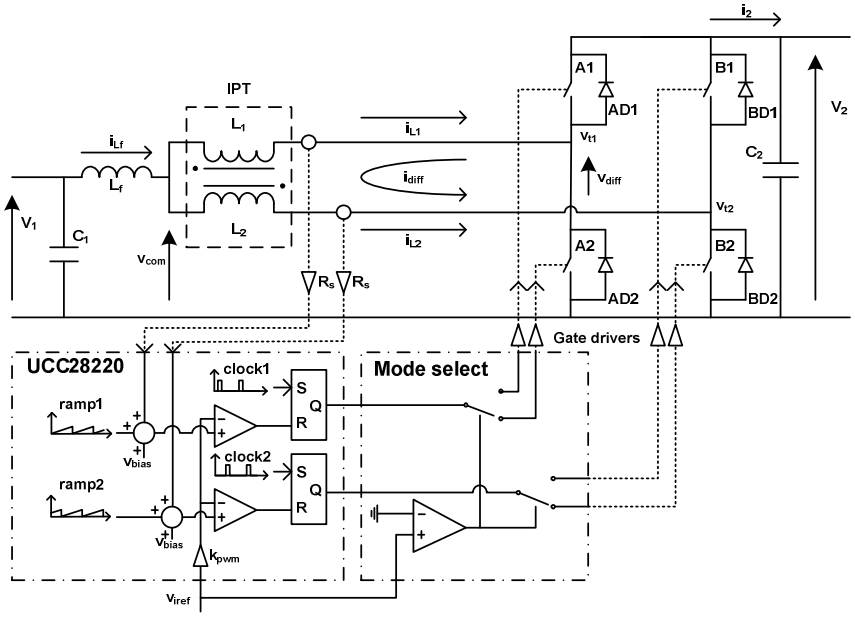


Figure A.3. Dual-interleaved converter with a peak current controller.

A.6 Peak current and average current equations

The di/dt expressions for the currents in each sub-circuit is given in Appendix A.3; the Δt_k for each sub-circuit can be expressed as a function of D, which can be obtained by using the method described in Appendix A.4. By substituting the expressions of di/dt and Δt_k into Equations (2.8), (2.9) and (2.10), the peak currents and average current can be obtained and are listed in Table A.5 and Table A.6 for boost mode and buck mode respectively. An algebra software package Maple is used to assist the equation derivation.

In more detail, the piecewise function of $I_{Lf\text{-}avg}$ and peak phase current $I_{L1\text{-}peak}$ taking the form of Equation (2.11) for boost mode can be obtained according to Figure 2.6, as:

$$I_{Lf-avg}(V_1,V_2,D)=\begin{cases}\begin{cases} I_{Lf-avg}\big|_{regionV}, 0\le D<d_{B3} \\ I_{Lf-avg}\big|_{regionVI}, d_{B3}\le D<d_{B1} \\ I_{Lf-avg}\big|_{regionVII}, d_{B1}\le D\le(1-M)\end{cases} & for\ M\in[0,0.5-2/L_r) \\ \begin{cases} I_{Lf-avg}\big|_{regionIII}, 0\le D<d_{B5} \\ I_{Lf-avg}\big|_{regionIV}, d_{B5}\le D<d_{B1} \\ I_{Lf-avg}\big|_{regionVII}, d_{B1}\le D\le(1-M)\end{cases} & for\ M\in[0.5-2/L_r,0.5) \\ \begin{cases} I_{Lf-avg}\big|_{regionIII}, 0\le D<d_{B5} \\ I_{Lf-avg}\big|_{regionIV}, d_{B5}\le D<d_{B4} \\ I_{Lf-avg}\big|_{regionII}, d_{B4}\le D\le(1-M)\end{cases} & for\ M\in[0.5,0.5+2/L_r) \\ \begin{cases} I_{Lf-avg}\big|_{regionI}, 0\le D<d_{B5} \\ I_{Lf-avg}\big|_{regionII}, d_{B5}\le D\le(1-M)\end{cases} & for\ M\in[0.5+2/L_r,1]\end{cases} \tag{A.23}$$

$$I_{L1-peak}(V_1,V_2,D)=\begin{cases}\begin{cases} I_{L1-peak}\big|_{regionV}, 0\le D<d_{B3} \\ I_{L1-peak}\big|_{regionVI}, d_{B3}\le D<d_{B1} \\ I_{L1-peak}\big|_{regionVII}, d_{B1}\le D\le(1-M)\end{cases} & for\ M\in[0,0.5-2/L_r) \\ \begin{cases} I_{L1-peak}\big|_{regionIII}, 0\le D<d_{B5} \\ I_{L1-peak}\big|_{regionIV}, d_{B5}\le D<d_{B1} \\ I_{L1-peak}\big|_{regionVII}, d_{B1}\le D\le(1-M)\end{cases} & for\ M\in[0.5-2/L_r,0.5) \\ \begin{cases} I_{L1-peak}\big|_{regionIII}, 0\le D<d_{B5} \\ I_{L1-peak}\big|_{regionIV}, d_{B5}\le D<d_{B4} \\ I_{L1-peak}\big|_{regionII}, d_{B4}\le D\le(1-M)\end{cases} & for\ M\in[0.5,0.5+2/L_r) \\ \begin{cases} I_{L1-peak}\big|_{regionI}, 0\le D<d_{B5} \\ I_{L1-peak}\big|_{regionII}, d_{B5}\le D\le(1-M)\end{cases} & for\ M\in[0.5+2/L_r,1]\end{cases} \tag{A.24}$$

and for buck mode:

$$I_{Lf-avg}(V_1,V_2,D)=\begin{cases}\begin{cases}I_{Lf-avg}\big|_{regionI},0\le D<d_{B5}\\ I_{Lf-avg}\big|_{regionII},d_{B5}\le D\le M\end{cases} & for\ M\in[0,0.5-2/L_r)\\ \begin{cases}I_{Lf-avg}\big|_{regionIII},0\le D<d_{B5}\\ I_{Lf-avg}\big|_{regionIV},d_{B5}\le D<d_{B4}\\ I_{Lf-avg}\big|_{regionII},d_{B4}\le D\le M\end{cases} & for\ M\in[0.5-2/L_r,0.5)\\ \begin{cases}I_{Lf-avg}\big|_{regionIII},0\le D<d_{B5}\\ I_{Lf-avg}\big|_{regionIV},d_{B5}\le D<d_{B1}\\ I_{Lf-avg}\big|_{regionVII},d_{B1}\le D\le M\end{cases} & for\ M\in[0.5,0.5+2/L_r)\\ \begin{cases}I_{Lf-avg}\big|_{regionV},0\le D<d_{B3}\\ I_{Lf-avg}\big|_{regionVI},d_{B3}\le D<d_{B1}\\ I_{Lf-avg}\big|_{regionVII},d_{B1}\le D\le M\end{cases} & for\ M\in[0.5+2/L_r,1]\end{cases} \tag{A.25}$$

$$I_{L1-peak}(V_1,V_2,D)=\begin{cases}\begin{cases}I_{L1-peak}\big|_{regionI},0\le D<d_{B5}\\ I_{L1-peak}\big|_{regionII},d_{B5}\le D\le M\end{cases} & for\ M\in[0,0.5-2/L_r)\\ \begin{cases}I_{L1-peak}\big|_{regionIII},0\le D<d_{B5}\\ I_{L1-peak}\big|_{regionIV},d_{B5}\le D<d_{B4}\\ I_{L1-peak}\big|_{regionII},d_{B4}\le D\le M\end{cases} & for\ M\in[0.5-2/L_r,0.5)\\ \begin{cases}I_{L1-peak}\big|_{regionIII},0\le D<d_{B5}\\ I_{L1-peak}\big|_{regionIV},d_{B5}\le D<d_{B1}\\ I_{L1-peak}\big|_{regionVII},d_{B1}\le D\le M\end{cases} & for\ M\in[0.5,0.5+2/L_r)\\ \begin{cases}I_{L1-peak}\big|_{regionV},0\le D<d_{B3}\\ I_{L1-peak}\big|_{regionVI},d_{B3}\le D<d_{B1}\\ I_{L1-peak}\big|_{regionVII},d_{B1}\le D\le M\end{cases} & for\ M\in[0.5+2/L_r,1]\end{cases} \tag{A.26}$$

where d_{B1} to d_{B5} are the corresponding boundary duty ratios defined in Table 2.3.

Table A.5. Summary of average inductor current and peak current for DCM regions in boost mode

	$I_{Lf\text{-}avg}$	$I_{L1\text{-}peak}$
Region I	$\frac{1}{4}\frac{(2LrV_1 - LrV_2 + 4V_2)V_2TD^2}{LrL_f(V_2 - V_1)}$	$\frac{1}{4}\frac{(2LrV_1 - LrV_2 + 4V_2)DT}{LrL_f}$
Region II	$\frac{1}{4}\frac{(2LrV_1 - LrV_2 + 4V_2)V_2TD^2}{LrL_f(V_2 - V_1)}$	$\frac{1}{4}\frac{(2LrV_1 - LrV_2 + 4V_2)DT}{LrL_f}$
Region III	$\frac{4V_1D^2TV_2}{L_f(4 + Lr)(V_2 - V_1)}$	$\frac{4V_1DT}{L_f(4 + Lr)}$
Region IV	$\frac{2\left(4Lr^2D^2V_1 - 2Lr^2D^2V_2 - 2Lr^2DV_1 + Lr^2DV_2 + 8LrD^2V_2 + 8LrDV_1 - 8LrDV_2 - 2LrV_1 + 2LrV_2 + 16dV_2 + 8V_1 - 8V_2\right)V_2T}{LrL_f(-2LrV_1 + LrV_2 + 4V_2)(4 + Lr)}$	$\frac{(4LrDV_1 - 2LrDV_2 - LrV_1 + LrV_2 + 8DV_2 + 4V_1 - 4V_2)T}{(4 + Lr)LrL_f}$
Region V	$\frac{64V_2LrV_1D^2T}{L_f(4 + Lr)^2(-2LrV_1 + LrV_2 + 4V_2)}$	$\frac{4V_1DT}{L_f(4 + Lr)}$
Region VI	$\frac{4V_2V_1T}{LrL_f(-2LrV_1 + LrV_2 + 4V_2)}$	$\frac{V_1T}{LrL_f}$
Region VII	$\frac{1}{4}\frac{TV_1V_2\left(4Lr^2D^2 - 4Lr^2D + Lr^2 + 16LrD - 8Lr + 16\right)}{LrL_f(-2LrV_1 + LrV_2 + 4V_2)}$	$\frac{1}{4}\frac{TV_1(2LrD - Lr + 4)}{LrL_f}$

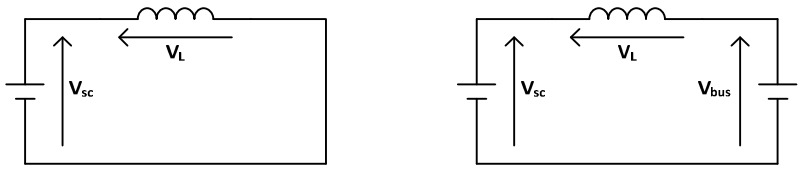
Table A.6. Summary of average inductor current and peak current for DCM regions in buck mode

	$I_{Lf\text{-}avg}$	$I_{L1\text{-}peak}$
Region I	$\frac{1}{4}\frac{D^2TV_2\left(-2LrV_1+LrV_2+4V_2\right)}{LrL_fV_1}$	$\frac{1}{4}\frac{\left(-2LrV_1+LrV_2+4V_2\right)dT}{LrL_f}$
Region II	$\frac{1}{4}\frac{D^2TV_2\left(-2LrV_1+LrV_2+4V_2\right)}{LrL_fV_1}$	$\frac{1}{4}\frac{\left(-2LrV_1+LrV_2+4V_2\right)DT}{LrL_f}$
Region III	$\frac{4\left(V_2-V_1\right)D^2TV_2}{L_f\left(4+Lr\right)V_1}$	$\frac{4TD\left(V_2-V_1\right)}{L_f\left(4+Lr\right)}$
Region IV	$\frac{2\left(4Lr^2D^2V_1-2Lr^2D^2V_2-2Lr^2DV_1+Lr^2DV_2-8LrD^2V_2+8LrDV_1-2LrV_1-16DV_2+8V_1\right)V_2T}{LrL_f\left(-2LrV_1+LrV_2-4V_2\right)\left(4+Lr\right)}$	$\frac{\left(-4LrDV_1+2LrDV_2+LrV_1+8DV_2-4V_1\right)T}{\left(4+Lr\right)LrL_f}$
Region V	$\frac{64V_2Lr\left(V_2-V_1\right)D^2T}{L_f\left(4+Lr\right)^2\left(2LrV_1-LrV_2+4V_2\right)}$	$\frac{4TD\left(V_2-V_1\right)}{L_f\left(4+Lr\right)}$
Region VI	$\frac{4TV_2\left(V_2-V_1\right)}{LrL_f\left(2LrV_1-LrV_2+4V_2\right)}$	$\frac{T\left(V_2-V_1\right)}{LrL_f}$
Region VII	$\frac{1}{4}\frac{TV_2\left(4Lr^2D^2V_1-4Lr^2D^2V_2-4Lr^2DV_1+4Lr^2DV_2+Lr^2V_1-Lr^2V_2+16LrDV_1-16LrDV_2-8LrV_1+8LrV_2+16V_1-16V_2\right)}{LrL_f\left(-2LrV_1+LrV_2-4V_2\right)}$	$\frac{1}{4}\frac{T\left(-2LrDV_1+2LrDV_2+LrV_1-LrV_2-4V_1+4V_2\right)}{LrL_f}$

B Energy storage system

B.1 Averaged DC-DC converter model for the ESS

For a single leg DC-DC converter shown in Figure 3.3, the voltage on the inductor V_L is V_{sc} when the bottom switch is on Figure B.1a, and is V_{sc}-V_{bus} when the upper switch is on Figure B.1b.



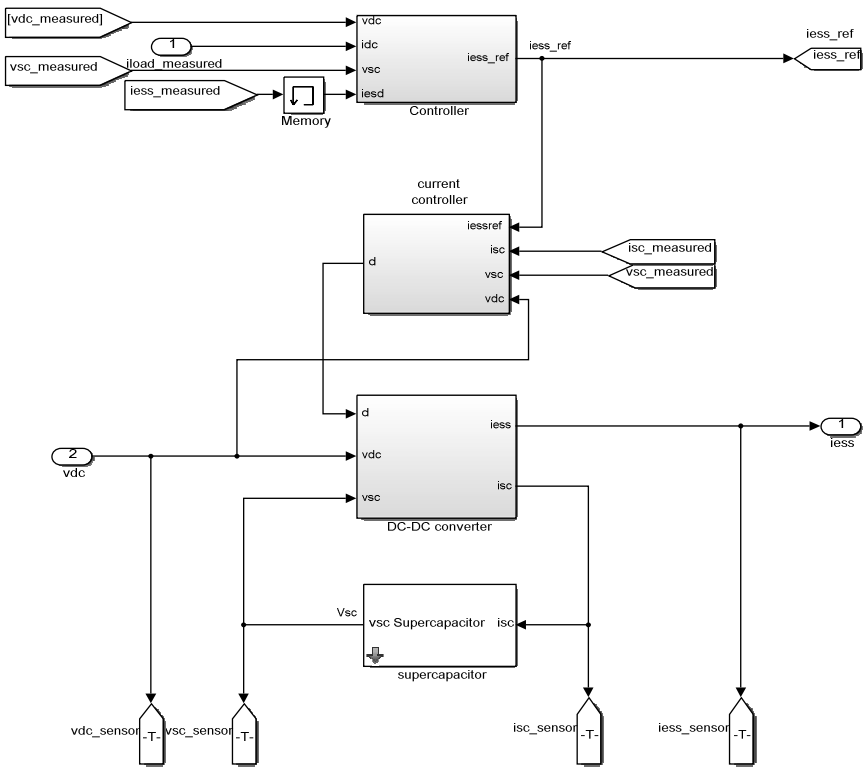
(a) When the bottom switch is on. **(b) When the upper switch is on.**

Figure B.1. DC-DC converter equivalent circuits.

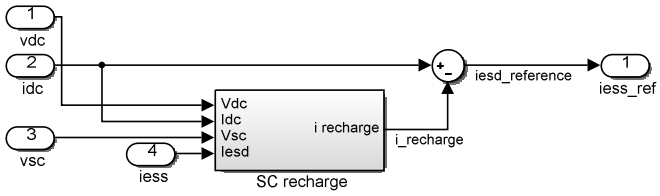
By denoting the duty ratio of the bottom switch as D, the average inductor voltage is thus obtained as:

$$V_L = V_{sc} \cdot D + (V_{sc} - V_{bus}) \cdot (1 - D) = V_{sc} - V_{bus}(1 - D) \tag{B.1}$$

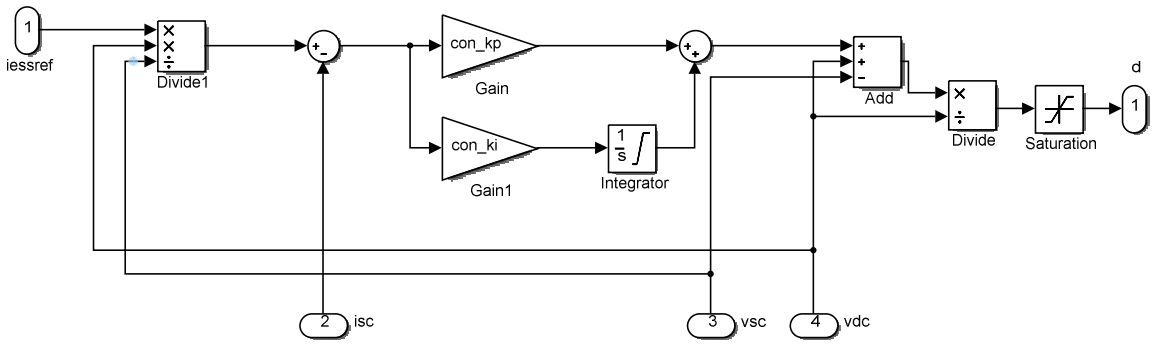
B.2 Simulink model of the energy storage system



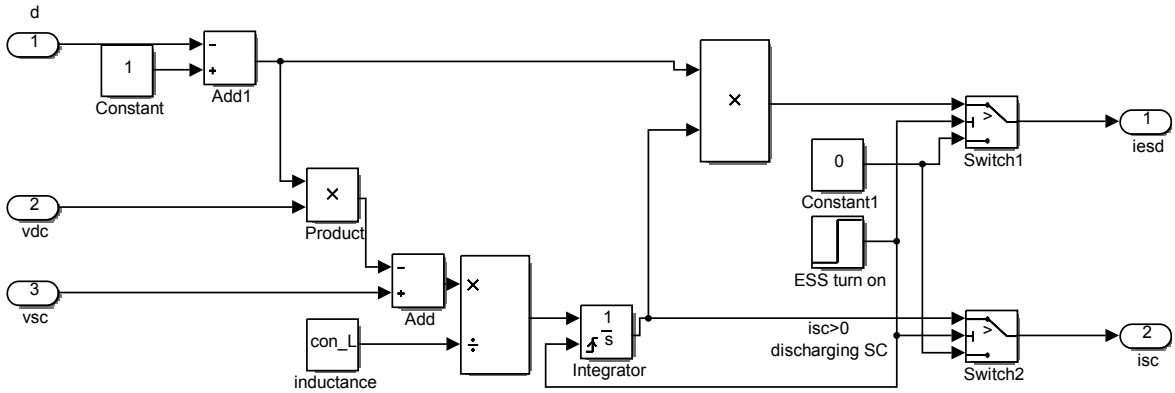
(a) Top-level model.



(b) State-of-charge control.



(c) Current control.

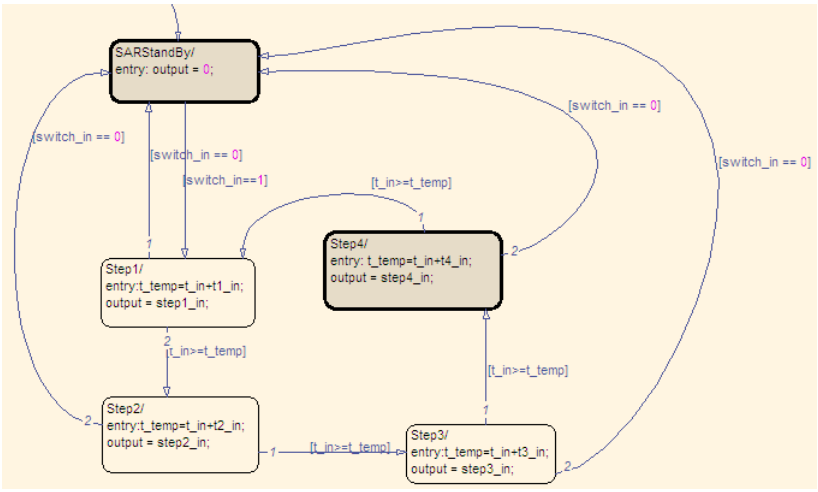


(d) Converter model.

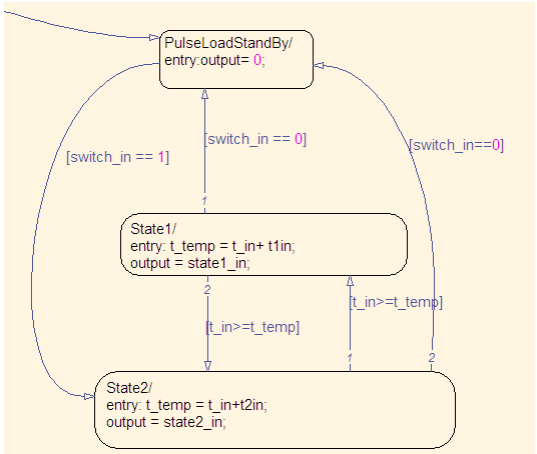
Figure B.2. Top level ESS Simulink model diagram.

B.3 Dynamic load emulation using the active load

Each box in the Stateflow diagram in Figure B.3 represents a state, which contains the information of power level and duration. The switching between different states and different power levels is triggered when the time elapsed meets the condition. The initial state starts from the 'Standby' box at the top of each diagram, and is triggered to jump to another designated state on receiving the signal 'switch_in' to be '1'. The system then returns from all other states by receiving the signal 'switch_in' to be '0', which achieves the function of turn-on and off load. For the state diagram for radar load, a total of four states are used, providing four power levels with adjustable periods; as to the pulsed load, only two states are used. The parameters can be changed in real-time via the Labview graphical user interface (GUI) described in Appendix B.4.



(a) Radar load.



(b) Generic pulse load.

Figure B.3. Stateflow diagram for dynamic load profiles.

B.4 Graphical user interface for the active load

A modified version of the original graphical user interface is shown in Figure B.4. The box on the bottom left is for defining the parameters for the emulated dynamic load, including the power level and duration. The bottom right box sets the operating modes of the ESS and shows the virtual super-capacitor voltage in real-time. Three different recharge profiles can be selected: the control method described in Chapter 3 with k_1=0.5, k_2=1, or k_1=0.64, k_2=1.5, and the proposed new method as described in Chapter 4.

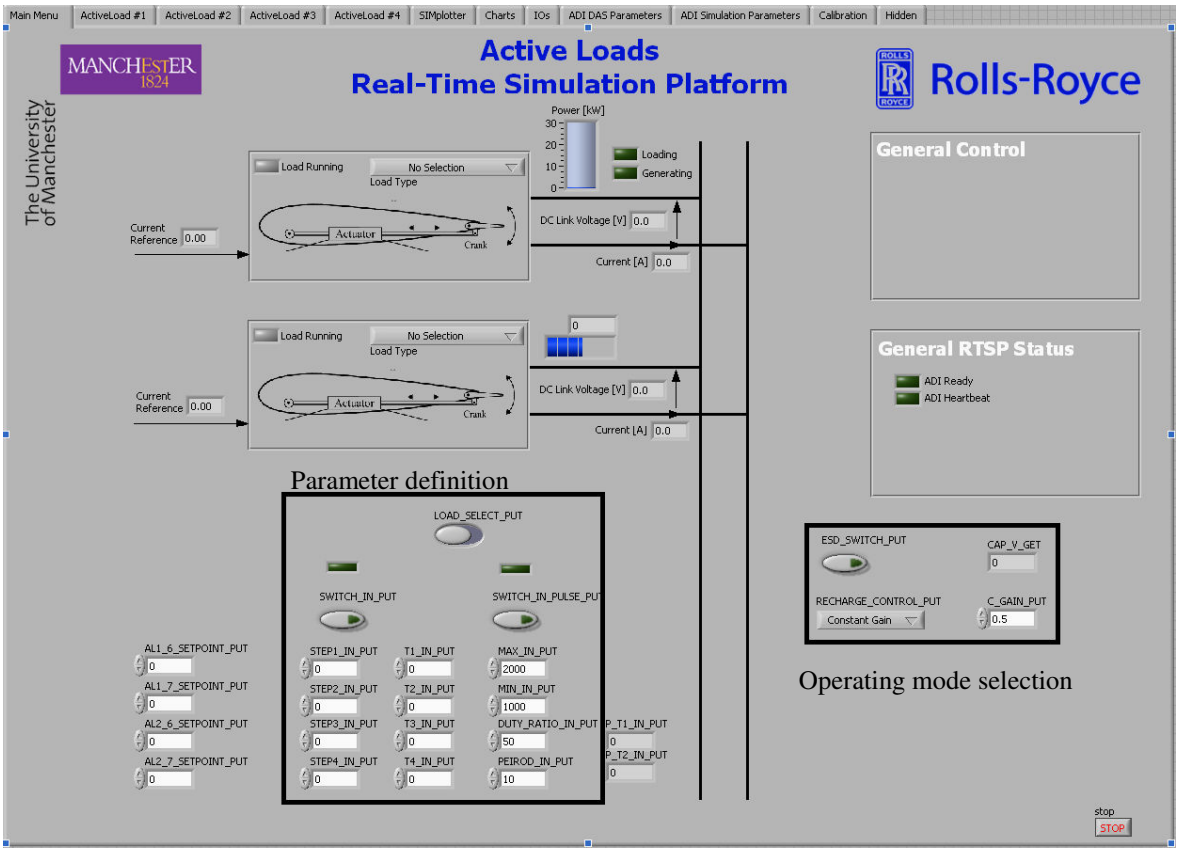


Figure B.4. GUI for setting load and ESS control modes.

B.5 Derivation of E versus P_S trajectory for a load step

The following shows the trajectory of the energy E remaining in the storage system versus source power P_S when the source is subjected to a load step of 1p.u. and the ESS responds with an instantaneous power step of 1p.u. and its output power then falls at a rate of $k_{c\text{-}pu}=k_{cmax\text{-}pu}$. The per unit parameterized system of an ESS as given in Section 4.3.1 is

recalled here to simplify the analysis. Considering a load step from zero to 1p.u., the power source output will rise/fall at a constant rate given by $k_{c\text{-}pu}=k_{c\text{-}max\text{-}pu}=0.5$p.u, Figure B.5.

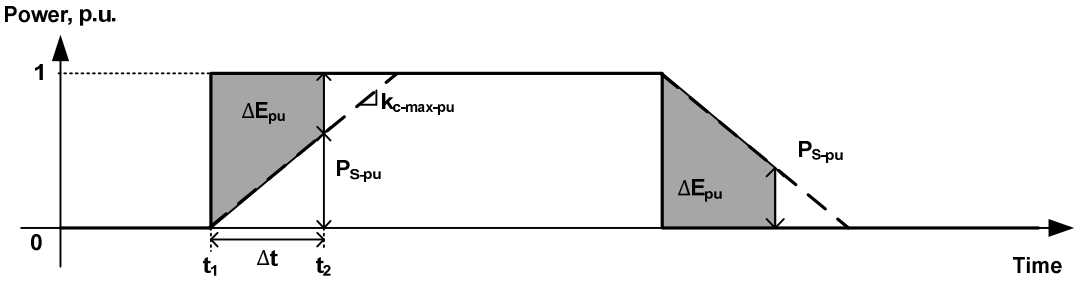


Figure B.5. ESS response to a load step step from zero to 1p.u.

The power source output at any time is therefore:

$$P_{S-pu} = k_{c-\max-pu} \cdot \Delta t \tag{B.2}$$

The energy consumption can be calculated as:

$$\Delta E_{pu} = \int_{t=t_1}^{t_2} (P_{L-pu} - P_{S-pu})dt = \frac{1}{2}(1+1-P_{s-pu})\Delta t \tag{B.3}$$

By eliminating Δt in Equation (B.3) using (B.2), the following is obtained:

$$\Delta E_{pu} = \frac{1}{2}(2-P_{s-pu}) \cdot \frac{P_{S-pu}}{k_{c-\max-pu}} = (2-P_{S-pu})P_{S-pu} \tag{B.4}$$

Starting from the 1p.u. initial energy in the ESS, then the remaining energy at any time is:

$$E_{pu} = 1-\Delta E_{pu} = 1-(2-P_{S-pu})P_{S-pu} = (1-P_{S-pu})^2 \tag{B.5}$$

Similarly, for a load decrease, the energy versus source power can be derived to be:

$$E_{pu} = 1-P_{S-pu}^2 \tag{B.6}$$

Equation (B.5) and (B.6) are parabolas and are in the same form as Equations (4.15) and (4.16) given in Section 4.3.1. Similar trajectories will occur for different size load steps.

B.6 Implementation of control reference v_{iref} calculation

A piece of C code is used to perform the linearized calculation of control reference v_{iref}. The flow chart of the control reference v_{iref} is shown in Figure B.6. Three signals are required to calculate v_{iref}, two of them, V_{sc} and V_{bus} are measured in real-time, while $I_{sc\text{-}ref}$ is determined by a higher level supervisory controller. A dead-band of 2A is added in the algorithm to avoid sudden changes in power flow direction. The code is transformed into an executable block in Simulink using built-in the 'S-function builder'. The code is then transferrable to other control platforms including DSPs, microcontrollers which use C language.

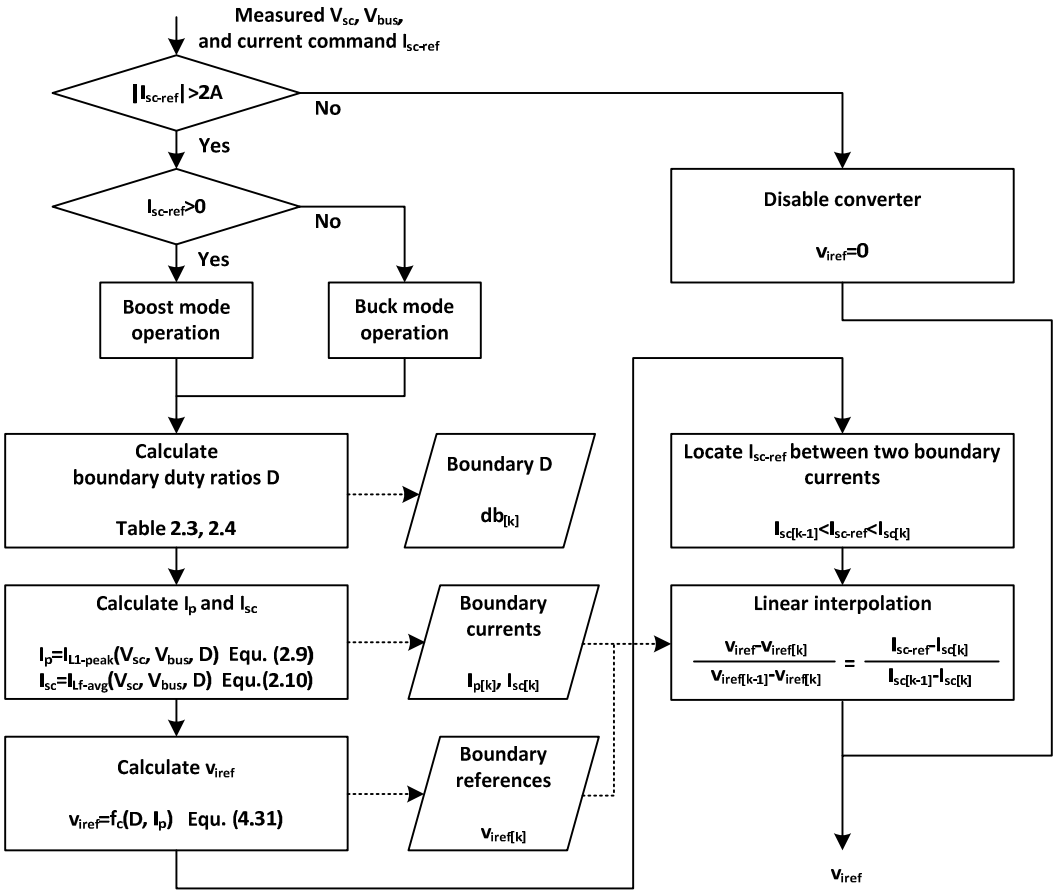


Figure B.6. Flow chart of the of control reference v_{iref} calculation.