Organic Logic Circuits: Fabrication Process and Device Optimisation

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Abbreviations and Symbols

μ	Mobility or micron
Å	Angstrom (1×10^{-10} m)
°	Degrees
π bond	Pi bond
σ bond	Sigma bond
Φ_w	Work function
a:Si:H	Hydrogenated amorphous silicon
ADS	Agilent Technologies - Advanced Design System
AFG	Arbitrary Function Generator
AFM	Atomic force microscopy
Al	Aluminium
Al_2O_3	Aluminium oxide
ALD	Atomic layer deposition
Au	Aurum / Gold
$BaTiO_3$	Barium titanate, Barium titanium oxide
BC	Bottom contact
BG	Bottom gate
BGBC	Bottom gate bottom contact
BGTC	Bottom gate top contact
BST	Barium strontium titanium oxide, barium strontium titanate
DCB	Dichlorobenzene
DLS	Dynamic light scattering
DPVAnt	Di(phenylvinyl)anthracene
EEE	School of electrical and electronic engineering
F8T2	Poly(9,9-dioctylfluorene-co-bithiophene)
FLC	Ferroelectric liquid crystal
GDSII	Graphic Database Stream II

HMBG	Hydroxymethyl benzoguanamine
HOMO	Highest occupied molecular orbital
Hz	Hertz
ICCAP	Agilent Technologies - Integrated Circuit Characterization and Analysis Program
IDE	Interdigitated electrodes
IGZO	Indium gallium zinc oxide
LUMO	Lowest unoccupied molecular orbital
MIM	Metal insulator metal
MOSFET	Metal oxide semiconductor field effect transistor
nm	Nanometers
ODT	Octadecanethiol
OFET(s)	Organic field effect transistor
OH	Hydroxyl
OTS	Octadecyltrichlorosilane
PAG	Photoacid generator
PANI	Polyaniline
PBTTT	Poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3, 2-b]thiophene
PDHTT	Poly(3,3 -dihexyl-2,2:5 ,2-terthiophene)
PDRA	Post doctoral research associate
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)
PEN	Polyethylene naphthalate
PES	Polyether-sulphone
PET	Polyethylene terephthalate
PET project	A project titled “Delivering Plastic Electronic Item Level Tracking for the Perishable Goods Supply Chain” funded by the Technology Strategy Board and Syngenta
pF	Picofarad
PFBT	Pentafluorobenzene thiol

PI	Polyimide
PMF	Poly(melamine-co-formaldehyde)
PMMA	Poly(methyl methacrylate)
Pt	Platinum
PTAA	Polytriarylamine
PTPA	Poly(tri-phenyl-amine)
PTV	Polythienylenevinylene
OSC	Organic semiconductor
PVA	Polyvinyl alcohol
PVP	Poly-4-vinylphenol
PαMS	Poly(α-methyl styrene)
RFID	Radio frequency identification
RMS	Root mean square
Rpm	Revolutions per minute
rr- P3AT	Regio-regular poly(3-alkylthiophene)
rr-P3HT	Regio-regular poly (3-hexylthiophene)
S	Sub-threshold slope
SAM	Self assembled monolayer
Si	Silicon
SiO_2	Silicon dioxide
SmA	Smectic A phase
SmC*	Chiral Smectic C phase
SoC	School of Chemistry
SoPA	School of Physics and Astronomy
TC	Top contact
TG	Top gate
TGBC	Top gate bottom contact
TGTC	Top gate top contact

Ti	Titanium
TIPS-pentacene	6,13-Bis(triisopropylsilylethynyl)-pentacene
TSB	Technology Strategy Board
UMEM	Unified Model and Parameter Extraction method
UoM	University of Manchester
UV	Ultraviolet
V_{FB}	Flatband voltage
VISA	Virtual Instrument Software Architecture
V_{OH}	Voltage output (high)
V_{OL}	Voltage output (low)
VRH	Variable range hopping
V_{th}	Threshold voltage

Abstract

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Initial research in the field of organic electronics focused primarily on the improvements in material performance. Significant progress has been achieved in the case of organic field effect transistors, where reported mobility values are now over 5 orders of magnitude higher than those of early devices. As a consequence, the use of organic transistors is now being considered for real-world applications in the form of integrated logic circuits. This in turn presents many new challenges, as the logic circuit requirements are more demanding on the transistor characteristics and corresponding fabrication processes.

This thesis investigates the feasibility of organic technology for its potential use in future low-cost, high-volume electronic applications. The research objectives were accomplished by practical evaluation of an organic logic circuit fabrication process. First, recent advances in the fabrication of organic circuits in terms of transistor structure, material usage and fabrication techniques are reviewed. Next, a lithographic logic circuit fabrication process using PVP gate dielectric and TIPS-pentacene organic semiconductor adapted from state of the art fabrication process is presented. The logic circuit design decisions and the methodology for the fabrication process are thoroughly documented. Using this process, zero-V_{gs} and diode-load inverter circuits were successfully fabricated. However, the process is in need of further refinement for more complex circuit designs, as the fabrication of a comparator circuit consisting of 11 transistors was unsuccessful.

Two optimisation techniques that are compatible with the logic circuit fabrication process were also explored in this work. To improve the capacitive coupling of the dielectric layer, the use of a polymer nanocomposite dielectric was investigated. The nanocomposite is prepared by blending PVP solution with a high-k inorganic nanoparticle filler, barium strontium titanate. Using the nanocomposite dielectric, both single transistors and integrated logic circuits were successfully fabricated. This is the first report on the use of PVP and barium strontium titanate nanocomposite dielectric with a lithographic based logic circuit fabrication process. The use of PFBT modified Au contacts for the fabrication process was investigated to improve the performance of the contact electrode layer. Using PFBT, mobility increased by one order of magnitude over untreated Au electrodes for the PVP and TIPS-pentacene transistors.

Declaration

No portion of the work referred to in the thesis has been submitted in support of any application for another degree or qualification of this or any other university or other institute of learning.

Copyright Statement

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1 Introduction

Organic electronics, also referred to as plastic electronics is a division of electronics which studies the application, fabrication and physics of devices constructed using organic compounds. The use of organic materials in the electronics industry is not new; typically they are used as supporting materials. Photoresist materials are an integral component in the fabrication process of semiconductor devices. Polymers are widely used as insulators, or as passivation and encapsulation layers. The discovery of conductive polymers has, however, changed the role of polymers in their use in electronic devices.

In 1977, Shirakawa, MacDiarmid and Heeger (Nobel prize in Chemistry, 2000) galvanised global research interest in conductive polymers when they reported over 7 orders of magnitude increase in conductivity of polyacetylene after doping with iodine [1]. This form of polymers or plastics gave a whole new perspective towards these materials, as they were previously known to be insulating. In the initial development phase, developed conductive polymers were used "passively". Example passive applications saw the use of polymers as substrates [2], antistatic coating [3], electromagnetic shielding [4] and corrosion coating [5]. Later development of conductive polymers saw exciting use of these materials as the active material in electronic devices. Present plastic electronic materials now exhibit various electrical characteristics such as light emission, current generation and semiconducting properties.

The interest in the use of polymers or organic materials over their inorganic counterparts can be attributed to their advantages in cost and processing. Physically, some organic materials are transparent and are capable of withstanding mechanical stresses, giving compatibility with flexible polymeric substrates such as polyethylene terephthalate (PET) and polyethylene naphthalate **(**PEN). Polymers in solution form can be deposited under low temperatures over a wide substrate area using large volume manufacturing such as roll-to-roll printing [6]. With these processing advantages, organic materials could become a key component in delivering next generation low-cost electronics. Their useful electrical properties combined with their processing advantages opens up the possibility of having interesting new technologies such as flexible displays, transparent electronics and cheap disposable devices.

This research is a component of a parent project titled “Delivering Plastic Electronic Item Level Tracking for the Perishable Goods Supply Chain” (PET project) which was jointly funded by the Technology Strategy Board [7] (TSB) and Syngenta [8]. The PET project consortium consisted of the Schools of Physics and Astronomy (SoPA), Chemistry (SoC) and Electrical and Electronic Engineering (EEE) at the University of Manchester (UoM); along with industrial partners Xennia [9] and Kingston Chemicals [10]. The PET project’s goal is to develop a low-cost sensor system for item level tagging, employing the use of passive RFID technology for the wireless transmission component. The sensor is a novel liquid crystal device capable of passive temperature logging, functioning without the use of batteries or any power source. Its mode of operation is based on the change in dielectric properties of a liquid crystal material and the development of the sensor is undertaken by the SoPA [11] and SoC groups. The EEE group was responsible for the integration of the temperature sensor with passive RFID tags via an electronic interface. The interface provides a means to probe and digitise the output from the sensor to obtain useful temperature information. This research runs in parallel to investigate the possibility of an organic equivalent of the silicon interfacing circuit. The focus of this thesis will therefore be on the use of solution processed organic field effect transistors (OFETs) for circuits and the feasibility of using organic technology in the manufacture of low cost electronics.

1.1 Background

1.1.1 Organic Semiconductor Materials and Charge Transport

Organic conductors and semiconductors are sometimes referred to as conjugated polymers, simply describing the bonding structure between the carbon atoms along the backbone of the polymer. In this class of materials, the carbon atoms are alternately single/double bonded or single/triple bonded. A useful starting point for this discussion would be at the atomic level. A carbon atom has 4 valence electrons with an electronic configuration of $1s^2\ 2s^2\ 2p^2$. There are two electrons in its first level orbital (denoted as 1s) and 4 electrons distributed in two of the second level orbitals (2s and 2p). The orbitals represent the energy levels (also known as states) of the electrons. The lowest level orbitals have the smallest energy levels and this increases for subsequent orbital levels.

1.1.1.1 Hybridisation

When a carbon atom bonds with other atoms, the four orbitals in the second energy level can undergo mixing and are replaced by hybridised orbitals. Four hybridised orbitals are formed when all second level orbitals (s, p_x, p_y and p_z) are involved in hybridisation. Such a configuration is known as sp^3 and the orbitals are orientated towards the corners of a tetrahedron shape. With sp^3 hybridisation, single bonds are formed as each of the valence electron is bonded with a large orbital overlap with the electrons of four other atoms. Each single bond contains a sigma (σ) bond that is strongly localised to the bonded atoms and do not take part in the charge transport.

Double or triple bonds arise when only two (sp) or three (sp^2) second level orbitals are involved in hybridisation. The remaining unchanged atomic orbital(s) overlap laterally with p-orbitals of other carbon atoms to form weaker pi (π) bonding molecular orbitals. Electrons involved in the π-bonding are delocalised over the molecule. The highest occupied molecular orbital (HOMO) is analogous to the valence band in inorganic conductors and the lowest unoccupied molecular orbital (LUMO) is analogous to the conduction band. Filling or manipulation of the molecular orbitals gives rise to the conducting properties of the conjugated polymers. This is accomplished by chemical doping (conductors), photo-excitation (photovoltaics) or by charge injection (semiconductors). Here, the discussion will be limited to the semiconducting properties.

1.1.1.2 Charge Transport

For organic semiconductor materials, one may initially think that charge transport occurs at the LUMO level, as the charge carriers are delocalised along the polymer chain. However, in disordered materials, the travel distance (mean free path) of the delocalised charge carriers is very small due to structural defects [12, 13], and as such do not follow classical band transport in inorganic materials.

Instead, charge transport in disordered materials occurs by hopping of charge carriers between localised states and is assisted by lattice vibrations (phonons) [14-16]. The phonon assisted transport is illustrated in Figure 1.1. In a perfect crystal, depicted as the straight line, a free carrier is delocalised and moves as a plane wave without scattering. In a real crystal however, there are always lattice vibrations that disrupt the

crystal symmetry. Mobility is reduced when carriers are scattered by phonons. With decreased temperature, the occurrence of phonons is lower and hence mobility increases. Conversely for the case of hopping transport, the movement of localised charge carriers from one site to another is aided by the phonons. Mobility increases with increasing temperature [17].

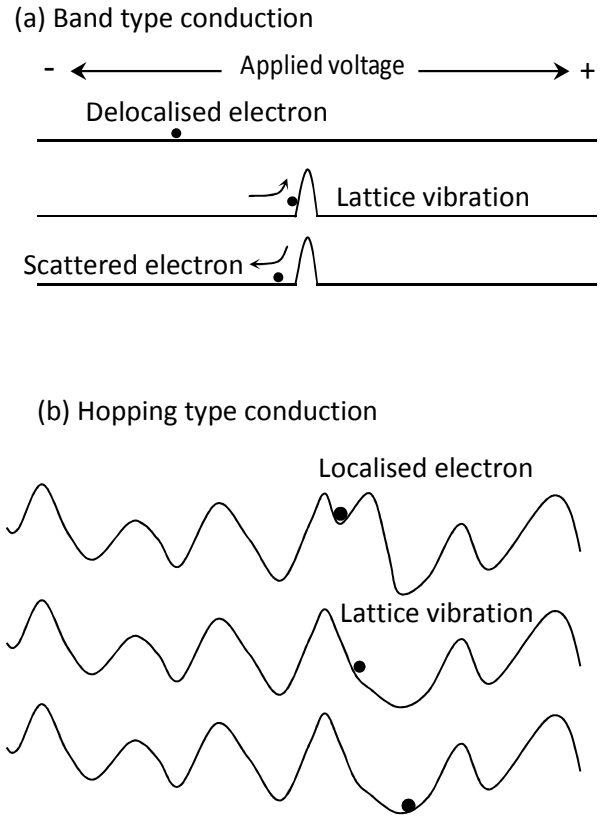


Figure 1.1: Band transport (a) and hopping transport (b). This figure is adapted from [1].

When a charge carrier is introduced to the conducting channel of an OFET, it is initially localised within a molecule or a segment of the conjugated polymer chain. The charge carrier then hops to another available localised state in another molecule within the chain or to adjacent chains in the direction of the applied electric field.

Several theories contribute to the localisation of charges. One theory that is often used in relation to the disorder in organic materials is by Anderson [15]. In his paper, it was suggested localisation in random lattices occur due to impurities and randomness of the lattice interactions. In Anderson's theoretical model, the randomness effect form energy levels that vary from site to site. Localisation occurs when the density of the energy levels is sufficiently low. Bassler [12] suggested that the defects in disordered

materials give a Gaussian distribution to the density of states instead of two distinct delocalised energy bands. This is based on the Gaussian shape of the optical spectra observed in disordered materials. Another localisation phenomenon is the electron-phonon interaction which is first described by the small polaron model by Holstein [18]. In the model, excess charge in crystalline solids are self trapped due to interactions with the lattice, and the lattice is deformed to accommodate the charge.

Despite the efforts in understanding the physics of organic materials, it is often stated that the exact nature of charge transport is not well understood yet. This is due to the fact that highly ordered or crystalline organic semiconductors can achieve field effect mobilities that are close to the limit of the hopping transport (between 0.1 and 1 cm^2/Vs [17, 19]), hence delocalised charge transport in such materials is plausible.

1.1.1.3 Charge Transport Models

Several models to estimate the field effect mobility in organic semiconductors have been developed over the years. Discussion in this section will however focus on the two classic models. Vissenberg and Matters [20] presented a percolation model under the concept of variable range hopping (VRH) [21]. Charge carriers are thermally activated and tunnel between localised states. The distance of the hops depend on the activation energy of the charge carriers. If high activation energy is required, the hop distance is small and vice versa. Resulting mobility values are proportional to the applied gate voltage according to a power law, a characteristic that is indeed observed in organic semiconductors [22-24].

The multiple trapping and release model by Horowitz [25] assumes charge transport in delocalised states. For this model, mobility is dependent on gate voltage and temperature. The transport mechanism is via charge carriers that are temporarily released to an extended transport band where its movement can be stopped due to the presence of shallow traps (energy states close to the transport band). At high gate voltages, the trapping sites are filled, hence mobility increases. This model is usually used to describe transport for polycrystalline organic semiconductors. Within the boundaries of a crystallite, the charge carriers move in delocalised states but are trapped at the grain boundaries where there are localised traps.

1.1.2 Organic Field Effect Transistors (OFETs)

OFETs are a type of field effect transistor fabricated by depositing thin films of materials in a sequentially layered structure and are used primarily in applications that require large area electronics. The majority of displays for computing or mobile phones today are thin film based, using polysilicon or amorphous silicon as the active material [26]. The organic variant is conceptually similar, but with a distinct difference in device performance. OFETs typically exhibit much slower switching frequencies, require higher operating voltages and have lower lifetime and stress stability [26, 27].

In terms of construction, one may presume that organic devices are fabricated entirely with solution processable materials. However, that notion is quite the contrary to the vast majority of the reported literature. The conductive polymers are often used in combination with inorganic materials, forming hybrid devices [19, 27, 28]. Nonetheless, it is reasonable to classify a transistor as organic if the semiconductor material alone is organic based [27]. Typical OFETs consist of gate, dielectric, contacts (source/drain electrodes) and semiconducting layers. The illustrations in Figure 1.2 show several common OFET structures. The terms top contact or bottom contact is distinguished by the sequence of the contact layer deposition relative to the semiconductor layer. In the case of the bottom gate structure, the bottom contacts are in plane with the conducting channel and for a top gate structure, the contacts are staggered from the channel.

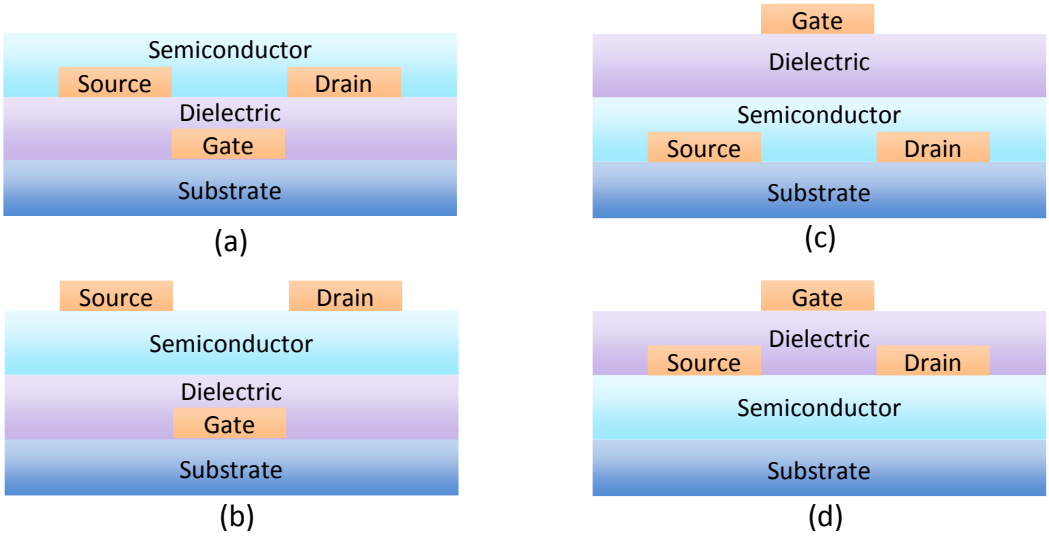


Figure 1.2: OFET structures. Bottom gate bottom contact – BGBC (a). Bottom gate top contact – BGTC (b). Top gate bottom contact – TGBC (c). Top gate top contact – TGTC (d).

An OFET is usually a three terminal device. The output current flowing between the source and drain electrodes is modulated by biasing the gate electrode. The following discussion will describe the operation of a standard p-channel OFET using pentacene as the semiconductor (Figure 1.3). The transistor is switched on by applying a negative voltage to the gate terminal. Biasing of the gate polarises the semiconductor and positive charges are accumulated at the gate dielectric-semiconductor interface. A channel between the source and drain electrodes is formed. An OFET usually operates in accumulation mode in contrast to depletion mode (channel inversion) with typical MOSFETs. Nevertheless, depletion mode OFETs have also been demonstrated [29, 30]. Positive charges are injected from the source contact into the organic semiconducting material and are collected by the drain electrode. Charge carriers are directed towards the drain by applying a negative potential to the drain electrode.

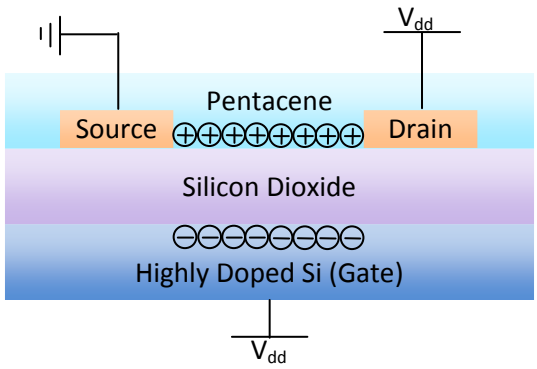


Figure 1.3: Bottom gate bottom contact OFET with Si gate, SiO_2 dielectric and pentacene semiconductor.

1.1.2.1 OFETs: Performance and Characteristics

Several device parameters are used in evaluating the performance of OFETs; these are mobility, on-off ratio, threshold voltage and subthreshold swing. The most common parameter to gauge overall transistor performance is the mobility parameter. Typically expressed in cm^2/Vs, mobility describes the average drift velocity of the charge carriers under an applied electric field. Threshold voltage (V_{th}) is the minimum gate voltage to induce mobile charges at the insulator/semiconductor interface [31]. Although it is desirable to have an OFET switch on immediately upon application of the gate voltage, a nonzero V_{th} (both positive and negative direction) is often the case due to several reasons. For a p-channel OFET, the presence of deep traps in the semiconductor must first be filled before the channel can conduct (negative threshold

voltage) [31]. Conversely, unintentional doping of the semiconductor can cause it to be conducting when V_{gs} = 0 (positive threshold voltage) [31]. Another important parameter is the "on-off ratio" which is defined as the source-drain current ratio between the transistor "on" and "off" states and it is usually expressed in the form of 10^X [32]. Sub-threshold swing or inverse sub-threshold slope (S) is a measure of how rapidly the device switches off by the gate voltage and is commonly expressed in V/decade [33]. For the performance parameters discussed, it is desirable to have high mobility and on-off ratio, low value for sub-threshold swing and a V_{th} that is ideally tuneable or close to 0 V.

To achieve high performance OFETs, a smooth dielectric interface is crucial as the majority of the charge transport occurs at the semiconductor-dielectric interface [34, 35]. Poisson's equation [36], numerical [37] and analytical [36] solutions have been used to estimate the channel thickness in organic semiconductors. In an empirical study by Dodabalapur *et al.* [38], a thiopene based semiconductor was varied in thickness from 2.5 nm to 150 nm. They found that all of the induced charges were within the first one or two monolayers (one monolayer is typically around 1.5 nm to 3 nm thick) of the semiconductor. Another important design consideration for high performance OFETs is the matching of energy levels of the contacts and the semiconductor. For example, high work function gold (Φ_w 5.1 eV [39]) or platinum (Φ_w 5.65 eV [39]) is typically used in conjunction with hole carrier affinity semiconductors as the charge injection barrier to the HOMO level is small (Figure 1.4).

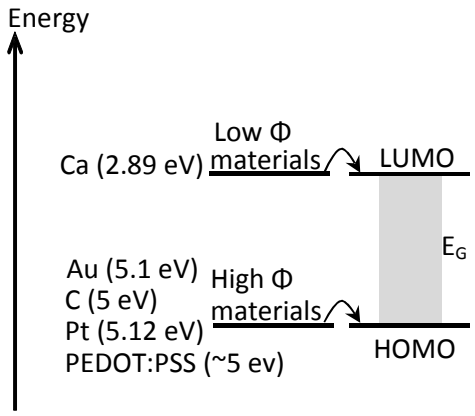


Figure 1.4: Energy diagram illustrating the injection of charges from matching work function contact materials into HOMO or LUMO levels of an organic semiconductor.

An interesting attribute of organic transistors stemming from its charge transport mechanism is that the term “p-channel” or “n-channel” is determined by the device as a whole, unlike inorganic MOSFETS which is defined by the dopants in the active material. An OFET can be either type depending on the matching of the source/drain electrodes and semiconductor material. To elaborate, a p-channel transistor can theoretically (provided the semiconductor exhibits electron transport affinity) be converted to n-channel by switching the source and drain contacts to a matching low work function metal (e.g. calcium) that is aligned with the LUMO level of the semiconductor. For simplicity however, the terms p-channel and n-channel in this thesis will be used based on the commonly used device operation mode for a particular OFET configuration.

1.2 Motivation and Research Aim

This research is motivated by the potential use of organic electronics as the driving technology for realising a low-cost sensor technology platform for aiding the delivery of more efficient supply chains, in particular for the distribution of chilled perishable produce. The margins within these chains can be very low so any reduction in wastage can have a significant impact on profitability.

Present research on electro active organic materials has reached a performance point which many consider to be acceptable for applications with modest performance requirements. This is seen in the emerging trend in research focus that has tended towards the use of OFETs for practical applications. Most notably, recent progress saw the successful fabrication of flexible displays [40] and RFID transponder tags [41]. However, despite the demonstration of the aforementioned organic devices, commercial use of organic electronic devices is still rare and unheard of in the case of devices incorporating organic transistors. Therefore, this research aims to uncover the technical barriers and limitation of the technology that is preventing a more widespread use and adoption of organic electronics. Suitable state of the art fabrication processes for organic logic circuits will be reviewed first. This knowledge is then applied, through the design and fabrication of a simple organic interfacing circuit, for the temperature sensor developed under the PET project [11]. This research prioritises the use of low cost solution processable materials that can be

transferred to future printing technologies. By practical evaluation of the state of the art processes, it is anticipated that a better understanding of organic technology will be obtained, specifically the feasibility and future outlook of the technology for low-cost electronics.

1.3 Research Challenges

The most challenging aspect of this research is the fabrication of organic logic circuits, which require OFETs that are specially designed to be logic compatible. Relatively little published research is available in this area with the focus on integrated circuits; essentially the use of organic transistors to form useful logic functions. When interconnecting multiple OFETs, careful consideration must be placed on the design of the transistor and the accompanying fabrication processes to ensure the organic materials are not damaged during processing. Despite the considerable improvements in the chemistry of organic materials and advances in processing techniques in recent years, the delivery of stable and high performance organic circuits that are ready for commercialisation, remains as a goal to be achieved. This thesis will hence provide insight on the manner in which research on organic circuits can be conducted. By detailed documentation of the fabrication processes and the design decisions of the investigated circuits, future researchers can have a better understanding of the requirements, methodologies and challenges involved in this research area.

1.4 Thesis Organisation

This thesis is arranged in 7 chapters. Chapter 2 reviews the literature on the fabrication technologies for organic logic circuits, comparing between laboratory and printing processes. The chapter also explores the state of the art organic devices.

Chapter 3 first introduces the operating principle of the liquid crystal temperature sensor and explains how it can be probed to extract temperature information. The overall silicon sensor system is then presented, followed by an assessment on the possibility of an equivalent organic circuit and the selection of a suitable logic circuit fabrication process. This chapter also details the design aspects of the research. This

includes the design of the inverter and comparator circuits, as well as a photomask that is used with the lithographic fabrication process.

Chapter 4 describes the methodology of the experimental work. The procedures for fabricating single transistors, capacitors and logic circuits using PVP gate dielectric are detailed. This includes the deposition and processing conditions for each layer of the transistor stack.

Chapter 5 details the fabrication results for the logic circuit process. The characteristics of the PVP gate dielectric layer are first discussed. Next, the performance of the single transistor, inverters and comparator circuit are presented. This chapter ends with a discussion on how the employed fabrication process can be further refined.

Chapter 6 reports the optimisation work conducted to improve the performance of the transistors used for the logic circuits. The work here extends the fabrication process presented initially in chapter 3 and 4, by attempting to address the high operational voltages (~20 V) and low mobilities (~10^{-3} cm^2/Vs**)** of the solution processed transistors. The first experiment investigates the use of a polymer and nanoparticle nanocomposite dielectric. A second experiment investigates the improvements in device performance after application of a surface modification treatment to the contacts layer of the transistor.

The thesis conclusions are presented in chapter 7, along with a discussion on potential future work.

2 Literature Review

2.1 Introduction

In the core research of organic electronics, successful implementation of new materials [42] or fabrication techniques [43] are normally demonstrated by the performance matrices of fabricated single transistors. This forms a trend where many new OFETs with good performance characteristics are reported, but in practical sense are not very useful as they are only applicable when fabricating isolated transistors. Considering that organic electronics is poised to be a cost effective replacement to existing silicon circuits, the reported OFETs should ideally be logic compatible.

The fabrication of organic logic circuits demands a step-up in complexity in processing when compared to single transistors, requiring formation of vias, interconnects and the control of threshold voltage [27, 44]. This is achieved by patterning each layer of the thin film transistor, which is a major challenge because polymeric and small molecule organic semiconductors are more prone to dissolution and degradation [32, 45]. Effectively, the patterning requirement places an upmost importance on the fabrication process to maintain the overall stack integrity of the transistors in an organic circuit. The processing of each individual layer of an organic thin film transistor must take into account the cross compatibility of materials, solvent use, deposition and patterning techniques.

This chapter first assesses the state of the art organic devices. Next, the enabling technologies behind the state of the art devices are analysed. Details on fabrication processes, commonly used organic materials as well as simulation techniques for organic logic circuit design will be covered.

2.2 Progress in Organic Logic Circuits

Innovative fabrication processes have previously been researched that enabled the transition of single transistors to organic logic circuits. Early attempts on the fabrication of organic logic circuits were spearheaded by influential institutions using both printing and laboratory techniques. Infineon [46], Cavendish Laboratory [47] (now Plastic Logic [48]) and Philips [40] among others reported on novel fabrication processes for simple logic blocks such as the inverter and ring oscillator. This

eventually paved the way to the more advanced organic devices with thousands of integrated transistors reported in recent years [41, 49, 50].

The versatility of the OFET is apparent, as a diverse combination of contact electrode, dielectric and semiconductor materials have been paired up successfully. Transistors can be fabricated on various substrates, be it silicon dioxide [51], glass [52] or flexible films such as polyimide [45]. Polymeric materials and metal oxides are normally used as dielectric layers. To conduct research on organic logic circuits, knowledge on the deposition and processing of the delicate organic materials becomes a fundamental requirement. Leading research groups take this fabrication knowledge to the next level, in that they are able to optimise a fabrication process to be useful from an electronics standpoint [40, 41]. This includes the non trivial tasks of controlling the threshold voltage of fabricated transistors, perfecting material combinations for consistent device characteristics and designing logic configurations to either improve logic performance or to form more complex digital functions.

2.2.1 State of The Art Organic Devices

Parallel to the pursuit of novel fabrication processes, research groups also investigated organic devices for real world applications. So far, applications include flexible displays [40, 53], sensors [54-57] and RFID transponder tags [41, 50, 58, 59]. The first trial on organic RFID tags as electronic tickets was conducted by PolyIC in 2007. The RFID transponder tags used were likely to be simple oscillator circuits on flexible substrates, as they only generate response signals without sending any identification information [60].

To define the meaning of state of the art in this section, the complexity and performance of the fabricated devices are considered. Philips demonstrated the first electronic paper in the form of a flexible monochrome display (Figure 2.1) that is driven by an active matrix backplane [40]. The backplane consists of 1888 organic transistors fabricated on flexible polyimide foil, which remains functional even when bent to a radius of 1 cm. The display is capable of delivering refresh rates up to 75 Hz, with a power consumption of 200 mW when operating at the maximum refresh rate. Physically, the display measures 3.5 cm^2 in area and is 300 µm thick.

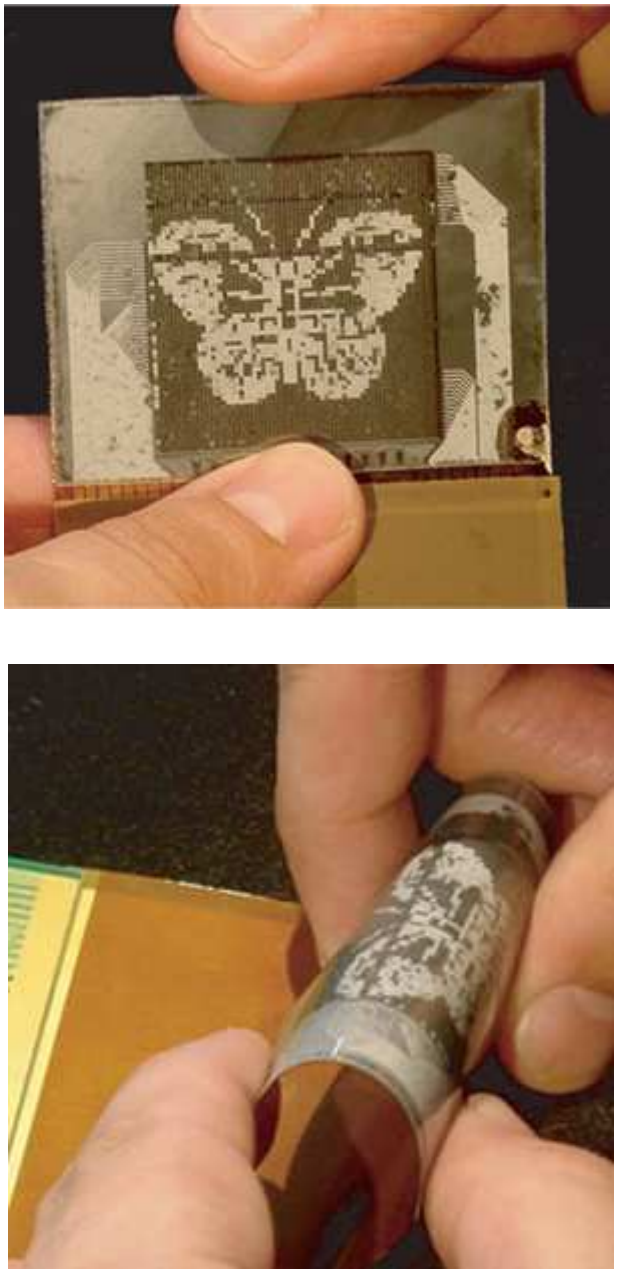


Figure 2.1: Flexible display using organic transistors. Image by Philips [40].

Recently, Polymer Vision, a spin-out company from Philips demonstrated a larger 6" flexible display named Readius (Figure 2.2) and claimed that functionality is retained even after being rolled up 25,000 times. The technical details surrounding the Readius display are sparse, with only a video demonstration of the display that can be viewed on their website [53] and a recent patent application for a flexible display (European Patent Application EP2281226).

Figure 2.2: A 6" Readius display. Image by Polymer Vision [53].

Among the state of the art applications, organic RFID transponder tags represent one of the most complex organic devices reported to date. Literature on simple ring oscillator RFID tags surfaced as early as 2003, by Baude *et al.* at 3M [61]. However, the first organic tag that has similar functionality to an actual RFID tag is the 64-bit tag (Figure 2.3) reported by Philips in 2006 [41]. The engineering of the Philips tag was far more sophisticated than all other reported organic RFID tags that precedes it; consisting of code generator (acting as memory), counter, shift register, encoder-decoder and signal modulation components. Their tag combines the use of basic building blocks of inverters and NAND gates which are stacked to produce more complex logic like the D flip-flop. One limitation of Philips' design is that it uses capacitive coupling as its wireless transmission medium, therefore requiring the generation of large tag reader voltage amplitudes to energise the tag even at short operating distances. Philips' tag design was later improved to employ inductive coupling by the research team formed by the collaboration of IMEC and TNO [50, 62]. Nonetheless, the original transponder design marked an important milestone of what is achievable with organic transistors for real world applications. Another important achievement with regards to complex organic circuits is the successful fabrication of an 8-bit microprocessor by IMEC-TNO [49], which adds programmable logic to the mostly hardcoded logic of current generation organic circuits. Their microprocessor consists of 4000 transistors that is fabricated using Polymer Vision's

dual gate process and is capable of standard binary logic (AND, OR, NOT) processing and arithmetic operations (addition, subtraction, etc).

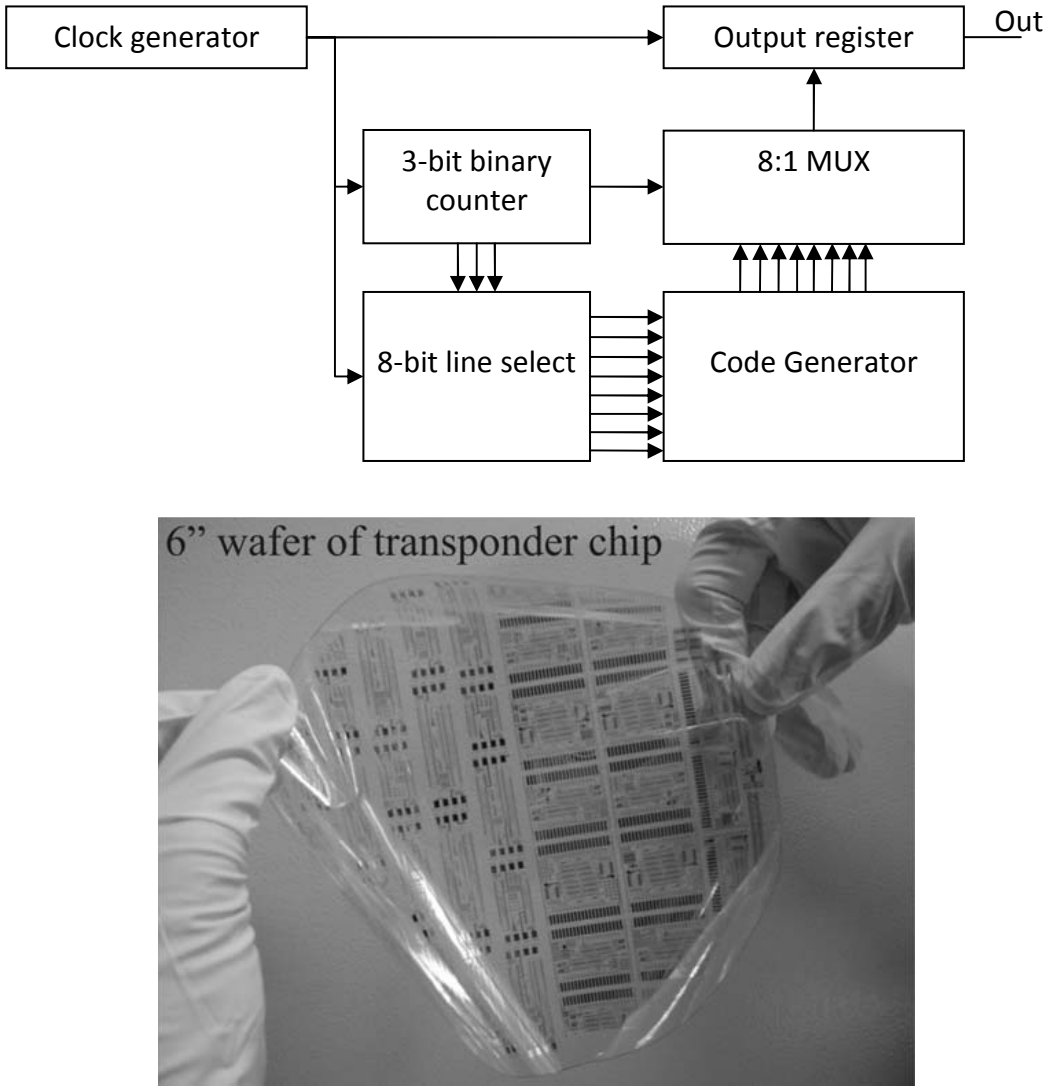


Figure 2.3: Organic RFID chip fabricated on polyimide substrate. Image by Philips [41].

With regards to performance, metal oxide dielectrics have contributed to the fastest and lowest power requirement organic devices. The lowest voltage organic circuit to date is reported by Klauk *et al.* [52]. In the paper, Al_2O_3 dielectric is surface modified using n-octadecylphosphonic acid (OPA) self assembled monolayer (SAM), forming a thin (5.7 nm) dielectric layer. The ultra-thin SAM treated metal oxide provides a hydrophobic interface that improves molecular ordering of the deposited semiconductors, resulting in transistors that operate at 1.5 V with p-channel mobility of 0.4 cm^2/Vs. More recently, the fastest organic RFID transponder (Figure 2.4) with

a data rate 50 kb/s have been reported by Myny *et al.* [59], also using Al_2O_3 gate dielectric.

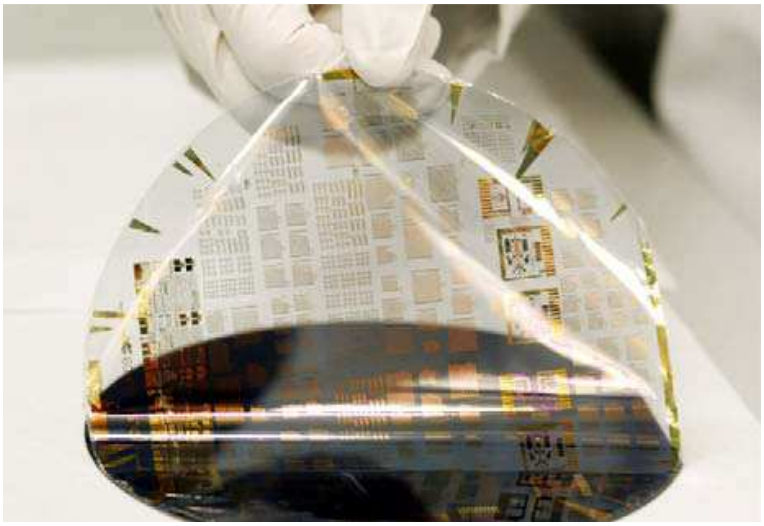


Figure 2.4: The fastest RFID chip to date using Al_2O_3 dielectric. Image by IMEC-TNO [59].

State of the art organic devices reported in the literature generally share many similar characteristics. Transistor logic is mainly constrained to p-channel and individual transistors operate at high voltages, often in excess of 20 V in magnitude. Complexity of organic circuits was initially limited to basic building blocks such as the inverter and ring oscillator, but successful fabrication of NAND gates have enabled more complex digital logic [41]. Although the fabrication process for fully organic [6, 63-65] (all polymer or solution processable materials) transistors exists, state of the art organic devices utilise organic transistors with hybrid structure; combining polymer dielectrics and organic semiconductors with inorganic metal contacts. This is attributed to the increased device performance and ease of processing when air stable metal contact materials are used. State of the art devices discussed in this section are also fabricated using the small molecule pentacene semiconductor, which has high mobility performance but only average shelf and stress stability [66]. It is therefore important to note that while sophisticated logic circuits have been developed, the poor stability of organic materials limit such devices to within the boundaries of laboratory testing.

2.3 Fabrication Process

Fabrication processes for organic logic circuits can be divided into two major streams, laboratory and printing based. The following sections compile and discuss fabrication processes from the literature, highlighting important techniques. A breakdown of each fabrication process is listed, including device operating voltage, structure, mobility, deposition and patterning technique for each layer.

2.3.1 Laboratory Based Processing

The use of conventional laboratory based processing for the fabrication of OFETs is expected due to the heavy reliance on photolithography in the present inorganic semiconductor industry. This class of fabrication normally employs the use of spin-coating, evaporation or drop-casting to deposit electronic materials onto substrates [67]. Deposited layers are patterned using photolithography [40, 68-70] and/or shadow masks [52, 61]. Laboratory processing is non continuous as processing steps such as evaporation and annealing may require substrates to be placed under vacuum or heated at high temperatures several times, with each step consuming several hours. Therefore, a completed logic circuit can take several days to fabricate. Depending on the equipment used, the substrate size is comparatively small (<12 inches) as existing equipment is intended to be used with standard silicon wafer sizes.

The main challenge for laboratory based processing for OFETs is the need for patterning to remove unwanted areas because deposition methods such as evaporation and spin-coating would normally result in a fully covered plane of the substrates [67]. Patterning of the dielectric layer is necessary to create openings for vias and interconnects while patterning of the semiconductor help reduce the off-state currents by several orders of magnitude [71, 72]. In practice, it is very challenging to design an OFET with the right material combination and corresponding patterning processes without compromising stack integrity. This is evident with the similarity of transistor structures and fabrication processes discussed in the following section.

2.3.1.1 Fabrication

Tables 2.1-4 break down the fabrication processes by groups reporting successful fabrication of organic logic circuits using laboratory based processing.

Table 2.1: Laboratory based fabrication techniques reported from 2000 to 2003.

Group	1. Philips [45]	2. Infineon [68]	3. Infineon [63]	4. 3M [61]
Year	2000	2002	2002	April 2003
Circuit Type	Inverter, ring oscillator, NAND gate, counter, decoder	Inverter, ring oscillator	Inverter	Ring oscillator
Voltage (V)	< -2.5 to -10	-20 to -80	-20 to -30	-40
V_{th} (V)	Unknown	-5 & 2	-4	-5
Structure	BGBC	BGBC	BGBC	BGTC
Logic Type	p-channel	p-channel	p-channel	p-channel
Min Channel Length	1µm	5µm	5µm	20µm
Mobility (cm^2/Vs)	10^{-2}	0.3 to 3	0.05 to 0.3	1.5
Substrate	Glass, Polyimide	Highly doped Si, PEN	Glass, PEN foil	Glass
Gate **(Deposition)** **(Patterning)**	200nm Polyaniline (Spin-coating) (Photochemical)	Ti (RF Sputtering) (Photolithography – wet etching)	100-140nm PEDOT:PSS (Spin-coating) (Photolithography)	3nm Ti + 50nm Au (Evaporation) (Shadow mask)
Dielectric **(Deposition)** **(Patterning)**	300nm SC100, Olin Hunt (Spin-coating) (Photolithography)	270nm PVP + PMF (Spin-coating) (Plasma etching)	280 - 360nm PVP + PMF (Spin-coating) (Plasma etching)	Al_2O_3 (Ebeam) (Shadow mask)
Source/Drain **(Deposition)** **(Patterning)**	Polyaniline (Spin-coating) (Photochemical)	30nm Au (Evaporation) (Photolithography – wet etching)	100-140nm PEDOT:PSS (Spin-coating) (Photolithography)	60nm Au (Evaporation) (Shadow mask)
Semiconductor **(Deposition)** **(Patterning)**	Pentacene, rr-P3HT, PTV (Spin-coating) (No patterning)	60nm Pentacene (Evaporation) (No patterning)	60nm Pentacene (Evaporation – 1nm/min) (No patterning)	30nm Pentacene (Evaporation) (Shadow mask)

Table 2.2: Laboratory based fabrication techniques reported from 2004 to 2007.

Group	5. Philips [40]	6. Dresden University [73]	7. Philips [41]	8. Max Planck Institute [52]
Year	2004	2006	2006	Feb 2007
Circuit Type	Shift register, inverter	Amplifiers	RFID tag, NAND gate, inverter, ring oscillator, D-flip flop, counter, code generator	Inverter, NAND gate, Ring oscillator
Voltage (V)	-20	-10 to -15	-10 to -20	-1.5 to -3
V_{th} (V)	-4.7	Unknown	Controllable	Unknown
Structure	BGBC	BGBC	BGBC	BGTC
Logic Type	p-channel	p-channel	p-channel	Complementary
Min Channel Length	2.5µm	5µm	1µm	30µm
Mobility (cm^2/Vs)	0.02	0.1 – 0.3	0.015	0.6 (p-channel) 0.02(n-channel)
Substrate	Polyimide	Glass, SiO_2	Polyimide	Glass
Gate **(Deposition)** **(Patterning)**	50nm Au (Unknown) (Photolithography)	Ti (Evaporation) (Photolithography)	50nm Au (Unknown) (Photolithography)	20nm Al + 20nm Au (Evaporation) (Shadow mask)
Dielectric **(Deposition)** **(Patterning)**	350nm PVP + Cross-linker + PAG (Spin-coating) (Photochemical)	100nm PVP + PMF (Spin-coating) (Photolithography)	350nm PVP + Cross-linker + PAG (Spin-coating) (Photochemical)	5.7nm Al_2O_3 + SAM (Solution immersion) (Self assembly on Al)
Source/Drain **(Deposition)** **(Patterning)**	Au (Evaporated) (Photolithography)	Gold (Unknown) (Photolithography)	Au (Evaporated) (Photolithography)	30nm Au (Evaporation) (Shadow mask)
Semiconductor **(Deposition)** **(Patterning)**	100nm Pentacene (Spin-coating) (Photolithography)	30nm Pentacene (Evaporation) (Shadow mask)	100nm Pentacene (Spin-coating) (Photolithography)	30nm Pentacene (p-channel), 30nm F16CuPc (n-channel) (Evaporation) (Shadow mask)

Table 2.3: Laboratory based fabrication techniques reported from 2007 to 2008.

Group	9. IT C&C Lab [74]	10. Uni of Tokyo [75]	11. Imperial College London [70]	12. Uni of Texas [76]
Year	Dec 2007	Nov 2008	Dec 2008	Dec 2008
Circuit Type	Inverter	Ring Oscillator	Ring Oscillator	Inverter
Voltage (V)	-40	-10	-50 to -120	-35
Vth (V)	-3.3	-3.3 (p-channel) 2.4 (n-channel)	Controllable	-2.5
Structure	BGTC	BGTC	BGBC	BGBC
Logic Type	p-channel	Complementary	p-channel	p-channel
Min Channel Length	50µm	100µm	1µm	5µm
Mobility (cm^2/Vs)	0.03	0.6 (p-channel) 17.1 (n-channel)	0.1	0.2
Substrate	PES	Glass	SiO_2	Si / Si_3N_4
Gate **(Deposition)** **(Patterning)**	3nm Ti + 80nm Au (Evaporation) (Shadow mask)	Ti + Si (RF sputtering) (Shadow mask)	Ti + Au (Unknown) (Photolithography	50nm Chromium (Unknown) (Unknown)
Dielectric **(Deposition)** **(Patterning)**	PMMA blend (PMMBM) (Spin-coating) (Photochemical)	132nm $TiSiO_2$ + SiO_2 (RF sputtering) (Shadow mask)	300nm PVP + Cross-linker + PAG (Spin-coating) (Photochemical)	100 -150nm Parylene (Unknown) (Unknown
Source/Drain **(Deposition)** **(Patterning)**	80nm Au (Evaporation - E–beam) (Shadow mask)	60nm Au (p-channel), Al (n-channel) (Evaporation - E-beam) (Shadow mask)	Au (Unknown) (Photolithography)	100nm Au (Unknown) (Unknown)
Semiconductor **(Deposition)** **(Patterning)**	100nm Pentacene (Evaporation – 1 Å/s) (Shadow mask)	Pentacene (p-channel), a-IGZO (n-channel) (Sputtering) (Shadow mask)	diF-TESADT :PTAA (Spin-coating) (Subtractive photo-lithography)	Pentacene 150nm (Evaporation – Vacuum 0.5 Å/s) (Unknown)

Table 2.4: Laboratory based fabrication techniques reported from 2010 to 2011.

Group	13. IMEC-TNO [62]	14. IMEC-TNO [77]	16. MIT [78]	17. IMEC-TNO [49]
Year	Feb 2010	March 2010	Dec 2010	Feb 2011
Circuit Type	Ring oscillator, NAND Gate, Inverter	Ring Oscillator	Differential amplifier, Op-amp, Comparator	Microprocessor, NAND gate, inverter
Voltage (V)	-20 to -45	-10 to -20	-10	-10 to -20
V_{th} (V)	1.6	0.3 (p-channel) 4.1 (n-channel)	-0.5 to 0.1	-0.5 to 0.1
Structure	Dual gate BC	BGBC	BGBC	Dual gate BC
Logic Type	p-channel	Complementary	p-channel	p-channel
Min Channel Length	1µm	1µm	5µm	5µm
Mobility (cm^2/Vs)	0.15	0.69 (p-channel) 0.26 (n-channel)	Unknown	0.19
Substrate	Unknown	N++ Si	Unknown	Unknown plastic foil
Gate **(Deposition)** **(Patterning)**	Au (Unknown) (Photolithography)	5nm Ti + 25nm Au (Unknown) (Photolithography)	25 nm Ti + 45 nm Pt or 70nm Al (Unknown) (Photolithography)	Au (Unknown) (Photolithography)
Dielectric **(Deposition)** **(Patterning)**	350nm PVP + Cross-linker + PAG (Spin-coating) (Photochemical)	100nm Al_2O_3 (Sputtering) (Unknown)	120nm Parylene-C (Vapour Deposition) (Plasma etching)	350nm PVP + Cross-linker + PAG (Spin-coating) (Photochemical)
Source/Drain **(Deposition)** **(Patterning)**	Au (Evaporated) (Photolithography)	Au + SAM + PαMS (Unknown) (Photolithography)	40nm Au (Unknown) (Photolithography – wet etching)	Au (Evaporated) (Photolithography)
Semiconductor **(Deposition)** **(Patterning)**	Pentacene (Spin-coating) (Photolithography)	Pentacene (p-channel) C60 (n-channel) (Evaporation) (Photolithography)	10nm Pentacene (Evaporation) (Photolithography)	Pentacene (Spin-coating) (Photolithography)

Laboratory Based Fabrication in General

The two patterning techniques employed in the fabrication of organic logic circuits are photolithography and shadow masks. Presently, IMEC-TNO is the leading research group working on state of the art organic devices, employing the fabrication process by Polymer Vision. All reported literature in the presented tables use the bottom gate transistor structure with the exception of Polymer Vision's recent dual gate process [49, 62, 79].

Bottom contact transistor structure is used with photolithography and top contact is used with shadow masks. The selection of the semiconductor material is fairly consistent across the listed processes. Small molecule pentacene is most widely used, with approximately 90% recorded usage. For the dielectric materials, the polymer poly-4-vinylphenol (PVP) and Al_2O_3 are most used. The following discussions are based primarily on the most commonly used materials and structures.

Patterning Using Lithography

With lithographic based patterning, a resist mask is typically used to define areas in which materials are to be present [67]. The mask can be used as a subtractive method (wet/dry etch lithography) to remove unwanted materials or, prior to deposition similar to a stencil (lift-off lithography). Photolithography has also been used to indirectly pattern materials. Chang *et al.* [43] reported the patterning of the semiconductor layer by delamination. This is made possible due to the weaker adhesion of the semiconductor to hydrophobic surfaces, prepared by pre-patterning OTS modified glass substrates using lithography. After patterning, resist masks may be kept on to serve as encapsulation layers or removed by stripping using the resist solvent.

The main advantage with photolithography processing is that the shrinking of transistor feature sizes can be consistently achieved, with reported channel lengths as short as 1µm [41]. However the disadvantage is that the organic materials used must be able to withstand the solvents necessary to complete the lithographic processes. Polymeric materials in particular will be most susceptible to damage due to the ease of being dissolved by commonly used solvents for photolithography such as acetone, methanol and isopropanol.

The lithographic fabrication process that stood out is the BGBC transistor structure using PVP as the gate dielectric. This combination of materials, processing and structure was first introduced by Klauk *et al.* in 2002 [63, 68] (Table 2.1, no. 2) and have since been extensively optimised by Polymer Vision [53] (Table 2.2, no. 5,7). Most of the state of the art organic devices [40, 41, 50, 58, 59] use Polymer Vision's process or similar derivative processes. With PVP dielectric, the yield is reported to be greater than 90% [46, 72], and likely to be close to 100% considering the many reports of successful fabrication of complex organic circuits such as RFID transponder tag [41], microprocessor [49] and display circuitry [40] consisting of several thousands transistors.

Patterning Using Shadow Masks

With shadow mask patterning, a mask with exposed patterns (similar to a stencil) is placed on the substrate before deposition of the material [67]. After material deposition, the mask is removed, leaving behind the patterned material. The difference between shadow mask and photolithography mask is that the former is physically separable and reusable, whereas a photolithography mask is formed on the substrate itself and usually removed after usage.

The advantage of patterning using shadow masks is that it does not require the use of solvents, photoresists and UV illumination. Therefore, the top contact geometry (offering improved charge injection [80]) can be used for bottom gate devices without damaging the semiconducting layer. Masks can be made using a variety of materials such as metals, polymers and silicon. Resolution of 4µm is achievable using nickel shadow masks [81], but larger sizes of above 10µm are typically the case for polymeric shadow masks [52, 61].

While the shadow mask technique is more commonly used for fabricating single transistors, Klauk *et al.* [52] (Table 2.2, no. 8) and Baude *et al.* [82] (Table 2.1, no. 4) reported the use of shadow masks to fabricate inverters and ring oscillators. Klauk's paper is particularly interesting as they demonstrated low voltage complementary organic logic circuits using ultra-thin Al_2O_3 + SAM dielectric, directly addressing the poor performance characteristics of typical organic circuits. In the report, 5 levels of polyimide shadow masks are employed for patterning each layer of the transistor stack. One limitation of their fabrication process lies in the lengthy processing

duration where over 16 hours is required for the deposition of the dielectric layer alone. Their fabrication process must also be improved to use an additional dielectric layer for circuits that require low capacitance interconnect crossovers. Therefore the overall process to support sophisticated circuit configurations will be more complex than what has been reported. Furthermore, there is the inherent disadvantage of using shadow masks. Shadow masks must be regularly replaced, as the quality of contacts will degrade with each use due to the stacking of materials on the mask. The masks are also prone to creasing, often causing the formation of "halos" or non uniform material spreading that surround creased areas of the mask [83, pg. 45]. Finally, the patterns on the shadow mask must be continuous and held together, complicating the deposition process of isolated patterns. In contrast, a photomask can have patterns formed at any location on the mask.

2.3.1.2 Transistor Structure for Laboratory Processed OFETs

Gate Electrode Placement

The bottom gate geometry is an obvious option for logic circuits fabricated using laboratory based processing. With the bottom gate geometry, the semiconducting material is deposited in the final steps, hence excluding the semiconducting layer from any harsh processing. This presents one main advantage; that is a wider selection of semiconducting materials can be used without worry of being irreversibly damaged by organic solvents or other processes. For example, stacking layers onto the semiconductor layer via solution based deposition may cause damage from solvents or contamination with photoresist materials; whereas vapour based deposition may result in diffusion of material particles into the semiconductor, damaging the film or altering its characteristics [32].

Polymer Vision employed a dual gate geometry to better control the threshold voltage of transistors to address the lack of good material combinations for forming complementary logic [62, 79]. However, this approach requires varying high voltage level biases for the secondary gates, complicating the design of the supply stage of such devices. To address the supply issue, Myny *et al.*[49] proposed the use of charge pumps to deliver sufficient voltage levels for the dual gate technology.

Source Drain Electrode Placement

With reference to a bottom gate placement, the use of bottom contact geometry is necessary for patterning using photolithography. The reasoning for this structure is similar to the gate electrode placement discussed above, which is to perform all harsh lithography and etching of the source/drain electrodes before deposition of the semiconductor. Using shadow masks on the other hand, allow top contact geometry to be used.

2.3.1.3 Materials for Laboratory Processed OFETs

Semiconducting Layer : Pentacene

From the compiled fabrication data, pentacene is used in the majority of the state of the art devices. It is among the best performing organic semiconductor to date, with reported mobilities of typically around 1 cm^2/Vs and as high as 5.5 cm^2/Vs [84]. The highest performance pentacene devices are reported from single crystal and evaporated form of the material. In recent years, two methods of depositing pentacene from solution have been developed. The first method is by using a pentacene precursor solution that is spin-coated and thermally converted to pentacene [85, 86]. The second method is to use a soluble form of pentacene (e.g. 6,13-Bis(triisopropylsilylethynyl)-pentacene (TIPS-pentacene)) [87, 88] that is formulated by substituting the primary structure with solubilising side groups. Soluble pentacene is also capable of delivering high performance OFETs, with reported mobility values as high as 1.8 cm^2/Vs [51].

Despite being a benchmark semiconductor material, the stability characteristics of pentacene as well as most other organic semiconductors is a barrier towards commercialisation. Studies have shown that pentacene devices under continuous signal cycling lose on average two orders of magnitude in mobility [40, 66, 89]. Similar stability degradations are observed in shelf life testing, where a shift in voltage threshold is also present in addition to the reduction in field effect mobility. Philips reported a 30% reduction in mobility after 3 months when devices are stored at 25 °C (50% humidity). A threshold voltage shift of 1.5 V was observed after biasing their device for 1 hour [40]. Their stability data was collected with polyvinyl alcohol (PVA) as the encapsulation layer.

Dielectric Layer

The compiled fabrication processes in tables 2.1-4 show that PVP is the favourite choice for polymeric based dielectric and Al_2O_3 is used when high-k dielectric is required.

PVP is deposited via spin-coating and has a permittivity of 3.6 [63, 72]. The advantage of using PVP over other polymers is that PVP can be thermally cross-linked to develop chemical resistance against many organic solvents, developers and acids. The analysis by Klauk *et al.* [46] also found that cross-linked PVP possesses comparable electrical insulating properties as thermally grown SiO_2. Excellent dielectric performance, coupled with the robustness of PVP against chemical processing makes it an ideal polymer choice for organic logic circuits.

Al_2O_3 is popular as aluminium is a relatively cheap metal and its oxide can be formed using various methods such as sputtering, atomic layer deposition (ALD) [90], anodization [91] and oxygen plasma treatment [52]. Al_2O_3 has a dielectric constant of 7 - 9.5 [90] and exhibits good tensile strength [91], allowing for a certain degree of physical flexibility when used with polymeric substrates.

Contact Materials

High work function materials gold and poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) are mainly deposited as contact electrodes for p-channel OFETs. Gold has a work function of 5.1 to 5.31 eV [39, 92], while PEDOT:PSS has a work function of 5.1 eV [93]. The high work functions are close to the HOMO level of pentacene, allowing positive charges to be easily injected to the material. Interestingly, gold contacts are also used for the reported complementary devices (Table 2.2, no. 8 and Table 2.4, no. 14) instead of low work function metals like calcium (2.87 eV [39]). N-channel OFET operation is obtained by using organic semiconductors with LUMO levels (F16CuPc, ~6.3 eV [94] and C60, 6.17 eV [95]) that are aligned with the work function of the electrodes. This is a sound approach as gold is air stable, and eliminates the need for the deposition of two types of contact materials for both the p-channel and n-channel devices.

2.3.2 Printing Based Processing

Printing techniques for organic materials have been extensively researched as it is synonymous with the idea of realising low cost, large area and high volume electronics. This approach places emphasis on continuous processing, where lengthy processes such as lithography, annealing and etching are to be avoided. Often, mass printing technologies such as gravure and flexography are investigated as they complement well the use of organic electronic inks.

Perhaps the most important characteristic of printing based processing is that the deposition of materials is additive. Material wastage is minimised as ink is deposited only where needed. Furthermore, specific area deposition eliminates the need for patterning, which is a major limitation with processes derived from conventional laboratory (lithographic) based processing. Without the need for harsh lithographic patterning processes, a wider selection of polymers and organic semiconductors can be used.

However, the shift to printing electronic devices from the classical use of printers for printing visual content is not without complications. First, the degree of flexibility in the selection of materials is limited by the choice of solvents. When printing OFETs, it is important to consider the sequence and solvents for the deposition of each layer to prevent underlying layers from being re-dissolved or damaged by incompatible solvents.

The second complication is on the dimensional aspect of printed OFETs. Conventional printing techniques are optimised to satisfy the human eye and thus, the typical resolution is in the range of 20-50 µm [47]. Such low resolution is undesirable for the fabrication of OFETs due to the low mobility of organic semiconductors, which is normally compensated by the design of shorter channel length (<10 µm) transistors. The poor resolution is a result of the spreading of inks upon deposition, which often requires additional processing to prevent shorting of the source and drain electrodes. A straight forward method is to leave sufficient lateral spacing between the printed areas, while more complex approaches rely on preparing the substrates with higher resolution processes prior to material deposition. Two examples for the latter approach include the use of substrates with pre-patterned polymeric “wells” [47] and

substrates pre-treated with repellent hydrophobic surfaces [65] to confine the spreading of the deposited inks.

Finally, there is also the complication with the physical qualities of printed thin films. Thin film properties such as homogeneity and film thickness play an important part in achieving high performance OFETs. However, printed films typically result in relatively rougher surfaces [6, 64], when compared to the smooth films attained with spin-coating. Such physical limitations place contrasting design requirements for printed OFETs, particularly with regards to the dielectric layer. On one hand, the thickness of the dielectric layer must be appropriately increased to prevent short circuits between the gate and source/drain contact layers. This is to achieve high fabrication yields. On the other hand, thicker dielectric layers require the application of large amplitude biasing voltages (>40 V), which is undesirable for practical applications.

So far, fabrication of organic devices using continuous printing processes has proven to be extremely challenging, as most reported literature on printed OFETs contain at least one non continuous step, or the use of non soluble materials.

2.3.2.1 Fabrication

Tables 2.5 – 6 compile the printing processes from 1994 to 2010, followed by a discussion on the transistor structure and materials used.

Table 2.5: Printing based fabrication techniques reported from 1994 to 2004.

Group	1. Laboratoire des Materiaux Moleculaires [96]	2. Bell Laboratories [97]	3. Epson Cambridge [47]	4. PolyIC [98]
Year	1994	1997	2000	2004
Circuit Type	Unknown	Unknown	Inverter, Ring Oscillator	Inverter, Ring Oscillator
Voltage (V)	-30 to -80	-30	-20	-30 to -100
V_{th} (V)	Unknown	Unknown	-10	-5 (PDHTT) 3 (P3HT)
Structure	BGBC	BGTC	TGBC	TGTC
Logic Type	P-channel	P-channel	P-channel	P-channel
Min Channel Length	200µm	100µm	5µm	20µm
Mobility (cm^2/Vs)	0.06	0.01 – 0.03	0.07	0.007 (P3HT), 0.0002 (PDHTT)
Substrate	Unknown	PET film	PI film	PET film
Gate **(Deposition)** **(Patterning)**	10µm Graphite-based ink (Stencil) (Stencil mask)	ITO (As purchased) (As purchased)	50nm PEDOT: PSS (Photolithography + inkjet) (Inkjet)	Carbon ink (Pad printing) (Pad printing)
Dielectric **(Deposition)** **(Patterning)**	1.5µm PET film (As purchased) (No patterning)	7.5µm Polyimide (Screen) (Screen mask)	500nm PVP (Spin-coating) (Inkjet punch-through)	0.5-1µm PMMA+poly4hydroxystyrene (Blade coating) (Blade coating)
Source/Drain **(Deposition)** **(Patterning)**	10µm Graphite-based ink (Stencil) (Stencil mask)	10µm Electrodag 479SS (Screen) (Screen mask)	PEDOT:PSS (Inkjet) (Inkjet)	Polyaniline (Blade coating) (Pad printing + etching)
Semiconductor **(Deposition)** **(Patterning)**	40 nm x,w-di- (hexyl)sexithiophene (Evaporation) (No patterning)	rr-P3AT (Printing - unknown) (Printing)	15-30nm F8T2 (Spin-coating) (No patterning)	P3HT, PDHTT (Blade printing) (Blade printing)

Table 2.6: Printing based fabrication techniques reported from 1997 to 2010.

Group	5. Chemnitz University [6]	6. Akademi University [99]	7. Polyera [100]	8. Sunchon National Uni [101]	9. Chemnitz University [64]
Year	2007	2008	Feb 2009	Feb 2010	Feb 2010
Circuit Type	Inverter, Ring Oscillator	Unknown	Inverter	Inverter, Ring Oscillator	Ring Oscillator
Voltage (V)	-40 to -80	-2	10 to 40	-10 to -80	-60 to -100
V_{th} (V)	Unknown	0.2	5 to 35	-3	Unknown
Structure	TGBC	TGBC	TGBC	BGBC	TGTC
Logic Type	P-channel	P-channel	Complementary	P-channel	P-channel
Min Channel Length	0.1mm	35µm	25µm	200µm	100µm
Mobility (cm^2/Vs)	0.001	Unknown	0.1 to 0.4	0.03 to 5.24	0.0005
Substrate	PET film	PET film	PET film	PET film	PET film
Gate **(Deposition)** **(Patterning)**	Silver ink (Flexography) (Flexography)	PEDOT:PSS (Inkjet) (Inkjet)	30nm Au (Evaporation) (Unknown)	75µm Silver ink (Paru PR-007) (Gravure) (Gravure)	200nm PEDOT:PSS (Gravure) (Gravure)
Dielectric **(Deposition)** **(Patterning)**	BuS Copolymer + $BaTiO_3$ (Gravure) (Gravure)	1.6µm PVP (Gravure) (Gravure)	1000-1200nm Various (Gravure Printing) (Gravure Printing)	4.5µm BaTiO3 + PMMA (Gravure) (Gravure)	2µm Merck P105 + PMMA (Gravure) (Gravure)
Source/Drain **(Deposition)** **(Patterning)**	600nm PEDOT / PSS (Offset Printing) (Offset Printing)	30nm Au (Evaporation)	30nm Au (Vapour - Unknown) (Shadow mask)	Single-Walled Carbon Nanotube (Inkjet) (Inkjet)	250nm PEDOT:PSS (Gravure) (Gravure)
Semiconductor **(Deposition)** **(Patterning)**	25µm F8T2 (Gravure) (Gravure)	30-40µm rr-P3HT (Gravure) (Gravure)	40-120nm ActiveInk N2200 (N-channel), P3HT (P-channel) (Gravure) (Gravure)	Carbon blend (Inkjet) (Inkjet)	300nm PPTPA2 (Gravure) (Gravure)

Printing Based Fabrication in General

Printing techniques such as screen, offset, gravure, flexography and inkjet have been studied as early as 1994. Most of the reported literature use the top gate bottom contact structure. PVP and poly(methyl methacrylate) (PMMA) are mainly used as dielectric layers while PEDOT:PSS is used for contact electrodes. To supplement the compiled fabrication processes, the general characteristics of the printing technologies are summarised in Table 2.7.

Table 2.7: Characteristics of various printing technologies. Table adapted from [62].

	Inkjet	Screen	Flexography	Offset	Gravure
Typical Lateral Resolution (µm)	>50	>100	>30	>20	>20
Typ. layer thickness (µm)	0.3–20	3–25	0.5–8	0.5–2	0.1–5
Typ. viscosity of ink (Pa.s)	0.001–0.04	1–100	0.05–0.5	30–100	0.01–0.2
Typ. max. printing speed (m/s)	0.5	1	8	15	15

Screen and Stencil

Screen and stencil [83, pg. 298] are two very similar methods of printing. Ink is pressed through defined openings (apertures) using an image carrier (mask). The main difference is that stencil printing uses a solid mask that is in contact with the substrate during printing whereas screen printing uses a flexible mesh mask that is placed slightly elevated from the substrate which is pressed down. A squeegee is stroked across the screen or stencil mask to transfer the ink to the substrate.

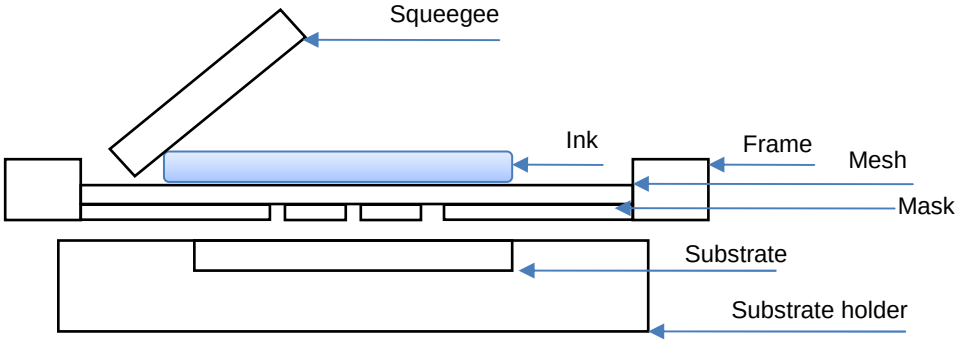


Figure 2.5: Screen Printer Setup

The first printed transistors employed stencil [96] and screen [97] printing, but were deemed as too large due to the poor resolution of such printing techniques. It must

also be noted that neither technique was used to fabricate logic circuits, but both processes were nevertheless included as a comparison between earlier and more recent printing techniques. Using stencil masks, Garnier *et al.* [96] (Table 2.5, no. 1) reported printed transistors with a lateral spacing of 200 µm between the source/drain electrodes. Better resolution of 100µm is achieved by Bao *et al.* [97] (Table 2.5, no. 2) using screen masks. The ease of obtaining and setting up screen/stencil masks is perhaps the reason why they were the earliest to be employed. However, both methods can be considered as legacy proof of concept techniques to demonstrate that functional transistors can indeed be achieved using printing. No newer literature has used either technique since, likely due to the poor resolution attainable.

Inkjet Printing

Inkjet printing [83, pg. 301] is presently the most popular printing solution for mainstream consumer use due to its low cost of ownership. However, unlike the consumer inkjet printers sold in computer stores, specialised equipment is used when jetting organic materials because a larger set of printing parameters must be taken into consideration. Industrial piezoelectric based printheads (e.g. from Dimatix-Fujifilm [102] and Xaar [103]) are typically fitted to provide higher resolution jetting and better compatibility with electronic inks. The operating principle of the printhead is quite simple; when voltage is applied to the piezoelectric transducer, the mechanical expansion and contraction of the transducer creates a compression force to the printhead chamber holding the ink. This in effect pushes the ink out via an output nozzle. Cartridges used must be chemically robust against organic solvents and usually contain ink heating functionality. Additionally, visual equipment is attached to examine print head clogging and to enable accurate manual alignment on previously jetted patterns; given that curved planes can occur when using flexible substrates [47].

The main advantage of inkjet printing is that patterns can be digitally modified, allowing quick design changes to the transistor configuration and feature sizes. However the disadvantage of the technology is that clogging of printheads can take place quickly, and may be costly to replace. In a comprehensive study by Polyera, ink-jetted films show higher surface roughness compared to mass printing technologies [100]. Resolution with inkjet printing is quite poor, with a lateral spacing of around 40µm [99]. Inkjet printing has been used by Sirringhaus *et al.* [47]

(Table 2.5, no. 3) and Minhun *et al.* [101] (Table 2.6, no. 8) to fabricate inverters and ring oscillators. In Sirringhaus' paper, vias are formed by repeatedly jetting "punch through" areas with droplets of solvent until the area is exposed [104].

Mass Printing Technologies

Among the printed techniques, gravure, offset and flexographic printing are the only types that truly break away from the non continuous laboratory based techniques. The substrate (usually a thick flexible polymer film) is passed through a series of cylinders or rollers that imprints the electronic inks onto the substrate. A high manufacturing throughput can be achieved using roll to roll printing, with literature reporting transistors printed at speeds of 0.5 – 1 m/s [6, 64].

Gravure

In gravure printing [83, pg. 300], the image patterns are engraved onto the print cylinder itself, forming recessed surfaces that hold the ink. The cylinder is partially immersed into the ink and as the print cylinder rotates, the engraved cells of the image are filled. A doctor blade wipes the excess ink from the cylinder surface. The gravure cylinder then comes in contact with the substrate, transferring the printed image with the help of the rubber impression cylinder, which pulls the ink from the engraved cells. Figure 2.6 illustrates the operation of a gravure printer.

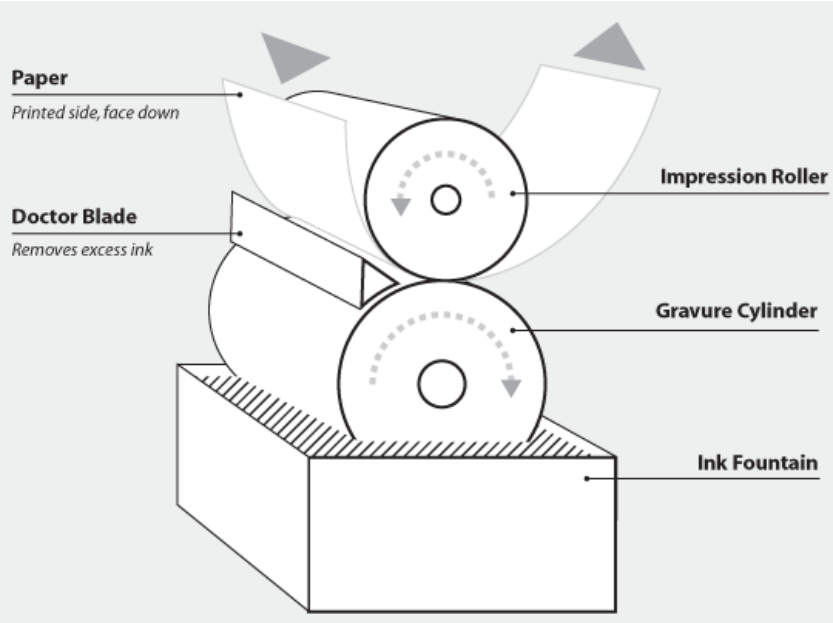


Figure 2.6: Gravure printer setup. Image by Devon International [105].

Among the mass printing technologies, gravure printing is perhaps the most compelling technique at present time, owing to the good resolution and homogeneity of gravure printed films.

Minhun *et al.* [101] (Table 2.6, no. 8) combined the use of gravure and inkjet printing to fabricate 1-bit RFID tags. Huebler *et al.* [6] (Table 2.6, no. 5) gravure printed poly(9,9-dioctylfluorene-alt-bithiophene) (F8T2) semiconducting layers, stating that the gravure technique is best used when printing low viscosity semiconductor solutions. Hambsch *et al.* [64] (Table 2.6, no. 9) printed inverters and ring oscillators solely using gravure printing, citing that the technique offers greater compatibility with organic solvents as the print cylinder is chrome plated. Yan *et al.* [100] (Table 2.6, no. 7) reported that gravure printed layers have comparable homogeneity to spin-coated layers, with RMS roughness of 4-6 nm. However, their report on the roughness data is contradicted by Hambsch *et al.* [64] and Kaihovirta *et al.* [106], where up to 100 nm peaks were observed on gravure printed films. Yan *et al.* attributes the superior film uniformity achieved by their group to the extensive optimisations of both the ink formulation and the volume of the engraved cells of their print cylinder.

Offset

In offset printing [83, pg. 299], image plates are created by lithography and etching to form ink receptive patterns on flexible plates (usually aluminium) that builds the image. The image area attracts ink and repels water, and the non-image area attracts water and repels ink. The image plates are then wrapped around plate cylinders and subsequently coated with water and ink. Ink from the image plate is transferred to a rubber blanket (another cylinder) that is in contact with the substrate and therefore does the actual printing.

The term "offset" is derived from the transfer, or offsetting, of the printed image from the plate to the rubber blanket and then to the substrate. Figure 2.7 illustrates the operation of an offset printer.

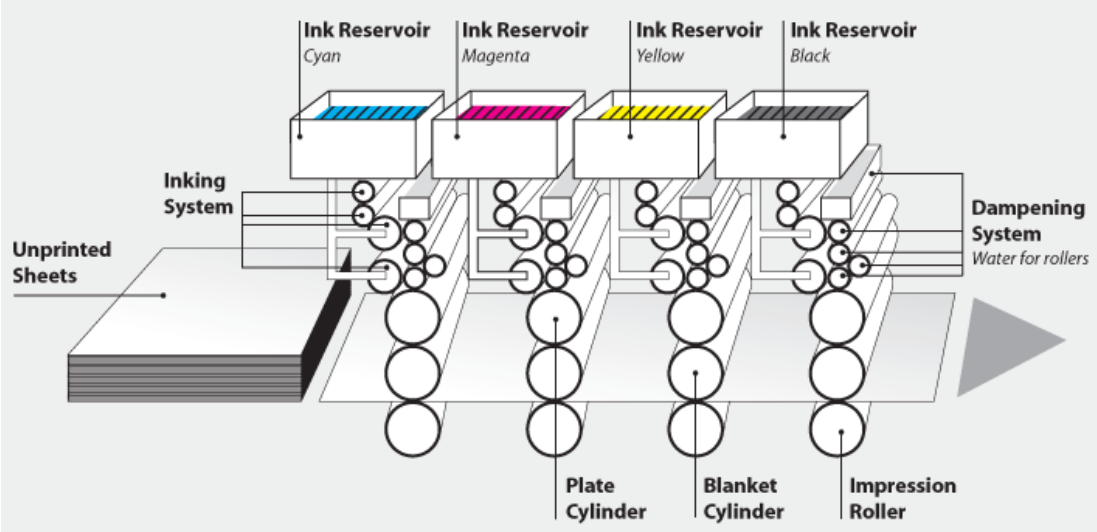


Figure 2.7: Offset printer setup. Image by Devon International [105].

The advantage of using offset is that the image patterns can be modified inexpensively without changing entire cylinders as with the case of gravure printing. Huebler *et al.* [6] (Table 2.6, no. 5) printed PEDOT:PSS source/drain contacts on polyester films and reported that highly inhomogeneous layers were attained [6]. However, a numerical roughness value was not supplemented.

Flexography

Similar to offset printing, flexographic printing [83, pg. 300] uses a rubber or other flexible material image plate that is wrapped around the print cylinder. The image plate is three dimensional, where the image to be printed is raised above the surface of the printing plate. Ink is deposited onto the raised surface of the printing plate using an engraved anilox roller with thousands of recessed cells that fill up with ink. The doctor blade controls the ink transfer to the image plate by wiping off all ink except what is held in the cells of the anilox roll. Figure 2.8 illustrates the operation of a flexographic printer.

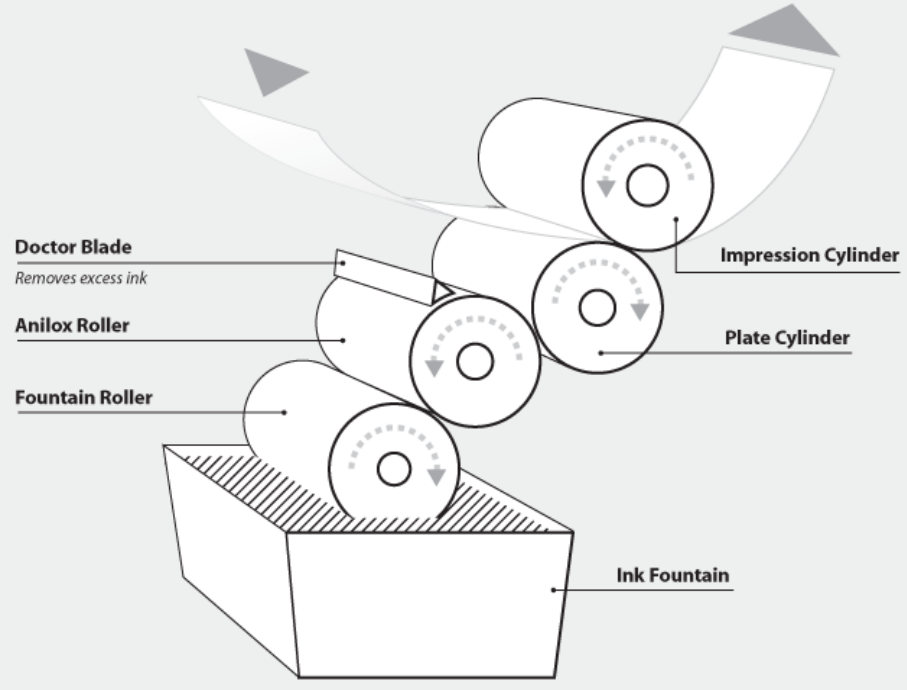


Figure 2.8: Flexographic printer setup. Image by Devon International [105].

Huebler *et al.* [6] suggested the use of flexographic printing for printing the top layers of the transistors to help prevent destruction of the underlying layers, caused by physical contact. This is because the amount of pressure applied on the substrate by the printing plate can be very small for a flexographic printer. Yan *et al.* [100] reported RMS roughness values of 8-9 nm for flexographic printed films, which is quite homogeneous compared to gravure and ink-jetted films.

2.3.2.2 Transistor Structure for Printed OFETs

Gate Electrode Placement

The top gate geometry is most used for printed devices; in contrast to the bottom gate geometry preferred for laboratory based processing. Top gate is perhaps the ideal geometry for printing due to the protection it offers to the semiconductor layer, as well as offering improved resolution control for the source/drain contacts. The semiconductor is deposited before the dielectric layer, with the gate electrode being the last material to be printed. This order of material stacking is beneficial to the semiconductor as the dielectric layer will serve as an encapsulation or passivation layer, effectively prolonging the shelf lifetime of non air stable organic semiconductors. Compared to the source/drain contacts, high resolution deposition is

less crucial for the gate electrode. Hence, it can be printed last on a stacked surface with higher surface roughness, as long as the gate electrode is correctly aligned and sufficiently covers the conducting channel.

Source Drain Electrode Placement

Bottom (staggered relative to a top gate structure) contact is generally used. Printing of the source/drain electrodes on the initially smooth substrate surface allows for better control of the lateral resolution between electrodes [28, 47, 65, 100, 107]. Studies by Street *et al.* [80] and Hill *et al.* [108] found that the contact resistance is approximately 2 orders magnitude lower for devices with staggered contacts. This is due to the larger contact area at the interface between the source/drain electrodes and the conducting channel. In the case of coplanar contacts (contacts that are on the same plane as the conducting channel), the contact area is determined by the thickness of the contacts and the channel width. Typically, the thickness of the contact layer is usually <100 nm. In contrast, the overall contact area is much larger with a staggered structure, where contact area is determined by the overlap between the gate and source/drain electrodes, which can easily be in the order of microns. Bottom contact structure also allows for substrate pre-patterning to create wells that confine spreading of inks. Sirringhaus *et al.* [47] demonstrated photolithographic pre-patterning of flexible polyimide substrates to achieve an inkjet printed resolution of 5 µm.

2.3.2.3 Materials for Printed OFETs

As expected, both the semiconductor and dielectric material choice is wider with printing technologies due to the inherent patterning advantage. For contact electrodes, the conductive polymer PEDOT:PSS as well as the inks of carbon, silver and graphite have been used. To cover all of the used semiconducting materials will be beyond the scope of this section therefore only a select few semiconductors will be discussed on the merits of performance in material stability and mobility.

Poly (3-hexylthiophene) (P3HT) is a very popular amorphous semiconductor for p-channel transistor operation, with a typical peak mobility of 0.1 cm^2/Vs. The stability characteristics of P3HT are poor, with the highest mobilities achieved under inert gas chamber environments. Without encapsulation, the P3HT has been reported to behave more like a conductor after 10 days of storage in ambient air due to atmospheric

oxygen doping [109]. Interaction between P3HT and oxygen forms a charge carrier complex that is responsible for the generation of charge carriers (increased material conductivity) [110]. A more stable p-channel semiconductor is F8T2 with a typical carrier mobility of 0.01 cm^2/Vs. Kempa *et al.* [111] reported a one order of magnitude reduction in F8T2 mobility after 1000 hours of storage in ambient air. More recently, Hambsch *et al.* [64] used poly(tri-phenyl-amine) (PTPA) to fabricate fully gravure printed circuits, achieving only a low mobility of $5x10^{-4}$ cm^2/Vs. However, PTPA has a much higher ambient and luminance stability than F8T2, with only a small reduction in mobility even after 8000 hours of storage [111].

For n-channel semiconductors, Polyera developed a soluble semiconductor material that is ambient stable, poly{[N,N'-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene)}, abbreviated as P(NDI2OD-T2). This material is commercially named as ActivInk N2200 [100]. The stability study of this material showed no change in mobility and off-currents after 10 weeks of storage under ambient conditions. However a shift in turn on voltage from 2.5 V to 4.5 V was observed [100].

With respect to dielectric materials, the polymer PMMA is used in almost all reported literature. PMMA has a permittivity of approximately 3.5 [112], and exhibits decent leakage characteristics (~10^{-6} A/cm^2 at 20 V for PMMA that is 2 μm thick [113]). Multi layer dielectric of (relatively low-k) PMMA and (high-k) barium titanium oxide (BaTiO) has been used to reduce the operating voltages of printed transistors [6]. One particularly interesting report is the HIFET transistor structure [99, 114], which uses a hygroscopic dielectric to significantly reduce the operating voltage of printed transistors. Hygroscopic PVP is used as the dielectric with resulting transistors functioning at 1.5 V (source drain voltage), in contrast to the >40 V typically needed for printed devices. However, the finding is rather questionable despite the proposed theory of improved drain currents due to the moisturised gate dielectrics by the authors. Instead, the increased drain current is likely due to the increased conductivity of the dielectric-semiconductor interface, which is in agreement with the reported high off-currents and low on-off ratios. Sirringhaus *et al.* [47] also used PVP which was ink-jetted to a similar transistor structure, but did not report this reduced supply voltage requirement phenomenon.

2.4 Simulation Techniques

As with any logic circuit design, circuit simulation is very useful to predict the behaviour of a particular circuit configuration, especially when investigating a new circuit design. Using circuit simulators, circuit designers are able to optimise feature sizes (channel width and length) of the individual transistors.

The modelling work done by Necliudov and Shur [115] found the characteristics of OFETs are quite similar to those of hydrogenated amorphous silicon (a:Si:H). Their work employed the use of the a:Si:H model (level 15) that is provided by the AIM-Spice [116] simulator. In order to use the transistor model, a set of fitting parameters must be extracted experimentally from measured transistor curves. This can be done using the equations provided by the model, or by using a supplementary tool (AIM-Extract) provided by the programmers of AIM-Spice.

The AIM-Extract [117] tool attempts to automatically extract the fitting parameters when a set of transfer and output characteristics are loaded into the program but it suffers from two limitations. Independent extraction cannot be done because extraction of certain parameters requires previously assumed values. Secondly, extraction of the knee shape parameter (M) is not precise as it must be done manually via curve fitting, the accuracy of which is determined visually by the user [118]. For that purpose, Estrada *et al.* [119] proposed their Unified Model and Parameter Extraction method (UMEM) that can automatically extract the fitting parameters mathematically using integration of the transistor curves. Yaghmazadeh *et al.* [120] used the UMEM method along with additional curve fitting using Agilent Technologies' Integrated Circuit Characterization and Analysis Program (ICCAP) and found that the relative error between the simulated and measured transistors characteristics are on average about 6%. A slightly different approach is adopted by Bartzsch *et al.* [107], by first extracting some of the fitting parameters with a combination of standard transistor equations and subsequently using AIM-Extract for curve fitting.

In addition to AIM-Spice, ATLAS is a commercial software developed by Silvaco that is capable of simulating organic transistor characteristics. However, no details of the use of ATLAS have been found in literature. In short, several steps are needed

leading to the simulation of organic transistors. A transistor is first fabricated and then measured to obtain its output and transfer curves. Next, a process referred to as parameter extraction is used to obtain numerical fitting parameters for the transistor model. A circuit simulator (AIM-Spice) can then be used to define the netlist of the transistors and produce simulated output behaviour. Figure 2.9 shows the design cycle of organic logic circuits.

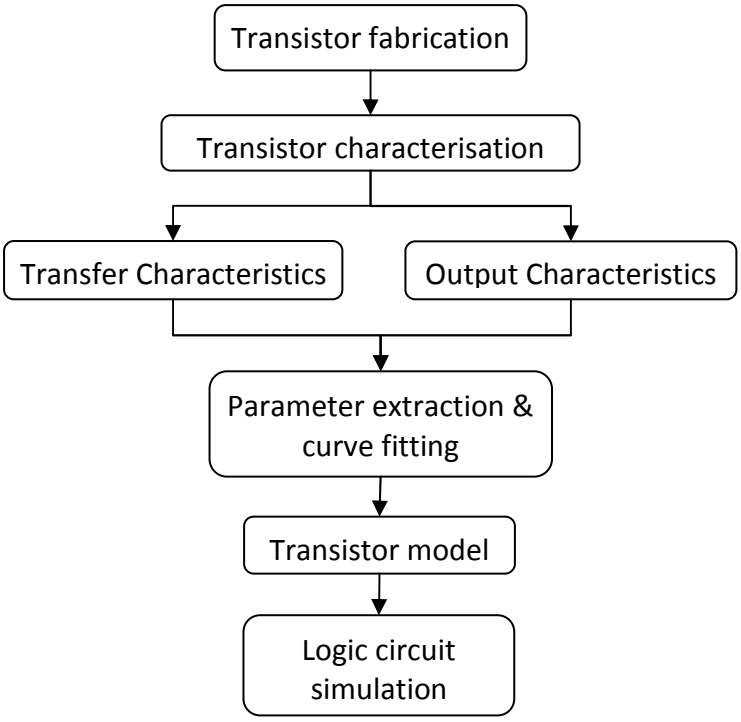


Figure 2.9: Organic logic circuit design cycle.

2.5 Discussion and Summary

Compared to silicon technology where the fabrication processes are well established and applications are diverse, organic devices are still in their early development stages. Research efforts concentrate on the fabrication processes for organic logic circuits, which is complicated by the delicate nature of the organic electronic materials. There are two major streams of fabrication, laboratory based and printing based.

Laboratory Based Fabrication

The progress in the fabrication of logic circuits is in a complex situation at the present state of organic technology. The use of conventional or laboratory based processing is still prevalent, which is a contrast to how organic electronics is envisioned to be, i.e printed electronics. The non continuous processing of laboratory based techniques is costly and time consuming, typically employing the use of photolithography and/or shadow masks for patterning deposited films. There is however a merit to the non continuous processing, in that many optimisations and performance enhancing techniques can be applied; such as surface modification of dielectrics or contact electrodes, and high temperature treatments (e.g. annealing of semiconductor films). One example is the work by Philips [41], where they employed spin-coating of a precursor solution that is thermally converted to pentacene instead of directly spin-coating soluble pentacene itself. Despite a less straight forward deposition process, this allowed Philips to control the threshold voltage of the transistors by altering the precursor formulation. Successful control of the threshold voltage enabled Philips to fabricate logic blocks such as the NAND gate and D flip-flops, which became the basic building block for their sophisticated RFID transponder tag [41].

Between using shadow mask and photolithography, photolithography is by far the better method for fabricating logic circuits owing to its superior resolution and achievable circuit complexity. Polymer Vision's BGBC and dual gate OFET fabricated lithographically is the most prominent process to date [40, 41, 79]. Their transistor stack uses PVP as the gate dielectric and pentacene as the active semiconducting layer. Reported transistor characteristics are impressive, with mobilities in the range of 0.01 to 0.1 cm^2/Vs, tuneable V_{th} and an on-off ratio $>10^6$. Their process has been used to fabricate the two most sophisticated organic devices to

date, the 128-bit RFID transponder tag (1286 transistors) [50] and the 8-bit microprocessor (4000 transistors) [49]. It is to be noted, however, that the state of the art organic devices are still quite primitive compared to silicon technology. In the case of organic RFID transponders, the basic functionality of exchanging information wirelessly has been successfully demonstrated. However, the tags do not implement standard RFID protocols nor contain programmable storage (memory).

The main disadvantage with using photolithography to pattern devices is that it requires chemically robust organic materials capable of withstanding the solvents used in the processing. This limits the choice of dielectric and semiconductor materials that can be used as well as the sequence of material deposition. So far, only cross-linked PVP and parylene have been reported for use as polymeric dielectrics when photolithographic based patterning is employed.

Printing Based Fabrication

On the other hand, there are the research groups working on printed OFETs that take advantage of the solution processable nature of organic materials. The main advantage of printing is that it is additive, so the patterning of the organic materials is automatically done. Stack integrity of the printed transistors are primarily governed by the careful selection of solvents; although other factors such as physical contact of the transistors with the print medium must also be considered in the case of mass printing technologies. Printed transistors typically use the TGBC geometry which provides natural encapsulation for the semiconducting layer, as well as improved charge injection from the staggered source/drain electrodes into the conducting channel. As opposed to laboratory based processing which has been used to fabricate sophisticated organic circuits, studies on printing based fabrication are more focused on the results of a particular deposition technique. Research is orientated towards improving the quality of printed electronic inks, since uniform thin films contribute to higher performance devices. Many printing techniques have been successfully used, such as inkjet, flexography, offset, gravure and screen printing. Among the possible printing solutions, gravure printing looks to be the most promising, excelling in terms of printing resolution, minimum layer thickness and printing speed. Nonetheless, high quality printed films are still usually several microns thick; significantly thicker compared to what is achievable with spin-coating.

The concept of the printed electronics research direction is less straight forward, as most of the reported literature employ the combination of printing and laboratory based processing. This means that at least one non continuous or non printing step is present in the fabrication process. In fact, only two research groups have successfully mass printed all polymer logic circuits, those which are the work by Hambsch *et al.* [64] and Huebler *et al.* [6]. Both reported the successful fabrication of inverters and ring oscillators (oscillating frequency <4 Hz), which pales in comparison to what can be achieved using laboratory based processing. It goes without saying that printing high performance organic circuits using mass printing technologies for roll to roll manufacturing is extremely challenging, evident by the small amount of literature on the subject. Also, the initial investment for industrial mass printers can be very costly. Fortunately, cheaper and smaller laboratory scale equipment for research such as the Mini-Labo printer [121] and the Dimatix Materials Printer [102] can be purchased commercially.

Materials

For the active layers, "benchmark" p-channel semiconductors such as pentacene, P3HT and F8T2 are mainly used. As a result, most reported logic configurations such as the inverter, ring oscillator and NAND gate are based on p-channel logic. The lack of n-channel devices is a result of the poor air and water stability of the organic semiconductors with electron transport affinity [122]. Nonetheless, there are several methods in which n-channel logic can be achieved. The first method is to use low work function metal contacts such as calcium that is aligned to the LUMO level of "p-channel" semiconductors. The second method is to develop semiconductors with LUMO levels that are aligned with high work function, air stable contacts such as gold and aluminium [6, 52]. The issue with the first and second method is that many semiconductors still exhibit electron trapping characteristics even with properly aligned energy levels between the contact electrode and semiconductor. The final and more recent method is the use of hydroxyl-free dielectrics that can bring out ambipolar semiconducting characteristics in certain material configurations [123]. Despite the challenges with n-channel semiconductors, several groups have reported the fabrication of circuits employing complementary logic. Klauk *et al.* [52] fabricated ring oscillators using $F_{16}CuPc$ for the n-channel transistors and Yan *et al.*

[100] demonstrated a new n-channel material (Polyera ActivInk N2200) that is relatively air stable.

Other high performance semiconductors have been also identified. Recently a high performance soluble polycrystalline semiconductor poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3, 2-*b*]thiophene (PBTTT) has been developed [42]. PBTTT performs well when grown on popular polymer dielectrics such as PMMA and PVP [43, 124], achieving mobilities up to 0.6 cm^2/Vs. Ambient stability of PBTTT devices however is quite poor, with two orders magnitude reduction in mobility after 5 days in storage [42]. Graphene is the latest super star in the field of semiconductors, owing to its very high charge carrier mobilities that far surpasses silicon. The use of graphene as an active layer was first reported by Novoselov *et al.* [125] in 2004. In his work, graphene films that are just a few atomic layers thick have been reported to achieve mobilities up to 10,000 cm^2/Vs. The research team at IBM reported the successful fabrication of 100 GHz field effect transistors using single atomic layer of grapheme [126]. However, the absence of a band gap in the material results in transistors that cannot be turned off easily. Therefore, graphene transistors exhibit very low on-off ratios, approximately 2000 in a recent publication also by IBM [127].

Materials research is still the key to realising stable organic devices that are ready for commercial use. The stability over performance preference has been observed. Hambsch *et al.* [64] opted to use lower performance PTPA over F8T2 for its much improved air stability and Klauk *et al.* [66] studied the use of di(phenylvinyl)anthracene (DPVAnt) over the more conventional pentacene, suggesting that research groups have begun to favour the importance of stable devices. Encapsulation layers have been used to prolong the lifetime of the materials, but this does not address the cycle lifetime stability. The detrimental outcome of the instability of the semiconductor can be better understood by observing the case for a basic inverter logic consisting of an active (always on) load transistor and a driver transistor. The reduction in mobility due to storage or device cycling lowers the turn on current for both the load and driver transistors. With the decreased distinction between the on and off states, the driver transistor will not have sufficient drive current to create a strong signal inversion, reducing the gain of the inverter.

3 Design

3.1 Introduction

This chapter describes the preparation and design aspects for the fabrication of organic logic circuits. The first design task relates to the sensor system for the PET project's liquid crystal temperature sensor. The method of interrogating the temperature sensor using silicon electronics is presented. An assessment is then made of the possibility of an equivalent organic system, which is used to establish the scope of study. The second design task relates to the selection of a suitable fabrication process and transistor structure for the organic circuits. Finally, the design of the transistor's geometry, logic circuit configurations and a photomask is discussed.

3.1.1 Using Liquid Crystals to Measure Temperature

This section gives some background to the temperature sensor investigated by the Physics and Chemistry group for the PET project as introductory material to the silicon sensor system design. Parts of this section are adapted from the EEE group's PET project report [128]. The temperature sensor is essentially a parallel plate capacitor filled with a ferroelectric liquid crystal (Kingston FLC10) material as the dielectric layer. The liquid crystal is thermotropic, where its molecular orientation (phases) changes under different applied temperatures, as shown in Figure 3.1.

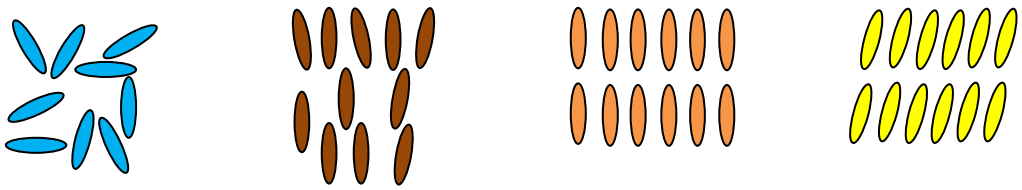


Figure 3.1: Orientation of the liquid crystal molecules in various phases [129].

Liquid crystals with a so called "ferroelectric" phase (chiral Smectic C, or SmC*) exhibit a significant change in their electrical properties between phases [130]. In the case of the Kingston FLC10 liquid crystal, changes in the electrical permittivity and conductance were observed over a range of frequencies from a few Hz up to ~100 kHz. The typical permittivity and conductance graphs for a 25 mm^2, 4.47 µm spaced sensor have been provided by Dr. Sarabjot Kaur [11] from SoPA and are shown in Figure 3.2 and Figure 3.3.

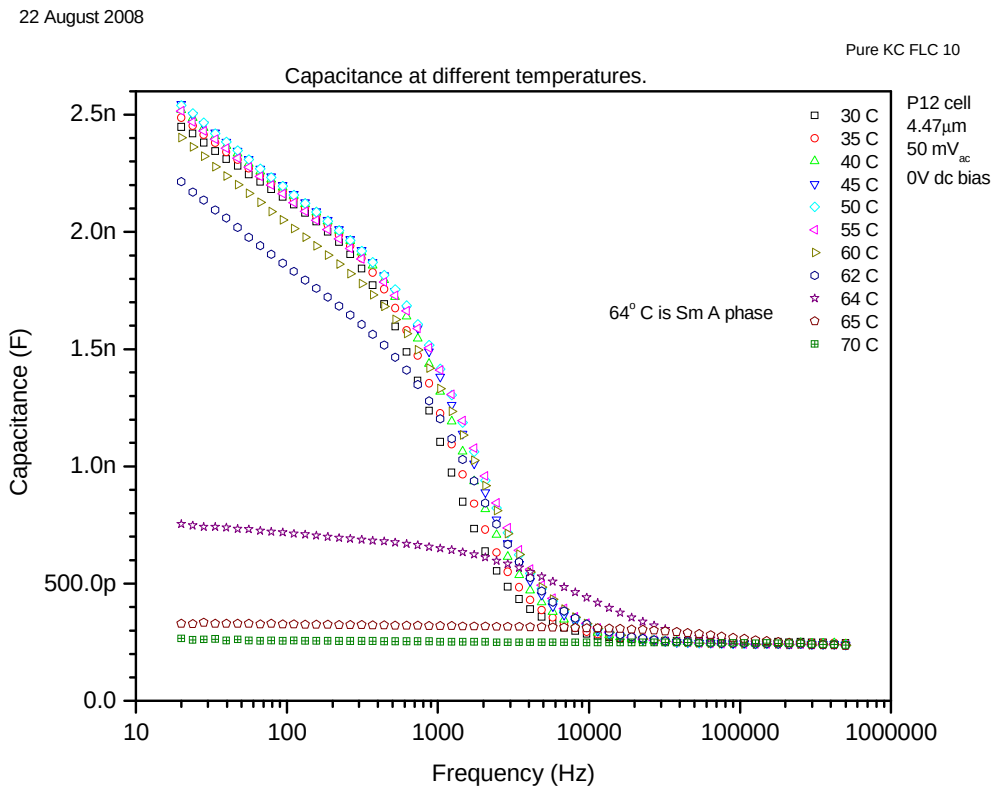


Figure 3.2: Variation in cell capacitance with frequency at various temperatures.

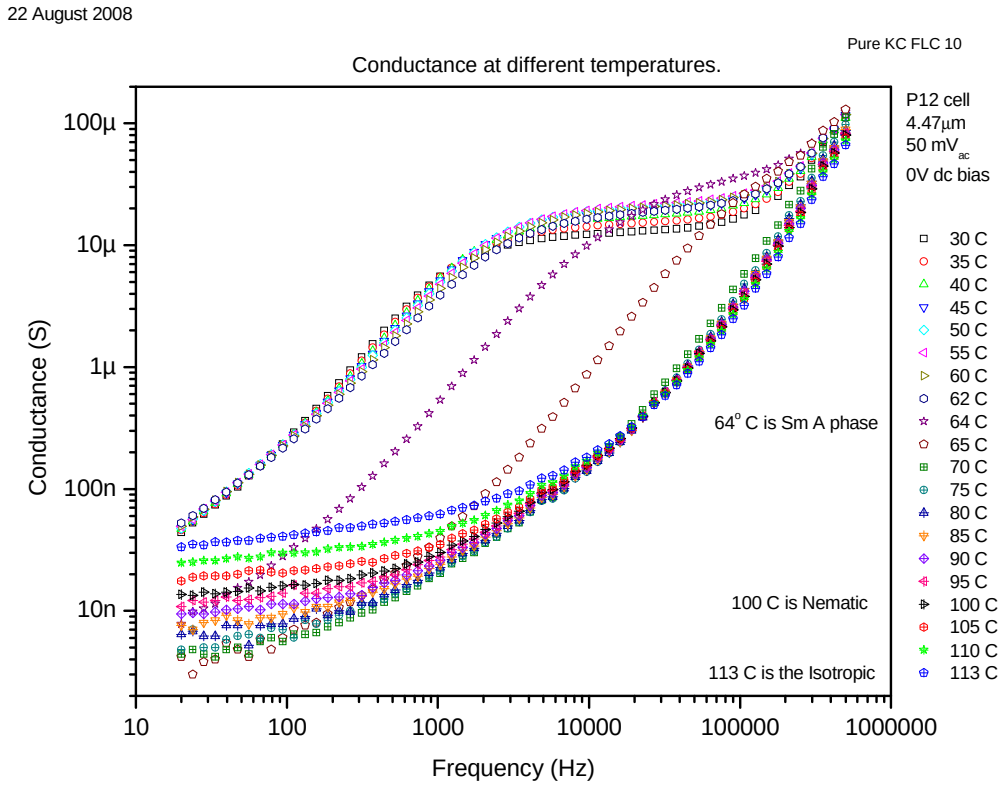


Figure 3.3: Variation in cell conductance with frequency at various temperatures.

The sensor can be considered to be a resistor in parallel with a capacitor, each of which has a frequency and temperature response as shown by the graphs. The phase transition where the liquid crystal changes from the SmC* to the SmA phase for the Kingston FLC10 material is around 64ºC. Effectively, a switch effect is obtained at the phase transition point. When probing the sensor, it would be desirable to operate at a frequency where the electrical properties of the dielectric experience the largest changes. From the two graphs, it is clear that the best area of overlap for this material is in the region from about 200 to 1000 Hz. The most significant effect is the change in conductance which is about two orders of magnitude in the region of interest, whereas the change in capacitance is about 4 to 5 times.

In this work, it was found that the temperature information can be obtained even in the simplified case where the sensor is a purely capacitive device. When the sensor is heated above the phase transition temperature, say 66ºC (SmA phase), capacitance changes by a factor of 5 compared to the initial value in SmC* phase. This change in capacitance forms the basis of a temperature measurement if a suitable measurement technique is applied to allow sufficient differentiation between the phases, e.g. a capacitance measurement circuit. Compared to conventional capacitance measurement however, extraction of actual capacitance values derived from the output of the sensing circuitry are not necessary. The detection strategy would simply rely on the circuit's output to be in the form of two distinct voltage levels that reflect the respective phases of the liquid crystal at the time of measurement.

To address the sensing methodology, standard capacitance measurement circuits were initially considered. The potential use of AC circuits such as the capacitance voltage divider and resonant circuit, as well as DC excitation type circuits such as the RC circuit is reported in Appendix A. However, it was also clear that an elaborate capacitance measurement circuit may not necessarily be able to detect the changes in liquid crystal phases, since the sensor had rather complex capacitance and conductance characteristics. Therefore, a more pragmatic approach was adopted by conducting sensor characterisation tests to determine the simplest circuit configuration that could be employed. The sensor characterisation experiment is discussed in the next sub-section.

3.1.1.1 RC Circuit for Sensing Liquid Crystal Phases

Figure 3.4 shows the RC time constant circuit setup used for characterising the sensor. The sensor is represented as a capacitor in the figure, with a 1 MΩ resistor connected in series with the sensor. The voltage across the sensor is measured using a Tektronix TDS2004B Digital Storage Oscilloscope. A Tektronix AFG3021B Arbitrary Function Generator (AFG) has been used to provide a signal source with variable frequency, voltage, and signal type.

In this experiment, a pulse signal is applied and the voltage response of the sensor is recorded. The experiment started at room temperature where the liquid crystal is in SmC* phase. The temperature of the sensor is then increased and measurements are taken at multiple temperature steps just before and after the SmC* to SmA phase transition temperature. Sensor heating is done by placing the sensor on a 15 Ω high power resistor (Tyco HSC100 15R J) connected to a power supply. The voltage on the power supply was adjusted and the surface temperature of the resistor was monitored using a surface thermometer (Amprobe TPP2-C1).

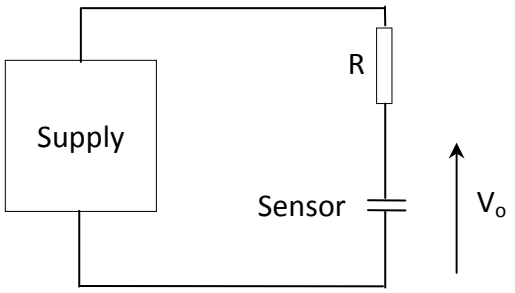


Figure 3.4: RC time constant circuit setup for sensor characterisation.

The graph of Figure 3.5 shows that the sensor's response either side of the transition temperature is very consistent in terms of the voltage levels and clearly distinguishable from each other across majority of the pulsed signal. The SmC* to SmA phase transition for this particular liquid crystal material is at 64ºC, which is seen with the steeper rise in voltage between 64ºC and 66ºC. Once the transition to SmA phase has occurred the response is very much like the charging of a pure capacitor; whereas in the SmC* phase the response shows a more gradual rise in voltage which peaks at approximately 200 mV. It was also found that the trajectory of the output signal was unchanged for pulse widths of 100 µs to 1 ms.

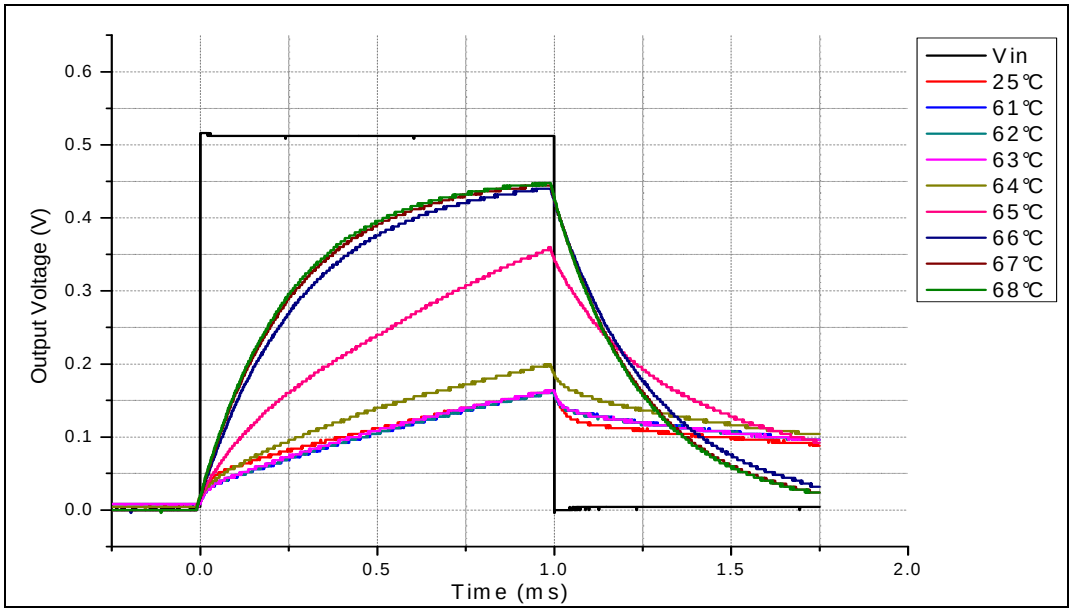


Figure 3.5: Sensor response to a 0-500 mV, 1 ms pulse at different temperatures [128].

The response of the sensor can be explained by taking into account the contributions from its conductance properties as shown in figure 3.3. In the SmA phase (>64ºC), the low capacitance and the low parallel conductance of the sensor ($\frac{1}{G} \gg R$) result in a similar response to that of a conventional RC circuit.

A more complex behaviour occurs when the sensor is in the SmC* phase (<64ºC), where the effects of conductance are apparent for a brief moment after the rising and falling edges of the charging pulse. Due to the rotation of the dipoles, the sensor's conductance values are relatively high (>100 μS) for times below 0.1 ms. During this time, the sensor's parallel resistor acts as a potential divider with series resistor R, resulting in a lower voltage potential across the capacitor, as well as a shorter time constant for the charging/discharging process. For the charging response, the consequence is an initial fast rise to a low value in the output voltage, followed by a more gradual increase in voltage. The gradual increase is because the sensor's conductance returns to a low value (<50 nS) at the end of the dipole rotation. At this point, the parallel resistance is much greater than the series resistance ($\frac{1}{G} \gg R$), so the output voltage aims for a new, higher value but with a longer time constant. This behaviour is also seen in the dipole relaxation stage, where there is a rapid drop in output voltage for a brief moment after the falling edge of the pulsed signal, followed by a more gradual discharge. The time constant of the circuit is given by (3.1), with

the effective resistance determined by converting the two resistors into its Thevenin equivalent circuit.

$$\tau = R_{eff}C = \frac{R \cdot R_c}{R+R_c}C \qquad (3.1)$$

The result of this sensor characterisation test is very positive, as the simple RC circuit is capable of delivering distinct voltage output levels that are representative of the liquid crystal phases. From the voltage response, two detection methods are applicable:-

1. Digital readout based on the output voltage being above or below a reference threshold at a fixed sampling time after the step voltage has been applied. The sampling time is appropriately set where the magnitude of the difference in voltage across the sensor in the SmC* and SmA phases is large, e.g. at the 0.75 ms point. The sensor's voltage output in SmA phase would be considered as a binary high and vice versa for the sensor in SmC* phase.
2. Time readout based on the time it takes for the output voltage to exceed a reference threshold. The time taken for the sensor in the SmA phase to charge up to the reference point, e.g. 0.1 V, will be shorter than when it is in the SmC* phase.

In the initial stages of the PET project, method 1 was selected as the sensing method of choice but method 2 was later adopted when the Chemistry group reported difficulties in locking in (polymerisation) the SmA phase. Dr. Sarabjot Kaur discovered that useful temperature information can be obtained when the device operated entirely under the SmC* phase [11], which prompted the change in the way the sensor was probed. However, an updated organic system was not pursued due to the loose coupling with the main PET project and the fact that the sensing method is not crucial in supporting the aims of this research. This will be discussed later in the following sections.

3.1.2 Silicon System Design

Having demonstrated the basis of the temperature sensing mechanism, this section discusses how a single unit of the sensor fits into the temperature measurement system as a whole using passive RFID technology. Figure 3.6 shows a high level block diagram of such a measurement system.

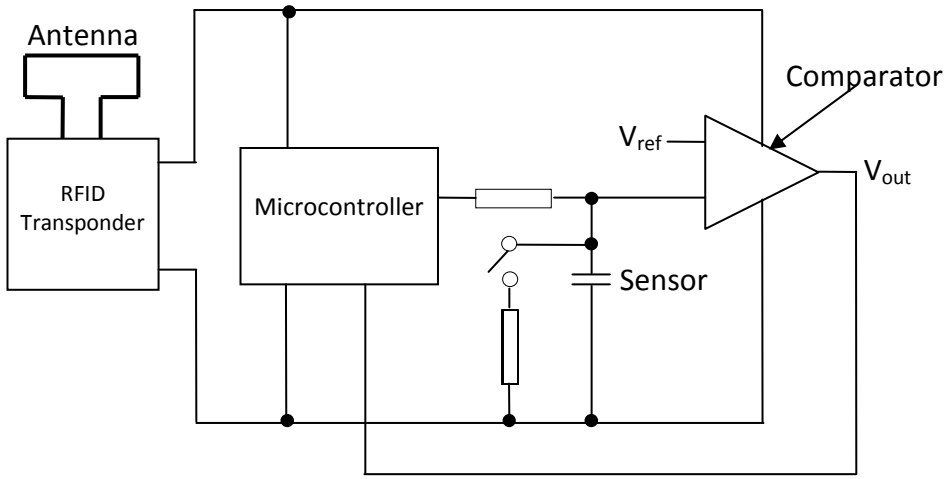


Figure 3.6: Block diagram of the RFID Sensor tag. Figure adapted from [128].

In operation, the RFID sensor tag is energised by harvesting the energy from a tag reader that is within its proximity. Both the RFID chip and the microcontroller are powered up and the sensor is interrogated. A sensor array can be designed to obtain both a temperature and time scale. The arrangement of such an array, formed from single sensor units, is supplemented in Appendix B. For each cell of the sensor array, the microcontroller first discharges the sensor by closing the switch to a resistor that is connected in parallel with the sensor. The discharge switch is opened and a pulse signal is subsequently applied to charge the sensor via the resistor connected in series (RC circuit setup). The comparator conditions the voltage across the sensor to give a binary type output that is fed back to the microcontroller, where the sensor's temperature is determined either using the digital or time readout as described previously.

3.2 Analysis of an Organic Sensor Circuit Equivalent

In the initial research plan, the primary objective was to construct an organic equivalent of the silicon sensor system. For that purpose, the complexity of the electronics as well as the capabilities of the organic fabrication technology within the EEE was considered. The state of the fabrication technology had to be assessed because any implementation of the system would need to be fabricated at the transistor level to form a chip, since off the shelf discrete organic components do not currently exist. From the system in Figure 3.6, the main components of the circuit are the measurement stage (RC time constant circuit), passive RFID transponder, microcontroller, sensor and comparator. For the sensor measurement stage, it is possible to maintain the same circuit configuration by replacing the charging resistor with a transistor, as shown in Figure 3.7.

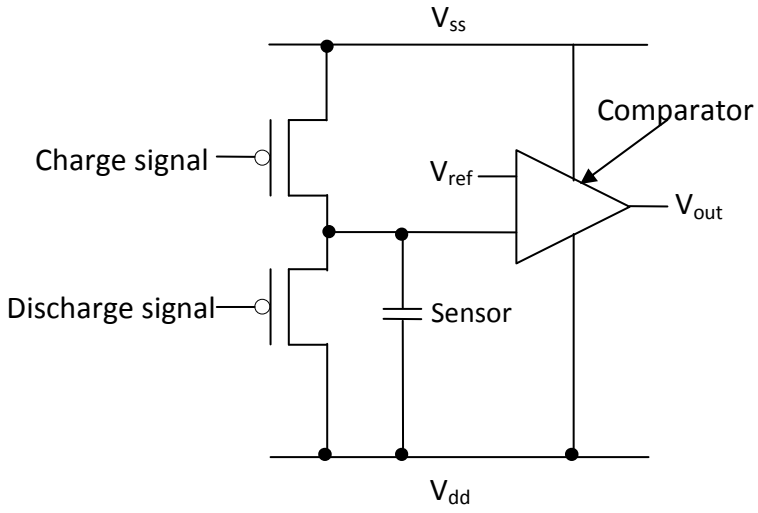


Figure 3.7: Organic capacitance measurement circuit.

To validate this circuit configuration, an experiment was conducted using discrete p-channel MOSFET (Zetex ZVP3306A). The circuit setup is shown in Figure 3.8 and the voltage response is shown in Figure 3.9. From the voltage response, it can be seen that the charging process occurs more slowly when the sensor is in SmC* phase (25 ºC), than when in SmA phase (71.5 ºC). A large voltage difference of approximately 4 V is observed between the two liquid crystal phases at the end of the 1.5 ms pulse. The experiment verifies that a simple transistor based charging circuit can be used to probe the sensor, as the equivalent circuit configuration to the RC time constant circuit (section 3.1.1).

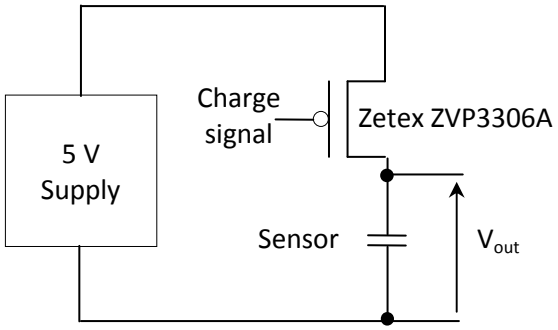


Figure 3.8: Transistor based transient time circuit using Zetex P-type MOSFET.

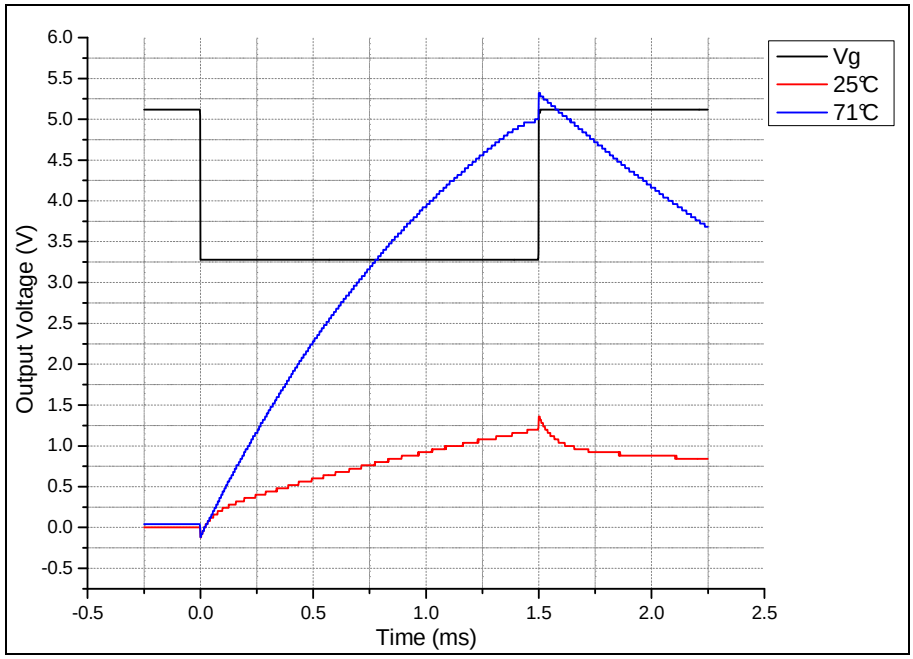


Figure 3.9: Voltage response of the sensor using the transient time circuit.

For the RFID transponder and the microcontroller for the sensor measurement system, it is clear that designing such sophisticated integrated chips from ground up cannot be accomplished given the time allocated for this research. A literature search was hence conducted, on the possibility of adapting an existing RFID chip schematic from prior art. However, the literature search was unsuccessful, as no relevant documents could be found apart from manufacturer datasheets, where only high level block diagrams of the RFID chip components are described. Although the organic RFID transponder tags [41, 50, 59] and microprocessors [49] have been demonstrated in the literature, they are proof of concept devices that are relatively basic in comparison with their silicon counterparts. Furthermore, such state of the art organic devices are only possible using highly optimised logic compatible fabrication processes. Simply having a fabrication process however, is not sufficient. The basic circuit building

blocks such as the inverter and logic gates must be successfully fabricated before attempting the design of more complex circuit configurations.

The possibility of fabricating organic circuits for this research leads to the assessment of the state of existing in-house fabrication technology. Unfortunately, no prior studies have been undertaken in the area of organic circuits within EEE. As a consequence, the methodology to design and fabricate organic circuits is not known. It became obvious that an organic implementation of the entire sensor measurement system or even a simple system cannot be realised, and that the pursuit of the original research objectives would be unfeasible. Any research of such nature within EEE was limited at the fundamental level, by the lack of a technology to manufacture the organic circuits.

3.2.1 Revised Research Focus

Since the research is intended to be in the field of organic electronics, a decision was made to address the core enabling technology for logic circuits, the fabrication process. The initial project aim to replicate an organic equivalent to the silicon system was therefore revised, to a new focus that is directed towards establishing a foundation for organic circuits research in UoM EEE. This involves the investigation of a method to fabricate transistors and circuits using solution processed materials for the transistor stack. In addition to documenting the logic capable fabrication process methodology in detail, the work in this research also documents the design of the organic circuits, such as the feature sizes of transistors, type of vias and interconnects, as well as simulation of circuits. To support the voltage output measurements of the fabricated circuits, a National Instruments LabVIEW software was used to control an Agilent Technologies' measurement mainframe (model E5270B).

3.3 A Suitable Fabrication Process

The selection of a suitable fabrication process is based on the consideration among the state of the art processes. The four most plausible fabrication processes from both the printing and laboratory based processing categories were considered.

Laboratory based:-

- Patterning using photolithography (Infineon [68], Philips - Polymer Vision [40])
- Patterning using shadow masks (Klauk *et al.* [52])

Printing based:-

- Inkjet printing (Sirringhaus *et al.* [47], Tobjörk *et al.* [99])
- Mass printing (Huebler *et al*. [6], Hambsch *et al.* [64])

For this research, the lithographic fabrication process was selected as it is the only approach that has been used to successfully fabricate complex logic circuits at high yields [40, 41, 50, 70, 73]. It is also a process that can be carried out with the existing equipment in the EEE's clean room. This includes the availability of a spin-coater, evaporator, mask aligner and oxygen plasma etcher. It was a safe decision to adapt from a process that has been reported by several groups to be practical; as the processing information available from literature significantly helps to minimise the time required to establish processing procedures.

The shadow mask patterning process using SAM dielectric was a compelling option for low voltage complementary logic circuits. However, the reported process is incomplete as circuits requiring crossovers cannot be fabricated until a method for insulating tracks is added to the process. The authors suggested the use of vapour deposited parylene for this purpose, but did not demonstrate the applicability of the additional dielectric layer. The main barrier in adopting this fabrication process is in terms of equipment required. The deposition of the active materials, pentacene and $F_{16}CuPc$, are via thermal evaporation. Such deposition cannot be conducted in EEE due to the lack of dedicated organic material evaporator units. This process also requires the alignment of the shadow masks to ensure proper stacking of deposited materials. Unfortunately, a shadow mask alignment tool is also not available in EEE. From the perspective of selecting a fabrication process with more future proof

potential, printing techniques are undoubtedly the better choice. However, there is a large investigation overhead when attempting to use non conventional methods of fabricating integrated devices. This includes investing in specialised mass printing equipment, formulation of inks and optimisation of printed films. The preparation necessary for printing is beyond the scope of this study, and carries with it a high risk that the printing process may be unsuccessful.

3.3.1 Transistor Structure, Processing and Choice of Materials

A five layer BGBC process with PVP as the gate dielectric and gold for the contacts was chosen. Figure 3.10 shows an overview of the stacking of the thin film layers, followed by justification of the choice of materials and accompanying processing techniques.

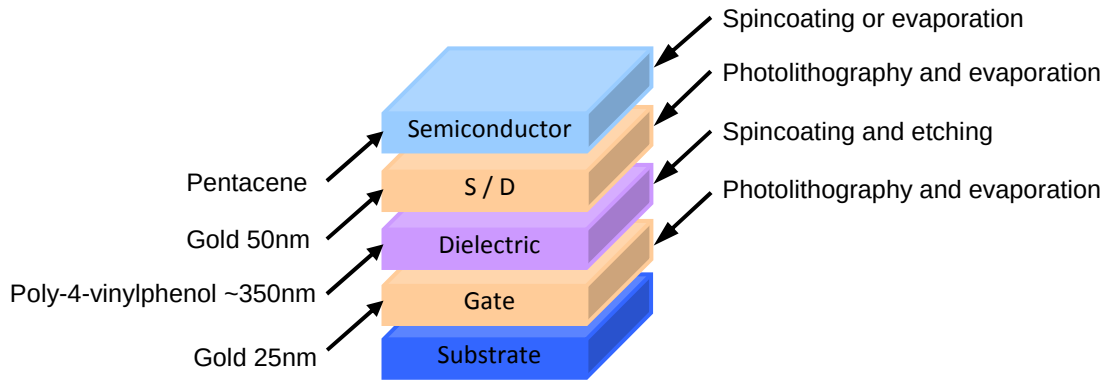


Figure 3.10: Bottom gate bottom contact transistor structure for logic circuit fabrication.

3.3.1.1 Dielectric

For the dielectric material, Al_2O_3 and PVP are the two viable options, as previously discussed in section 2.3.1.3. To address the printability aspect of the fabrication process, the polymer PVP is chosen. PVP can be patterned either by oxygen plasma etching or a photochemical process involving photo-initiated cross-linking of PVP that is followed by development of the PVP dielectric. In the former technique, the cross-linker poly(melamine-co-formaldehyde) (PMF) is mixed together with the PVP solution and deposited PVP films are thermally cross-linked at 200 °C. An etch mask is then formed on the PVP layer and PVP is etched using oxygen plasma. In the latter technique, a photoacid generator (PAG) and cross-linker are added to the PVP solution. Unfortunately, the PAG and cross-linker material combination used by

Polymer Vision was not revealed in any of their publications. Nonetheless, two reported combinations found in literature are trimethylolpropane triglycidyl ether + benzoyl peroxide + triphenylsulfonium triflate by Lee *et al.* [131] and 1,2,4,5-tetraacetoxymethylbenzene + 2,4-bis(trichloro methyl)-6-aryl-1,3,5-triazine by Hee *et al.* [132]. The spin-coated PVP film is first exposed through a photomask and illuminated with UV light (similar to a photolithography process) to induce cross-linking. Once completed, the PVP film is hardened by baking at reduced temperatures of 100 – 150 °C. Non irradiated areas of the PVP film are then removed by a developer solution. The advantage of this technique is primarily the low baking temperature, which allows compatibility with flexible polymer substrates. Also, developing PVP to pattern it is a quicker process compared to oxygen plasma etching.

Although the photo-initiated cross-linking + developing process is arguably the better method to pattern PVP, the oxygen plasma patterning method was ultimately chosen. The main reason for not using the PAG approach is specific to the mask aligner available for the cross-linking step. When levelling the wafer chuck in preparation for UV illumination, the sample must not physically be in contact with the photomask to prevent damage to the soft, non cross-linked PVP film. This requires a mask aligner with assisted proximity levelling mode, a feature that is absent from our manual mask aligner. PVP thickness is targeted at 350 nm, a thickness value that gives comparable leakage characteristics to 100 nm thermally grown SiO_2 [46, 68].

3.3.1.2 Contact Electrodes

Gold was selected as the electrode material as its deposition and patterning, using lift-off photolithography, is well established within the nanoelectronics fabrication group of EEE. Electrode thickness was set to be approximately 25-50 nm. Gold can be substituted with PEDOT:PSS for an “all polymer” transistor. However, using PEDOT:PSS results in transistors with low mobility and on-off ratio (10^2) [72]; which is over four orders of magnitude smaller than is achievable using metal contacts. The fabrication process is also significantly more complicated when using PEDOT:PSS, as etching of PVP during patterning has to be controlled so that the PEDOT:PSS gate layer is not etched away as well.

3.3.1.3 Semiconductor

For the semiconductor, the initial plan was to use evaporated pentacene to obtain high performance OFETs. Unfortunately, the clean room within EEE is not fitted with a dedicated pentacene evaporator. The evaporation of pentacene using the existing metal evaporator is not permitted due to potential contamination of the chamber. The alternative was to use the evaporator unit within the SoC, which was out of service. Maintenance work was carried out on that particular unit with Dr. Jeffrey Kettle of the SoC, but was not completed until the end of year two of this research.

In order to progress according to the research plan, TIPS-pentacene was purchased instead and deposited via solution in the interim; and was subsequently used throughout the study due to the convenience of "in-house" deposition. This allowed the samples to remain within the clean room environment until completion of fabrication, without the need to be transported between SoC and EEE.

3.3.1.4 Limitation of Fabrication Process

Despite the process' similarity to Polymer Vision's state of the art fabrication process, the selection of processing and materials introduced several limitations. The first limitation is that fabricated transistors will require moderately high biasing voltages due to the use of a relatively thick polymeric dielectric. Secondly, the 200 °C cross-linking step is incompatible with many flexible polymer substrates which have typical maximum processing temperature of 100-150 °C [2, 83, pg. 163]. Thirdly, there is no patterning step for the semiconducting layer. Such optimisation steps are initially dismissed in order to keep processing minimal to that which is absolutely necessary to fabricate logic circuits. As a result, the unpatterned semiconductor layer will place a limit on the minimum transistor feature size to maximise on-off ratios due to the higher off-currents. Therefore, wide channel width inverter circuits are also included in the photomask design. The details of the transistor channel features are discussed in section 3.4.1.3. Lastly, the fabrication process does not manipulate the semiconducting layer in any way to enable the control of transistor threshold voltages. Semiconductor materials are used as obtained from the chemical supplier, with no further modification to their chemical properties.

3.4 Logic Circuit Configuration and Geometry

This section details the transistor configurations for the organic circuits investigated in this work; the inverter and comparator circuit. It is to be noted that the circuits have been designed to use p-channel logic only, following the use of the five layer BGBC fabrication process. Transistor orientation is maintained in all presented figures where the source electrodes are on the top and vice versa for the drain electrodes.

3.4.1 Inverters

The inverter circuit was included in the photomask because it is a simple logic circuit that can be used to validate the fabrication process. A typical inverter configuration consists of two transistors and requires only one via and one interconnect. Two configurations were investigated, the diode-load and the zero-V_{gs} inverter. Several characteristics are desirable for an inverter circuit, such as a large separation between the stable logic high (V_{OH}) and logic low (V_{OL}) output voltage levels, large noise margin as well as large inverter gain. A large inverter gain ensures that the binary logic is immediately reversed at the switching point. The inverter gain is calculated by the division of the differential output voltage with the differential input voltage. Maximum gain is usually obtained at the mid section of the inverting slope. Large separation of logic levels V_{OH} and V_{OL} allows for maximising of the noise margins when connecting the output of a particular inverter to subsequent stages of the circuit in a practical device. Noise margin can also be improved by controlling the trip point, which is defined as the point where V_{in}=V_{out}. Ideally, the trip point lies in a symmetrical position (V_{in} = V_{dd}/2, V_{out} = V_{dd}/2) in the input output characteristics of the inverter, as shown in Figure 3.11.

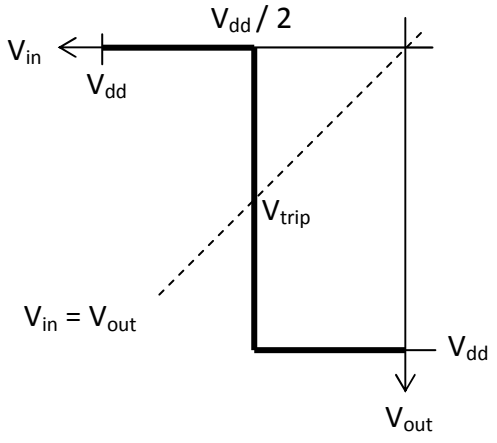


Figure 3.11: Characteristics of an ideal inverter.

3.4.1.1 Zero-V_{gs} Inverter

In a zero-V_{gs} inverter configuration (Figure 3.12), the channel width of the load transistor is R_w times wider than the driver transistor. The load transistor is always biased off by connecting the gate and source electrodes together. When V_{in} is high ($V_{in} = V_{ss}$), both driver and load transistors are switched off with $V_{gs} = 0$ V. Since current flowing through both transistors is equal, the V_{ds} for the load transistor decreases because the load transistor can supply a higher current than the driver transistor due to the larger channel width. Therefore, output voltage is pulled down towards V_{dd}. The logic low voltage is governed by the ratio of the transistor channel widths (R_w).

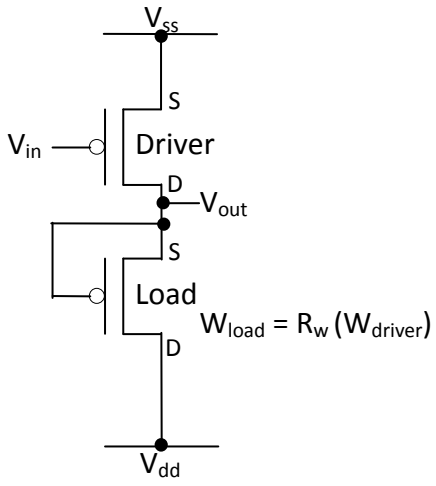


Figure 3.12: Transistor configuration of the zero-V_{gs} inverter [133].

When V_{in} is low ($V_{in} = V_{dd}$), the driver transistor switches on and becomes the lower resistance path, pulling output voltage towards V_{ss}. To maximise the separation between the logic levels, the channel width ratio must be large enough so that the distance between the low and high logic levels is close to the magnitude of the applied voltage. However, if the load transistor is made excessively wide, its low resistance will lower the gain of the overall device when the driver transistor is in the on state. Philips reported that a channel width ratio of 8-10 is optimal [41, 133], with such ratios achieving inverter gains of approximately 11 [83, pg. 337].

One notable characteristic of the zero-V_{gs} configuration is the highly asymmetric trip point position, which is usually reached when V_{gs} is just slightly negative. In order to have sufficient load pull down to V_{dd} when $V_{gs} = 0$ V, it is desirable to have a slightly positive threshold. On the other hand, the positive V_{th} causes the driver transistor to be

rapidly switched on when V_{gs} is lowered with the application of a small negative V_{in}, resulting in the asymmetry of the trip point. It is therefore difficult to tune this inverter configuration to maximise noise margins when using a fabrication process with only one V_{th}. The maximum theoretical gain of this inverter configuration has been previously approximated by Cantatore and Meijer [133], using (3.2).

$$A_{max} = \frac{(V_{dsL} - V_{dsH})}{R_w} \times \frac{\frac{\partial I_d}{\partial V_{gs}}|_{V_{gs}=0,\ V_{ds}=V_{dsH}}}{I_d\,|_{V_{gs}=0,\ V_{ds}=V_{dsH}} - I_d\,|_{V_{gs}=0, V_{ds}=V_{dsL}}} \qquad (3.2)$$

where V_{dsH} is a large negative V_{ds} and V_{dsL} is a small negative V_{ds}.

3.4.1.2 Diode-Load Inverter

For this inverter configuration (Figure 3.13), a short channel width transistor is used as a load. The term diode load refers to a transistor where its drain and gate electrodes are interconnected; hence, the load transistor is always biased on. When V_{in} is high (V_{in} = V_{ss}), the driver transistor is biased off and becomes a high resistance path compared to the load transistor. Output voltage is pulled down towards V_{dd}. Conversely, when V_{in} is low (V_{in} = V_{dd}), the driver transistor switches on strongly due to its longer channel width. The driver transistor is now a low resistance path compared to the load transistor, hence output voltage is pulled up towards V_{ss}.

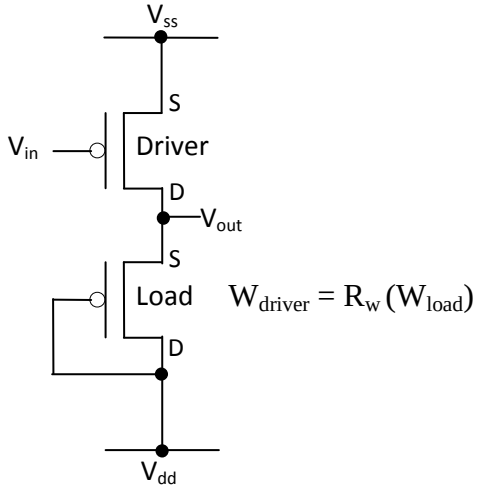


Figure 3.13: Transistor configuration for the diode-load inverter [133].

Compared to the zero-V_{gs} configuration, the diode-load inverter gives a more gradual switching slope (lower gain) and consumes more power as the load transistor is always switched on. However, the diode-load inverter switches faster due to larger

pull down current, at the expense of higher idle power consumption. Philips reported a one order of magnitude faster response with this inverter configuration than the zero-V_{gs} inverter [133]. They also reported average gain values of 2.3 [83, pg. 339]. The maximum theoretical gain however, can be calculated using (3.3) [133]. The derivation for the gain equation is provided in Appendix H.

$$A_{max} = \frac{g_{m\,driver}}{g_{m\,load}} = \frac{\sqrt{2I_D \mu_n C_{ox} \frac{W_{driver}}{L_{driver}}}}{\sqrt{2I_D \mu_n C_{ox} \frac{W_{load}}{L_{load}}}} = \sqrt{\frac{W_{driver} L_{load}}{W_{load} L_{driver}}} \qquad (3.3)$$

3.4.1.3 Geometric Configuration

In this research, two sets of geometric sizes were used for both inverter configurations. The large inverter set uses a maximum size of 1 mm for the channel width, while the small inverters have a maximum channel width of 0.16 mm. The use of different geometric sizes is mainly to account for the unpatterned semiconductor layer. For all inverter circuits, a ratio of 8 was maintained for the load and driver transistor channel widths ($R_w = 8$).

3.4.2 Comparator

The comparator circuit is adapted from the work by Nicolas Gay [73]. Gay's single ended differential amplifier design was modified to include a binary output (inverter) to form a simple comparator circuit. An internally supplied voltage bias section was also removed, to allow for manual biasing so that the reference voltage to the comparator can be varied. The resulting circuit is shown in Figure 3.14.

Transistor M1 serves as a manual bias to the differential section (M2 – M5) of the circuit. Depending on the input voltages at M2 and M3, transistor M1 is biased so that the common voltage point to M2 and M3 is slightly higher than the respective input voltages V_{in} and V_{ref}. This ensures that transistors M2 and M3 are not permanently in saturation, so that there is gate voltage dependence for their respective drain currents. Transistor M3 is biased with the reference voltage (V_{ref}) to be compared. Transistor pairs M2, M4 and M3, M5 form the differential section which is essentially an inverter with transistors M4 and M5 connected as diode loads. The output of the differential section is buffered with source follower transistors M6 and M7. The

source follower transistors connect to a current mirror that combines the differential voltages to a single voltage output. The combined voltage biases a diode-load inverter (M10 and M11) that produces the binary type output.

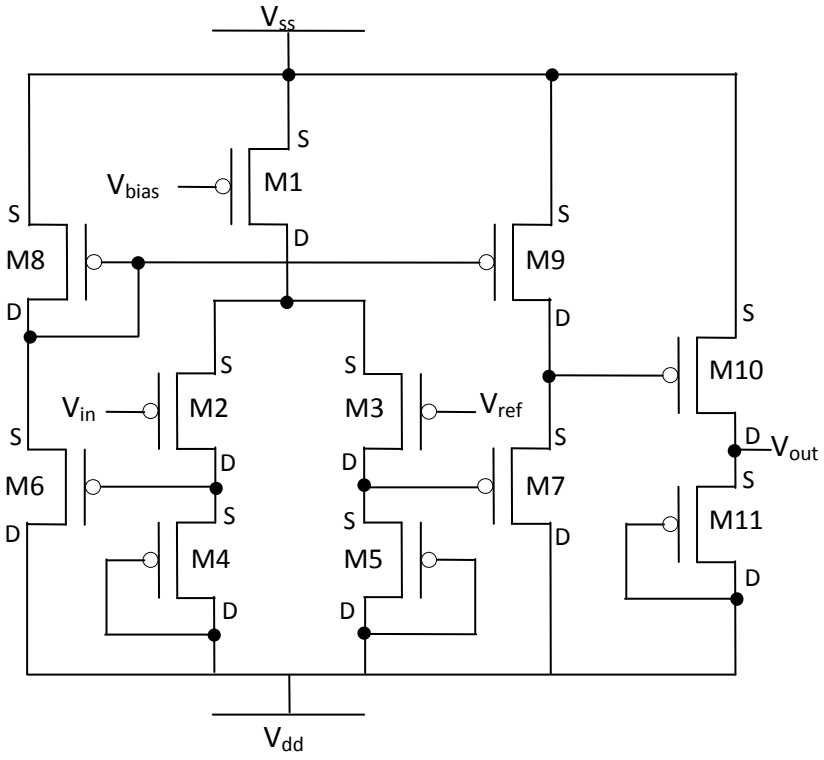


Figure 3.14: P-channel organic comparator based on a single ended differential amplifier [73].

The comparator's operation can be described by assuming a V_{ref} of -5 V. Consider the case of biasing the input (gate of transistor M2) with a voltage from 0 V to -10 V. When V_{in} is high, transistor M2 is biased off and the voltage drop across its load transistor M4 decreases. Transistor M6 is biased on and the voltage drop across it is low, biasing the current mirror transistors M8 and M9 on. At the same time, the voltage bias from the M3-M5 branch results with transistor M7 being a larger load than transistor M9. Hence, the input to the driver transistor M10 will be pulled up towards V_{ss}, biasing it off. Finally, the output of the comparator is pulled down to V_{dd} by the load transistor M11, which is always biased on. As the input voltage V_{in} decreases towards -5 V (V_{ref}) and lower, transistor M2 is switched on. Voltage drop across its load transistor M4 increases and biases transistor M6 off. In turn, the current mirror transistors are biased off, supplying a low input that biases the driver transistor M10 on. The comparator's output is therefore pulled up towards V_{ss}.

3.5 Photomask Design

The photomask is perhaps one of the most challenging aspects of this study. As the photomask is used to validate the logic circuit fabrication process, it had to be designed without prior confirmation that the fabrication process was correct. Two mesa designs were therefore included in the photomask to account for potential mistakes from the initial assumptions on the film stacking behaviour of each layer.

Agilent Technologies' Advanced Design System (ADS) was used to create the layout of each layer of the fabrication process. Each layer of the transistor structure has a corresponding layer in the photomask design that is carefully aligned with each other to ensure proper stacking of materials during fabrication. The design is saved in Graphic Database System II (GDSII) format and the output file was sent to Qudos Technology (Oxon, United Kingdom) for the manufacture of the actual 4"x4" photomask. A standard chrome mask on quartz substrate was specified for the order.

Figure 3.15 shows the complete design of the photomask that was sent to Qudos for manufacturing. The photomask contain patterns for two types of devices. Set 1 is used to fabricate single transistors and inverters, while Set 2 is for fabricating the comparator and the capacitance measurement circuit. An additional pentacene etch mask was included for the Set 2 transistors, but is not used with the fabrication process. For each device, electrical contact points extend out to form large contact pads. In addition to the logic circuits, the masks also contain essential alignment markings.

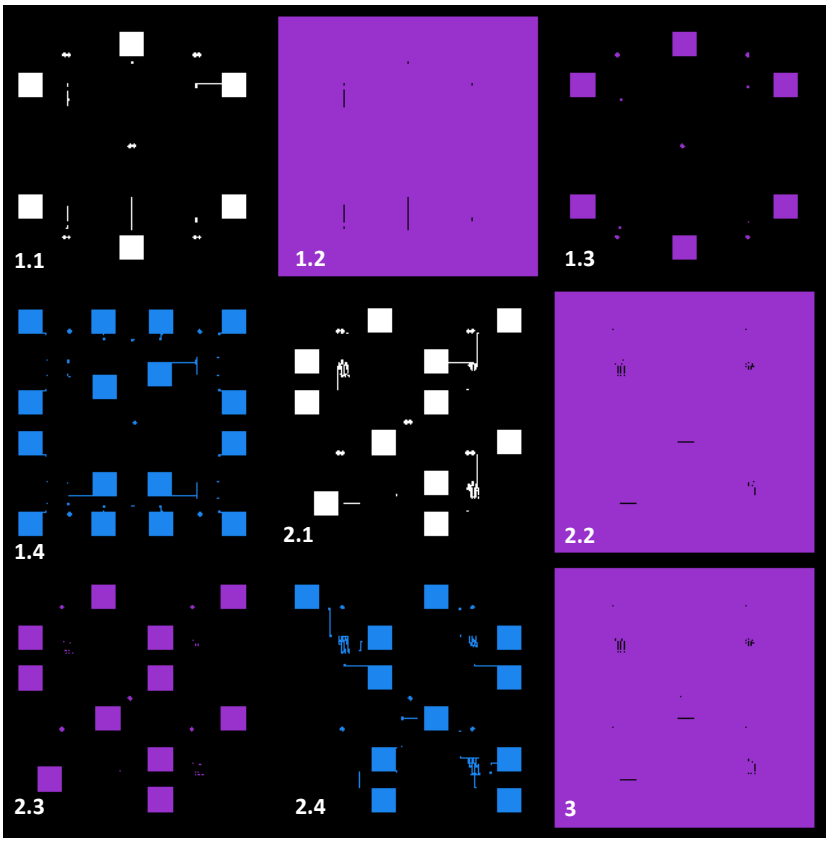


Figure 3.15: Full photomask design consisting of the inverter and comparator patterns.

Table 3.1: Description of the full photomask patterns.

Number	Mask Pattern
1.1	Inverter mask, gate layer
1.2	Inverter mask, mesa layer (full etch)
1.3	Inverter mask, mesa layer (partial etch)
1.4	Inverter mask, source/drain layer
2.1	Comparator mask, gate layer
2.2	Comparator mask, mesa layer (full etch)
2.3	Comparator mask, mesa layer (partial etch)
2.4	Comparator mask, source/drain layer
3	Pentacene etch mask

Figure 3.16 shows the stacked patterns for the inverter mask which holds two types of devices. Each corner of the mask is populated by the diode-load and zero-V_{gs} inverter circuits. Two single transistors are placed in the middle section.

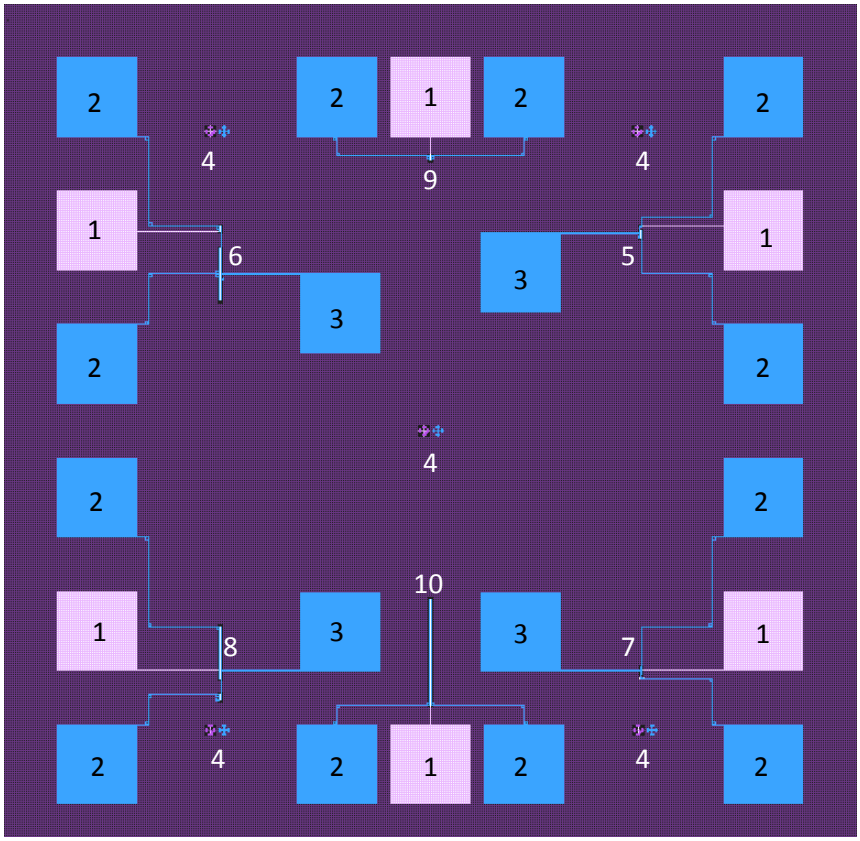


Figure 3.16: Stacked layers of the inverter and single transistor mask.

Table 3.2: Description of the inverter and single transistor photomask patterns.

Number	Mask Pattern
1	Gate contact pad
2	Source/drain or supply contact pad
3	Voltage output contact pad
4	Alignment marks
5	Small zero-V_{gs} inverter
6	Large zero-V_{gs} inverter
7	Small diode-load inverter
8	Large diode-load inverter
9	Transistor L=10 µm W=125 µm
10	Transistor L=10 µm W=1 mm

Figure 3.17 shows the stacked patterns for the comparator mask. The top portion of the mask is populated by the comparator (left) and a differential amplifier circuit (right). The bottom half of the mask is the sensor measurement circuit discussed previously in section 3.2. Figure 3.18 shows the actual photomask that was manufactured by Qudos.

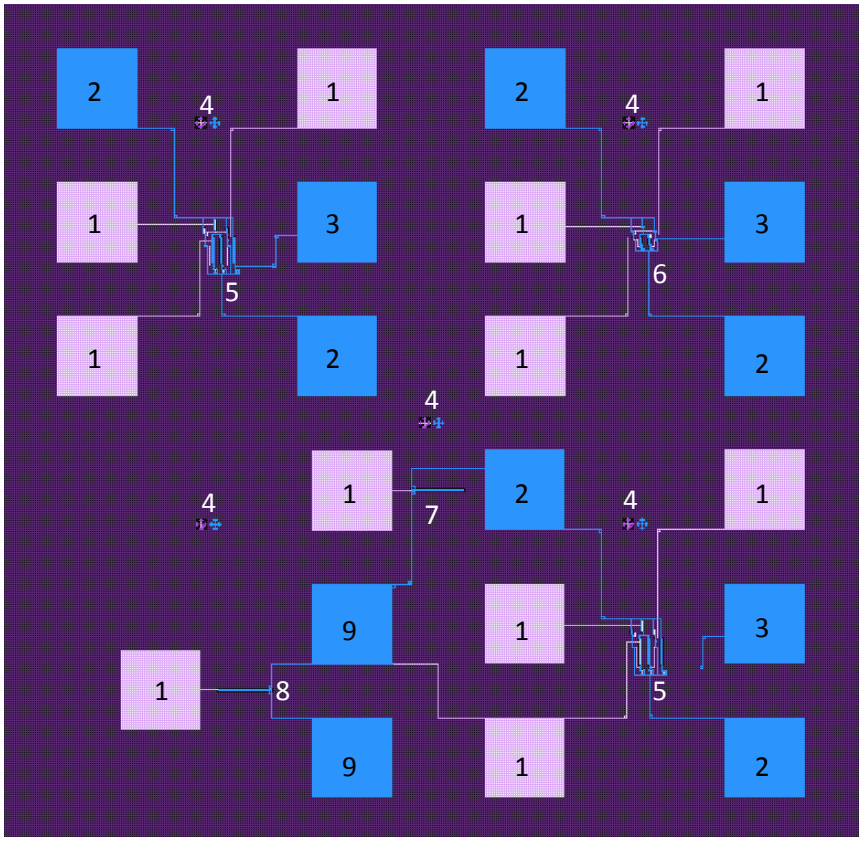


Figure 3.17: Stacked layers of the comparator mask.

Table 3.3: Description of the comparator photomask patterns.

Number	Mask Pattern
1	Gate contact pad
2	Source/drain or supply contact pad
3	Voltage output contact pad
4	Alignment marks
5	Comparator
6	Single ended differential amplifier
7	Charge transistor
8	Discharge transistor
9	Sensor contact pad

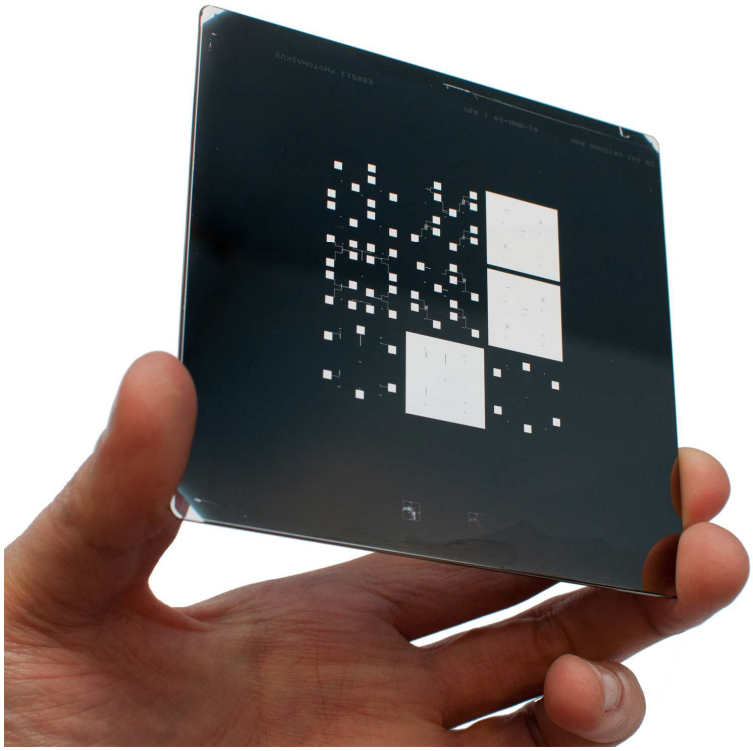


Figure 3.18: The actual photomask manufactured by Qudos.

3.5.1 Design Discussion

To explain the design decisions for the photomask, the section for the comparator circuit is used as an example (top left section of Figure 3.17). The stacking of each layer of the comparator is discussed sequentially to address all elements contained in the photomask. Following the use of positive resist, patterns on the mask represent the areas that would be illuminated during UV exposure and later removed by the developer solution.

3.5.1.1 Gate Layer

Fabrication begins with the deposition of the gate layer onto the substrate. The gate layer (Figure 3.19) contains gate bond/contact pads, transistor gates and alignment marks. Note that the following figures are focused on the main circuit area; consequently, the contact pads are not shown. The gate electrode is designed to be just slightly larger than the conducting channel to account for errors in alignment. Circuit tracks from the gate to the contact pads are set to be 20 μm wide. Although our mask aligner is capable of feature sizes down to 1 μm, a more conservative 20 μm is chosen

because the tracks can be several millimetres long. The use of thick track widths will be more resilient towards damage (e.g. discontinuities) during resist lift-off.

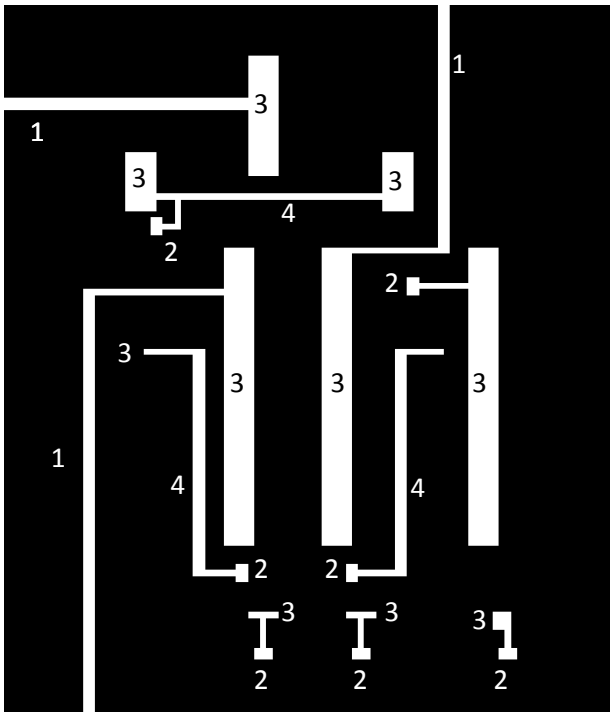


Figure 3.19: The gate layer patterns of the comparator circuit.

Table 3.4: Description of the gate layer patterns.

Number	Mask Pattern	Feature Size (µm)
1	Tracks	W=20
2	Via pad	30x20
3	Gate, various transistors	Varies
4	Interconnect	W=10

Contact pads (shown in Figure 3.17) have an area of 1.5 mm^2, which is very large relative to the size of the transistors. The reason for this is because fabricated devices using the BGBC process cannot be bonded using a conventional bonding machine as with the case of MOSFET devices due to the thin electrode layer thickness (30-60 nm). Attempts to bond a wire to the contact pad will result in peeling of the electrode layer when the bonding tip strikes the contact pad. As a workaround, contact pads are designed to be large to facilitate the use of conductive epoxy when making external connections to the device (e.g. attaching the temperature sensor). In practice, contact

pads can be designed significantly smaller and electrical contact should be made with the aid of micromanipulator probes.

Two types of vias were used in the circuit design. With reference to Figure 3.20, the first via is a through hole type, formed by etching 5 μm^2 square area of the PVP dielectric layer. The second via type is formed by the overlap of contact electrodes at the edge of the dielectric. This type of via requires the dielectric layer to cover only the channel area of individual transistors. Therefore, non channel areas are removed during the etching process.

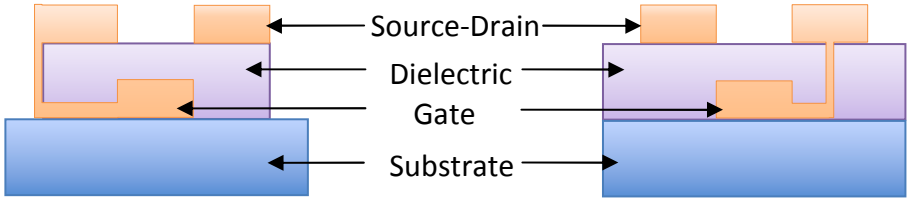


Figure 3.20: Contact electrode overlap vias (left) and through hole vias (right).

For the alignment marks, cross shape marks are placed on four corners of the sample, as well as in the centre. The positioning of such patterns has proved to be quite effective in aiding alignment, and can be used to align patterns as small as 1 µm. Figure 3.21 illustrates the shape of the alignment mark, along with its feature sizes. Each marking area holds two alignment marks, as there are two subsequent instances of the patterning processes following the gate layer deposition, which are the patterning of mesa and source/drain layer.

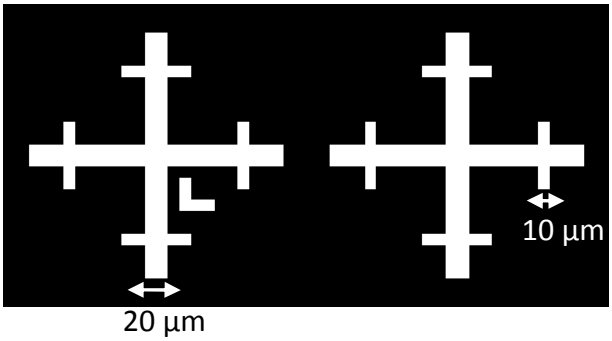


Figure 3.21: Alignment mark patterns for the gate layer. Mark for mesa layer (left) and mark for source/drain layer (right).

3.5.1.2 Mesa Layer

For the mesa (dielectric) layer shown in Figure 3.22, patterns are reversed as this is a removal process instead of an additive process as with the case of the contact electrode deposition. In addition to forming the etch mask for PVP dielectric, the mesa layer also has patterns to ensure that circuit crossovers are insulated. The dielectric area is set to be at least 10 μm wider and longer than the gate electrodes, as can be seen with the surrounding black areas. For circuit overlaps and crossovers, the bottom track is insulated with a dielectric area that is 20 μm wider than the track. A layer transparency of 50% is used in the following figures to give visibility to the bottom gate layer.

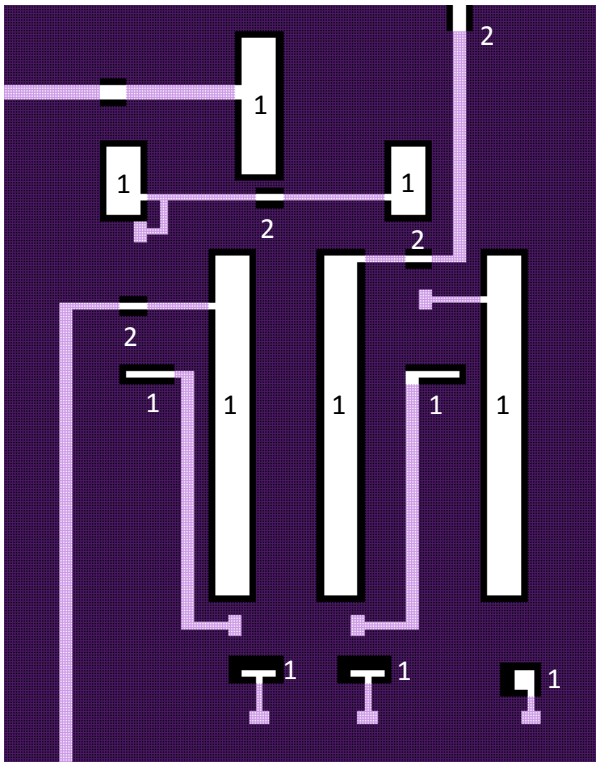


Figure 3.22: Stacked gate and mesa patterns of the comparator circuit.

Table 3.5: Description of the mesa layer photomask patterns. Marked areas are protected by the photoresist during etching.

Number	Mask Pattern
1	Gate dielectric
2	Crossover dielectric

3.5.1.3 Source Drain Layer

As seen in Figure 3.23, this mask layer holds the pattern for the source/drain contacts as well as markers for the gate layer alignment marks. The shortest lateral spacing between the source and drain electrodes (channel length) is 5 μm.

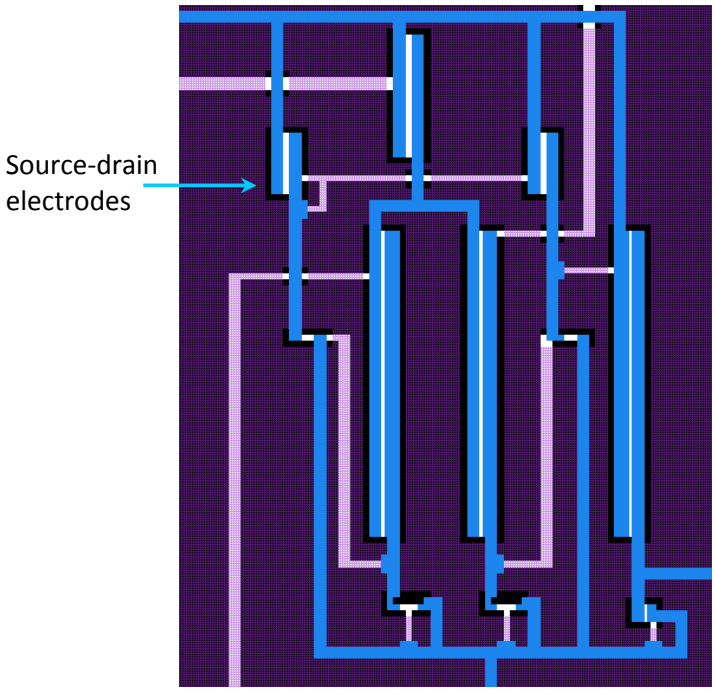


Figure 3.23: Stacked gate, mesa and source/drain patterns for the comparator circuit.

3.6 Summary

The PET project temperature sensor is essentially a parallel plate device filled with liquid crystal as the dielectric. The liquid crystal is thermotropic, where its molecular orientation changes under different applied temperatures. The sensor can be interrogated by using a RC time constant circuit to obtain useful temperature information. Under such circuit setup, the sensor assumes the characteristics of a capacitor, with a resistor connected in series. The output from the RC circuit is two distinct voltage levels that are in accordance with the liquid crystal phase, when measuring the voltage across the sensor. The sensor's voltage response can then be conditioned using a comparator following a digital or time based read out. In the former method, the comparator produces a binary output depending on the sensor's voltage level after a specific charging duration. In the latter method, the time taken for the sensor to charge to a specific voltage threshold level is used to determine the liquid crystal's phase.

During the design phase of the study, the research objectives had to be revised. The initial plan to investigate an equivalent system to the RFID sensor tag system [128] developed in the parent PET project was changed, to a new plan that is targeted towards establishing a foundation for organic logic circuit research within UoM EEE. The original objectives could not be met due to the lack of existing knowledge on the design and fabrication technology for organic circuits.

A process using photolithography was adapted from state of the art for the fabrication of organic circuits in this research. The transistor stack consists of five layers with the BGBC structure. Gold is selected as the material for the contact electrodes. Cross-linked PVP is selected for the gate dielectric and TIPS-pentacene for the active layer. To facilitate the fabrication process, a photomask containing the circuit configuration for single transistors, inverters and a comparator was designed.

4 Methodology

Three types of devices have been fabricated in this work, namely, capacitors, single transistors and logic circuits (inverter and comparator). Device fabrication was carried out under ambient environment in a class 10,000 clean room within the EEE. The equipment used includes the following:-

1. Spin-coater: Laurell model WS-400B 6TFM LITE.
2. Plasma etcher: A combination of a Headco Hivac chamber and a ENI Power Systems model ACG-5 plasma generator.
3. Thermal evaporator: Edwards model E306A.
4. Photomask aligner: A Karl Suss MJB UV 300/400 mask aligner fitted with a 350 W, 365 nm ultraviolet (UV) lamp.

Gold (99.99%) wire sources for evaporation are purchased from Cookson Gold. All other materials are obtained from Sigma-Aldrich UK unless otherwise stated.

4.1 Substrate Preparation and Cleaning

Experiments use Si-SiO_2 and highly doped n-type silicon wafers from Si-Mat. Wafers are cut into smaller square pieces depending on the area required by the device.

4.1.1 Procedure

1. Cut wafer into desired sample sizes using diamond scriber. 1x1 cm^2 is a sufficient size for a single transistor device, following the size of the shadow masks.
2. Blow sample with nitrogen gun to remove edge debris from wafer cutting.
3. Place sample in a beaker filled with Decon 75 and deionised water at 1:5 ratio. Sonicate in ultrasonic bath for 5 minutes. The Decon 75 detergent is effective for removing oil based contaminants and edge debris.
4. Repeat step 3 using acetone, methanol and isopropanol for 10 minutes each.
5. Blow sample dry using nitrogen and bake at 120 °C for 10 minutes to remove excess solvents.
6. Let sample cool down for 10 minutes before next processing step.

4.2 Solvent Preparation

All solutions were prepared in the clean room at room temperature and stored in glass vials wrapped with paraffin film for better sealing of the lids. The material solid is first weighed and loaded into a pre-cleaned glass vial using a spatula. Vial cleaning is performed similar to the substrate cleaning procedure. The solvent for the solution is then added to the vial using a syringe. The resulting solution is stirred using Teflon coated magnetic stirrers overnight to ensure that the solids are fully dissolved. Finally, the solution is filtered through Acrodisc Teflon filters before usage. Two primary solutions were prepared in this work, PVP+PMF and TIPS-pentacene solution.

4.2.1 Procedure for PVP + PMF solution

1. Dissolve 10 wt% PVP (SigmaAldrich 436224, Mw ~25,000) powder in PGMEA (99.5% SigmaAldrich 484431) and stir overnight.
2. Add 5 wt% PMF (SigmaAldrich 418560, 84 wt% in 1-butanol) to the solution using a syringe and stir overnight.
3. Filter solution (using a 0.25 μm PTFE syringe filter) into a new vial before use.

For the PVP solution, care must be exercised when selecting the purity level of the PGMEA solvent. It was found that the deposited PVP layers are highly non-uniform when using PGMEA of lower purity levels, e.g. <99.5%. This could be due to the hygroscopic nature of PVP that reacts with the higher concentrations of water molecules when using lower purity level PGMEA.

4.2.2 Procedure for TIPS- pentacene solution:

1. Dissolve 1 wt% TIPS-pentacene (SigmaAldrich 716006) solids in dichlorobenzene (DCB) and stir overnight.
2. Wrap vial with aluminium foil for storage.

4.3 Single Transistor Fabrication

Bottom gate bottom contact transistors are fabricated on highly doped n-type silicon substrates that also serve as the gate layer. PVP dielectric is deposited on cleaned substrates and thermally cross-linked. Next, the gold source and drain contact electrodes are thermally evaporated onto the substrates that are covered with shadow masks. After fabrication, substrates are exposed using a diamond scriber so that contact can be made with the gate electrode during transistor characterisation. Here, the method and duration required for thermal cross-linking of PVP films are described.

Figure 4.1: Structure of the single transistor.

4.3.1 Procedure

1. Heat PVP solution at 50 °C for 10 minutes on a hot plate.
2. Spin-coat PVP onto cleaned substrate. Set spin-coating speed to 2000 rpm with maximum acceleration to obtain a film thickness of approximately 350 nm.
3. Place sample in an annealer or hot plate and allow nitrogen to fill chamber for 5 minutes to purge ambient air.
4. Slowly increase annealing temperature to 50 °C and hold temperature for 1 minute. Then increase to 100 °C for 2 minutes to dry the spin-coated PVP film.
5. Increase temperature to 200 °C for 1 hour to induce cross-linking. After cross-linking, PVP film will harden and develop strong chemical resistance.
6. Turn off heating and allow sample to slowly cool down to room temperature before collecting. Turn off the nitrogen gas supply.
7. Align shadow mask on sample and evaporate 50 nm gold at a rate of 0.1 nm/s to form source and drain contacts.
8. Spin-coat semiconductor material and perform annealing step to dry the film.

9. Use diamond scriber to repeatedly scratch one corner of the sample to expose gate electrode.
10. Use wooden toothpick to pattern the semiconductor layer by repeatedly scratching the film to create separation among adjacent transistors.

4.4 Capacitors

Metal insulator metal structure (MIM) capacitors are fabricated using highly doped n-type silicon substrates as the first metal layer. The process is similar to the single transistor fabrication, but excludes the deposition of the semiconductor. PVP is spin-coated onto the substrates and cross-linked. Finally gold contacts are evaporated onto the dielectric layer, patterned with shadow masks.

Figure 4.2: Structure of the MIM capacitor.

4.5 Logic Circuit fabrication

Logic circuits are fabricated using Si-SiO_2 substrates, with oxide thickness of 300 nm. The main difference between the single transistor and the logic circuit fabrication is that patterning of each layer is done with lift-off photolithography instead of shadow masks. The 5 layer transistor structure employs 3 patterning stages for the gate, dielectric and source/drain layers. The lift-off photolithography process is first described, followed by the deposition and patterning of subsequent layers.

4.5.1 Procedure I: Lift-Off Photolithography

For the lift-off photolithography process, positive resist Shipley S1813 is spin-coated onto the sample, illuminated and developed to expose areas for deposition/etching.

1. Spin-coat Shipley S1813 photoresist on substrate at 4000 rpm for 2 minutes.
2. Bake sample on hotplate or oven at 115 °C for 90 seconds.
3. Let sample cool down for 10 minutes.

4. Set up sample on mask aligner and align correctly against the photomask.
5. Expose sample to UV lamp for 65 seconds using the light integration mode.
6. Soak sample in chlorobenzene for 20 minutes. Blow sample dry with nitrogen gun after soaking. Due to the toxicity of chlorobenzene, ensure that the beaker containing it is placed deep inside the processing bench so that released vapours can be effectively extracted.
7. Develop photoresist film by soaking sample in developer solution using Microposit developer and deionised water (1:1 ratio). Developing time is approximately 50-60 seconds.
8. Blow sample dry using nitrogen gun.
9. Perform required material processing step. E.g. evaporation of metal contacts or etching.
10. Strip off photoresist by soaking sample in acetone filled beaker under room temperature for 5 minutes. Acetone can be heated up to 50 °C if photoresist does not peel off. In case the chlorobenzene soak step is accidently skipped or forgotten, it will be necessary to place beaker in ultrasonic bath.

The chlorobenzene soak is used to assist the lift-off of the photoresist when evaporating metal contacts. Soaking samples in chlorobenzene for 20 minutes hardens the surface of the photoresist. This result in an undercut resist profile after development, as the hardened surface is more resistant towards the developer solution. When evaporating metal contacts, the undercut resist profile causes a discontinuity between the intended contact areas and the areas pending removal. Therefore, a clean and rapid lift-off is attained when stripping off the resist film.

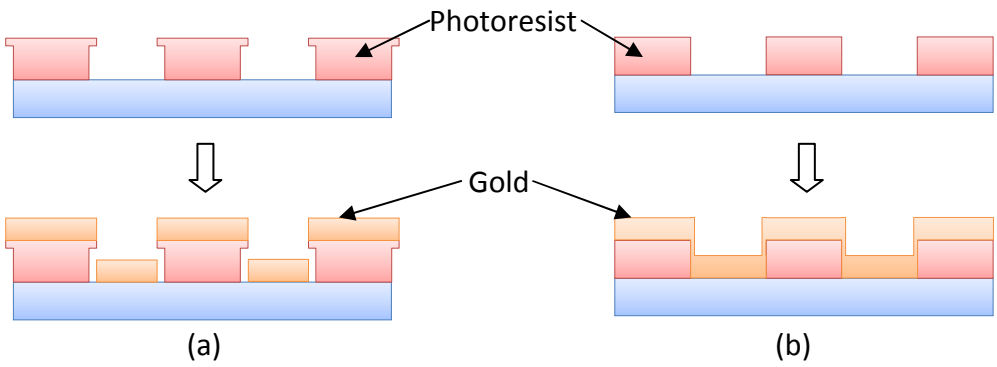


Figure 4.3: Resist and evaporated metal profile of developed films with chlorobenzene soak (a) and without (b).

4.5.2 Procedure II: Gate Layer Deposition

Figure 4.4 illustrates (not to scale) the steps taken for the gate layer deposition. Interconnects have similar physical thickness as the gate electrodes but are intentionally drawn thinner for easier reference.

The deposition of a thin chromium interlayer (not shown in illustration) is used to improve adhesion of gold to the SiO_2 substrate. Although the use of the interlayer is considered a standard practice, experiments in this research have discovered that thin gold layers (<50 nm) appears to be not, or less, susceptible to peeling during lift-off even when the interlayer is not deposited.

1. Prepare resist mask as described in procedure I.
2. Evaporate 5 nm chromium at a vacuum pressure of 10^{-6} mbar at a rate of 0.1 nm/s.
3. Allow evaporator chamber to cool down for 30 minutes.
4. Evaporate 25 nm gold at a vacuum pressure of 10^{-6} mbar at a rate of 0.1 nm/s.
5. Lift-off or strip resist mask using acetone.

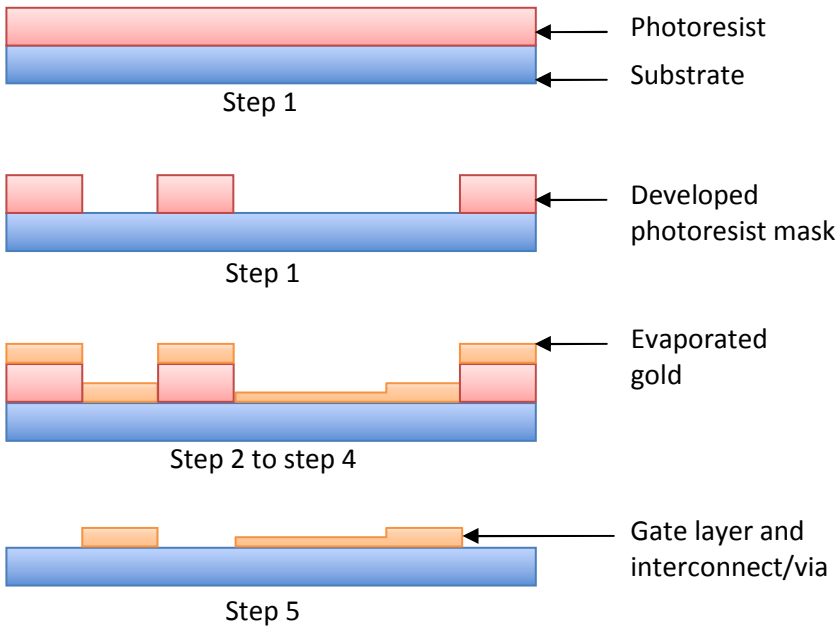


Figure 4.4: Processing steps for gate layer deposition.

4.5.3 Procedure III: Dielectric Layer Deposition and Patterning

The most important aspect of this procedure is that the etch mask must be considerably thicker than the PVP layer, as both materials are etched at a comparable rate under oxygen plasma. Using the Shipley S1813 photoresist, the etch mask is ~1.2 μm thick when spin-coated at 4000 rpm. This is an ample thickness when etching ~350 nm PVP. Chlorobenzene soak is excluded for this procedure as it is only necessary when depositing the metal contacts.

1. Heat PVP solution at 50 °C for 10 minutes on a hot plate.
2. Spin-coat PVP onto substrate at 2000 rpm for 2 minutes.
3. Place sample in an annealer or hot plate and allow nitrogen to fill chamber for 5 minutes to purge any ambient air.
4. Slowly increase annealing temperature to 50 °C and sit for 1 minute. Then increase to 100 °C for 2 minutes to dry the spin-coated PVP film.
5. Increase temperature to 200 °C for 1 hour to induce cross-linking.
6. Turn off heating and allow sample to slowly cool down to room temperature.
7. Prepare resist mask as described in procedure I.
8. Etch sample using oxygen plasma for 6-7 minutes at 50 W plasma power, 50 sccm oxygen flow and 0.1 mTorr chamber pressure.
9. Strip off etch mask using acetone.

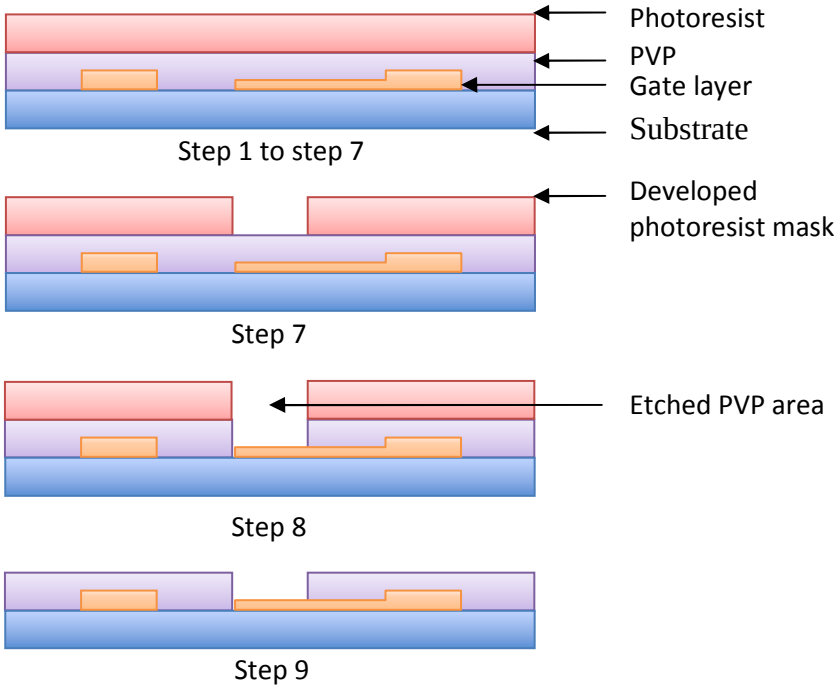


Figure 4.5: Processing steps for dielectric layer deposition.

4.5.4 Procedure IV: Source Drain Layer Deposition

For the deposition of the source and drain contacts, the chromium interlayer is not used. This is because the interlayer will be aligned to the conducting channel. Its presence will cause the majority of the charge injection to be from chromium into the conducting channel instead of gold. The work function of chromium is ~4.4 eV [134], so there will be a large injection barrier into the HOMO level of TIPS-pentacene (5.3 eV [135]).

1. Prepare resist mask as described in procedure I.
2. Evaporate 50 nm gold on a vacuum pressure of 10^{-6} mbar at a rate of 0.1 nm/s.
3. Strip off photoresist by soaking sample in acetone under room temperature.

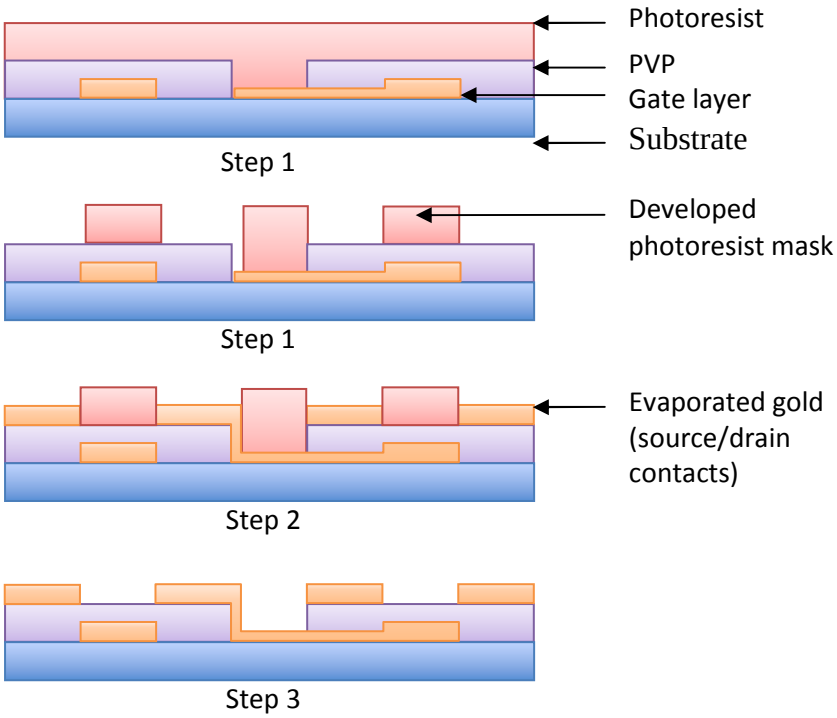


Figure 4.6: Processing steps for source/drain layer deposition.

4.5.5 Procedure V: Semiconductor Deposition

For the semiconductor layer, 3 types of deposition methods used are evaporation, drop-casting and spin-coating. Evaporated pentacene films produce highly crystalline morphology and as such gives the best device performance. Drop-casting and spin-coating use the soluble form of pentacene (TIPS-pentacene), with the former being better for attaining high field effect mobility.

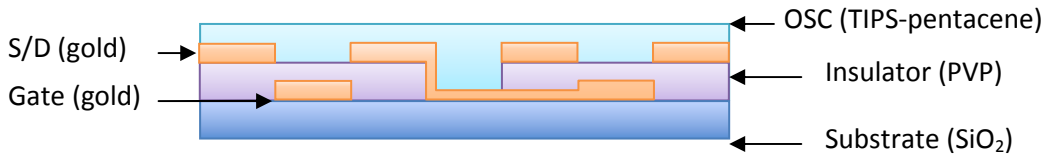


Figure 4.7: Structure of a BGBC transistor.

Dropcasting

1. Fill pipette with small amount of TIPS-pentacene and release on sample.
2. Allow dropcasted film to dry deep inside wet bench (approximately 15 minutes), so that released DCB vapor is safely removed by the fume extractor.
3. Anneal sample at 60 °C for 5 minutes and allow slow cool down to room temperature.

Spin-coating(TIPS-pentacene)

1. Spin-coat TIPS-pentacene semiconductor at 1000 rpm for 2 minutes at the lowest acceleration speed.
2. Anneal sample at 60 °C for 5 minutes under nitrogen flow and allow slow cool down to room temperature.

Spin-coating(PBTTT)

1. Heat PBTTT solution at 80 °C for 10 minutes or until the solution becomes translucent and fluid.
2. Spin-coat PBTTT semiconductor at 2000 rpm for 2 minutes at the highest acceleration speed.
3. Anneal sample at 160 °C for 10 minutes under nitrogen flow and allow slow cool down to room temperature.

Evaporation

1. Fill evaporator crucible with 5 mg of pentacene. This quantity is sufficient for evaporating 70-80 nm of pentacene.
2. Maintain substrate temperature at 90 °C.
3. Evaporate 50-60 nm of pentacene at a rate of 1 nm/minute.
4. Cool down to room temperature before collecting sample.

4.6 Device Simulation

For simulation of organic circuit configurations, AIM-Spice was used. The prerequisite for the simulation process is to obtain the fitting parameters for the a:Si:H level 15 model provided by AIM-Spice. The definitions for the fitting parameters as well as a brief review of the equations used for the level 15 model are supplemented in Appendix J.

4.6.1 Parameter Extraction

AIM-Extract is used for this step. The transistor is first characterised to obtain both the transfer and output characteristics. Before the data set for the drain current can be used, it must first be converted to assume an n-channel transistor by reversing the polarity of the gate voltage. This is because AIM-Extract assumes an n-channel amorphous silicon data input. Once converted, the transfer and output data set is then loaded into AIM-Extract and visual curve fitting is performed by trial and error. Finally, the model is converted back to p-channel and the simulation is conducted using AIM-Spice.

4.6.2 AIM-Spice Simulation

The prepared model can now be used with AIM-Spice for the circuit simulation. For a particular logic circuit configuration, the netlist is first generated using Linear Technology's LTspice by constructing the same circuit using the schematic builder. The circuit netlist is then converted to AIM-Spice format by replacing the LTspice transistor model with the previously extracted model.

4.7 Device Characterisation and Measurements

The processing described in the following sub-section were conducted under ambient conditions (humidity ~80-95%, temperature 15-20 °C) in a separate laboratory that is not a clean room environment.

4.7.1 Device Characterisation

Device characterisation is performed using an Agilent Technologies' E5270B measurement mainframe fitted with four E5287A source measure units. Each source measure unit is connected with a Karl Suss PH100 micromanipulator probe.

Fabricated devices are placed on a probe station and electrical contact between the probes and device electrodes are made with the aid of the probe station's microscope.

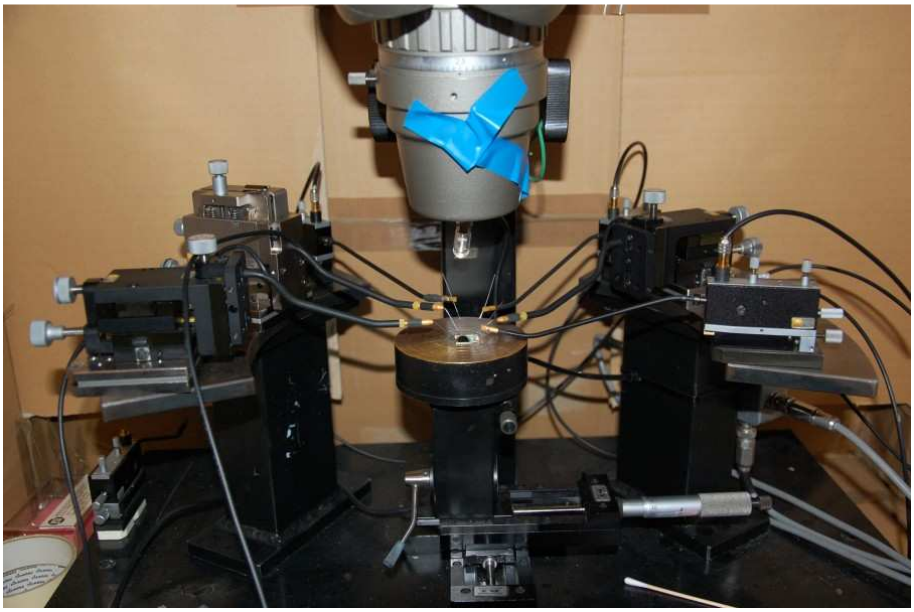


Figure 4.8: Probe station with six micromanipulator probes.

For the inverter and comparator circuits, a National Instruments LabVIEW program was coded to support voltage measurements, on top of the standard current measurements. Communication between LabVIEW and the measurement mainframe is via a general purpose interface bus (GPIB). The voltage measurement program uses the Virtual Instrument Software Architecture (VISA) library API for its voltage and current manipulation functions. Essentially, it performs a gate voltage sweep and measures the voltage of a particular measurement channel. The configuration of the LabVIEW program is shown in Appendix E.

4.7.2 Surface Profiling

Dielectric thickness and surface uniformity are determined using atomic force microscopy (Thermomicroscopes model Autoprobe CP-Research) and a surface profiler (Dektak model 150). To prepare PVP samples for thickness measurements, lithography is employed to remove half of the PVP thin film from the substrate. The edge of the polymer film is then profiled. For atomic force microscopy (AFM) generated images, the WSxM software by Nanotec Electronica [136] is used for post processing as well as extraction of thickness and surface roughness data.

4.7.3 Permittivity Measurement

A simple capacitance equation [83, pg. 134] is used for calculating the dielectric constant of the dielectric films. ε_0 is the free space permittivity, A is the area of the contact and t is the thickness of the dielectric layer. The capacitances of fabricated capacitors are determined using an Agilent Technologies' E4980a LCR meter. The frequency of the applied voltage is adjusted until a capacitive phase shift of (or close to) -90° is observed.

$$C = \frac{\varepsilon_0 \varepsilon_r A}{t} \quad (4.1)$$

$$\varepsilon_r = \frac{tC}{\varepsilon_0 A} \quad (4.2)$$

4.8 Calculation of Transistor Characteristics

The performance metrics of fabricated transistors are calculated based on standard equations for a MOSFET in saturation. All calculations use the transfer characteristics (I_d -V_g) data set. The drain current for a transistor operating in saturation region is expressed in (4.3) [31], where I_d is the drain current, μ is the mobility, C is the dielectric capacitance per unit area, W is the channel width and L is the channel length.

$$I_d = \frac{1}{2}\mu\ C\frac{W}{L}(V_{gs} - V_{th})^2 \quad (4.3)$$

On-off ratio is calculated by division of the highest and lowest measured drain currents. Mobility and threshold voltage are extracted from the plot of the square root of the drain current versus applied gate voltage. A straight line is fitted to the linear region of the plot and its slope is determined. The slope value is then substituted into (4.6) to obtain the mobility value.

Apply square root to both sides of (4.3).

$$\sqrt{I_d} = \sqrt{\frac{1}{2}\mu C\frac{W}{L}}\ (V_{gs} - V_{th}) \quad (4.4)$$

$$Slope = \sqrt{\frac{1}{2}\mu C \frac{W}{L}} \quad (4.5)$$

$$\mu = \frac{2\,L\,(Slope)^2}{W\,C} \quad (4.6)$$

Using the same linear fit for the mobility calculation, the threshold voltage is determined by the intersect value of the x-axis. The approximation of the threshold voltage is expressed in (4.8).

Using (4.4), when I_d = 0 A and V_s = 0 V

$$0 = \sqrt{\frac{1}{2}\mu C \frac{W}{L}}\,(V_g - V_{th}) \quad (4.7)$$

$$V_g = V_{th} \quad (4.8)$$

For the sub-threshold swing, the transfer curve (I_d-V_g) is first plotted. A straight line is then fitted for the sub-threshold linear region of the curve. The slope of the fitted line is then used to determine the sub-threshold swing, represented in voltage per decade.

5 Fabrication Results

5.1 PVP as a Polymer Dielectric for Organic Transistors

Several desirable film properties are required for PVP to function as the dielectric layer for the logic circuits; e.g. smooth interface, low leakage and pinhole free morphology. The experiments discussed in this section examine the physical and chemical properties of cross-linked PVP. This is to ensure that the methodology of preparing and cross-linking PVP is indeed correct and that the deposited film can withstand all the necessary processing steps of the lithographic based fabrication process.

Since the exact fabrication parameters for PVP thin film deposition are not commonly attainable in published papers, additional research was required to determine these specific processing parameters and methodologies. The following subsections report the data on the spin-coating speed (film thickness), surface uniformity, chemical compatibility and rate of etching of PVP.

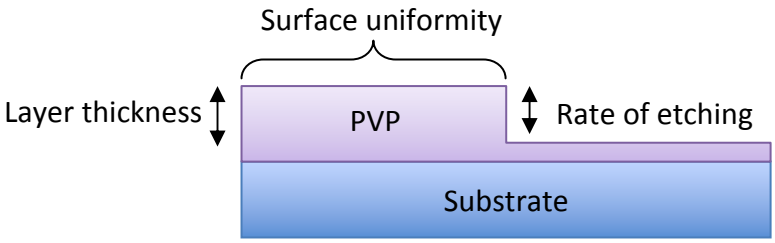


Figure 5.1: Investigated PVP characteristics.

5.1.1 Film Thickness

To determine the film thickness, 10 wt% PVP was spin-coated onto Si-SiO_2 substrates at various speeds using the Laurell spin-coater. Deposited films were subsequently cross-linked at 200 °C for 1 hour under inert nitrogen gas flow. To form a polymer edge topology, half of the PVP thin films were removed from the samples using photolithography and oxygen plasma etching. The remaining PVP thin films were then surface profiled using AFM. Nanotec WSxM was used to process the image files to extract the thickness values.

The targeted PVP thickness range was achieved with spin-coating speeds of 2000 – 3000 rpm. PVP thickness is approximately 350 nm when the deposition is performed at 2000 rpm. Over three measured samples, a mean value of 353 nm was calculated, with a standard deviation of 15.7 nm. At 3000 rpm, the mean value over two measured samples was calculated to be 276 nm (± 1.4 nm). No pinhole formation was observed for PVP that is spin-coated at 3000 rpm.

5.1.2 Dielectric Properties

To determine PVP's dielectric properties, a metal insulator metal (MIM) capacitor was fabricated, using highly doped n-type silicon substrate as the base contact plate. The thickness of the cross-linked PVP is 350 nm. The aluminium contact electrodes are deposited through a shadow mask, with each electrode covering an area of 1.2 mm^2. The plot of the current density as a function of electric field is shown in Figure 5.2.

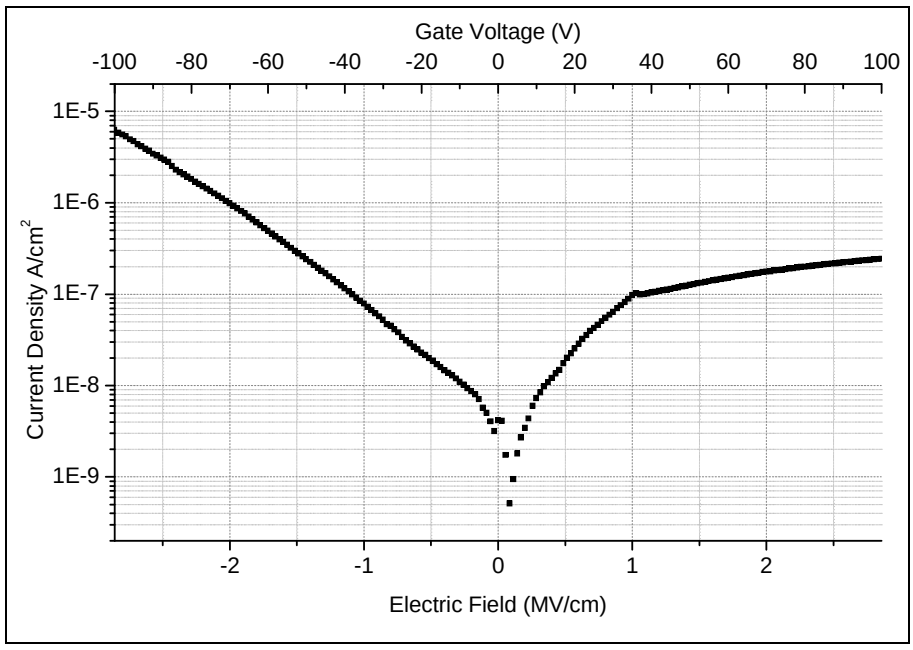


Figure 5.2: Leakage current through PVP dielectric layer.

No electrical breakdown was observed at the maximum applied voltage magnitude of 100 V, suggesting good dielectric strength for a polymer based dielectric. Higher voltages were not applied because 100 V is already over thrice the typical operational voltages of the transistors that are characterised in this research (15-30 V). The negative sweep shows a more linear profile where the current density is in the 10^{-6}

A/cm^2 region at -100 V, compared to the positive sweep direction where the current density is in the 10^{-7} A/cm^2 region at 100 V. The 0 V probe was placed on the aluminium contact electrode, suggesting that the electrons are more easily injected in the Si to aluminium direction. This is due to the formation of a depletion layer at the interface between the highly doped n-type silicon substrate and PVP dielectric when a positive voltage is applied to the substrate. The current density at 20 V is 25 nA/cm^2 in the positive sweep, which is in the expected range when compared to a previously reported value of 250 nA/cm^2 with thinner (280 nm) PVP [46].

5.1.3 Dielectric Constant

MIM capacitors were also fabricated to determine PVP's dielectric constant. Capacitance data from the impedance analyser for two samples are shown in Table 5.1. For PVP with M_w ~25,000, the dielectric constant is measured to be 4.4. For this experiment, the film thickness values for PVP were determined by fabricating and surface profiling additional reference samples. The dielectric constant of PVP is frequency dependent and capacitive phase shift is obtained at a frequency range of 200-300 Hz.

Table 5.1: Dielectric constant of cross-linked PVP.

Sample	Capacitance	Thickness	Permittivity
1	125 pF	373 nm	4.38
2	107 pF	441 nm	4.4

5.1.4 Rate of Oxygen Plasma Etching

This experiment is intended to determine the etch duration required for exposing via and interconnect areas on the PVP film. With reference to Figure 5.3, PVP is first spin-coated and cross-linked. Shipley S1813 photoresist is then spin-coated onto the PVP layer and soft baked. The sample is placed on the mask aligner and a photomask is aligned to cover half of the sample area. The exposed half is illuminated and developed away, which subsequently exposes half of the underlying PVP area. The sample is then etched using oxygen plasma for 6 minutes to fully remove the exposed PVP area. The protective photoresist layer is stripped away using acetone and AFM is used to determine the initial film thickness. Lastly, etching is repeated for 1 minute to

reduce the film thickness, and PVP layer is profiled again to determine the final film thickness and the rate of etching.

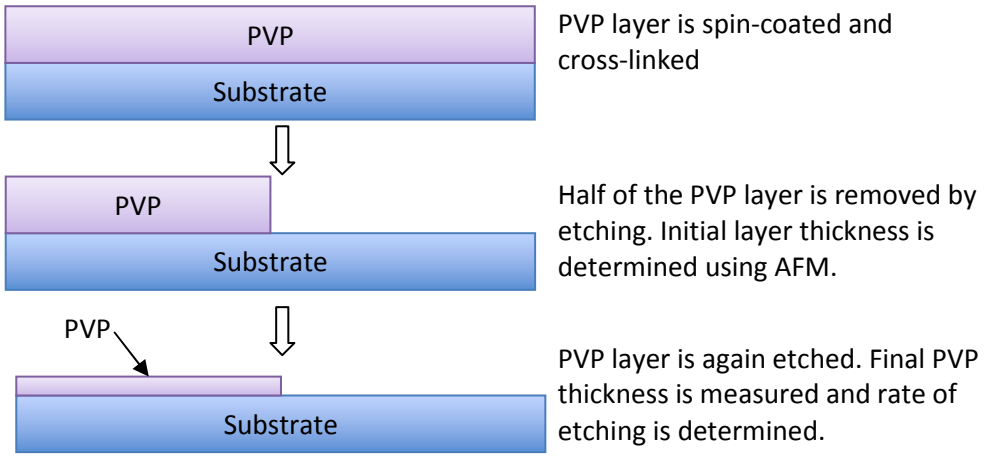


Figure 5.3: Fabrication steps to determine the rate of oxygen plasma etching for PVP.

From the thickness data compiled in Table 5.2, the rate of etching is approximately 100 nm per minute. This rate is obtained with a plasma power setting of 50 W, 50 sccm oxygen flow rate and 0.1 mTorr chamber pressure. The S1813 photoresist is spin-coated at 4000 rpm to obtain a 1.2 μm resist thickness. The plasma can be turned on for approximately 14 minutes (etching rate ~85 nm/min) before the photoresist film is completely etched away. The thicker photoresist film and its slower etch rate allows 350 nm of PVP film to be comfortably over-etched (7-10 minutes) without affecting the protected PVP areas. This experiment was only completed once as it is sufficient to discover the approximate etching rate. This is because the etching process is less time sensitive when etching with low plasma power.

Table 5.2: Etching rate of cross-linked PVP.

Parameter	Value
Plasma Power	50 W
Oxygen flow rate	50 sccm
Chamber pressure	0.1 mTorr
Initial PVP thickness	275 nm
Final PVP thickness	175 nm
Rate of etching	100 nm per minute

5.1.5 Photolithography Process on PVP

To determine the compatibility of cross-linked PVP with lift-off photolithography, PVP's surface uniformity and film thickness is examined before and after a full lithographic and etching process is applied. The photolithography process subjects the PVP film to acetone, isopropanol, S1813 photoresist, Microposit developer, deionised water and chlorobenzene. Figure 5.4 and Figure 5.5 show the AFM surface profiles of the unprocessed and lithography processed films. AFM surface profiling were performed on areas close to the centre of the samples.

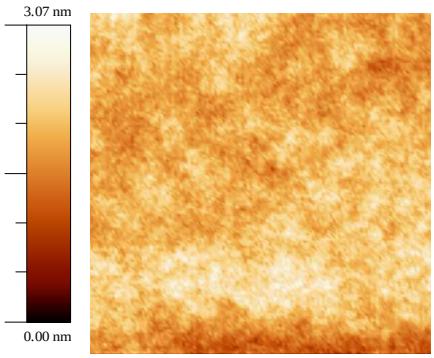


Figure 5.4: AFM surface profile of unprocessed cross-linked PVP layer (5x5 μm area).

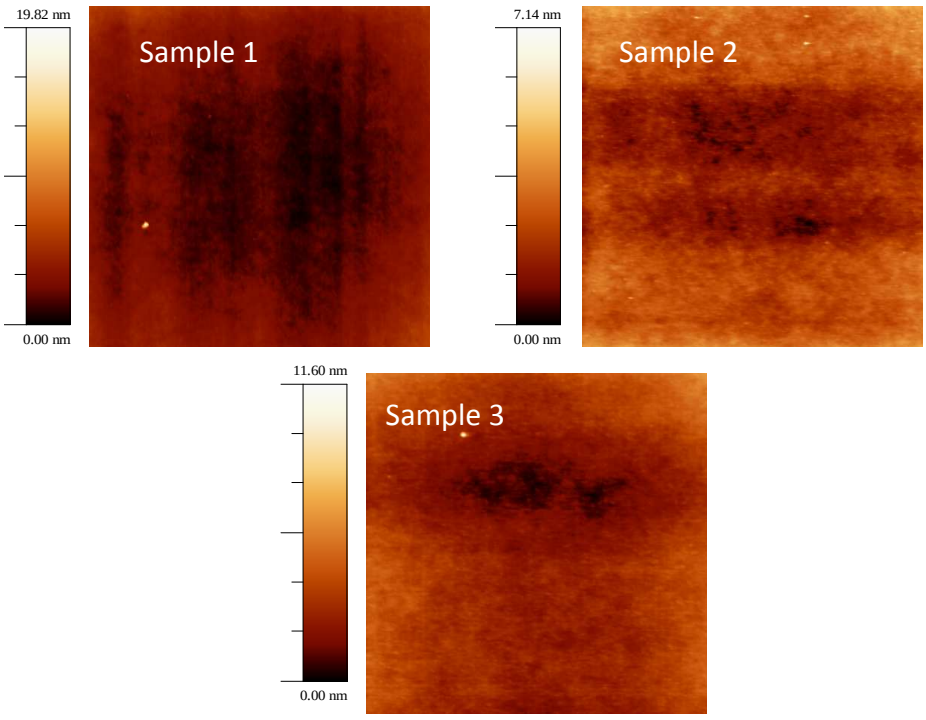


Figure 5.5: AFM surface profiles of three different cross-linked PVP samples after lift-off photolithography processing (10x10 μm area).

From the surface profile of two samples, the mean RMS roughness of the initial and unprocessed PVP layer is 3.8 Å (± 0.77 Å), indicating a highly uniform polymer interface. As shown with the results in Table 5.3, surface uniformity of the PVP layer deteriorated slightly after lift-off photolithography processing with a mean RMS roughness value of 8.9 Å (± 0.75 Å) over three samples, consistent with the results reported by Klauk *et al.* (7 Å) [46].

Table 5.3: Cross-linked PVP roughness data prior to and after lift-off photolithography processing.

Sample	RMS Roughness (Å)	Average Roughness (Å)
1	8.8	7
2	8.2	6.9
3	9.7	7.6

Although the roughness value increased by over a factor of two, the lithography processed surface is still considered a highly uniform interface. As a comparison, polished SiO_2 wafers have RMS roughness values in the single digit range (7 Å [137], 5 Å [138]). For the samples examined in this experiment, film thicknesses were unchanged. The sustained film thicknesses and surface uniformity data confirm that PVP layer is chemically stable against all solvents and processes used to complete a lift-off photolithography process.

5.2 Single Transistor Results

Figure 5.6 shows a transistor sample with PVP dielectric and spin-coated TIPS-pentacene, fabricated on highly doped n-type Si substrate.

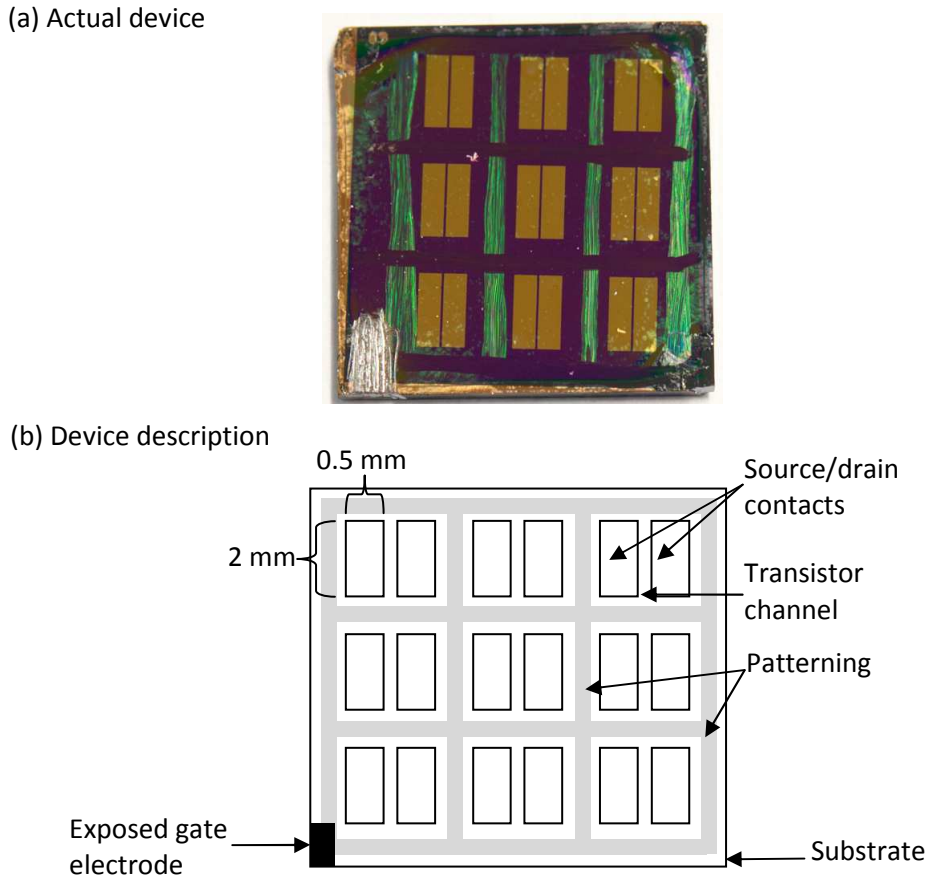


Figure 5.6: PVP + TIPS-pentacene single transistor sample.

The transfer and output characteristics of a typical single transistor are shown in Figure 5.7 and Figure 5.8. The transfer curve shows moderate hysteresis and a gradual rise in drain current with applied gate voltage. For this transistor, mobility is calculated to be 3.95 x 10^{-3} cm²/Vs, threshold voltage is -2.39 V, sub-threshold swing of 2.96 V/decade and on-off current ratio of 1x10^{3}. For the output characteristics, a well defined linear and saturation region are observed. Below -20 V V_{ds}, the saturation region of the lower gate bias lines (5 V to -10 V) curve downwards due to leakage currents.

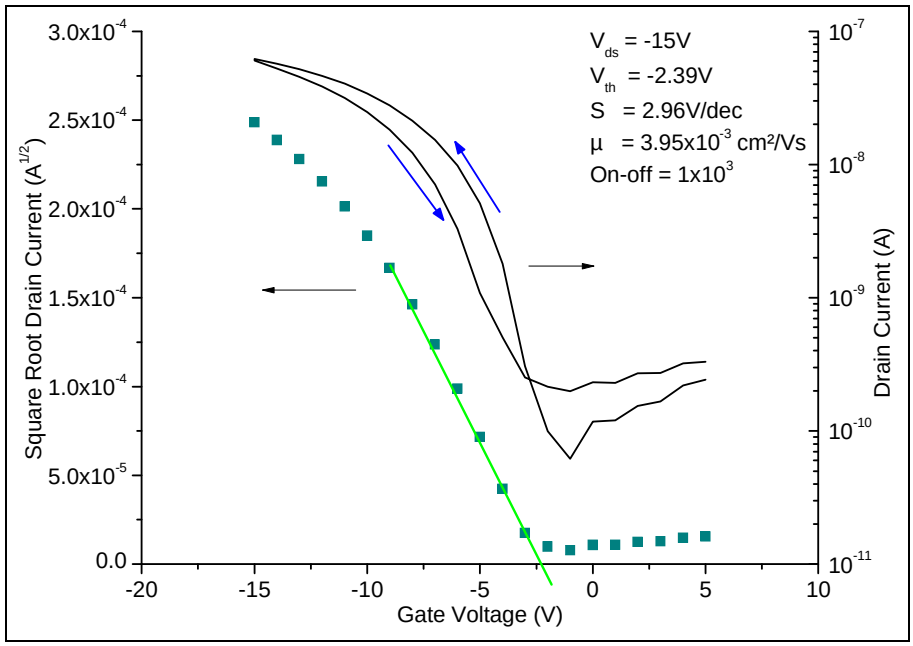


Figure 5.7: I_d-V_g characteristics of a BGBC transistor with PVP dielectric and spin-coated TIPS-pentacene (1000 rpm). V_{ds}=-15 V, W=2 mm and L=60 μm. The square root curve is from the forward voltage sweep.

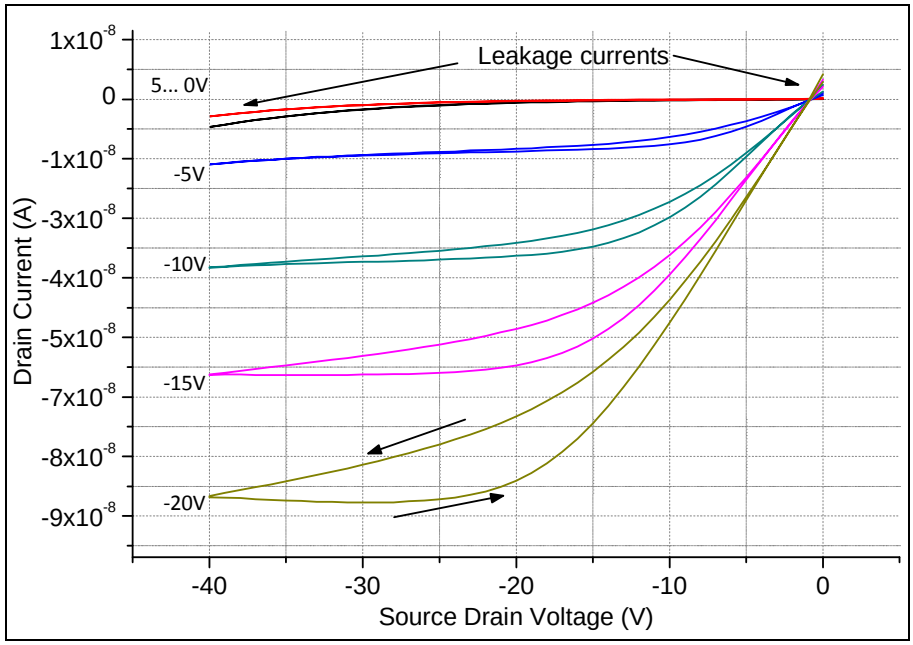


Figure 5.8: I_d-V_{ds} characteristics of a BGBC transistor with PVP dielectric and spin-coated TIPS-pentacene (1000 rpm).

Over 5 measured transistors (V_{ds} = -15 V), the mean mobility value is 2.1 x 10^{-3} cm²/Vs (± 1.8 x 10^{-3} cm²/Vs). The mean threshold voltage is -0.63 V (± 1.8 V) and a mean value of 3.3 V/dec (± 1 V/dec) was calculated for the subthreshold swing. The small data set is due to the exclusion of earlier devices that were characterised with much higher voltages, e.g. with V_{ds} above 40 V in magnitude. Yield of the single transistor device is 77% over 22 tested transistors. The relatively large standard deviation for the respective performance parameter is attributed to the use of TIPS-pentacene as the active layer. This is discussed later in this section.

In comparison, a BGTC transistor using evaporated pentacene reported by Halik *et al.* [63] has a mobility of 0.2 cm²/Vs, on-off ratio of 10^5 and a sub-threshold swing of 1.7 V/decade. The lower performance characteristics obtained with the reference transistor is expected when using the bottom contact structure with larger contact resistance, and the use of spin-coated TIPS-pentacene as opposed to deposition methods that allow for high crystallinity morphology (e.g. dip-coated or drop-casted TIPS-pentacene). The mobility of the TIPS-pentacene transistor is quite similar to that of transistors using PBTTT as the active layer. However, the PBTTT solution available to use in the EEE clean room has been considerably doped after several months in storage, resulting in fabricated transistors that exhibit large positive voltage threshold. The performance of a PBTTT + PVP transistor is reported in Appendix C.

The main disadvantage of using spin-coated TIPS-pentacene is the intrinsic anisotropy of its crystal grains [139]. The orientation of the grains directly affects the charge carrier mobility, with changes in mobility values up to a factor of 10 having been reported [140, 141]. Higher mobilities are obtained when the direction of crystal growth is parallel with the conducting channel. The anisotropy also causes shifts in threshold voltages. Of 4 transistors fabricated on the same substrate, threshold voltages ranged from -2.39 V to 1.6 V, with mobilities of 8x10^{-4} to 4x10^{-3} cm²/Vs and on-off ratios of 10^2 to 10^3. The detrimental effects of the TIPS-pentacene anisotropy reported in the literature are in agreement with the fabricated device characteristics.

Figure 5.9 shows the orientation of spin-coated TIPS-pentacene captured using optical microscopy. The patterns show occurrences of grains that do not have any preferential orientation when deposited on either PVP or SiO_2.

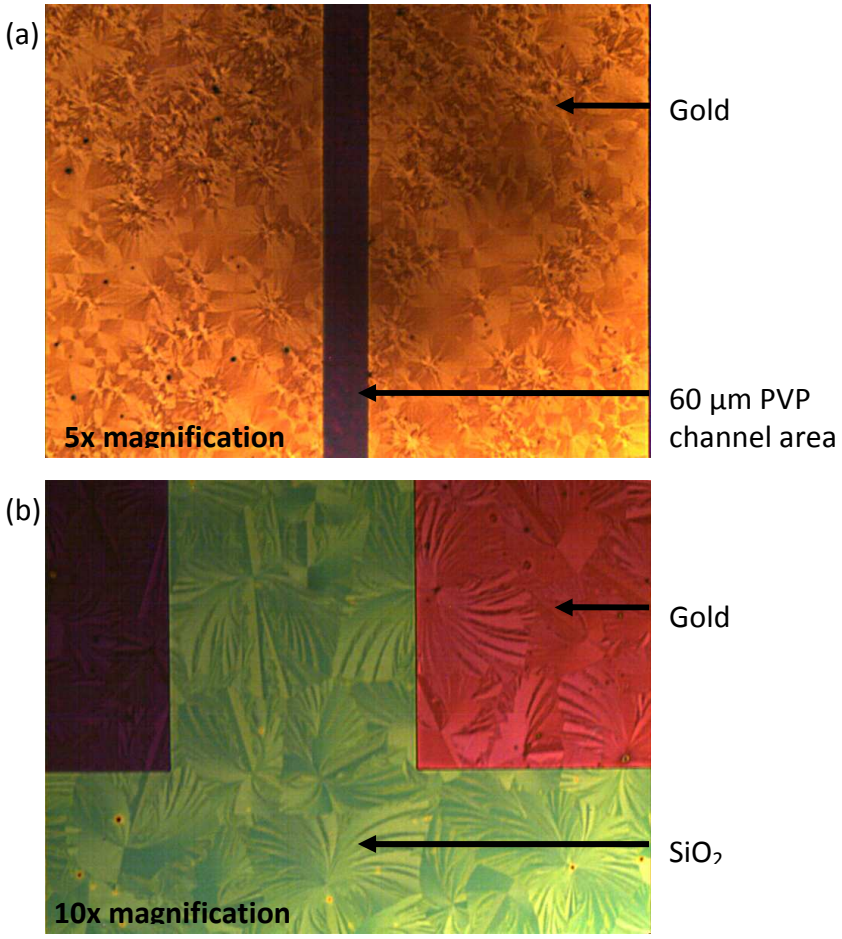


Figure 5.9: Grain growth of spin-coated TIPS-pentacene on (a) gold, PVP and (b) SiO_2 surface.

The small on-off ratio values are due to the relatively large off-currents, which is a result of the coarse patterning of the semiconductor layer when using wooden cocktail sticks. The semiconductor material still has a relatively large coverage area that can be further confined to just the proximity of the channel by patterning across the source/drain contacts.

The characteristic of large off-currents due to un-patterned (coarsely patterned in the case of this discussion) semiconducting layers is well known and have been previously reported in the literature [69, 71, 142]. First, the bulk conductivity of deposited organic semiconductor layers create parasitic leakage paths between adjacent transistors [71]. Second, the effective area of the source/drain contacts is expanded by the un-patterned semiconducting layer, giving a larger overlap area between the source/drain and gate electrodes. The gate leakage currents would

therefore be proportionally larger for devices with a common gate plane, as used by the single transistors.

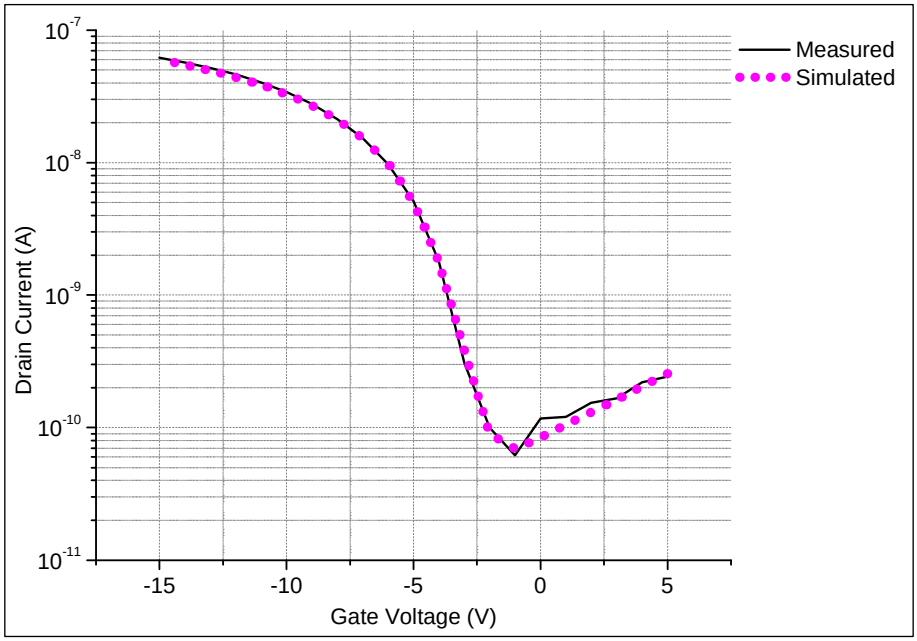
With regards to the device hysteresis, several studies have linked the characteristic to the presence of the hydroxyl groups (OH groups) in PVP [84, 143], which causes trapping of charges at the dielectric interface. Lee *et al.* [84] and Lim *et al.* [143] found that hysteresis can be suppressed with the substitution of the OH groups during synthesis or by reducing its amount using a cross-linker. Although it is tempting to attribute the hysteresis behaviour to the OH groups, it was found that the morphology of TIPS-pentacene at the contact interface to be the main contributor of hysteresis, suggesting that trapping of charges is more dominant at the contact-semiconductor interface rather than the dielectric-semiconductor interface. This finding is supported by the investigation of SAM modified contacts discussed later in Chapter 6 (section 6.2), which was found to significantly reduce hysteresis of fabricated TIPS-pentacene OFETs and improve mobility by one order of magnitude.

Overall, the performance characteristics are as expected for the PVP and TIPS-pentacene reference device because the materials are used as supplied and no surface modifications to either the electrodes or the dielectric interface were performed.

5.3 Simulation Results

To support the experimental work, AIM-Spice was used to estimate the performance of the logic circuits before fabricating the devices. The simulated I_d-V_g curve for the single transistor is plotted against the actual measured characteristics in Figure 5.10. The AIM-Spice code used for generating the simulated data is supplemented in Figure 5.10.

(a)



(b)

```
***Single transistor Simulation***

*TransistorName Drain Gate Source Body ModelName L=ChannelLength W=ChannelWidth
MTransistor 3 2 1 0 TIPS_PENT l=60u w=2000u

*Source Voltage (0V)
V1 1 0 0

*Input Voltage (Sweep from 0 to -15V)
V2 2 0 0

*Drain Voltage (-15V)
V3 3 0 -15

.model TIPS_PENT pmos level=15 alphasat=0.44 defo=0.6 delta=5 emu=0.02
+  el=0.1 eps=3 epsi=4.4 gamma=0.48 gmin=1e+023 iol=1e-011 kvt=-0.01
+  lambda=0.0008 m=1 muband=0.0001 rd=2.7e+007 rs=2.7e+007 sigmao=1e-014
+  tnom=27 tox=3.7e-007 vaa=75000 vdsl=6.7 vfb=-1.1 vgsl=4.5 vmin=0.3
+  vo=0.12 vto=2.39
```

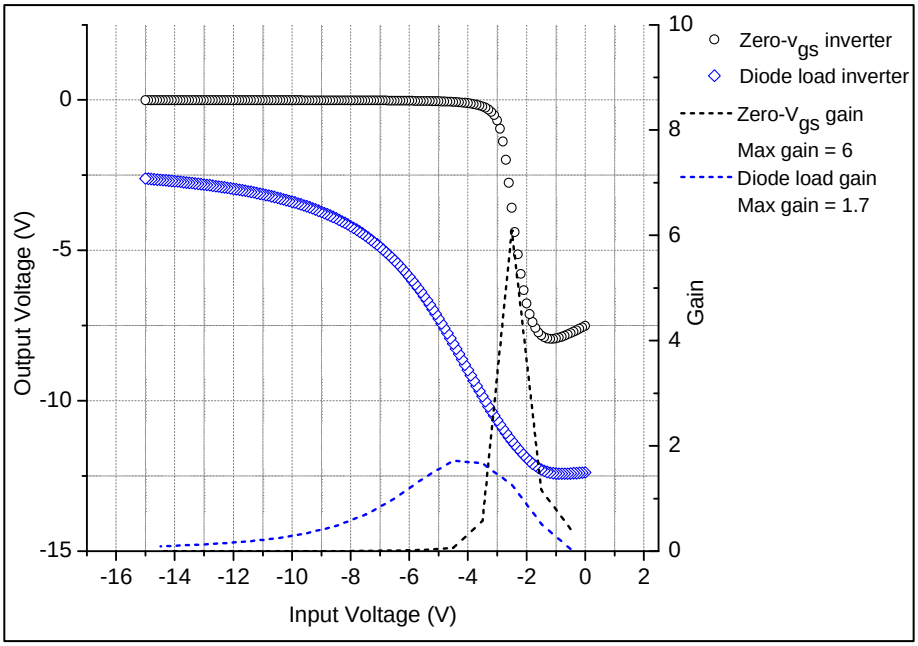
Figure 5.10: Simulated and measured I_d-V_g characteristics of the single transistor (a). The AIM-Spice code used for simulation (b).

The AIM-Spice level 15 transistor model was constructed using AIM-Extract, with manual visual curve fitting. This is because the automatic extraction feature of AIM-Extract could not provide a good fit to any of the measured data sets of the fabricated PVP + TIPS-pentacene transistors. Using this approach, the average relative error for the simulated characteristics is 7%. The region with the largest error is from -2 V to 3 V, with relative error of 17%. The large error is due to the non optimised set of values for the fitting parameters used to define that particular region. Such is the disadvantage of visual curve fitting performed by a human operator, as it is difficult to determine precise or meaningful values for each fitting parameter when adjusting the values in a trial and error manner. The error may be reduced using software that is capable of automatic optimisation of the set of fitting parameters; i.e. software to perform continuous iterations through a range of values for each fitting parameter of the AIM-Spice a:Si:H level 15 model to give a fit with the least amount of error. Although a perfect fit is not obtained for this particular transistor, the simulated characteristic is adequate for estimating the inverter and comparator performance.

Figure 5.11a and Figure 5.12a show the simulation results for the inverter and comparator circuits. For the inverter circuit, simulation results are as expected, with the zero-V_{gs} inverter (gain = 6) exhibiting better gain compared to the diode-load inverter (gain = 1.7). Similarly, correct operation is obtained with regards to the comparator circuit. The switching point appears to be in accordance to the reference voltage of -5 V when sweeping the input voltage from 0 to -10 V. However, the output stage inverter exhibits a rather gradual transition slope due to the relatively low performance of the PVP + TIPS-pentacene transistors.

Note that the supplemented simulation codes for the logic circuits are only for the transistor configuration and voltage source connections. The simulations use the same extracted single transistor model presented previously in Figure 5.10b.

(a)



(b)

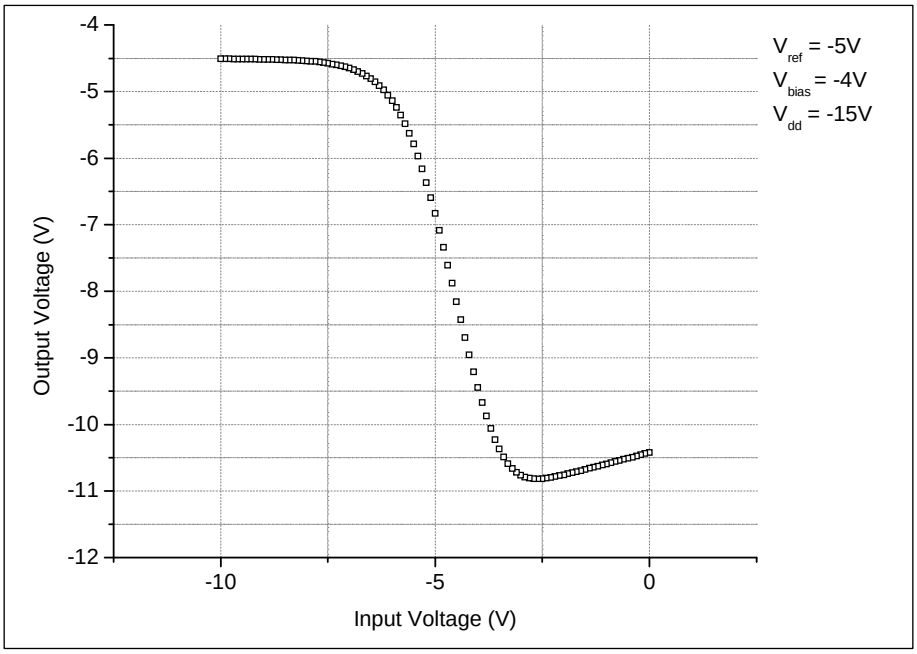
```
***Zero-Vgs Inverter Simulation***

*TransistorName Drain Gate Source Body ModelName L=ChannelLength W=ChannelWidth
MDriver 3 2 1 0 TIPS_PENT l=10u w=125u
MLoad 4 3 3 0 TIPS_PENT l=10u w=1000u

*Source Voltage (0V)
V1 1 0 0

*Input Voltage (Sweep from 0 to -15V)
V2 2 0 0

*Drain Voltage (-15V)
V4 4 0 -15
```

(c)

```
***Diode Load Inverter Simulation***

*TransistorName Drain Gate Source Body ModelName L=ChannelLength W=ChannelWidth
MDriver 3 2 1 0 TIPS_PENT l=10u w=1000u
MLoad 4 4 3 0 TIPS_PENT l=10u w=125u

*Source Voltage (0V)
V1 1 0 0

*Input Voltage (Sweep from 0 to -15V)
V2 2 0 0

*Drain Voltage (-15V)
V4 4 0 -15
```

Figure 5.11: Simulated inverter characteristics for the zero-V_{gs} and diode load configuration (a). The AIM-Spice code used for the simulation of the zero-V_{gs} (b) and diode load (c) inverters.

(a)



(b)

```
***Comparator Circuit***

*Differential Section
M1 N003 N001 0 0 TIPS_PENT l=10 w=200
M2 N008 N004 N003 0 TIPS_PENT l=5 w=500
M3 N007 N005 N003 0 TIPS_PENT l=5 w=500
M4 N010 N010 N008 0 TIPS_PENT l=30 w=10
M5 N010 N010 N007 0 TIPS_PENT l=30 w=10

*Current Mirror
M6 N010 N008 N002 0 TIPS_PENT l=20 w=10
M7 N010 N007 N006 0 TIPS_PENT l=20 w=10
M8 N002 N002 0 0 TIPS_PENT l=10 w=100
M9 N006 N002 0 0 TIPS_PENT l=10 w=100

*Output Stage Inverter
M10 N009 N006 0 0 TIPS_PENT l=5 w=500
M11 N010 N010 N009 0 TIPS_PENT l=5 w=30

*Bias voltage (-4V)
V1 N001 0 -4

*Input voltage (Sweep from 0 to -10V)
V2 N004 0 -10

*Reference voltage (-5V)
V3 N005 0 -5

*Drain voltage (-15V)
V4 N010 0 -15
```

Figure 5.12: Simulated comparator characteristics (a). The AIM-Spice code used for the simulation (b).

For the transistor model, a number of parameters were set in advance from known values before performing the visual curve fitting process in AIM-Extract. The values were determined either through measured transfer characteristics, known process parameters, or estimated from the literature. These parameters include the channel dimensions (W and L), threshold voltage (VTO), thickness of the dielectric (TOX), the dielectric permittivity (EPSI), as well as the conduction band mobility parameter (MUBAND). MUBAND can be considered as the intrinsic semiconductor mobility and is usually set as 10 cm^2/Vs for amorphous silicon. In this work, a lower mobility was assumed for spin-coated TIPS-pentacene. Hence, the MUBAND parameter was set to a lower value of 1 cm^2/Vs.

Other parameters were determined during the curve fitting process. The source and drain (RS and RD) contact resistance was extracted to be a relatively high value of $2.7x10^7$ Ω, which is acceptable in the case of the BGBC structure as high contact resistance is expected when the contacts are in plane with the channel. For this electrode configuration, values in the order of 10^4 to 10^9 Ω have been reported in the literature [80, 144, 145]. The minimum leakage current (IOL) was increased three orders of magnitude to $1x10^{-11}$ A from the default value of $3x10^{-14}$ A. The increase reflects the contributions from the bulk current of a TFT structure and the typically higher leakage when using polymer dielectrics. The flatband voltage (VFB) was extracted to be -1.1 V, which is reasonable due to the small mismatch between the HOMO (5.3 eV [146]) level of TIPS-pentacene and the work function of the gold contacts (5.1 eV [39]) .

The strategy for the visual curve fitting process was to first simultaneously adjust the mobility fitting parameters (VAA and GAMMA) and the saturation modulation parameter (ALPHASAT) until an approximate fit is obtained for the above threshold region. The flatband voltage (VFB) and the knee shape parameter (M) are then adjusted to fit for the linear region as well as the linear to saturation transition region. Finally, the below threshold parameters (VDSL and VGSL) are adjusted to complete the fitting process. Default values were used for the remaining parameters such as the dark Fermi level (DEF0) and capacitance parameters. It was not possible to fit for the above threshold region if DEF0 was set to a value between the HOMO (5.3 eV [146]) and LUMO (3.8 eV [146]) level of TIPS-pentacene.

In general, the semi-empirical approach of curve fitting with AIM-Extract and simulation using AIM-Spice is a simple and straight forward approach to predicting the response of circuits. However, future use of AIM-Extract is rather uncertain as the program has not been maintained since year 1997 and is no longer downloadable from AIM-Spice website at the time of writing. Future work on logic circuit simulation that require accurate representation of measured transistor characteristics will have to resort to alternative curve fitting software. One example approach is by Yaghmazadeh *et al*. [120], where they implemented the AIM-Spice a:Si:H level 15 model in Verilog-A. Instead of using AIM-Extract to obtain the values for the fitting parameters, they employed the UMEM [119] parameter extraction technique. The extracted values are further optimised by additional curve fitting using Agilent Technologies' ICCAP to produce models that result in 6 - 10% relative error.

5.4 Logic Circuit Results

5.4.1 Inverter Circuit

Figure 5.13 shows an inverter sample with PVP dielectric and spin-coated TIPS-pentacene, fabricated on Si-SiO_2 substrate.

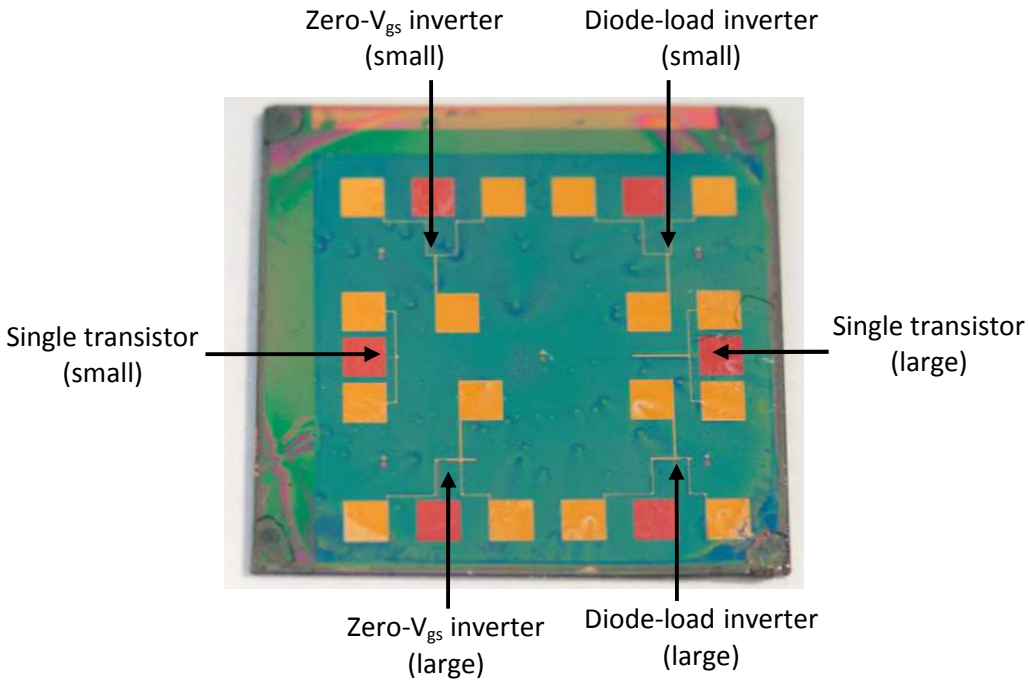


Figure 5.13: Inverter circuit fabricated using the BGBC logic circuit process.

Figure 5.14 shows the V_o-V_i characteristics for fabricated zero-V_{gs} inverters with W_{load}/W_{driver} = 8 and supply voltage of -40 V. Note that the zero-V_{gs} inverters were not characterised at lower supply voltages. Logic level separation is clearly observed with the transition from binary high to binary low with gains of 6-7 at the transition region, indicating correct inverter operation. For sample 2, the difference between V_{OH} and V_{OL} logic levels is approximately 33 V. Non ideal logic level separation (40 V) is expected as the load transistor is not completely switched off as in the case of CMOS logic inverters. The anisotropy of the TIPS-pentacene crystal grains is seen with the obvious difference in the switching point and logic level separation between sample one and two. The signal inversion midpoint is at -14 V for sample 1 and -10 V for sample 2.

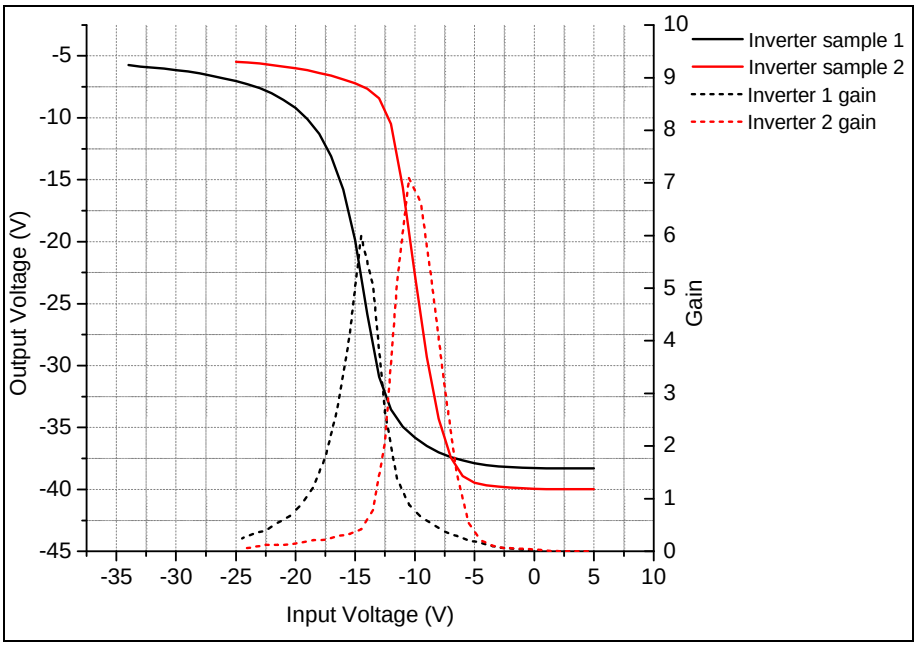


Figure 5.14: V_o-V_{in} characteristics of two zero-V_{gs} inverters. V_{ds} = -40 V. Driver transistor, W=125 μm L=10 μm. Load transistor, W =1 mm L=10 μm.

Figure 5.15 and Figure 5.16 show the characteristics for the large and small diode-load inverter configuration, with W_{driver}/W_{load} = 8. The measured gain is approximately 4 (V_{ds} = -30 V) for the large diode-load inverter. For the small diode-load inverter, the separation of V_{OH} and V_{OL} is smaller, being about 16 V at -40 V supply voltage, compared to 25 V for the large diode-load inverter. Inverter gain is also comparatively lower, measured to be 2.8 (V_{ds} = -10 V).

The smaller separation of V_{OH} and V_{OL} for the small inverter is likely due to the unpatterned semiconducting layer as well as the use of the large 1.5 mm^2 contact pads for the transistor electrodes, which causes the leakage currents of the driver transistors to be similar for both the small or large inverter configuration. The load transistor for the small inverter will therefore be a relatively smaller load and thus have a weaker voltage pull down to V_{dd}. Similarly, gain is lower because of the low on-off ratio of the driver transistor. That is, the on-current is only slightly higher than the leakage through the semiconductor bulk and gate dielectric.

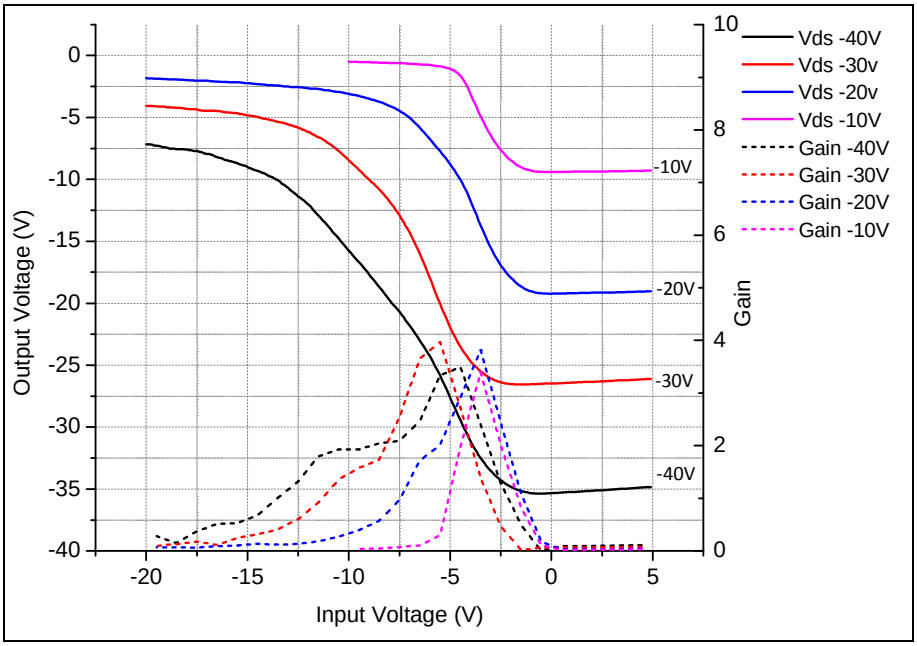


Figure 5.15: V_o-V_{in} characteristics of the large diode-load inverter. Driver transistor, W=1 mm L=10 μm. Load transistor, W=125 μm L=10 μm.

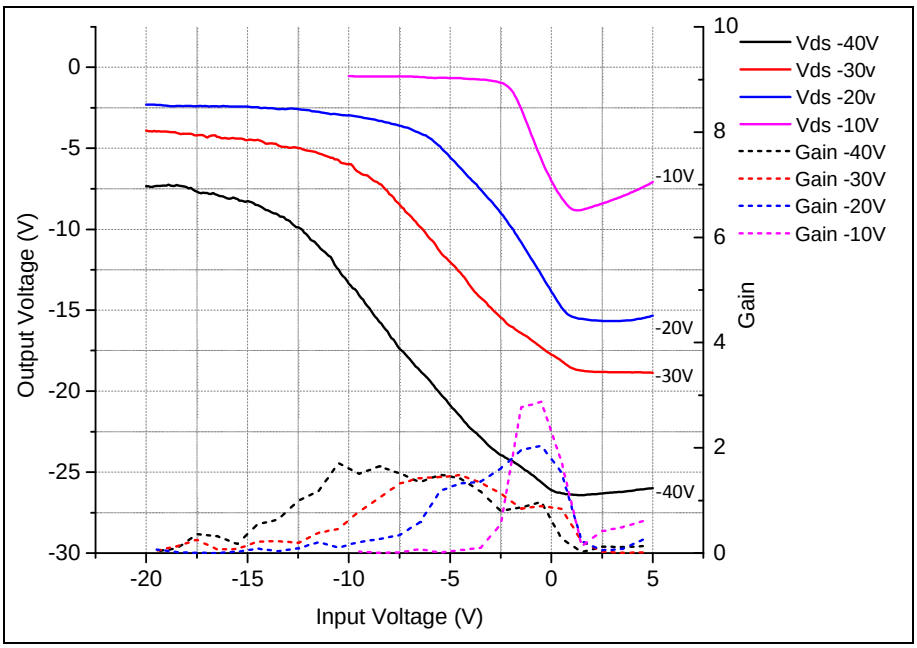


Figure 5.16: V_o-V_{in} characteristics of the small diode-load inverter. Driver transistor, W=160 μm L=10 μm. Load transistor, W=20 μm L=10 μm.

For the zero-V_{gs} inverter, it was found that the gain values are similar to the value estimated from simulation (section 5.3). However, the gain for the large diode-load inverter was measured to be higher than both the simulated performance as well as the theoretical maximum. The maximum gain is 2.8 when W_{driver}/W_{load} = 8 (section 3.4.1.2). This can be explained by the mismatch in the performance of the individual transistors, caused by the anisotropy of the TIPS-pentacene grains. In this case, the mobility is higher for the driver transistor compared to the load transistor.

Determination of the yield for the inverter device is less straight forward as continual improvements were introduced to the fabrication process throughout the research. However, out of 5 samples (20 inverters) containing functional inverters, a yield of 35% was obtained (7 functional inverters).

5.4.2 Comparator Circuit

Having validated the fabrication process by the successful fabrication of the inverter circuits, the fabrication of the comparator circuit was attempted. Initially, the fabrication attempts were unsuccessful due to shorting of the source/drain electrodes, which was later resolved by optimising the deposition process. The details on the optimisation are discussed in section 5.5.3. Once the issue on the deposition of the source/drain layer was resolved, repeated fabrication attempts did not yield any devices with functional comparator logic.

One example of the measured V_o-V_{in} characteristic of the fabricated comparator circuits is shown in Figure 5.17. For this measurement, V_{ref} is set at -5 V and the comparator input is swept from 5 V to -30 V. The measurement is repeated using varying V_{bias} voltages to take account of the mismatch of the bias transistor due to TIPS-pentacene's grain anisotropy. However, at no point did the output characteristics exhibit the expected comparator response, which in ideal case will show a binary signal inversion from V_{OL} to V_{OH} when V_{in} is at -5 V.

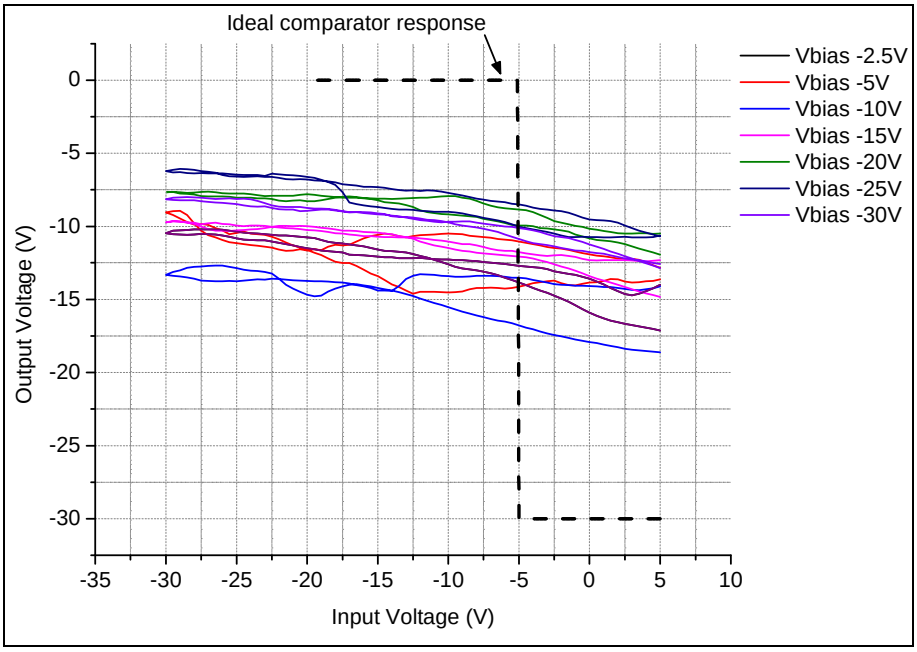


Figure 5.17: An example voltage response of the comparator circuit.

This outcome is expected when using spin-coated TIPS-pentacene, as both of the differential amplifier and the current mirror sections of the comparator circuit require good matching of the individual transistor characteristics. Unfortunately, the voltage response of each stage of the circuit could not be determined because probing points were not included in the photomask design. It would have been useful to determine if the failure of the circuit was due to the mismatch of the transistors at respective circuit sections or if it is inherent to the design of the circuit itself.

Working towards a functional comparator circuit will require a more incremental approach, starting with the characterisation of smaller and individual sections of the comparator circuit. It will be necessary to design an additional photomask that comprise of separate circuits for the differential amplifier, current mirror and output stage inverter. The output of each circuit can then be used as the input for subsequent stages in AIM-Spice to better optimise the transistor channel features via simulation. It is also clear from the comparator circuit fabrication attempts that a more refined fabrication process is necessary when scaling beyond a two transistor inverter circuit to more complex circuit configurations.

5.5 BGBC Logic Circuit Fabrication Process

This section evaluates the deposition of each layer of the logic circuit fabrication process in greater depth as well as discusses potential improvements.

5.5.1 Gate Layer

Thin layers of gold ~25 nm were sufficient to serve as the gate layer. The chromium interlayer (chapter 4, section 4.5.2) was found to be unnecessary for thin gold layers to adhere to SiO_2 substrates. Nonetheless, the interlayer step is included in the full process to conform to conventional processing methodologies when using gold contacts. For SiO_2 substrates that have been cleaned according to procedures listed in section 4.1, no peeling of the gate layers was observed for up to 60 nm of gold, upon completion of the BGBC fabrication process. Thicker layers, however, were not investigated. One may question the use of the relatively expensive gold instead of cheaper metals like aluminium or copper that can also be used to generate the electric field for accumulation of charges at the semiconductor interface. The reason is primarily due to the restriction of metal choices with the EEE's evaporator unit. To minimise chamber contamination, only chromium, gold, titanium and aluminium are permitted as sources. The gate material decision is also motivated by Philips' work [41], where gold gate electrodes are used with pentacene for tuning the flatband voltage (V_{FB}). Combining their pentacene precursor formulation with gold gate electrodes, they were able to obtain threshold voltages that are slightly positive or close to 0V.

5.5.2 Dielectric layer

Following the discussion in Chapter 3, section 3.5.1.1, two types of mesa patterns were included in the photomask. Both pattern types expose vias and interconnect areas so that PVP can be etched away by oxygen plasma. The first pattern is a full etch where PVP layer remains only on the required dielectric areas after the etching step. The second pattern selectively exposes only the via and interconnect areas, leaving unwanted PVP areas to remain on the substrate. The latter was included in anticipation of the potential peeling of the gold source/drain contacts due to its weak adherence to SiO_2, which may require the contacts to be deposited on the PVP surface instead. The resulting etched PVP layer is also less topological, which may help

reduce the potential discontinuities of the tracks at the dielectric edges. However, as discussed previously, thin layers of gold turned out to adhere sufficiently well to SiO_2. Consequently, the first etch mask was primarily used because most of the mask areas are transparent, which aids in rapid alignment of the samples. With regards to the formation of vias, both the “through hole” type and the “dielectric edge overlap” type (section 3.5.1.1) can be used with 350 nm thick cross-linked PVP.

One potential area of future work for this layer would be to investigate the minimum PVP thickness that can be used whilst maintaining high fabrication yields. This would require experimenting with spin-coating speeds and solution temperatures to find out if thinner (<350 nm) pinhole-free PVP films can be deposited. Gay *et al*. reported the use of 100 nm PVP with a rather similar fabrication process, but the fabrication yield was not discussed in the paper [73].

5.5.3 Source Drain Layer

The source drain layer was the primary reason for the low yields (approximately 10%) in the early stages of establishing the fabrication process. The lift-off photolithography process was often unsuccessful, forming short circuits between the electrodes.

Figure 5.18 captures the incomplete photoresist lift-off profile for a comparator circuit sample, where the mask patterns continue to remain on the sample near the top right of the figure. This is an unusual lift-off behaviour as most of the photoresist areas are easily removed except for specific spots that would consistently fail to lift-off, even when photoresist stripping was done using heated acetone (45 °C) and an ultrasonic bath. This occurs more regularly for the comparator circuit compared to the inverter circuit, suggesting that certain resist patterns are more susceptible.

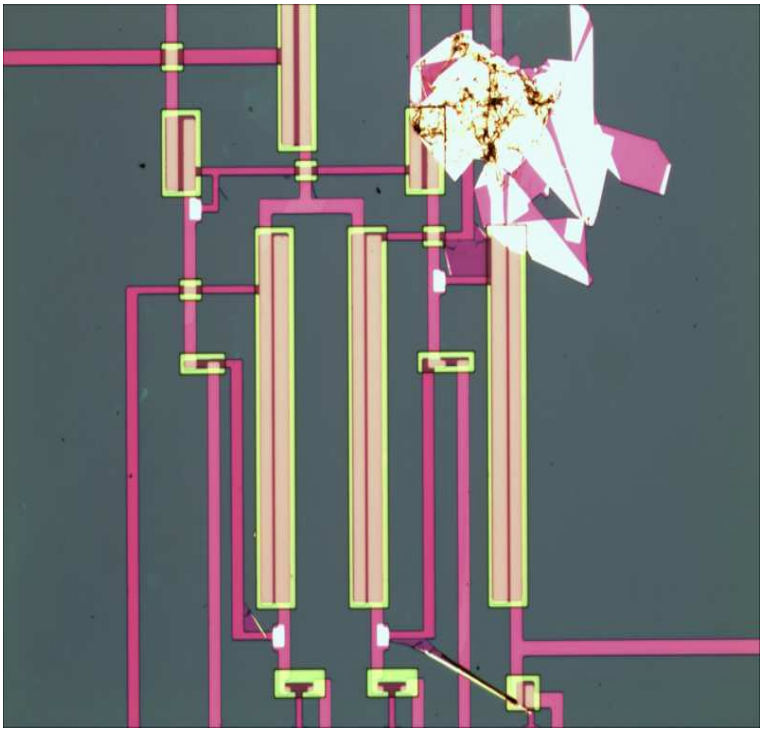


Figure 5.18: Incomplete photoresist lift-off during the deposition of the source/drain contact electrodes.

By systematically repeating the lift-off process and changing fabrication parameters each time (e.g. resist thickness, UV exposure duration and evaporated gold thickness), the poor lift-off was discovered to be due to the insufficiently hardened resist surface prior to the developing step. As chlorobenzene soak is used for hardening the photoresist surface, the duration of the soaking step had to be increased to 20 minutes, from the initial 3 minutes as per established processing procedures of the EEE nanoelectronics fabrication group. Once the root cause was identified and resolved, clean and rapid resist lift-off was consistently achieved.

The design of the contact layer's electrode configuration can be improved with the use of interdigitated electrodes (IDE). Long continuous electrodes can be replaced with shorter parallel electrodes, which offers larger current density for a given gate area. IDE electrodes can also help minimise the mismatch of transistors in the case of electrode discontinuities. For instance, a particular transistor can be considered as permanently switched off if a discontinuity occurs at the start of a long conventional electrode. With multiple shorter interdigitated electrodes, a discontinuity formed at one electrode would not significantly change the overall amount of current at the drain electrode.

5.5.4 Semiconductor Layer

Despite the straight forward deposition method of using spin-coated TIPS-pentacene, the semiconducting layer is perhaps the layer that requires the greatest amount of further optimisation work. There is a need for a patterning step to reduce off-currents and to remove excess semiconductor material from the contact electrodes. Straight forward patterning of pentacene can be accomplished using shadow masks or etch masks. The most widely employed approach however, is the PVA etch mask [147, 148] that also serves as the encapsulation layer for pentacene to prolong its shelf life. For this approach, PVA is photosensitised with ammonium dichromate to act as a negative type resist that can be developed using water. Since the mask is water based, pentacene is not dissolved or damaged during the patterning step.

To improve mobility and device consistency of transistors using TIPS-pentacene, it would be desirable to control the growth direction of the grains to be in parallel with the conducting channel. One method to achieve preferential grain growth direction is to place the substrates in a chamber with controlled (directional) inert gas flow when drying the TIPS-pentacene films [140]. Another method would be to employ dip-casting [149] as the deposition technique, to obtain grains that are orientated in parallel to the dip axis.

Another important optimisation aspect is the control of V_{th}. Polymer Vision's [41] method of utilising a pentacene precursor solution seems most appropriate, as it allows tuning of V_{th} by changing the formulation of the precursor. Two alternative methods have also been employed in recent years. The first method is based on the tuning of V_{FB}, where metals of different work functions are used for the gate layer. One recent report is by Nauseida *et al.* [78], using aluminium (V_{th} = -0.43 V) and platinum (V_{th} = 0.23 V) with thermally evaporated pentacene. The second method relies on voltage biases from secondary gate electrodes deposited after the semiconducting layer, essentially a dual gate structure as demonstrated by Polymer Vision [79]. However, the fabrication steps for the secondary gate layer were not revealed fully in their paper. One possible sequence for fabricating the dual gate stack is as follows:-

1. After deposition of TIPS-pentacene, pattern semiconductor layer with PVA etch mask and leave mask on.
2. Evaporate a thin layer of parylene to form a layer that can withstand photolithographic processing. It is to be noted that Polymer Vision used a 1.4 μm thick PVP layer for this step, instead of parylene. However, the temperature at which PVP is cross-linked to give chemical resistance without damaging the PVA etch mask and semiconducting layers is not known.
3. Deposit second gate layer via lift-off photolithography.

5.6 Summary

This chapter reports on the performance characteristics of transistors and logic circuits using the PVP gate dielectric and TIPS-pentacene combination. When spin-coated PVP is cross-linked with PMF at 200 °C degrees for 1 hour, uniform and robust dielectric thin films are obtained. The PVP thin films are chemically stable against IPA, acetone, methanol, chlorobenzene, dichlorobenzene and microposit developer solution. The oxygen plasma etching rate of the film is 100 nm/minute using plasma setting of 50 W, 50 sccm oxygen gas flow and 0.1 mTorr chamber pressure. Film thickness of approximately 350 nm is obtained when spin-coating at 2000 rpm using the Laurell spin-coater.

The PVP + TIPS-pentacene single transistors typically have mobilities in the range of 10^{-3} cm²/Vs and on-off ratio of 10^2 to 10^3. Such performance characteristics are sufficient for use in inverters to obtain inverting gains >1 when biased with -10 V (V_{ds}). The reference device shows noticeable hysteresis due to the trapping of charges at the contacts-semiconductor interface. The hysteresis can be reduced by surface modification of the contacts which is discussed later in chapter 6, section 6.2.

Using the BGBC logic circuit fabrication process, inverter circuits were successfully fabricated. Inverter gains were measured to be 6-7 for the zero-V_{gs} configuration and approximately 3 for the diode-load configuration. The same process was applied to fabricate a more complex comparator circuit, but, no comparator type response could be obtained. Nonetheless, functional inverters confirm the validity of the fabrication process and the design of the photomask described in the methodology chapter of this thesis. This means that the vias and interconnects necessary for integrated logic circuits are formed successfully using the fabrication's processing steps.

While the fundamental processing steps have been established, several optimisations could be implemented to improve the fabrication technology for logic circuits. First, the patterning of the semiconductor layer is needed to reduce off currents. Secondly, consistency of transistor characteristics needs to be improved, either by post deposition processing on the TIPS-pentacene layer, or with the use of alternative semiconductors. Finally, there is also a need to control the threshold voltage of the transistors. Further work on extending the fabrication process to include the

semiconductor patterning steps and control of V_{th} was not investigated as it is beyond the scope the research plan.

6 Device Optimisation

This chapter details the optimisation work on the contact and dielectric layers for the BGBC transistor stack used in this research. For the dielectric layer, the use of high-k polymer-nanoparticle nanocomposites is investigated. For the contact layer, surface modification using SAM is investigated.

6.1 Polymer Nanocomposite Dielectric with High-k Nanoparticles

6.1.1 Introduction

In the present state of organic technology, transistors and logic circuits typically require relatively high voltage biases. To cope with the increased voltage requirement, circuits can either be designed to include internal voltage boosting stages or be biased with high voltage amplitude sources. Although such voltage requirement can be accommodated within the research environment, in practice it would be challenging to integrate organic circuits with existing electronic devices where logic voltage levels are normally 5 V and below.

Various methods have been used in the development of low voltage OFETs. The simplest approach is to reduce the thickness of the dielectric from typically several hundreds of nanometers to below 100 nm [124, 150]. The second method is to use high-k metal oxide dielectrics [151] and finally the last method employs high-k inorganic nanoparticles that are either mixed with polymer dielectrics or deposited as part of a multi layer dielectric [152, 153]. For the first method, ultra thin polymer films suffer from pinhole formation which results in decreased yield, and is likely only attainable with laboratory deposition methods such as spin-coating and evaporation, rather than printing. The same limitation applies to metal oxide dielectrics, where its deposition typically relies on high temperature/vacuum evaporation and sputtering systems. In contrast, the use of high-k nanoparticles is a more elegant solution because it is compatible with both laboratory based deposition and printing.

This section discusses the use of barium strontium titanate $(Ba,Sr)TiO_3$, abbreviated as BST, as an inorganic filler for PVP to produce high-k PVP-BST nanocomposite

dielectric. The use of polymer nanocomposites has been previously demonstrated in the fabrication of single transistors [154]. However, the use of nanocomposites in a lithographic logic circuit fabrication process has not been previously studied. The work discussed here incorporates the PVP-BST nanocomposite layer into the BGBC logic circuit fabrication process described in Chapter 4. To obtain the BST nanoparticles, a synthesis was initially attempted from a recipe obtained in literature. Conducted experiments however, used commercially available BST from Sigma-Aldrich.

BST is a ferroelectric material with a perovskite structure that is attractive for use in capacitors, memory and transistor devices due to its very high dielectric constant, low leakage and high resistance reliability [155]. In bulk form, the dielectric constant of BST can be as high as 20,000 [156] but reduces to several hundreds in thin film form [157, 158]. Accordingly, the dielectric constant value becomes even smaller in nanoparticle form. Huang *et al.* [152] reported a dielectric constant of 47 for BST nanoparticles that are 25 nm in size. The same group also reported a dielectric constant of 18 for a PMMA–BST blend with 1:1 ratio (PMMA dielectric constant = 2.5). Although BST nanoparticles do not share the large dielectric constant values as in its bulk or thin film state, it has the advantage of being able to be mixed into polymers to form nanocomposites. This improves the effective permittivity of the dielectric layer while retaining processing benefits of the polymers (low temperature deposition, solubility and printability).

6.1.2 Preparation of PVP-BST Solution

6.1.2.1 Synthesised BST

For the preparation of the nanocomposite, the primary consideration is the amount of nanoparticles that can be added to the polymer matrix before the increased surface roughness of the nanocomposite outweighs the benefits of the dielectric constant increase. This is because transistors using nanocomposite dielectrics with very high nanoparticle loading will exhibit reduced mobility as a result of the rougher dielectric-semiconductor interface where charge transport occurs. The size distribution of commercially available (Sigma-Aldrich) BST is in the range of 50-100 nm, which is rather large when considering the relative thickness of the spin-coated PVP that is

~350 nm. By using smaller nanoparticles that are synthesised in-house, one can theoretically increase the loading of nanoparticles whilst maintaining the surface roughness of the nanocomposite.

This section reports on the synthesis of BST nanoparticles using a recipe by Huang *et al.* [152]. The recipe is a solvothermal process that involves the alcoholysis between a metal organic precursor (mixture of barium isopropoxide, strontium isopropoxide and titanium isopropoxide) and ethanol. Selection of this recipe is due to the reported small nanoparticle sizes (8-30 nm), as well as the relatively low temperature processing.

Synthesis Procedure

This recipe is for preparing ($Ba_{0.7}$, $Sr_{0.3}$) TiO_3 nanoparticles from a mixture with precursor molar ratios of 0.7 : 0.3 : 0.7. Calculations of the amount of materials used are supplemented in Appendix D. Prepared mixture is approximately 22 ml.

1. Transfer raw materials and a weighing scale into glovebox.
2. Transfer 0.196 g barium isopropoxide powder into a glass vial using a spatula.
3. Transfer 0.068 g strontium isopropoxide powder in the same manner as step 1.
4. Seal vial using parafilm in preparation for removal of the vial from the glovebox.
5. Quickly reseal with a rubber seal after vial transfer. The intermediary parafilm seal is used to prevent release of the rubber seal when moving through the antechamber (due to the vacuum and nitrogen purge).
6. Purge a balloon with nitrogen and attach a metal syringe tip. Inject into rubber seal. Then inject 6 ml anhydrous ethanol and anhydrous isopropanol into the vial. The balloon is used to collect displaced nitrogen gas when adding the solvents.
7. Add ethanol 10 ml 96% to the mixture using a metal tip syringe.
8. Transfer vial back into the glovebox. Replace rubber seal with parafilm for this step.
9. Add 0.226 ml titanium isopropoxide drop by drop using an automatic pipette while continuously stirring the mixture.

10. Transfer mixture into a Teflon lined autoclave vessel. Seal tightly with the vessel lid and heat at 200 °C for 48 hours to allow the synthesis reaction to complete.
11. Take vessel out of the autoclave and leave to cool overnight. Then transfer precipitated (white) BST nanoparticles into a centrifuge tube using a spatula.
12. To clean the collected BST nanoparticles, add ethanol to the centrifuge tube and sonicate for 30 minutes to re-disperse the BST nanoparticles.
13. Place tube in centrifuge and set rotation speed to 3000 rpm. Start centrifugation for 1 hour.
14. Remove ethanol from the tube using a syringe with a long metal tip.
15. Repeat steps 12 - 14 three times to ensure a thorough cleaning of the BST nanoparticles.
16. After the final ethanol removal step, transfer BST precipitate into a round glass flask and heat using a solvent evaporator (Buchi Rotavapor R-200) until ethanol is completely evaporated, leaving behind dried BST.
17. Scrape BST nanoparticles from the walls of the flask into a glass vial for storage using a spatula.

Synthesis Results

The synthesis of BST nanoparticles was completed with the aid of a mBraun MB-200 nitrogen glovebox within UoM's School of Chemistry clean room facility. The main challenge for the synthesis was maintaining the moisture sensitive mixture under nitrogen atmosphere throughout the processing. However, in steps 4 and 8 of the synthesis, the vial containing the mixture was momentarily uncapped to facilitate the transfer of the vial out and back into the glovebox. The transfer was necessary as the particular glovebox is fitted with a carbon filter that would degenerate when non compatible solvent vapours are passed through during chamber recirculation. As ethanol is one of the incompatible solvents, the addition of ethanol to the mixture was completed outside the glovebox to minimise filter damage. Consequently, the momentary exposure introduced an unknown influence to the air sensitive synthesis.

Additionally, the lack of high capacity vessels limited the amount of mixture that can be synthesized at a time. The total volume of the mixture is restricted to approximately half of the volume capacity of the autoclave vessel to prevent

overflowing of the mixture when pressure builds up during the synthesis reaction (step 10). In the case of the equipment used for the synthesis, a 40 ml vessel is filled with 22 ml of the synthesis mixture. Nevertheless, a bigger scale synthesis can be achieved by splitting a large mixture volume across multiple vessels.

After completion of the synthesis reaction, the size distribution of nanoparticles is determined using a Malvern Zetasizer that utilises dynamic light scattering (DLS) as its measurement technique. The Zetasizer is capable of detecting particles as small as 10 nm which is sufficient for the expected size of synthesised nanoparticles.

Figure 6.1 shows the size distribution of the BST nanoparticles that remained in suspension from the mixture after completion of the reaction. The solution sample is taken right after the vessel cooled down to room temperature (step 11). Figure 6.2 shows the size distribution of the BST nanoparticles that is considered as the product of the synthesis. The solution sample is taken from the dispersed BST solution after sonication, at the final cycle of the BST cleaning procedure (steps 12 – 14). For each solution sample, 2 ml of BST in ethanol were extracted using long metal tip syringes and transferred into quartz cuvettes for measurement.

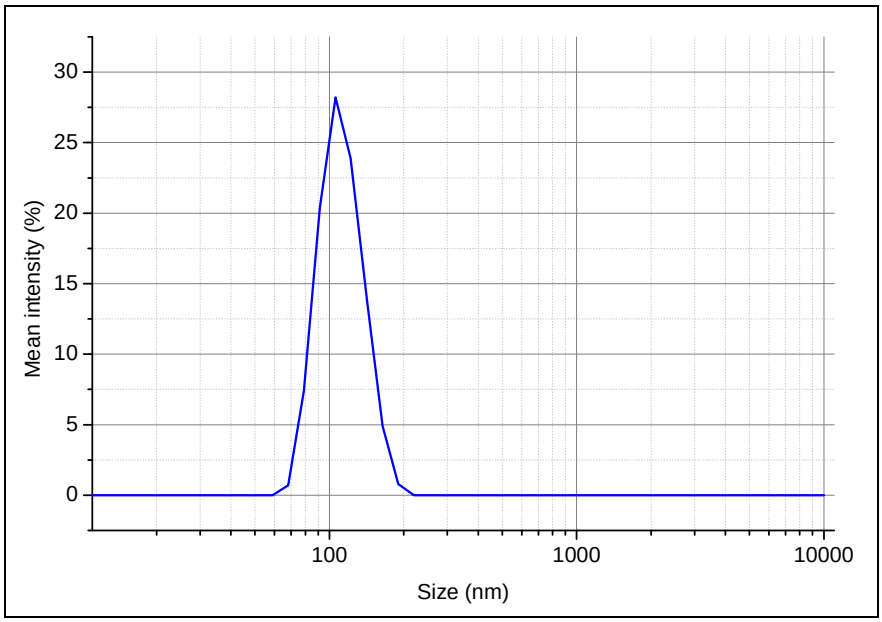


Figure 6.1: Size distribution of the suspended BST nanoparticles after completing the synthesis reaction (step 11). Sample is taken from the top portion of the synthesis mixture directly from the autoclave vessel. Peak = 113 nm.

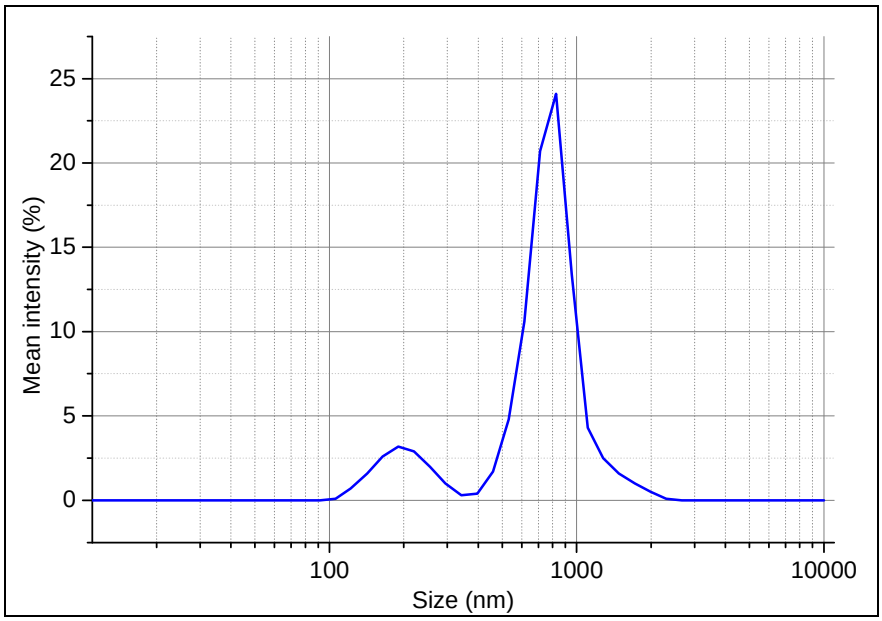


Figure 6.2: Size distribution of the BST nanoparticles taken during the final cycle of the cleaning procedure. Peak 1 = 202 nm, Peak 2 = 824 nm.

From the size distribution figures, three distinct peaks of 113 nm, 202 nm and 824 nm were detected. It is difficult to conclude which of the peaks is representative of the majority size of the nanoparticles due to limitation of the DLS technique, where the presence of larger particles obstructs the detection of smaller particles. Nonetheless, the measured peaks are still much larger than the expected nanoparticle size of 8-30 nm, even when considering the smallest recorded size value of 113 nm. Unfortunately, no information on the discrepancy of the nanoparticle size could be obtained from the authors of the paper citing the recipe. The most critical setback however, was the small amount of the synthesis product. From the 22 ml mixture that was prepared, only 90 mg of BST was obtained. This is insufficient for experiments requiring even modest loading of BST nanoparticles. For instance, a 8 wt% nanoparticle loading in 10 ml of PVP-BST solution will require 800 mg BST nanoparticles. This equates to a minimum completion of 9 syntheses for our available equipment. Although larger amounts of BST with smaller particle distribution may potentially be attainable in subsequent synthesis attempts, no further syntheses were conducted. The idea of pursuing small nanoparticles from self synthesis is concluded to be not feasible under the circumstances, as it would require a long duration for optimising the synthesis recipe, along with the high material costs to produce a sufficient amount of BST.

6.1.2.2 Commercial BST + PVP Solution

This section discusses the preparation of the PVP-BST solutions for 8 wt% (PVP-BST8), 16 wt% (PVP-BST16) and 24 wt% (PVP-BST24) nanoparticle loading using BST purchased from Sigma-Aldrich (product code 633828). The BST is in nanopowder form, with a specification of <100 nm particle size. The size distribution of the nanoparticles, measured using the Zetasizer, is shown in Figure 6.3. The BST nanoparticles were dispersed for 5 hours in ethanol using an ultrasonic bath. It is possible that the nanoparticles were still partially aggregated and not fully dispersed, resulting in the detection of larger particle sizes as shown by the size distribution.

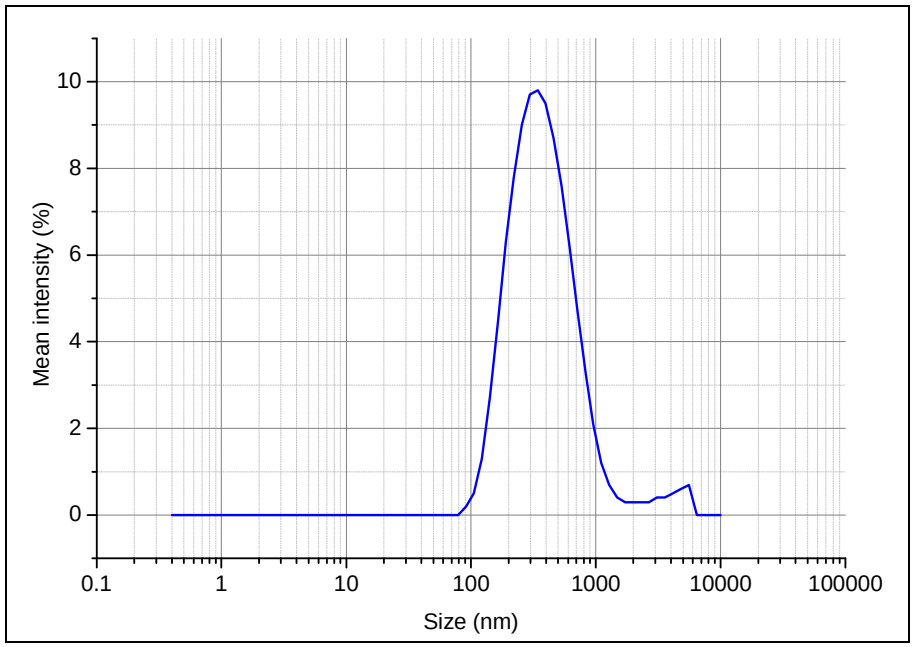


Figure 6.3: Size distribution of BST nanoparticles obtained from Sigma-Aldrich. Peak = 334nm.

PVP-BST Preparation

In the initial attempt, a straight forward blend was conducted by dispersing nanoparticles in the PVP solution using an ultrasonic bath for 1 hour. However, the solution prepared using this method could not be filtered as it would immediately clog the 0.45 μm syringe filters. Improvising, an additional high power sonication stage was employed to improve dispersion of the BST nanoparticles. To summarise the preparation process, BST is first added to the polymer solution and dispersed using two stages of sonication. Throughout the sonication, the solution is kept cool with ice to minimise solvent loss. After nanoparticle dispersion, the solution is centrifuged at

low rotational speeds for several hours to separate any large particles that are not in stable suspension. Finally, the PVP-BST solution is filtered through 0.45 μm and 0.2 μm PTFE syringe filters. The use of double filtering process is to prevent instantaneous clogging of the 0.2 μm filter in case large particles are still present after centrifugation.

1. Prepare 10 wt% PVP solution with PGMEA solvent.
2. Weigh the PVP solution and record initial solution + bottle weight.
3. Add BST nanopowder into the bottle using a spatula, to the desired BST loading. Determine precise amount of BST by weighing the bottle and comparing with the initial weight obtained in step 2. Full body protection (double gloves along with 3M respirator mask and goggles) must be worn for this step.
4. Seal bottle with its cap and place into ultrasonic bath for 1 hour to disperse the BST nanoparticles. Keep sonic bath temperature cool by using ice cubes or ice packs.
5. To further disperse the nanoparticles, perform sonication using a high power probe sonicator (Misonix Sonicator 3000). Fill a glass beaker with ice and position the solution bottle in the centre. Configure sonication cycle to be 1 minute on and 1 minute off intervals for a period of 1 hour. Dip sonicator probe into the solution and start sonication with a power setting of 3. The on-off intervals along with the use of ice filled beaker minimises solvent loss as the solution will heat up rapidly during sonication.
6. Add 5 wt% PMF cross-linker into the solution and stir with magnetic stirrers for 5 hours.
7. Transfer solution into a centrifuge tube, and centrifuge at 1500 rpm for 2 hours to push down the larger (heavier) nanoparticles. This forms a separation of suspended and precipitated nanoparticles.
8. Extract the top half portion of the solution from the centrifuge tube using a long metal tip syringe and transfer into a glass vial.
9. Filter extracted solution through a 0.45 μm PTFE (Acrodisc) syringe filter to remove large particles that remained after centrifugation.
10. Filter solution again through a 0.2 μm PTFE syringe filter.
11. Sonicate solution in ultrasonic bath for 30 minutes before usage.

The prepared nanocomposite solutions are milky white in colour that becomes less translucent with increased nanoparticle loading, as shown in Figure 6.4. Nanoparticle suspension is stable for approximately two weeks before a noticeable gradient in translucency is observed, as shown in Figure 6.5.

Figure 6.4: PVP-BST nanocomposite solution with 8, 16 and 24 wt% nanoparticle loading.

Figure 6.5: PVP-BST nanocomposite solution with 8, 16 and 24 wt% nanoparticle loading that have been stored in upright position after two weeks.

On average, 3 ml of PVP-BST nanocomposite solution can be extracted after the centrifugation step, from an initial 10 ml solution. It is important to note that the BST loading of 8, 16 and 24 wt% are not true representations of the nanoparticle loading in the final solution. The actual values are highly dependent on how the centrifugation step is performed. For the reported procedures, it is estimated that 50% of BST nanoparticles are removed after the centrifugation step. Theoretically, the centrifugation step can be accomplished with either low rotational speed over a long duration or, high rotational speed over a short duration. In the case of our processing, the low rotational speed method was employed to minimise the risk of having all of the dispersed nanoparticles pulled down. The ideal centrifugation speed to remove only the larger nanoparticles however, was not investigated. Nonetheless, it was reasonable to perform the centrifugation process at a speed of 1500rpm for 2 hours, as the incremental loading of BST nanoparticles is maintained. This is verified by the decreasing translucency of the solutions, from PVP-BST8 to PVP-BST24. Similarly, the higher the nanoparticle loading, the harder it is for the PVP-BST solution to pass through the PTFE syringe filters.

To evaluate the performance of using PVP-BST dielectric, the nanocomposite films were first characterised, followed by the fabrication of single transistors. PVP-BST dielectric thickness and surface uniformity were determined by surface profiling using AFM. Dielectric constant values were derived from the capacitance data, which in turn were obtained from impedance measurements of MIM capacitors. Single transistors with BGBC structure were fabricated as per procedures described in section 4.3. Physical and electrical characterisation of the nanocomposite layer is first discussed, followed by the discussion on fabricated single transistors.

6.1.3 Characterisation of PVP-BST Thin Films

Figure 6.6 shows the height encoded AFM scans of the surface of the PVP-BST thin films, where the lighter colours correspond to greater heights. The BST nanoparticles are clearly seen in the form of bright spots surfaced over the entire scanned area. The capacitance and surface roughness data are presented in Table 6.1.

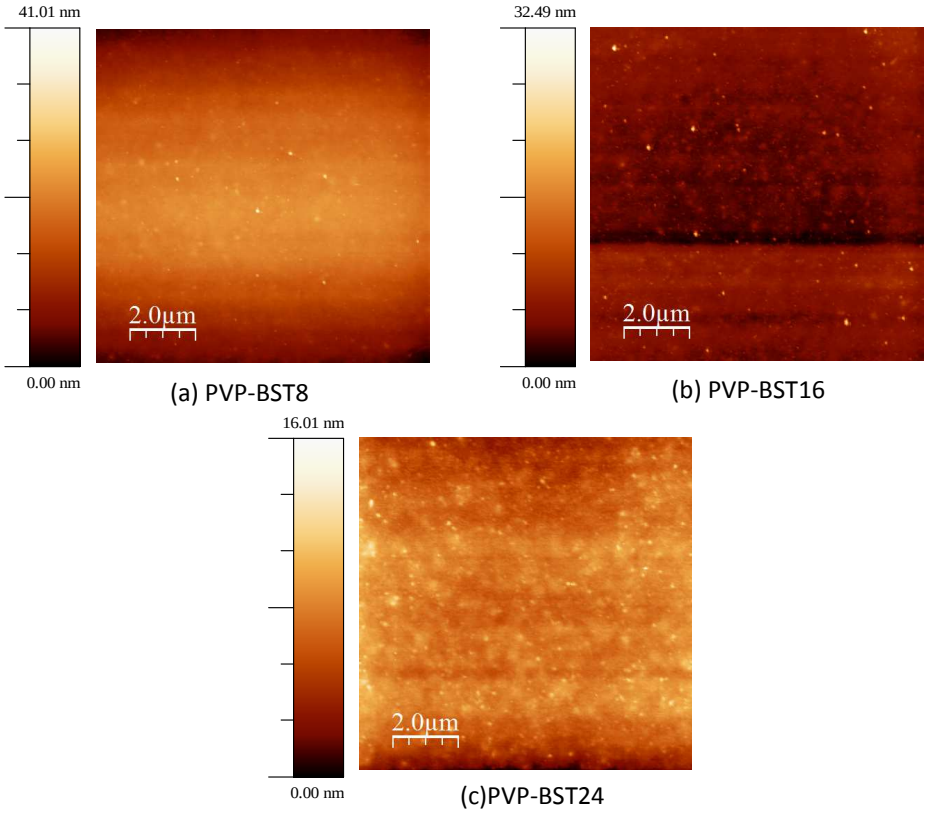


Figure 6.6: AFM surface scan of PVP-BST films.

Table 6.1: Comparison of the dielectric constant of PVP and PVP-BST dielectric.

Loading %	Frequency (Hz)	Capacitance (pF)	Thickness (nm)	Surface Roughness (RMS)	Dielectric Constant
0	200, 300	125	373	2.5 Å	4.38
8	300 – 15K	127	400	5.6 nm	4.77
16	300 – 1K	133	371	1.6 nm	4.62
24	300 – 2K	137	352	1.7 nm	4.53

From the data in Table 6.1, the measured capacitances are frequency dependent and capacitive phase shifts were obtained at a supply frequency of around 300 Hz for both PVP and PVP-BST films. However, the PVP-BST films maintained its capacitive

phase for a wider frequency range. Compared to the pure PVP films, the surface roughness values of the PVP-BST films increase approximately one order of magnitude to the single digit nanometer range, up to a maximum RMS roughness value of 5.6 nm for PVP-BST8. While a progressive increase in surface roughness proportional to the BST loading is expected, it is not the case as PVP-BST8 recorded the highest surface roughness. This is likely due to the greater amount of BST nanoparticles present at the particular scanned area of the PVP-BST8 film.

An interesting observation is on the film thickness. Despite maintaining the same spin-coating speed, the PVP-BST films were measured to be thinner with increased nanoparticle loading. This behaviour was also observed in a second fabrication attempt, and is consistent with the data reported by Yunseok *et al*. [154]. When using the film thickness data as obtained from surface profiling, the dielectric constant values decrease with increased nanoparticle loading. The highest dielectric constant achieved is 4.77 with PVP-BST8 and decreases to 4.53 with PVP-BST24. The maximum increase in dielectric constant is thus a factor of 1.09 over pure PVP, in contrast with a factor of 1.7 reported by Yunseok *et al*. using 11 % BST loading. In the second attempt, the measured dielectric constant values were 4.55 for PVP-BST8, 4.29 for PVP-BST16 and 4.22 for PVP-BST24.

It is worth noting at this point that the dielectric constant results require further analysis and should not be accepted as they are. In particular, the dielectric thickness data is inconsistent with the increase in BST nanoparticle loading, as thicker films are expected from the higher viscosity PVP-BST solutions. The inaccurate thickness data explains the small gain in dielectric constant values, since they are proportional to the dielectric thickness when using the parallel plate capacitor equation. It is also the reason for the small discrepancies in dielectric constant values between the two experiment attempts. The difficulty with obtaining accurate measurement of the dielectric thickness is discussed in the next section.

6.1.3.1 Investigation on PVP-BST Film Thickness

To explain the reduction of film thickness behaviour, the etched portion of the PVP-BST films were examined. With AFM surface profiling, it was discovered that a residual layer would form on the surface of the substrate. The location of the residual layer is illustrated in Figure 6.7, together with a phase image that shows the nanocomposite's edge profile.

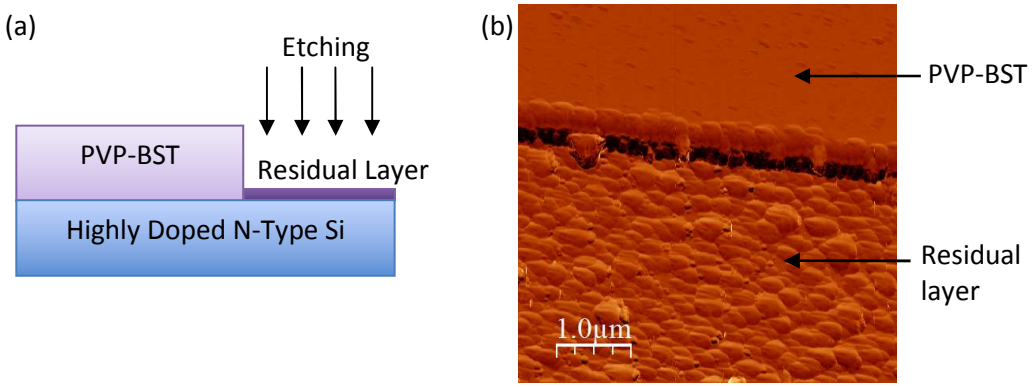


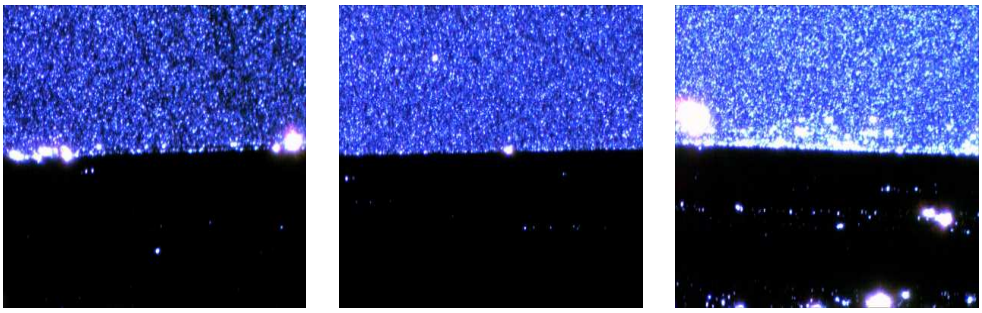
Figure 6.7: Residual layer formed by the oxygen plasma etch of PVP-BST (a). Phase image of the residual layer on SiO_2 (b).

Effectively, the presence of the residual layer prevents accurate thickness profiling of the nanocomposite layer. This is because the film height will appear to be lower than its actual value due to the elevated substrate surface.

The morphology of the residual layer suggests the aggregation of the BST nanoparticles which is unexpected, as the nanoparticles are suspended in a polymer matrix host. Therefore, the etching of PVP should have removed the nanoparticles as well, as seen with the distinct depth of the etched areas. The formation of the residual layer was initially thought to be due to the high temperature cross-linking step, whereby the use of high temperature processing caused aggregation of the BST nanoparticles that sunk to form the residual layer at the substrate-dielectric interface. This initial hypothesis led to the investigation of hydroxymethyl benzoguanamine (HMBG) as a low temperature cross-linker. The research team at IMEC reported that HMBG can be used to cross-link PVP [159] at a lower temperature of 130 °C. However, HMBG was not used in later experiments because the experiments that were conducted found that it is unable to cross-link PVP as effectively as PMF. The details on the usage of HMBG are reported in Appendix G.

The residual layer was later discovered to be a by-product of the etching process which adheres strongly to the substrate and cannot be removed by extended etching duration (>15 minutes) or solvent rinse (acetone, methanol, isopropanol). This behaviour is confirmed by etching the samples immediately after the deposition of the PVP-BST films, without first performing the cross-linking step. For this case, the residual layer continued to form on the substrates. In a second experiment, the formation of residual layer did not occur when the PVP-BST film is immediately stripped with acetone after its deposition. Based on the findings, it is proposed that the oxygen plasma reacted with the BST inherently suspended at the substrate-dielectric interface. Prior literature has also confirmed that BST thin films are not removed by oxygen plasma etching. Instead, the active oxygen ions from the plasma passivates the BST thin films by reducing oxygen vacancies [160].

To establish the relationship between nanoparticle loading and the formation of the residual layer, a cocktail stick was used to repeatedly scratch the residue area to expose the substrates. The scratched samples were then viewed under a microscope with 50x magnification (Figure 6.8), using dark field illumination with constant light intensity for all three samples.



PVP-BST8 PVP-BST16 PVP-BST24

Figure 6.8: Dark field illumination of the PVP-BST residual layer for 8-24 wt% nanoparticle loading.

It can be seen that the etching residue (blue colour) becomes brighter proportional to higher nanoparticle loading. The increased light scattering confirms that the residual layer for PVP-BST24 film is denser and likely thicker than the other PVP-BST films with lower nanoparticle loading. This could be the reason that the profiled PVP-BST24 film recorded the lowest thickness value among the three investigated PVP-BST solutions. Having established the presence of the residual layer, it is then

reasonable to reject the validity of the dielectric thickness data obtained with AFM surface profiling. With this interpretation, the increase in dielectric constant becomes more significant as even a small height addition to the measured thickness value can result in a rather large improvement to the dielectric constant value. For instance, the dielectric constant of PVP-BST8 increases to 5.36 by taking into account a 50 nm thick residual layer.

6.1.3.2 Estimation of Dielectric Constant Values Using Composite Mixing Rules

Since the dielectric constant values of the PVP-BST dielectric could not be accurately determined experimentally, this section will discuss the theoretical estimates from the known volumes and permittivities of the individual materials in the nanocomposite. Series (6.1) and parallel (6.2) mixing equations give the lower and upper limits of the dielectric constant values [161, 162] :

$$\varepsilon = V_1\varepsilon_1 + V_2\varepsilon_2 \,, \qquad (6.1)$$

$$\frac{1}{\varepsilon} = \frac{V_1}{\varepsilon_1} + \frac{V_2}{\varepsilon_2} \,, \qquad (6.2)$$

where ε_1 and ε_2 are the average dielectric constants of the materials in the composite, and V_1 and V_2 are their volume fractions.

The effective permittivity can be estimated using Lichtenecker's logarithmic mixing equation [163, 164], which assumes a combination of series and parallel interactions between the components of a composite material. For a nanocomposite dielectric comprising of two materials, the Lichtenecker's equation is given by (6.3).

$$\log \varepsilon = V_1 \log \varepsilon_1 + V_2 \log \varepsilon_2 \,. \qquad (6.3)$$

Table 6.2 presents the dielectric constant values calculated using the series, parallel and logarithmic equations. Also included for each nanoparticle loading is the data for the scenario where 50% of the BST nanoparticles are removed after the centrifugation stage during the PVP-BST solution preparation process. For the calculations, a dielectric constant value of 50 is assumed for the BST nanoparticles [152]. Detailed calculations are reported in Appendix K.

Table 6.2: Dielectric constant values calculated using series, parallel and logarithmic mixing equations.

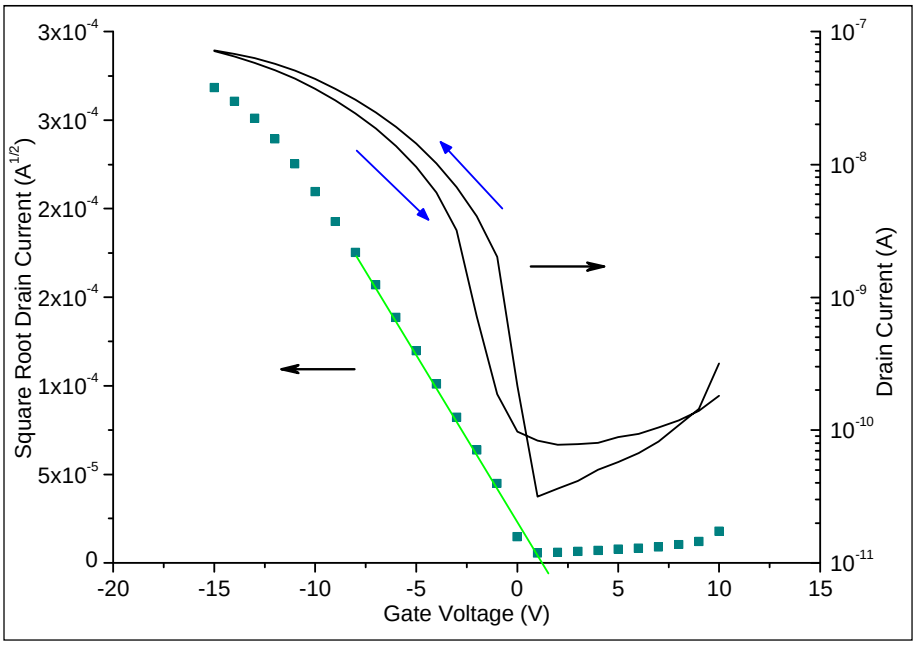
Solution	Dielectric Constant					
	Series	Series (50% BST Loss)	Parallel	Parallel (50% BST Loss)	Logarithmic	Logarithmic (50% BST Loss)
PVP-BST8	5.2	4.8	11.7	8.3	6.5	5.4
PVP-BST16	5.8	5.2	16.7	11.7	8.5	6.5
PVP-BST24	6.6	5.5	20.8	14.4	10.6	7.5

The calculated values indicate that the dielectric constant values obtained experimentally are in the expected range, under the assumption that the residual layer thickness is proportional to the nanoparticle loading. Consider the case for PVP-BST8. As previously discussed, the dielectric constant value for PVP-BST8 is 5.36 when correcting for the actual dielectric thickness value by taking into account a 50 nm thick residual layer. The corrected value compares well with the value calculated using the logarithmic equation ($\varepsilon = 5.4$), for the case where 50% BST is lost after centrifugation.

6.1.4 Single Transistor Results

The following figures show the measured characteristics of the single transistors fabricated using PVP-BST 8 to 24 wt%. The PVP-BST dielectric layer is thermally cross-linked in a similar manner as with the regular PVP films, using the steps described in chapter 4, section 4.3. Table 6.3 compiles the performance matrices of the fabricated single transistors.

(a)



(b)

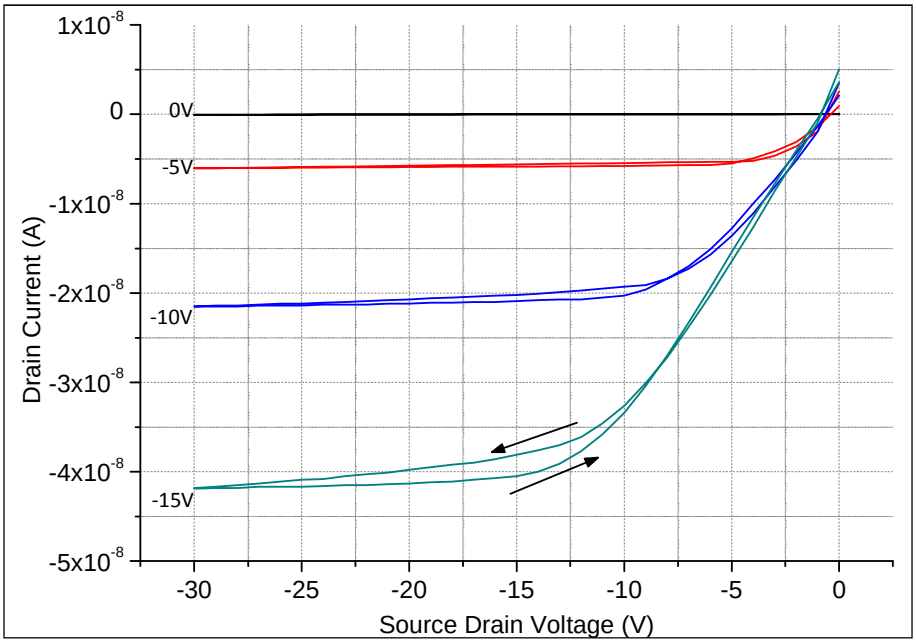
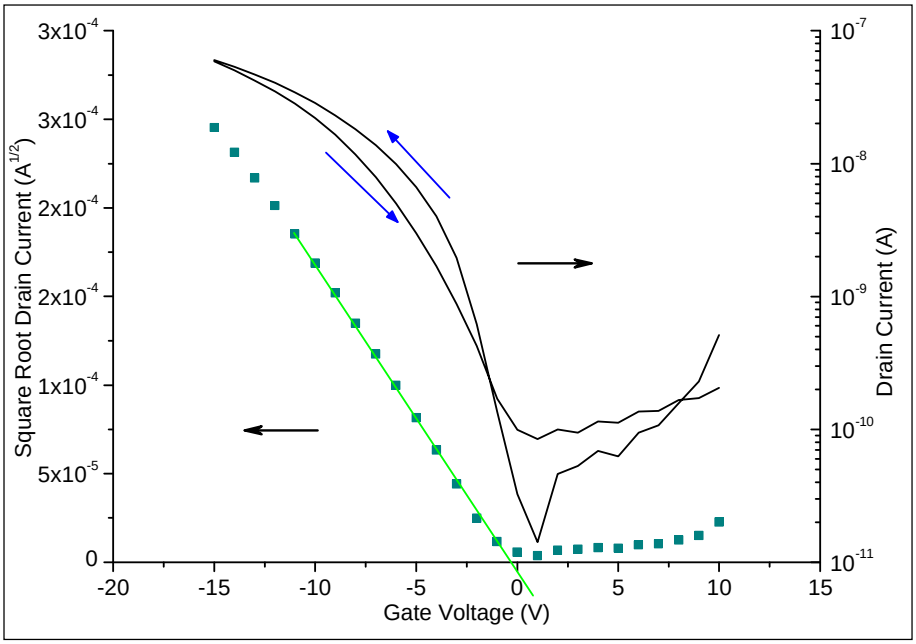


Figure 6.9: I_d-V_g (a) and I_d- V_{ds} (b) characteristics of a PVP-BST8 single transistor. W=2 mm and L=60 µm. The square root curve is from the forward voltage sweep.

(a)



(b)

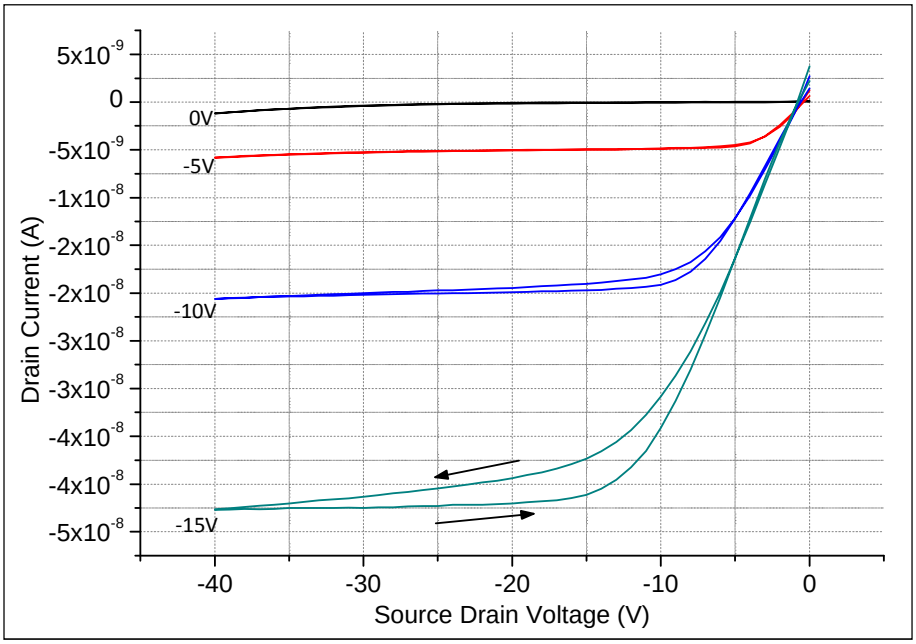
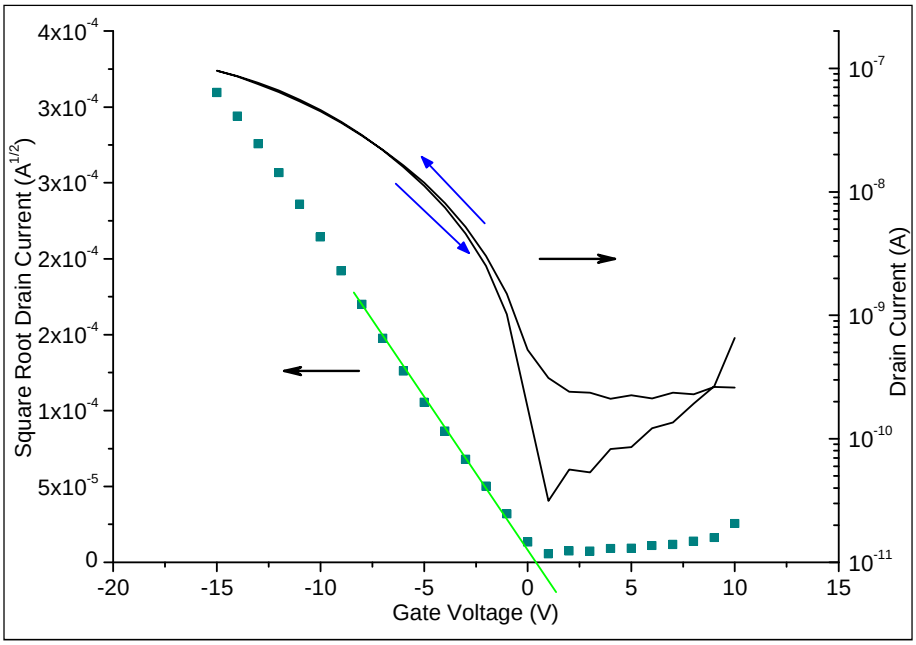


Figure 6.10: I_d-V_g (a) and I_d- V_{ds} (b) characteristics of a PVP-BST16 single transistor. W=2 mm and L=60 μm. The square root curve is from the forward voltage sweep.

(a)



(b)

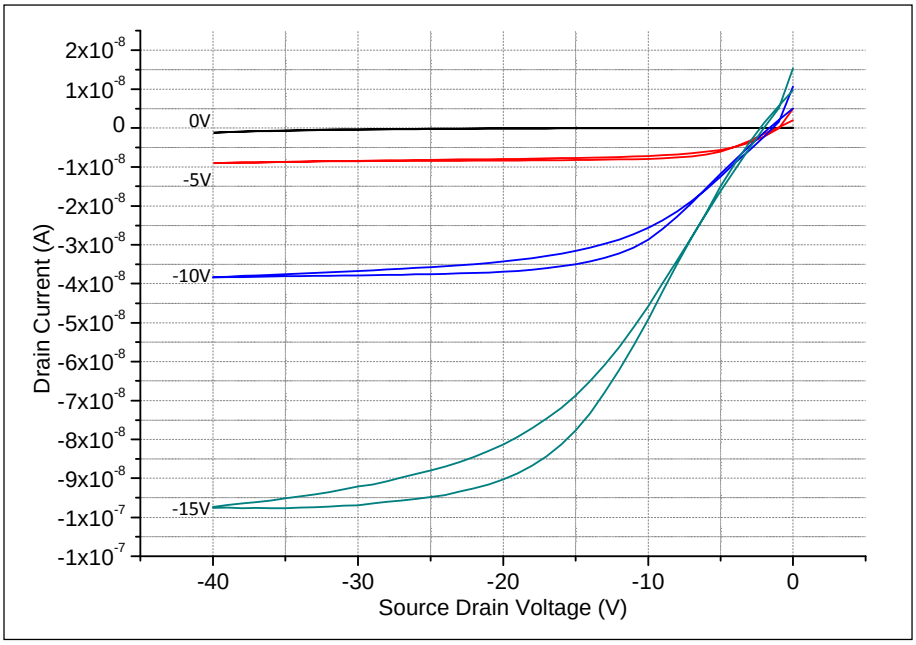


Figure 6.11: I_d-V_g (a) and I_d- V_{ds} (b) characteristics of a PVP-BST24 single transistor. W=2 mm and L=60 μm. The square root curve is from the forward voltage sweep.

Table 6.3: Performance matrices of PVP-BST transistors for 8 to 24 wt% loading. Mean values calculated from four measured devices.

BST Loading (wt %)	V_{th} (V)	On-off ratio	Mean On-off ratio	Sub-threshold swing (V/dec)	Mean Sub-threshold swing (V/dec)
8	1.4	$2x10^3$	$1.8x10^3 \pm 0.7x10^3$	1.2	1.6 ± 0.4
16	0.48	$4x10^3$	$3.1x10^3 \pm 0.9x10^3$	1.3	1.8 ± 0.3
24	0.16	$3x10^3$	$2.7x10^3 \pm 0.3x10^3$	1.3	1.8 ± 0.5

The mobility data are not included in Table 6.3 because the calculations require the dielectric thickness data, which could not be accurately determined as mentioned previously. The following discussion thus addresses the other performance indices, which gained subtle improvements from the addition of BST nanoparticles to the PVP dielectric layer. With reference to the transistor characteristics (Figure 6.9, Figure 6.10, Figure 6.11), single transistors fabricated using PVP-BST show reduced hysteresis, which is apparent with the I_d-V_{ds} (output characteristics) curves. Sub-threshold swing improves to as low as 1.2 V/decade. A yield of 44% was obtained by measuring 63 transistors comprising of samples with all three nanoparticle loading percentages, suggesting that the spin-coating speed of 3500 rpm must be lowered to obtain thicker pin-hole free PVP-BST films.

6.1.5 PVP-BST Nanocomposite for Logic Circuits

This section investigates the compatibility of the PVP-BST nanocomposite with the logic circuit fabrication process. As reported previously, the formation of a residual layer occurs when etching PVP-BST with oxygen plasma. For the BGBC logic circuits, the residual layer would form upon the gate electrode layer as shown in Figure 6.12. Given its dense morphology, its presence might prevent the formation of vias and interconnects between the source/drain and gate electrodes. The issue of the residual BST layer needed to be addressed and investigated, since it might mean that the practical usage of PVP-BST is limited to devices that do not require vias and interconnects, unless, an alternative residue free technique for patterning the PVP-BST dielectric layer is discovered.

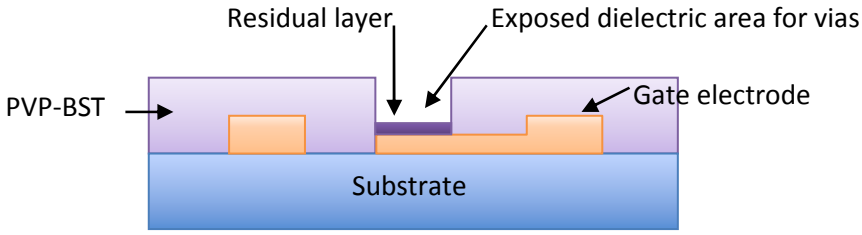


Figure 6.12: Formation of the residual layer on the gate electrode interconnect area.

Attempting to circumvent the formation of the residual layer, the use of an underlying sacrificial layer was investigated. The concept is to first coat the substrate with a thin sacrificial layer before the deposition of the nanocomposite film. The additional layer serves as a temporary platform at the substrate-dielectric interface, where its removal during the etching step would also remove the residual layer formed on top of it. If successful, the plasma etched dielectric areas will show smooth surface morphology of the Si-SiO_2 substrate when profiled with AFM. For the experiment, a bottle of dilute PVP 1 wt% solution was prepared. First, the solution is spin-coated onto the substrate at 4000 rpm and subsequently cross-linked. The resulting sacrificial layer is ~25 nm thick, measured using AFM. Next, PVP-BST16 is spin-coated onto the sacrificial layer and cross-linked. Half the PVP-BST16 film is then etched. The sample is profiled using AFM to assess the morphology of the etched areas.

However, the use of the sacrificial layer was unsuccessful, as the etching by-product continued to remain on the substrate. Figure 6.13 shows the phase image of the

nanocomposite's edge profile, where both the PVP-BST16 and the residual layers are clearly seen. It is possible that the dense packing of the residual layer prevented the oxygen plasma from penetrating through to the underlying layer, rendering the sacrificial layer ineffective.

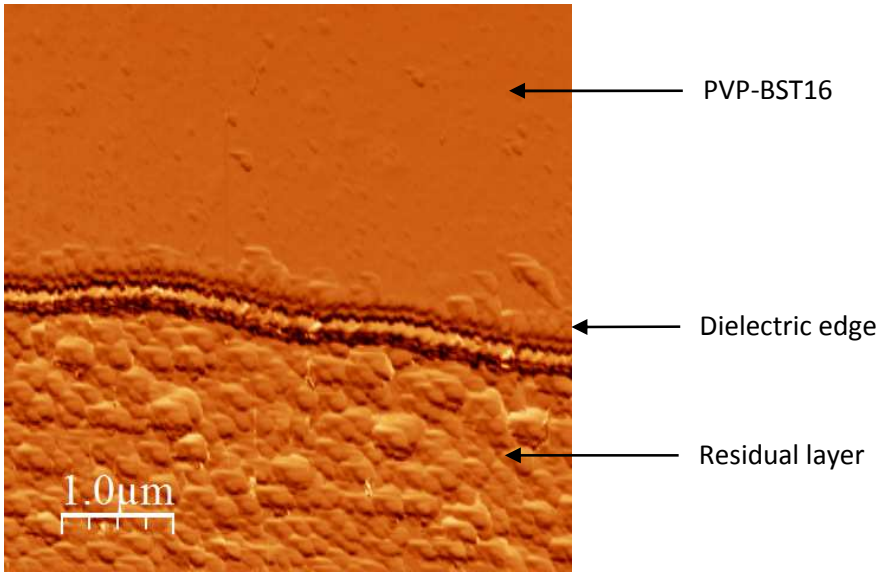


Figure 6.13: AFM phase image of the etched PVP-BST area when using the sacrificial layer.

In a second experiment, a post deposition processing approach was employed. The experiment investigates the use of aqua regia as an etchant to remove the residual layer after it has been formed. For this experiment, the aqua regia solution was prepared by mixing 3 parts of hydrochloric acid 36% (HCL) with 1 part of 70% nitric acid (HNO_3).

Unfortunately, this experiment also did not yield positive results, as cracks would form on the PVP-BST films within 2 minutes of rinsing samples in the aqua regia solution. Figure 6.14 shows the before and after images of a plasma etched PVP sample that is rinsed in aqua regia. The images were captured using identical white balance settings. Formation of cracks is clearly seen on the post-rinsed sample. The change in colours suggest thinning of both the PVP dielectric and the residual layer. There are also other concerns with this post deposition processing approach. The use of aqua regia may be incompatible with the BGBC logic circuit fabrication process, as it etches gold at an approximate rate of 2 µm per minute in the vertical direction. This

can damage the first layer gate electrodes if samples are over-etched, both in the vertical and lateral direction.

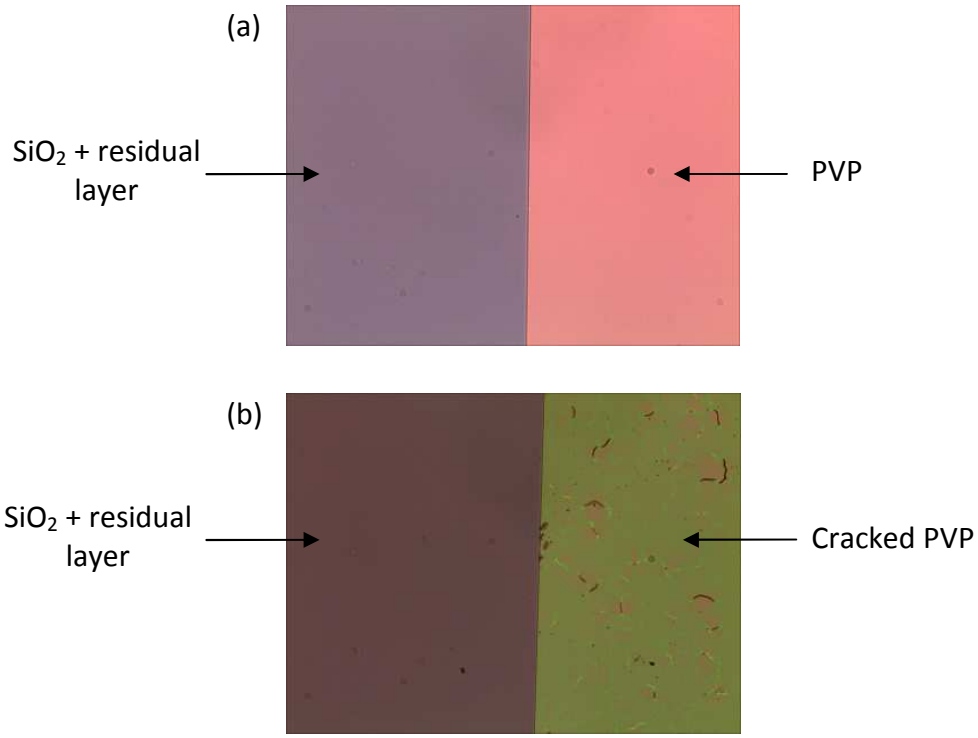


Figure 6.14: Before (a) and after (b) images of a PVP sample rinsed in aqua regia for 2 minutes.

The use of more aggressive gases to etch the PVP-BST dielectric layer was also considered. Kim *et al*. [165] reported that several gas mixtures (Cl_2/Ar, CF_4/Cl_2/Ar, BCl_3/Cl_2/Ar) can be used with reactive ion etching (RIE) to etch BST. However, this approach was not put to test as these gas mixture combinations are not allowed to be used with the plasma etcher in EEE.

At this point, a decision was made to proceed with the fabrication of inverters to assess the effect of the residual layer on the formation of vias and interconnects. Interestingly enough, the residual layer did not interfere with the formation of vias and interconnects as logic circuits were successfully fabricated.

6.1.5.1 Inverter Circuit Results

The PVP-BST16 solution was used in the fabrication of the inverters. For the spin-coating step, the Headway Research Inc spin-coater was set to 3000 rpm. All other processing steps are as described in section 4.5. The V_o-V_{in} characteristics for the zero-V_{gs} inverters are shown in Figure 6.15 and Figure 6.16. The V_o-V_{in} characteristics for the diode-load inverters are shown in Figure 6.17 and Figure 6.18. The inverter gains are compiled in Table 6.4.

A yield of 100% was achieved from a sample size of two, which consisted of 20 transistors in total. The devices constructed with the transistors include 8 inverters and 4 single transistors. This amount of functional logic circuits and single transistors was deemed sufficient to confirm the compatibility of PVP-BST with the logic circuit fabrication process. For the large inverters, maximum gains of 3 (zero-V_{gs}) and 6.2 (diode-load) were obtained at V_{ds} = -40 V. The maximum gains for the small inverters are approximately 1. The channel features for the driver and load transistors are reported in the caption for each figure.

Table 6.4: Gain of inverters fabricated using PVP-BST16.

V_{ds} (V)	Max Gain			
	Zero-V_{gs} (large)	Zero-V_{gs} (small)	Diode-load (large)	Diode-load (small)
-10	2.5	1.2	1.4	0.6
-20	2.6	1.4	3.2	1
-30	2.9	1.3	4.3	1
-40	3.3	1	6.9	1

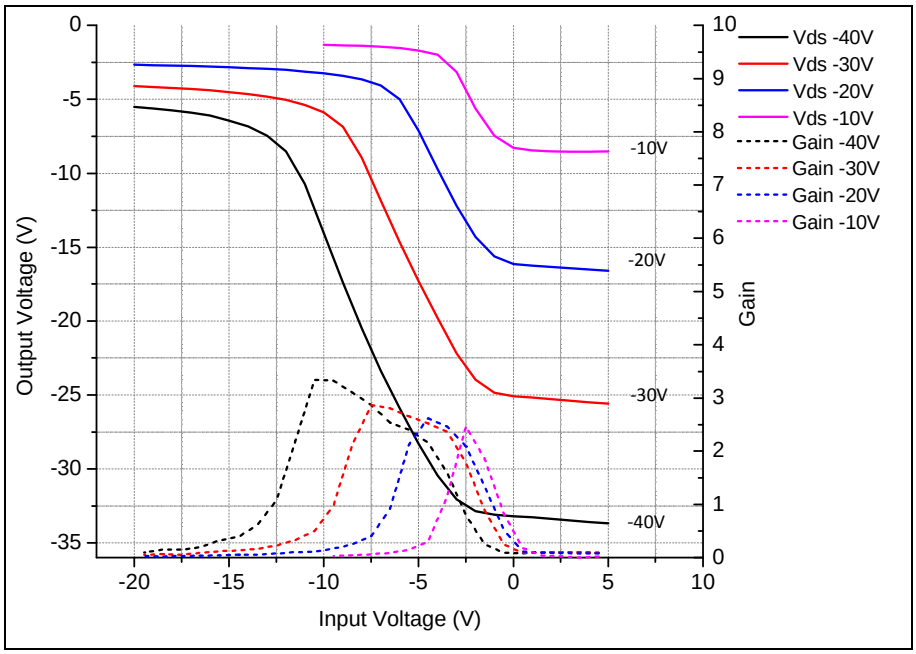


Figure 6.15: V_o-V_{in} characteristics of a large zero-V_{gs} inverter using PVP-BST16 dielectric for V_{ds} -10 to -40 V. Driver transistor, W=125 µm L=10 µm. Load transistor, W=1 mm L=10 µm.

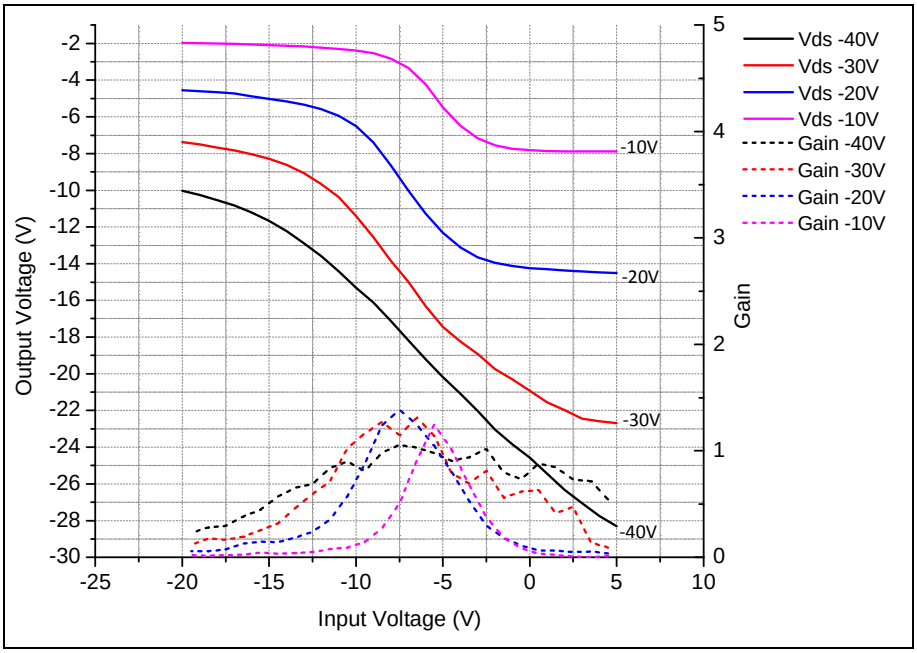


Figure 6.16: V_o-V_{in} characteristics of a small zero-V_{gs} inverter using PVP-BST16 dielectric for V_{ds} -10 to -40 V. Driver transistor, W=20 µm L=10 µm. Load transistor, W=160 µm L=10 µm.

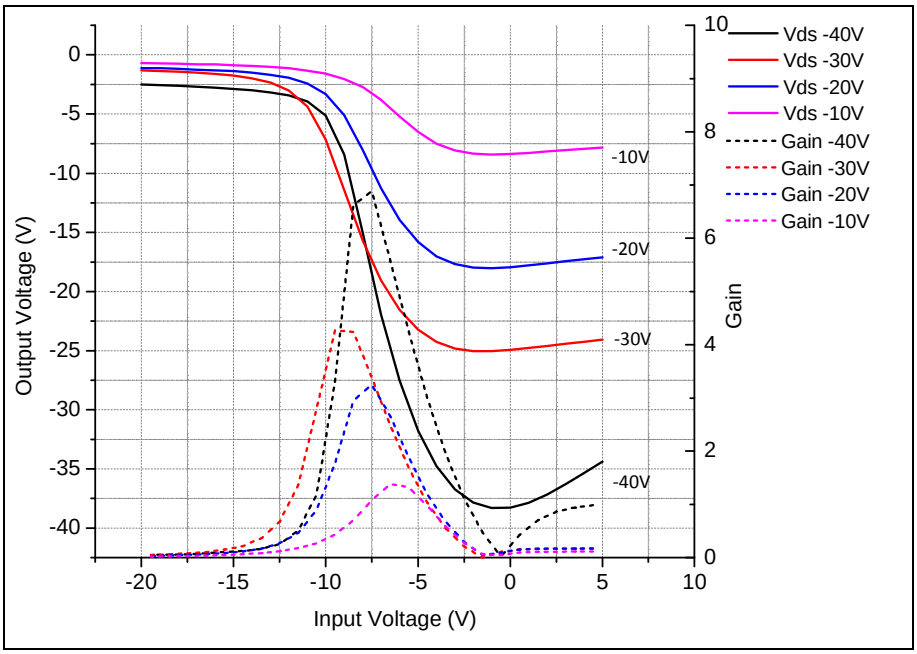


Figure 6.17: V_o-V_{in} characteristics of a large diode-load inverter using PVP-BST16 dielectric for V_{ds} -10 to -40 V. Driver transistor, W=1 mm L=10 µm. Load transistor, W=125 µm L=10 µm.

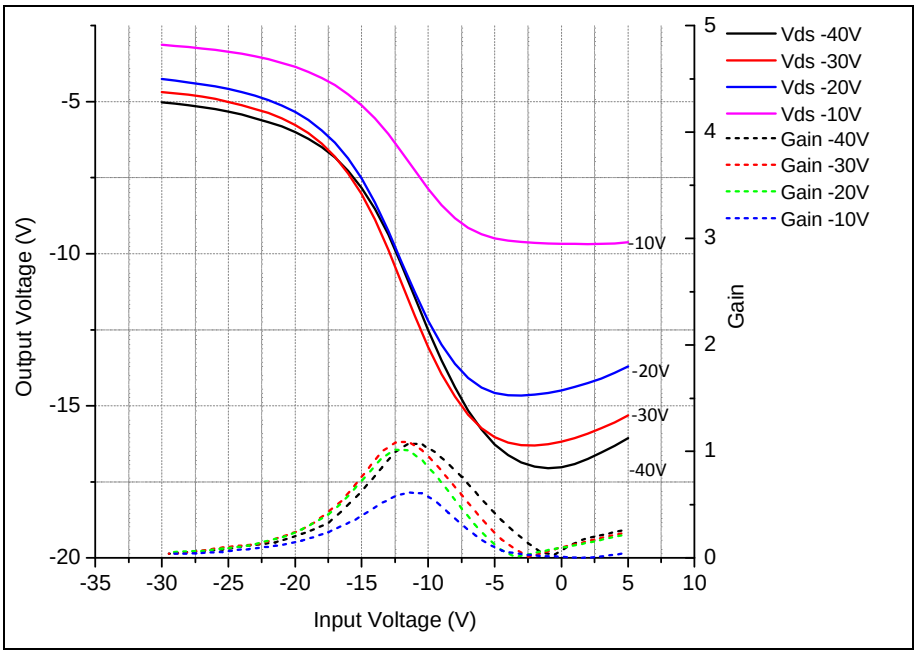


Figure 6.18: V_o-V_{in} characteristics of a small diode-load inverter using PVP-BST16 dielectric for V_{ds} -10 to -40 V. Driver transistor, W=160 µm L=10 µm. Load transistor, W=20 µm L=10 µm.

The attained 100% yield confirms that the vias and interconnects were successfully formed for each inverter despite the presence of the residual layer. To investigate the reason for this, an experiment was conducted to examine the morphology of the BST residual layer that is formed on the first level gate layer. Figure 6.19a shows the surface scan of thermally evaporated gold layer. Figure 6.19b shows the surface scan of the BST residual layer formed on 50nm thermally evaporated gold. The circular particle-like features on the residual layer image is clearly distinguishable from the pristine gold image. With reference to the phase image (Figure 6.19c), the residual layer appear to be less densely packed when formed on gold surface. Therefore, it is likely that the deposition of the circuit vias were unaffected because the evaporated gold particles were able to pass through the micro pores of the residual layer to form conducting paths with the gate layer. It can also be seen from the phase image that the diameters of the residual layer particles are around 200 nm, which could be from the aggregation of the 100 nm BST nanoparticles from Sigma-Aldrich.

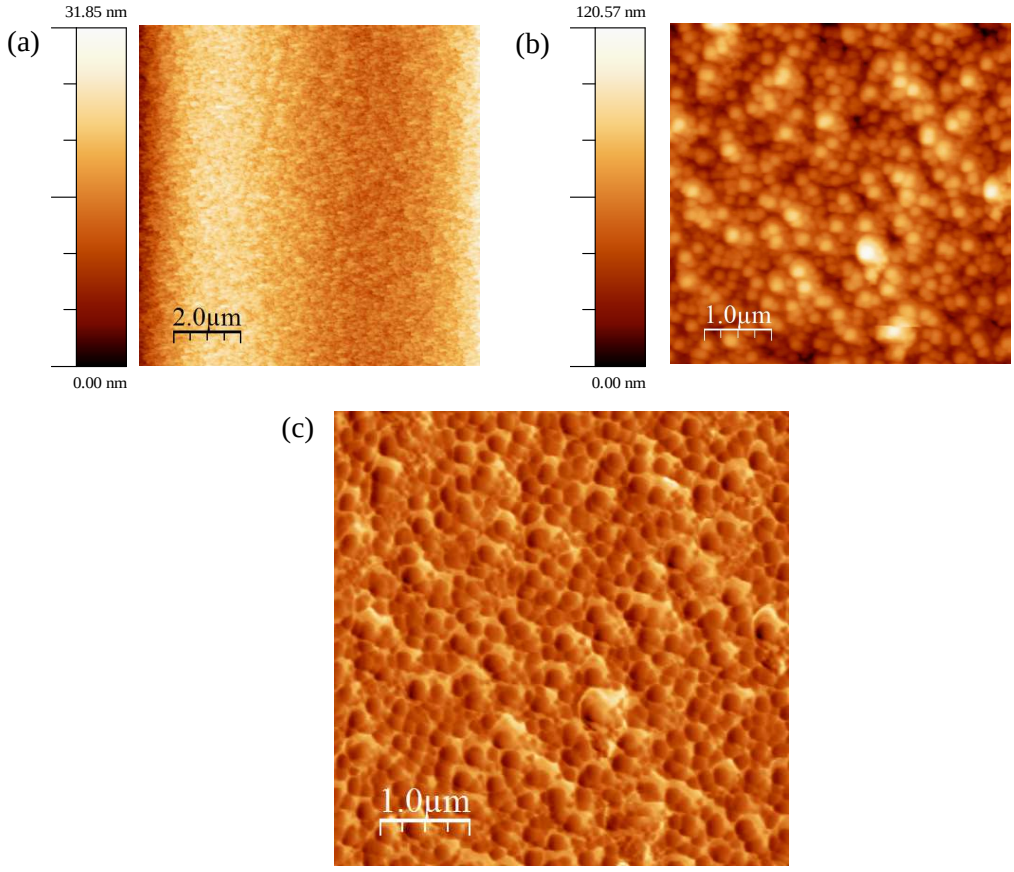


Figure 6.19: AFM image of the surface of gold (a) and etched PVP-BST (b) on gold. Phase image of etched PVP-BST on gold (c).

6.1.6 PVP-BST Dielectric Discussion

In this study, BST nanoparticles were used in conjunction with PVP polymer to form nanoparticle-polymer composites. The use of self synthesized BST nanoparticles with narrow size distribution (8-30 nm) was initially intended for the PVP-BST solutions. This approach did not turn out as planned, as the size of the synthesized BST nanoparticles was measured to be over 113 nm. Furthermore, the amount of BST nanoparticles obtained from a single synthesis (90 mg per 22 ml mixture) is insufficient for preparing the PVP-BST solutions. Thus, the experiments had to use BST purchased from Sigma-Aldrich with a specification of <100 nm. The difficulty with the latter approach is that commercial BST nanoparticles may contain a wider size distribution than the quoted specification. Fortunately, the larger or aggregated nanoparticles can be separated from the PVP-BST solution via centrifugation in the solution preparation stage. For future preparation of the PVP-BST solution, one improvement for the centrifugation step can be considered to maintain the initial loading of the nanoparticles. The centrifugation process should use slower rotational speeds as well as shorter spin duration to minimise precipitation of the BST nanoparticles, thereby reducing the amount of BST nanoparticles lost after centrifugation.

The characterisation of PVP-BST films yielded very interesting results. RMS surface roughness increased by one order of magnitude compared to pure PVP, to the single digit nanometre range. Data obtained from AFM surface profiling give decreasing film thickness values with the increase in nanoparticle loading. However, the thickness data is inaccurate due to the formation of by-product (residual layer) when etching PVP-BST with oxygen plasma. This in effect raises the height of the substrate and results in thinner thickness readings for the PVP-BST films. As a result, the increase in material permittivity is small when the calculations use the thickness data obtained from surface profiling. The residual layer is likely to be a thin layer of aggregated BST that is approximately 100 – 200 nm thick, following the size specification of the BST nanopowder purchased from Sigma-Aldrich. Since the residual layer prevented accurate profiling of the film thickness, it is proposed that the dielectric constant values are actually higher than the measured data.

Without accurate dielectric thickness data, the device performance metrics such as mobility, dielectric constant and dielectric strength could not be accurately calculated. Nonetheless, several observations can be made from the analysis of the measured characteristics.

The data for PVP-BST8 confirm that the addition of BST nanoparticles increases the overall dielectric constant, even when calculations do not take into account the height of the residual layer. The higher on-off ratios of the single transistors suggest that the PVP-BST films have similar or better dielectric performance compared to pure PVP. While the increased dielectric constant and good dielectric properties are positive findings, there are other factors that contribute to the overall performance of a dielectric layer.

From the single transistor transfer characteristics, the drain currents of the PVP-BST single transistors are similar at the maximum applied voltage of 15 V, in the 10^{-8} A range, when compared to the reference PVP device. Therefore, it can be deduced that no significant operational voltage reduction is attained with the PVP-BST dielectric, when its deposition is performed in a similar fashion as PVP dielectric. The similarity in processing refers to the resulting dielectric thickness, e.g. with spin-coating speed = 3500rpm (Headway Research Inc EC101 spin-coater), PVP-BST > 400 nm whereas PVP = ~370 nm. Under such a condition, several factors can explain the lack of significant increase in device performance.

First, despite the increase in dielectric permittivity, the density of accumulated charge carriers in the channel may not necessarily increase significantly when biased with similar voltage potentials as the reference device, due to the thicker PVP-BST films. Second, it is likely that the positive effect from the increased dielectric constant is negated by the presence of BST nanoparticles suspended at the dielectric-semiconductor interface. Previous studies [166, 167] have shown that mobility can decrease several orders of magnitude when the dielectric interface is rough, due to scattering and localisation of charge carriers. It is also possible that the surface energy of PVP-BST results in a less favourable morphology of the TIPS-pentacene grains, reducing the mobility of charge carriers.

In this work, two strategies were investigated to address the formation of the PVP-BST residual layer. The first method involves the use of a sacrificial layer, serving as a temporary platform for the residual layer. The second method employed aqua regia as an etchant to remove the residual layer. Unfortunately, neither method was successful in the prevention or removal of the residual layer. The mentioned techniques, albeit being unsuccessful, are from the practical perspective, as measures to prevent potential complications with the fabrication of logic devices. It is nonetheless useful to obtain the PVP-BST dielectric thickness data for other research purposes. One potential solution would be to employ other thickness measurement techniques such as focused ion beam or ellipsometry. It may also be possible to prevent the formation of the residual layer, by the use of the alternative PVP photochemical patterning process as discussed in Chapter 3, section 3.3.1.1. Since oxygen plasma is not used in the photochemical patterning approach, the formation of the residual layer will likely not occur.

To obtain more significant device performance improvements, it may be necessary to use PVP-BST solutions of higher nanoparticle loading, e.g. 50 wt% for 10 wt% PVP. In this case, the dielectric layer will likely require an additional smoothing layer due to the increased surface roughness. This can be accomplished using a thin layer of spin-coated PVP, deposited after cross-linking the first PVP-BST layer.

It is clear from this study that the use of nanocomposites is quite challenging both in preparation of the solution and fabrication of devices, where compatibility of the nanocomposite with the fabrication processes must be considered. Despite the initial difficulty in the characterisation of PVP-BST, the work discussed in this section is the first report on the successful incorporation of PVP-BST dielectric with the BGBC logic circuit fabrication process. Both the zero-V_{gs} and diode-load inverter circuits were successfully fabricated, with a 100% yield attained over 20 characterised transistors that form the logic circuits. It is to be noted however, that the experiment confirming the compatibility of PVP-BST with the logic circuit fabrication process was conducted using PVP-BST16. From optical microscopy of the residual layer, it is known that its density increases with increased nanoparticle loading. Therefore, at higher nanoparticle loadings, the formation of vias and interconnects may potentially

be disrupted if the thermally evaporated gold cannot pass through the dense packing of the aggregated BST residual layer.

6.2 Contact Layer Optimisation

6.2.1 Introduction

The usage of thiol based SAMs is quite common in the fabrication of OFETs to improve the performance of gold contact electrodes. The surface properties of gold can be modified by capping its surface with SAMs such as 1-hexadecanethiol [168], octadecanethiol (ODT) [169] and pentafluorobenzene thiol (PFBT) [170]. Such surface modification typically results in improved ordering and wetting of the semiconductor at the contact interface, hence improving overall device performance. This section discusses the use of PFBT SAM, formed on the gold source/drain contact electrodes via liquid deposition for the PVP and TIPS-pentacene transistor stack. Figure 6.20 shows the chemical structure of PFBT.

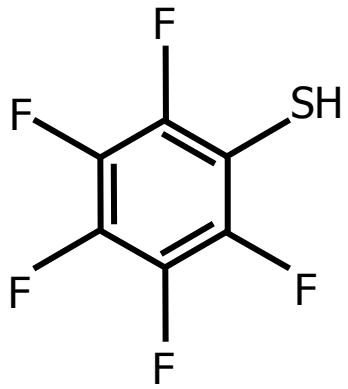


Figure 6.20: Chemical structure of PFBT. Image adapted from Sigma-Aldrich [171].

6.2.2 Experimental

Single transistors were fabricated for this experiment. The fabrication method described in chapter 4 (section 4.3) is used, with the addition of the SAM treatment step where samples are submerged in 10^{-2} mol/L PFBT (Aldrich, product code P5654-5G-A) solution (using isopropanol as the solvent) for 1 hour before the deposition of the semiconductor layer. The monolayer is formed on the gold source/drain electrodes and does not appear to degrade the dielectric properties of PVP.

6.2.3 Results and Discussion

Figure 6.21a and Figure 6.21b show the I_d-V_g and I_d-V_{ds} curves of a single transistor with PFBT modified contacts.

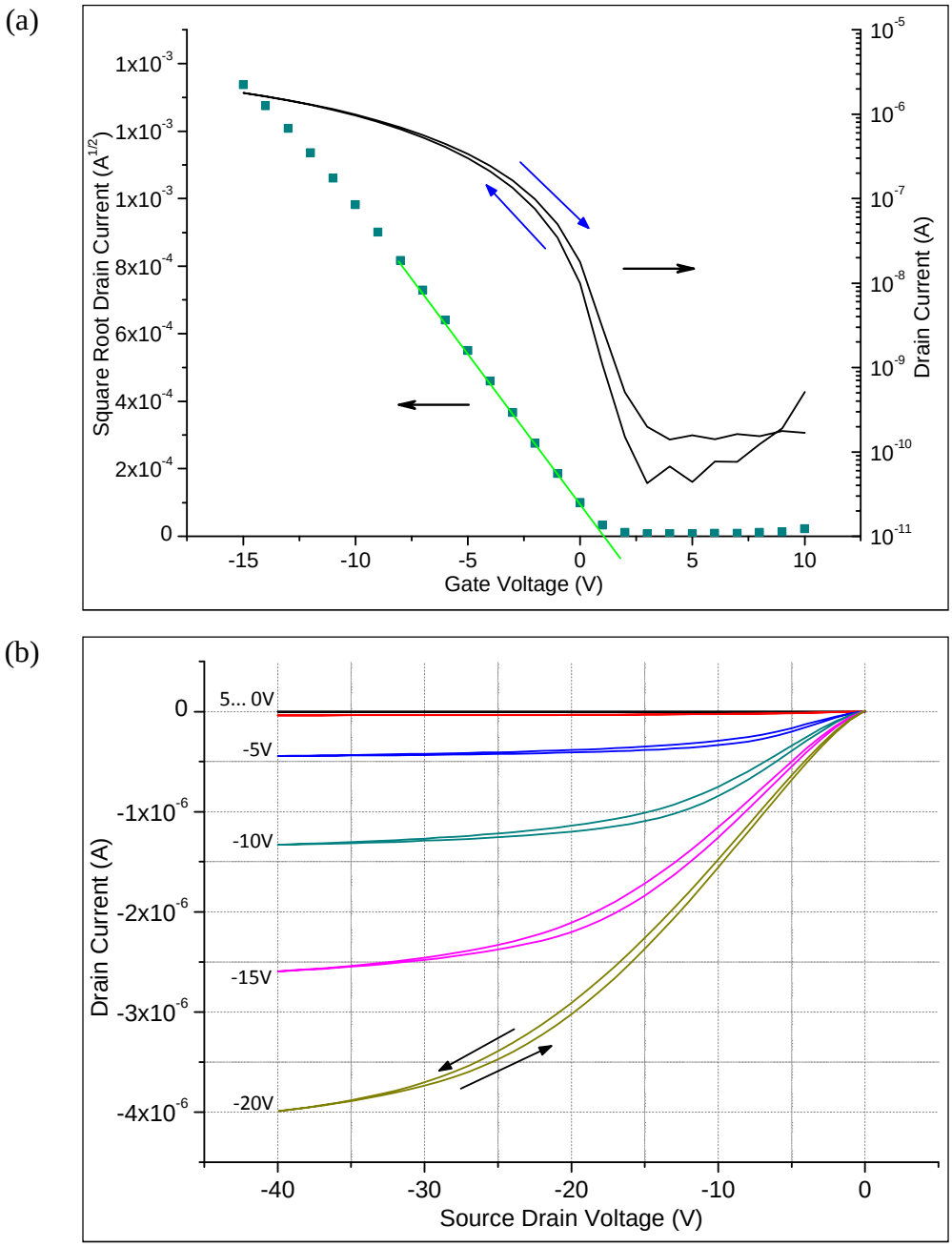


Figure 6.21: I_d-V_g (a) and I_d-V_{ds} (b) characteristics of a transistor treated with PFBT. Channel length 60 μm, channel width 2 mm.

Table 6.5: Performance metrics of the transistor treated with PFBT. Mean values are over 7 devices.

Transistor Parameters	Value	Mean Value
Threshold Voltage (V)	1.07	1.49 ± 1.1
Inverse Sub-threshold Slope (V/dec)	1.1	1.27 ± 0.32
On-off Ratio	$4x10^4$	$3.3x10^4 \pm 2.9x10^4$
Mobility (cm^2/Vs)	$4.8\ x10^{-2}$	$2.7x10^{-2} \pm 1.8x10^{-2}$

For this particular transistor, the mobility is calculated to be 4.8 $x10^{-2}$ cm^2/Vs, the inverse sub-threshold swing is 1.1 V/decade, the threshold voltage is 1.07 V and the on-off ratio is 41,000. The performance numbers indicate a clear improvement in all of the calculated transistor characteristics, when compared to the reference PVP + TIPS-pentacene device. Inverse sub-threshold slope improves as well to approximately 1 V/decade. Hysteresis is almost eliminated but not negligible, in contrast to the relatively moderate hysteresis with untreated devices discussed previously (chapter 5, section 5.2).

Average performance and deviations over 7 devices were also as expected when using the TIPS-pentacene semiconductor, with mean values of 1.49 V for threshold voltage, 1.27 V/dec for subthreshold swing, 3.3 $x10^4$ for on-off ratio and 2.7 $x10^{-2}$ cm^2/Vs for mobility. However, a relatively large standard deviation of 2.9 $x10^4$ was calculated for the on-off ratio. The data show that PFBT SAM treated contacts increase transistor mobility and on-off ratio by about one order of magnitude. Another interesting observation is on the threshold voltage of the SAM treated devices. As shown in Figure 6.22, all of the measured samples have a positive and varying threshold voltage, suggesting that there could be a small 1-2 V positive voltage shift. However, it is more difficult to substantiate this finding due to the intrinsic variability of V_{th} when using spin-coated TIPS-pentacene. There is a possibility that the TIPS-pentacene grains are orientated in a manner that result in positive V_{th} for all of the measured samples.

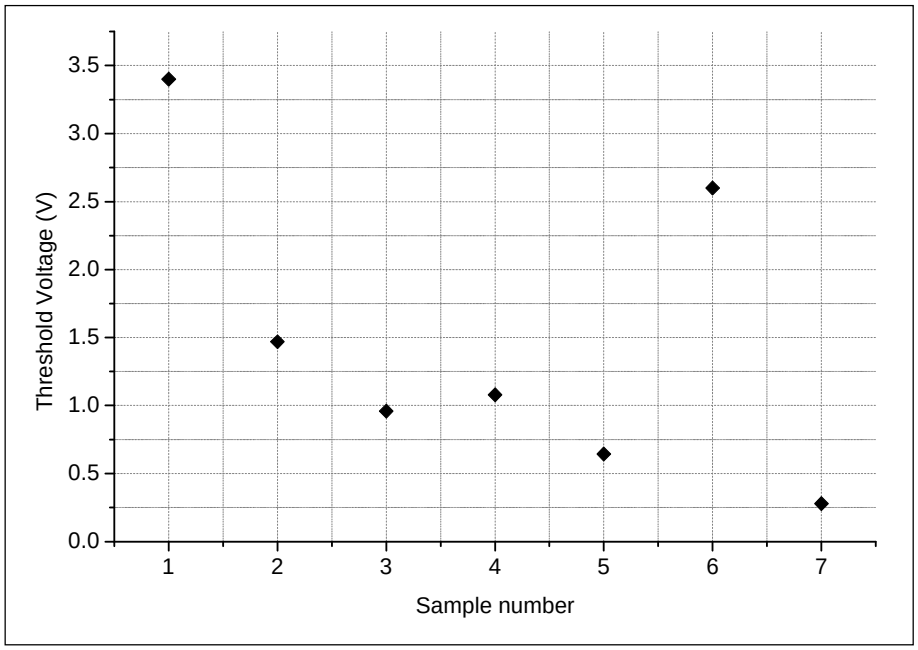


Figure 6.22: Threshold voltage values for 7 transistors treated with PFBT.

Considering its relatively simple processing, the use of PFBT modified contacts give a very significant increase in performance for the PVP + TIPS-pentacene transistor. The performance improvement mechanism has been previously discussed by Gundlach *et al.* [170] and Kyu [172]. Compared to untreated gold [173], the lower surface energy (θ_{H2O} = 86°) of PFBT modified gold appears to promote favourable wetting of the 1 wt% TIPS-pentacene solution (in DCB) at the contact interface, as demonstrated by the improved performance characteristics. When used with amorphous semiconductors, both Gundlach *et al.* and Kyu also found the growth of microstructure crystals around the contacts which extends into the transistor channel that contributes to improved charge transport. Interestingly, transistor performance increases despite a larger injection barrier into TIPS-pentacene (HOMO level of 5.30 eV [135]). PFBT modified gold has a work function of 4.77 eV [174], hence the injection barrier is 0.53 eV. This value is larger compared to a barrier of 0.2 eV when using pure untreated gold (Φ_w 5.1 eV [39]).

In terms of process compatibility, PVP is chemically stable against the isopropanol solvent. Therefore, the liquid deposition approach to modify the gold contacts is compatible with the logic circuit fabrication process. There was also no delamination of the gold source/drain electrodes when soaking samples in isopropanol for 1 hour. In this work, the impact of the immersion time was not investigated. The cited sample

immersion time can potentially be reduced to as low as 2 minutes, following the fabrication methodologies from literature [170, 172]. Nevertheless, this work identifies a method to considerably reduce hysteresis and increase mobility by improving the morphology of the semiconductor at the contact-semiconductor domain via a simple contact interfacial treatment. It would be interesting to incorporate the PFBT treatment into the BGBC logic circuit fabrication process and observe the performance improvements of fabricated circuits. For the inverter circuits, the increased mobility of individual OFETs would allow the inverters to achieve similar inverting gain performance at reduced bias voltages. Such an investigation was unfortunately not conducted in this research due to time constraint, as the investigation on the PVP-BST dielectric took much longer to complete than anticipated.

7 Conclusion

This research started as a project with the primary objective of replicating the PET project's liquid crystal sensor measurement system using solution processed polymer transistors. The expected outcome was the fabrication of a simple organic RFID transponder tag, as well as the interface circuit for probing the liquid crystal sensor. However, the original project aims had to be revised, leading to the investigation of a fabrication process for OFETs that are logic capable. Essentially, the revised plan focused on establishing a foundation for organic circuits research for UoM EEE. This decision was made after evaluating existing equipment and prior knowledge of this field within the school. The new research aims were accomplished with the successful demonstration of a logic circuit fabrication process.

A lithographic based fabrication process, adapted from state of the art was employed, instead of a printing based fabrication process. The transistor stack follows a bottom gate bottom contact structure; using evaporated gold for the electrodes, cross-linked PVP for the gate dielectric and TIPS-pentacene for the active semiconducting layer. Patterning of the electrodes is accomplished with lift-off photolithography. Similarly, the PVP gate dielectric is patterned using photolithography and oxygen plasma etching. PVP is thermally cross-linked with PMF so that deposited dielectric thin-films are chemically stable against acids and various organic solvents. This allows PVP to be used with lithographic and etching processes that would normally cause irreversible damage to polymeric materials.

Fabricated single transistors have a typical mobility in the range of 10^{-3} cm^2/Vs and on-off ratio of 10^2 to 10^3. Due to the use of the relatively thick polymer dielectric layer (~350 nm), transistor operation requires voltage supply in the 15-30 V (magnitude) range. Inverter circuits were successfully fabricated, with measured gains up to 7 for the zero-V_{gs} configuration and 3 for the diode-load configuration. The fabrication of a comparator circuit consisting of 11 transistors was also attempted, but was unsuccessful. Measured output characteristics of the fabricated comparator circuit did not match simulated characteristics. Such an outcome was expected as the comparator circuit consists of differential amplifier and current mirror sections that require good matching between individual transistors. Unfortunately, consistent device performance is rather challenging when using TIPS-pentacene as the active

layer, due to the anisotropy of the randomly orientated grains when deposited via spin-coating.

Two methods to improve individual transistor performance while maintaining compatibility with the logic circuit fabrication process have been investigated. The first optimisation work involved the use of PFBT SAM on the gold source/drain electrodes. Using PFBT modified contacts, a more favourable ordering of TIPS-pentacene semiconductor is obtained when spin-coating is used as the deposition technique. Typical device mobility increases to 10^{-2} cm^2/Vs and hysteresis is significantly reduced. There is also the tendency of devices to have a slightly positive threshold voltage.

For the second optimisation work, the use of nanocomposite polymer dielectric was investigated. The aim of this work was to reduce the operational voltages of the OFETs by increasing the dielectric constant of the polymer dielectric layer, thus improving the capacitive coupling between the gate and semiconductor layer. The nanocomposite was essentially a PVP solution that was blended with BST nanoparticles (SigmaAldrich, product code 633828). The methodology for preparing the nanocomposite solution to obtain well dispersed nanoparticles is documented in Chapter 6, section 6.1.2.2. BST nanoparticles were stable in suspension for approximately 2 weeks in the PVP host before noticeable sinking of the nanoparticles was observed. A dielectric constant of 4.77 was measured using 8 wt% BST loading over the 4.4 for PVP. However, the actual dielectric constant value is proposed to be higher as accurate profiling of the dielectric film thickness could not be obtained. This was due to the formation of a residual layer that raises the substrate height, giving inaccurate dielectric film thickness when profiled. The residual layer occurs when PVP-BST is etched with oxygen plasma and cannot be removed with solvent rinse. The PVP-BST films have a surface roughness value in the range of 1-5 nm, which is approximately one order magnitude higher than PVP. This is expected when introducing finite sized nanoparticle fillers into the PVP solution. Single transistors and inverters have been successfully fabricated using the nanocomposite dielectric. This is the first reported work on photolithographic fabrication of fully integrated organic logic circuits using the PVP-BST dielectric. Fabricated single transistors

exhibited improved sub-threshold swing to 1.2 – 1.3 V/decade compared to the typical >2 V/decade for PVP transistors.

With regards to the feasibility and future outlook of organic technology, it is clear from the literature review that organic technology is still in its early research and development phase. Current generation OFETs can already achieve high mobilities above 1 cm^2/Vs, and relatively complex organic devices such as RFID transponders and microprocessors have already been demonstrated. However, further research addressing practical aspects of the technology are necessary in order to move towards commercialisation of this technology. Carrier mobility is undoubtedly an important factor, but it is perhaps less crucial compared to the other transistor characteristics such as shelf life, stress stability and logic compatibility when considering organic technology for real world applications. Nonetheless, it is anticipated that future developments in this field will enable organic devices to be fabricated with a low cost process at high yields, using materials that allow for devices with high stress and shelf life stability. It is also useful to evaluate the technology from a different viewpoint. Instead of pursuing highly optimised fabrication processes for high performance organic devices to replace conventional inorganic circuits, it is perhaps more sensible to first determine niche applications that can benefit from the capabilities of current organic devices.

7.1 Future Work

7.1.1 PVP-BST Nanocomposite Dielectric

To improve the effectiveness of using the PVP-BST nanocomposite dielectric layer, a higher loading of the nanoparticles can be investigated to further increase the overall dielectric constant. One reasonable concentration would be a blend of 50 wt% nanoparticles and 10 wt% PVP. Pre-treated BST could be employed to aid dispersion of the BST nanoparticles in the polymer solution during the solution preparation stage, as well as to reduce phase separation of BST from the polymer matrix host when the prepared nanocomposite solution is in storage. Such a treatment typically involves the hydroxylation of the nanoparticle surfaces, followed by the surface modification process using surfactants or polymer coatings.

To mitigate the rougher dielectric interface as a consequence of the high nanoparticle loading, a smoothing layer can be added to the fabrication process. One candidate material is parylene that is vapour deposited, which is compatible with lithographic processes in the logic circuit fabrication process. Parylene has a relatively low dielectric constant of 2.6, hence, the deposited smoothing layer must be as thin as possible (e.g. <50 nm) to minimise the reduction in overall capacitance of the dielectric stack. Parylene can be substituted with thin, cross-linked PVP for an all solution processed dielectric layer. However, thin PVP layers will be susceptible to pin-hole formation that may impact the growth of the semiconductor material.

Further investigation could be to investigate the thinnest possible PVP-BST layer that can be used before the fabrication yield is adversely reduced. The challenge would be to determine the thickness of the deposited PVP-BST films. It would require a PVP-BST patterning method that does not promote formation of the residual layer, with the photochemical patterning being a potential approach.

7.1.2 Optimisation of the BGBC Logic Circuit Fabrication Process

When scaling beyond simple inverter circuits, the BGBC logic circuit fabrication process presented in this thesis can be considered, but with the following refinements and recommendations. For the gate layer, different metals such as platinum, aluminium, copper and titanium could be used to tune the threshold voltage of resulting transistors. This could lead to more symmetrical ($V_{dd}/2$) trip points and higher gains for inverter circuit building blocks. For the PVP dielectric layer, the patterning process could employ the photochemical approach, instead of the presented oxygen plasma etching approach. Photochemical patterning allows PVP to be cross-linked at 150°C, rather than 200°C when cross-linking with PMF.

For the source/drain contacts layer, the deposited gold layer is best treated with PFBT SAM when using TIPS-pentacene as the active semiconducting layer. Deposition of PFBT requires only simple processing steps, but significantly improves device characteristics such as mobility, on-off ratio and hysteresis. For the semiconducting layer, the TIPS-pentacene film could be treated post deposition to obtain transistors with more consistent device characteristics. This could be achieved by placing

samples in a chamber with controlled and directional inert gas flow, so that grain growth is in parallel to the transistor's conducting channel.

The semiconducting layer will also require a patterning step to reduce off-currents. For TIPS-pentacene, a PVA etch mask or an aligned shadow mask could be used with oxygen plasma etching to remove unwanted semiconductor material. It would also be practical to document and characterise other potential semiconductors for the BGBC logic circuit fabrication process, based on their shelf life and stress stability. For such an investigation, the characterisation of the semiconductor could be on the ambient, photo and stress cycle stability. In addition to testing with PVP, the semiconductors could also be tested in combination with other commonly used polymer dielectrics such as PMMA and PVA.

7.1.3 Printed OFETs

Another possible area of research relates to the printing technologies for OFETs. Although printed OFETs have been previously demonstrated, the practical aspects of the fabrication are seldom addressed. It would be useful to investigate viable materials and solvent choices for real world manufacturing environments. To elaborate, information such as the cost, stability, wetting and drying characteristics of the electronic inks must be thoroughly addressed. For such a project, a positive outcome would be to demonstrate a technique for mass printing defect free sub-micron thin films.

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Appendix A : Potential Capacitance Measurement Circuits for the Liquid Crystal Sensor

A.1 Introduction

There are a number of considerations that must be taken into account when trying to decide on an appropriate excitation technology for the liquid crystal temperature sensor. The dielectric spectroscopy experiments were typically undertaken under 0 V DC bias conditions and with low amplitude sinusoidal signals of 50 mV peak to peak. This is because the mechanism that gives rise to the spontaneous polarisation associated with the ferroelectric phase, and thus its electrical properties, is suppressed as the applied voltage is increased. Providing that the electric field strength is kept below about 0.1 V/µm, then there will be little suppression of the dielectric properties of the liquid crystal [1, 2].

Other factors of concern are the amount of power, and the time required to make the measurement. Power is very important since the power source is the RF field generated by the RFID portal. The sensor tag must be capable of performing all the RFID functions and any sensor signal processing functions without reducing the read range of the tag, or compromising the speed of transit through the RFID portal.

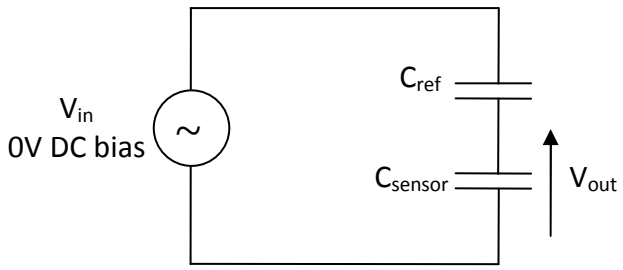
In the following discussion, the candidate capacitance measurement circuits do not reflect an exhaustive list. Instead, the primary focus is on simplicity of the circuit's construction and overall operation to account for the low power supplied by the passive RFID tag. For the purpose of discussion, the sensor is assumed to be purely capacitive, hence ignoring the changes in conductance with respect to temperature.

A.2 AC excitation

A.2.1 Capacitance Divider Circuit

The capacitance voltage divider circuit is perhaps the most obvious choice. This technique requires a sinusoidal source of about 500 to 1000 Hz which connects to the sensor via either a suitably sized capacitor or resistor, as shown in Figure_Apx A.1. The output of this potential divider network would be the voltage across the sensor, with V_{out} obtained using Equation_Apx A.1.

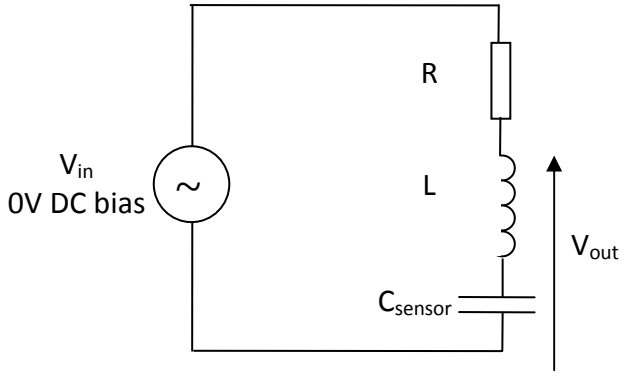
$$V_{out} = V_{in} \frac{C_{ref}}{C_{ref} + C_{sensor}} \qquad \text{Equation\_Apx A.1}$$



Figure_Apx A.1: AC excitation of capacitive divider.

A.2.2 LC Tuner

A second AC excitation based circuit is the LC tuner, or resonant circuit. This circuit consists of a resistor, an inductor and a capacitor that are connected in series or in parallel.



Figure_Apx A.2: Tuner circuit with capacitance and inductance in series.

With L and C connected in series to an AC power supply, inductive reactance magnitude (X_L) increases as frequency increases while capacitive reactance magnitude (X_C) decreases with the increase in frequency. At a particular frequency the two reactances are equal in magnitude but opposite in sign, resulting in minimum impedance across the LC section. The frequency at which this happens is the resonant frequency for the given circuit. By selecting an appropriate inductor value, it is then possible to tune the circuit for the capacitance value at SmA or at SmC* phase. This forms the basis of the measurement, with the output voltage (Equation_Apx A.2) taken across the LC section.

$$V_o = V_{in}\frac{Z_{LC}}{Z_{Total}} = V_{in}\frac{\sqrt{\left(2\pi fL - \frac{1}{2\pi fC}\right)^2}}{\sqrt{R^2 + \left(2\pi fL - \frac{1}{2\pi fC}\right)^2}} \qquad \text{Equation\_Apx A.2}$$

For a series connected tuned circuit with capacitance C and supply frequency f, the resonant frequency can be calculated using Equation_Apx A.3:-

$$f = \frac{1}{2\pi\sqrt{LC}}$$ Equation_Apx A.3

Pragmatically, it would be unfeasible to employ this circuit due to the small capacitance values as well as the low operating frequency (200 Hz – 1 kHz) range of the temperature sensor, where its change in electrical properties are most significant. This can be demonstrated by the following example:-

Assume best case scenario with supply frequency of 2000 Hz, and tuning for a sensor capacitance of 1nF at the SmC* phase. The inductor value required from Equation_Apx A.4:-

$$L = \left(\frac{1}{2\pi f}\right)^2 \frac{1}{C}$$ Equation_Apx A.4

L = 6.3 Henry

As can be seen, the circuit would require rather large inductor values that are difficult to achieve when considering the integrated circuit form.

A.3 AC Circuit Challenges

There are potentially a number of problems with the AC techniques. The AC outputs from the circuits require signal processing in order to obtain a DC voltage that is representative of the sensor voltage (liquid crystal phase). The signal processing would be either rectification and filtering, or peak detection and hold. Similarly, the supply stage will require an oscillating type supply. An analogue oscillator will take time to start up and stabilise, and they tend to have amplitude and frequency stability problems due to thermal effects associated with the components used to define the oscillator's parameters. Stability issues can be addressed by additional circuitry, or tighter tolerance components, but this makes it more difficult to integrate on an IC. On the other hand a digitally synthesised oscillator could be turned on much more quickly, but requires the addition of a DAC to the system; this adds complexity and additional power consumption.

Next, consider the processing steps involved in either rectification and filtering, or peak detection and hold. The suggested operating voltage for the sensor is less than 500 mV peak (assuming a 5 µm cell); this presents a problem for diode rectification, or for peak hold circuits, since the forward voltage drop of a diode is of the order of 600 to 700 mV. Active rectifiers and peak hold circuits can be readily achieved using

op-amps, but would require careful design within what is essentially a single supply system. Alternatively, it would be possible to apply gain to the low voltage sensor output, although this would also increase the noise. Filtering of the rectified waveform also presents a number of problems; the principle one being the time for the filter to settle to its final value. For a 1 kHz input signal it would be desirable to have a filter cut-off frequency at 100 Hz or below. This presents a considerable timing problem if many sensors are to be read during the transit of the tag through the RFID portal.

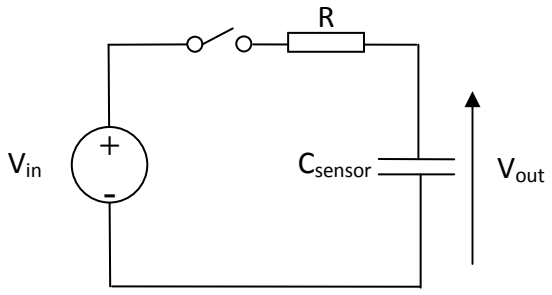
A.4 DC Excitation

A.4.1 RC Time Constant Circuit

In this circuit configuration, a resistor is connected in series with the sensor, as shown in Figure_Apx A.3. Here, the measurement technique employs the transient response of the circuit, essentially the charging voltage of the capacitor. If a step voltage is applied to the purely capacitive sensor via a suitably sized resistor, the circuit responds as shown in Equation_Apx A.5. The capacitance of the sensor depends upon the phase of the liquid crystal, which is temperature dependant.

$$V_{out} = V_{in}\,(1 - e^{-\frac{t}{RC}}) \qquad \text{Equation\_Apx A.5}$$

In effect, there will be two different time constants for the sensor depending upon the temperature of the sensor material. If the sensor voltage and an appropriate reference voltage are fed to a comparator, and the output from the comparator is sampled at a set time, then a digital output that reflects the phase of the sensor can be realised.



Figure_Apx A.3: RC circuit configuration.

[1] F. Gouda, K. Skarp, and S. T. Lagerwall, "Dielectric studies of the soft mode and Goldstone mode in ferroelectric liquid crystals," *Ferroelectrics*, vol. 113, pp. 165 - 206, 1991.

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Appendix B : Passive Liquid Crystal Temperature Sensor Array

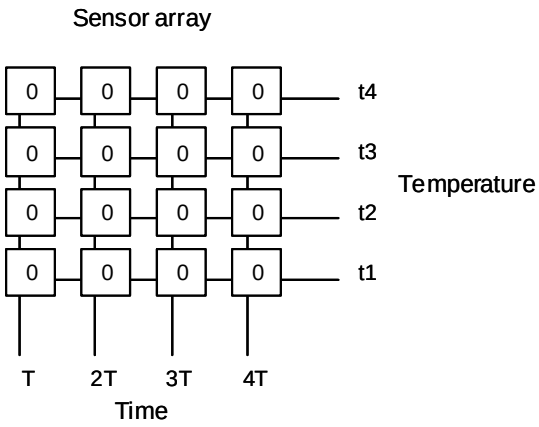
This appendix discusses how the sensor system can be designed to achieve passive temperature logging capability with an array of single sensor units. Consider a number of single sensors, each with a slightly different liquid crystal formulation, and thus each possessing a different temperature threshold for the SmA to SmC* phase change. This gives a temperature scale, and thus a thermometer; albeit on a rather coarse scale. From this, a method of creating a passive clock is required so that a temperature logging sensor array can be formed.

Creating a time scale passively is conceptually quite simple. Individual sensor units are added a particular combination of monomer and initiator material that will polymerise over a certain time period. The basis of a passive time scale is achieved by using different formulations that will polymerise over different time periods. This has been further explored by the School of Chemistry and has subsequently been combined with liquid crystal material to form a sensor that reflects the temperature under which the polymerisation took place.

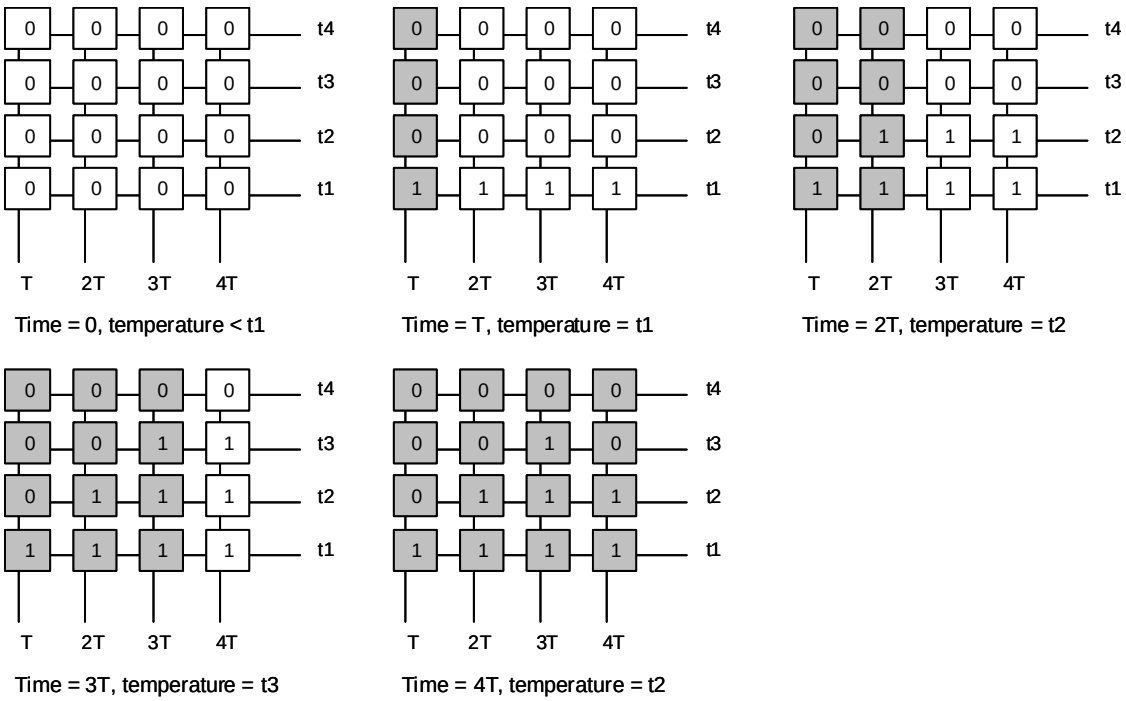
Combining the liquid crystal with the passive clocking technology gives a temperature scale over time. In essence, a temperature scale is obtained by adjusting the formulations of the liquid crystal and a time scale is obtained by adjusting formulations of the monomer and initiator. It was expected that after a certain elapsed time the phase of the liquid crystal material due to its incorporation in to a polymer matrix would become locked. Temperature changes that would normally have caused a phase transition to occur in the material would have no effect since the liquid crystal has been incorporated in to the polymer in a particular phase, and its phase cannot now change, thus preserving the electrical properties associated with the phase it was in when polymerisation occurred.

The resultant structure is an array with temperature along one axis (rows), and time along the other axis (columns). Each row has a higher transition temperature that the previous row, and each time column has a longer polymerisation time than the previous column. Each element of the array is a temperature sensor, and needs to be probed to determine the phase of the sensor so that the temperature record can be extracted from the array. The array could be probed in a number of ways, but perhaps the most efficient way is to probe the temperature rows of one time column in parallel, and then move on to the next column, and so on until the entire array has been read.

The diagram of Figure_Apx B.1 shows a simple array of four rows and four columns. The sensors are shown as having logic ‘0’ reading, thus showing that the ambient temperature is below the lowest transition temperature ‘t1’. Figure_Apx B.1 shows how the sensor array gradually polymerises with time, locking in the sensor’s temperature indication. Here, a convention is adopted where a sensor in the SmA phase (higher temperature) will result in a logic ‘1’, whereas a sensor in the SmC* phase will result in a logic ‘0’.

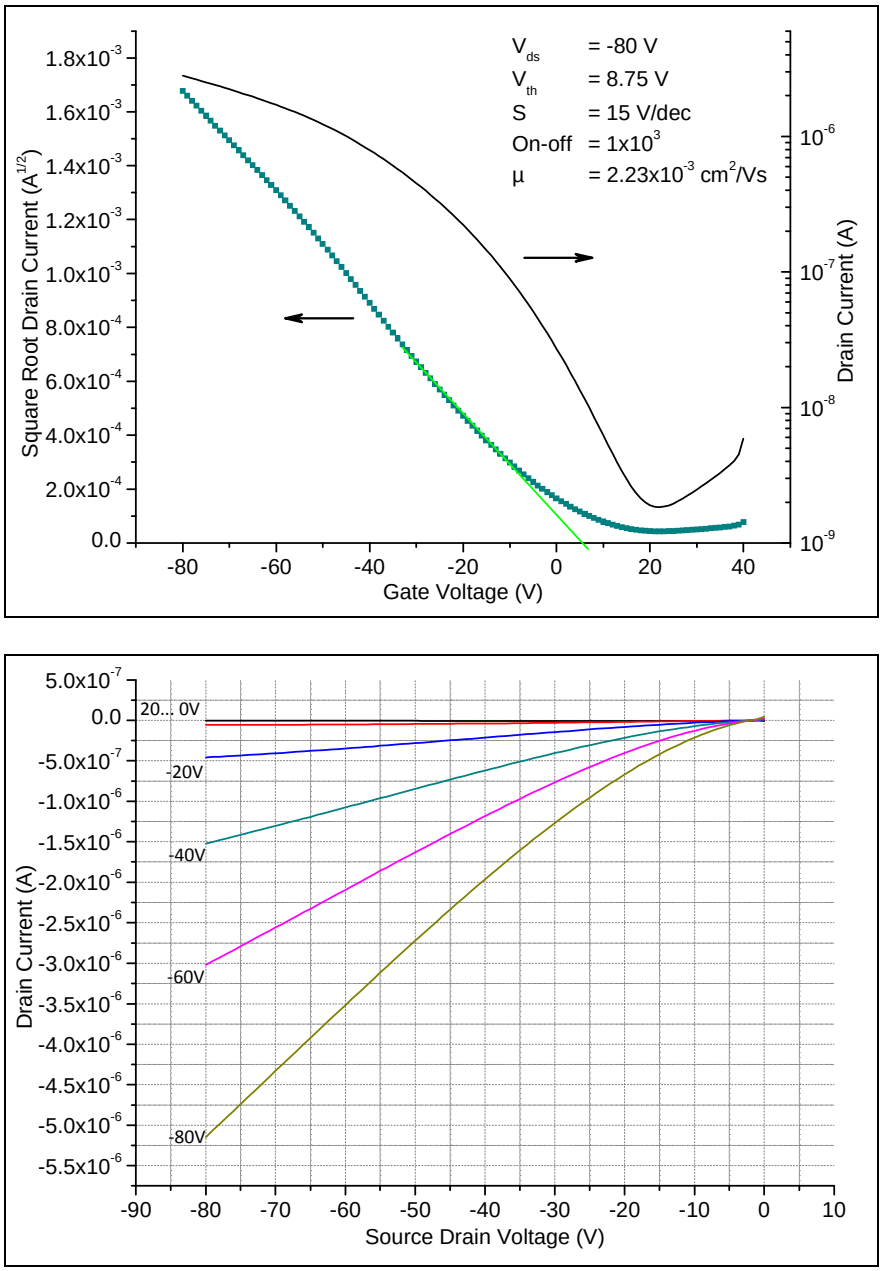


Figure_Apx B.1: Sensor array.



Figure_Apx B.2: Gradual polymerisation of sensor array.

Appendix C : PVP + PBTTT Transistor Performance



Figure_Apx C.1: Transfer and output characteristics of a transistor using PBTTT semiconductor, highly doped n-type Si substrate and 650 nm of PVP dielectric layer.

Appendix D : PVP-BST Raw Material Calculation

Molecular Weight

Barium isopropoxide = 255.5 g/mol
Titanium isopropoxide = 284.22 g/mol
Strontium isopropoxide = 205.79 g/mol

Density

Titanium isopropoxide = 0.962 gcm^{-3}

Misc

Precursor volume = 12 ml
$1cm^3$ = 1 ml

Molecular weight = mass of solute to obtain 1M solution in 1 litre of solvent.

$$Molarity = \frac{moles\ of\ solute}{litres\ of\ solution}$$

Barium Isopropoxide

Using 0.196 g of barium isopropoxide

$$Moles of\ solute = \frac{0.196}{255.5} \times 1M = 0.000769$$

$$Molarity = \frac{0.000769}{12ml} = 0.064090019$$

Titanium Isopropoxide

Mass = volume x density
= 0.226 ml x 0.962 gcm^{-3}
= 0.226 ml x 0.962 gml^{-1}
= 0.2174 g

$$Moles of\ solute = \frac{0.2174}{284.22} \times 1M = 0.0007649$$

$$Molarity = \frac{0.0007649}{12ml} = 0.06374$$

Strontium Isopropoxide

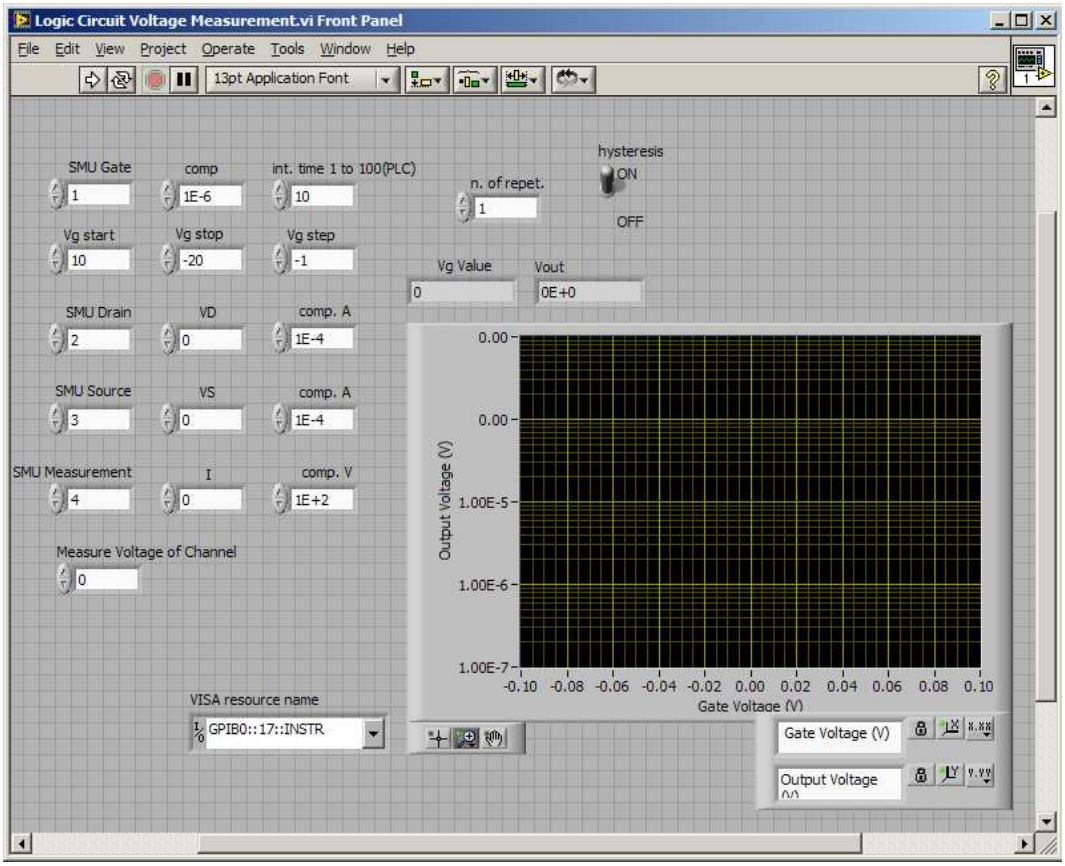
Molar ratio of Br : Sr : TiO_3 = 0.7:0.3:0.7

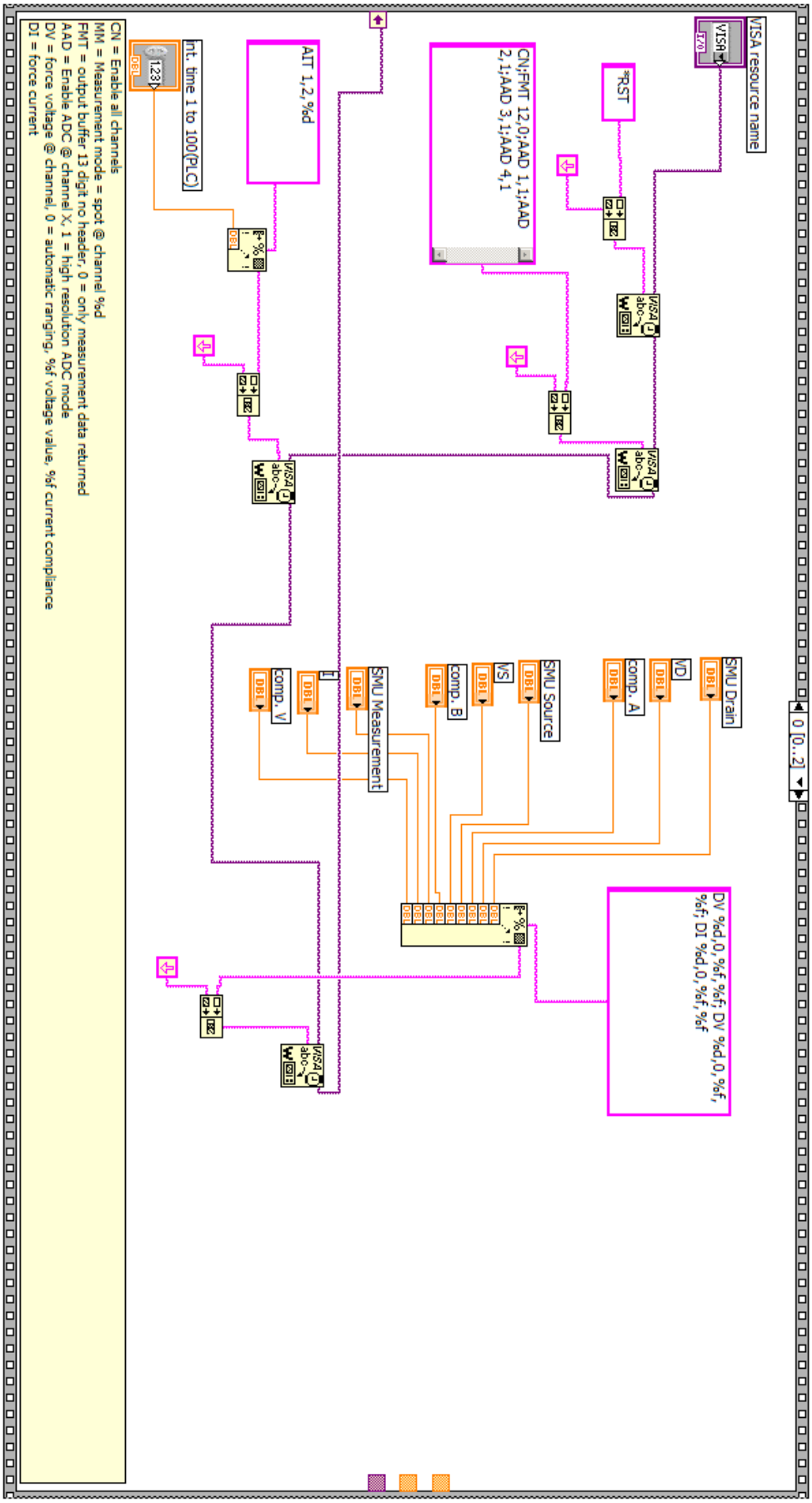
Molarity required $= \frac{0.06409}{0.7} \times 0.3$
$= 0.027467151$

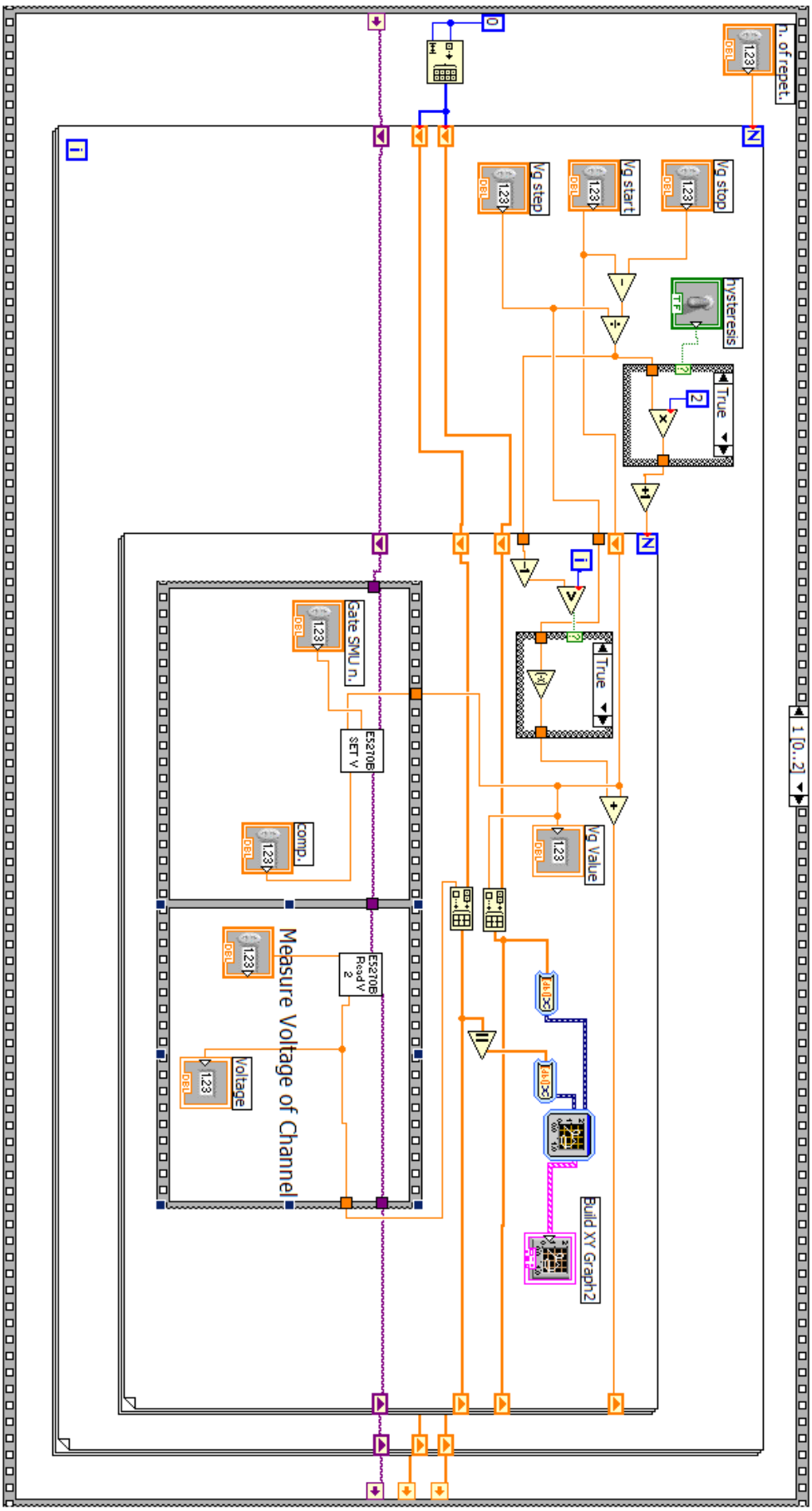
Moles of solute = molarity x volume
= 0.0274 x 12 ml
= 0.0003296

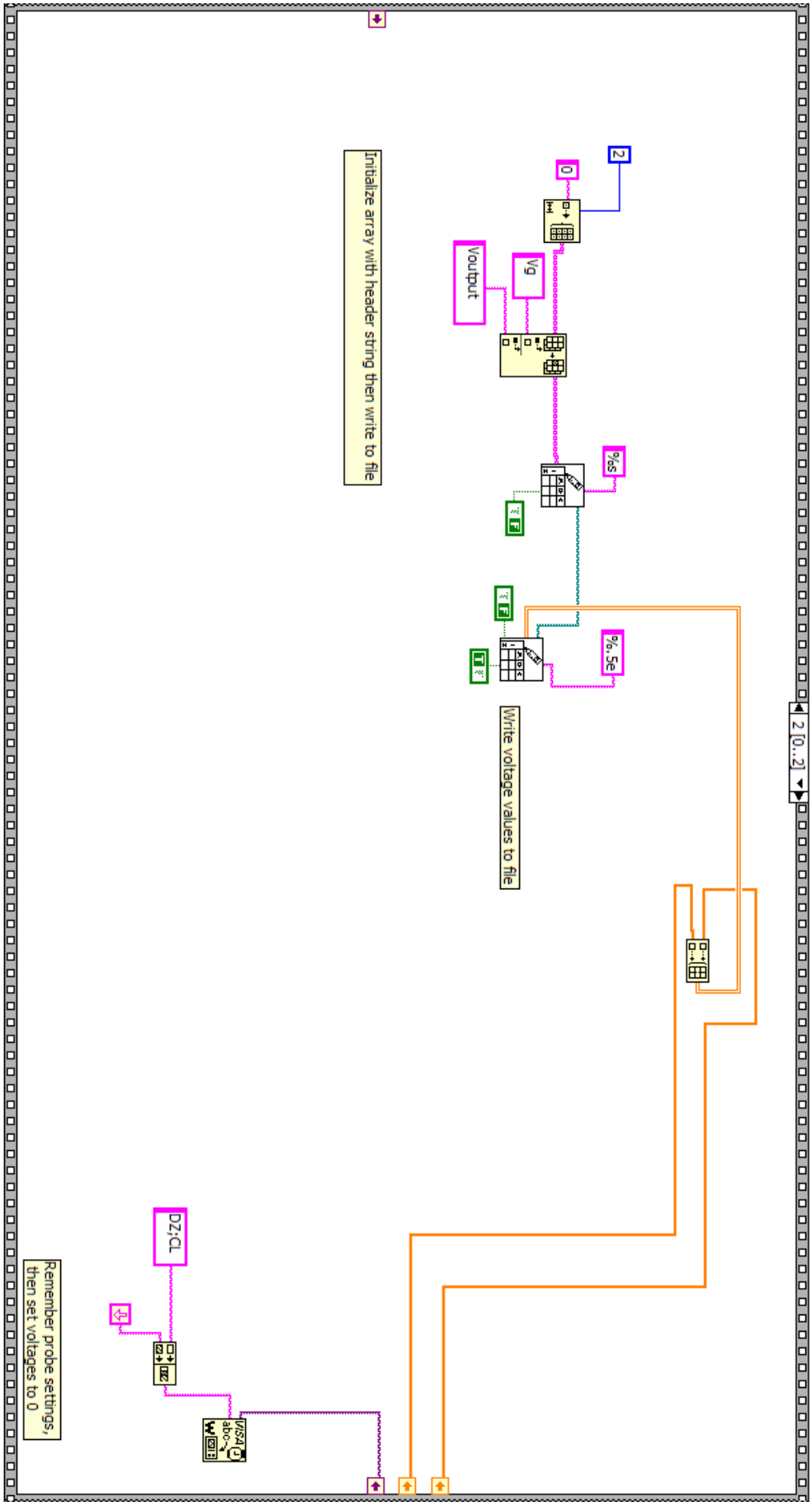
Mass of solute = moles of solute x molecular weight
= 0.0003296 x 205.79
= 0.0678 g

Appendix E : LabVIEW Program for Logic Circuit Characterisation

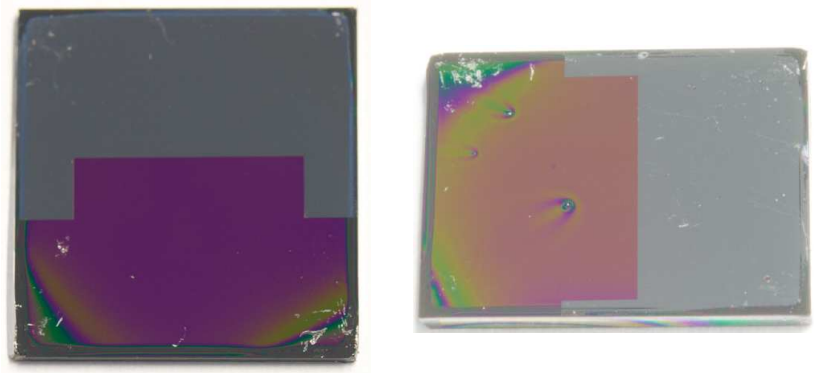



VISA resource name
*RST
CN;FMT 12,0;AAD 1,1;AAD 2,1;AAD 3,1;AAD 4,1
AIT 1,2,%d
Int. time 1 to 100(PLC)
SMU Drain
VD
Comp. A
SMU Source
VS
Comp. B
SMU Measurement
I
Comp. V
DV %d,0,%f,%f; DV %d,0,%f, %f; DI %d,0,%f,%f
0 [0..2]
CN = Enable all channels
MM = Measurement mode = spot @ channel %d
FMT = output buffer 13 digit no header, 0 = only measurement data returned
AAD = Enable ADC @ channel X, 1 = high resolution ADC mode
DV = force voltage @ channel, 0 = automatic ranging, %f voltage value, %f current compliance
DI = force current

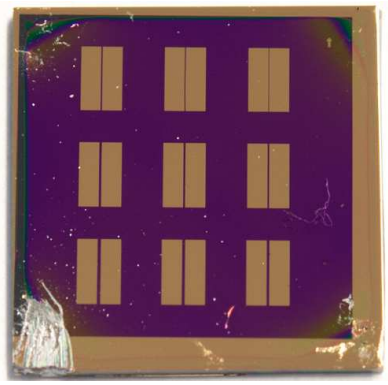

n. of repet.
Vg step
Vg start
Vg stop
hysteresis
True
Gate SMU n.
ES270B SET V
comp.
Vg Value
Measure Voltage of Channel
ES270B Read V 2
Voltage
True
1 [0..2]
Build XY Graph2


Initialize array with header string then write to file
Voutput
Vg
%s
%.5E
Write voltage values to file
2 [0..2]
Remember probe settings, then set voltages to 0
DZ;CL
VISA

Appendix F : Fabricated Devices



Figure_Apx F.1: Etched PVP samples using highly doped n-type Si substrates for dielectric thickness measurement.

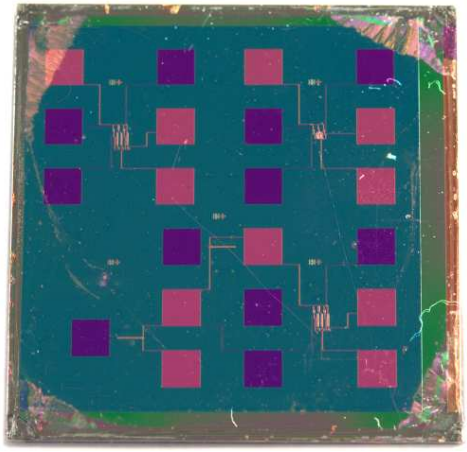


Figure_Apx F.2: MIM capacitor using gold contact electrodes for capacitance and gate leakage measurements.

Figure_Apx F.3: Single transistors using PVP and spin-coated TIPS-pentacene on highly doped n-type Si substrates.

Figure_Apx F.4: Inverter circuit using PVP and spin-coated TIPS-pentacene on Si-SiO_2 substrates.

Figure_Apx F.5: Inverter circuit using PVP and drop casted TIPS-pentacene on Si-SiO_2 substrates.



Figure_Apx F.6: Comparator circuit using PVP and spin-coated TIPS-pentacene on Si-SiO_2 substrate.

Figure_Apx F.7: The first functional organic inverter in UoM EEE fabricated on Si-SiO_2 substrates. PTAA is used as the active layer and (conductive) epoxy bonded wires were employed for forming interconnects.

Appendix G : Cross-linking PVP with HMBG

G.1 Introduction

Until recently, PMF has been the standard cross-linking agent for thermally initiated cross-linking of PVP films. However, a recent paper by IMEC reported the use of an alternative low temperature cross-linker, hydroxymethyl benzoguanamine (HMBG). They found that the PVP + HMBG combination, cross-linked at 130 °C, showed comparable chemical resistance as well as threshold voltage shifts. The reduced cross-linking temperature allows for process compatibility with a wider selection of substrates, particularly polymer substrates that are sensitive towards high temperature treatments. This appendix discusses our experience with the HMBG cross-linker for PVP.

G.1.1 Experimental

The original experiment reported by IMEC was attempted, following their recommended solution preparation and dielectric film processing conditions. Dielectric solutions of 1.25 wt% HMBG and 10 wt% PVP were prepared. The dielectric solution was spin-coated onto Si-SiO_2 substrates and cross-linked at 130 °C under nitrogen atmosphere for 3 hours. To examine the chemical resistance of the deposited films, samples are then rinsed in an acetone filled beaker for 5 minutes, dried and observed under a microscope. Optical imaging of the PVP + HMBG films were performed with a fixed white balance setting to ensure any colour deviations are due the polymer film itself.

G.1.2 Results and Discussion

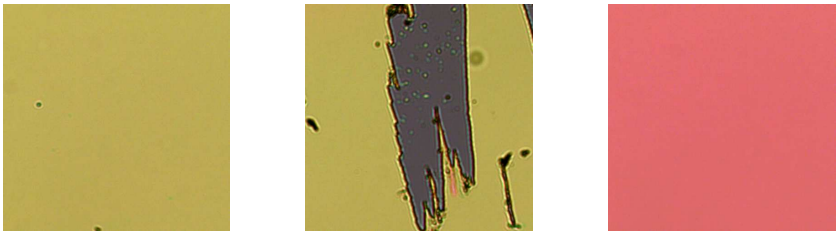
The results reported in this section were obtained using the PVP-BST8 + HMBG solution. Results are consistent regardless of the addition or absence of the BST nanoparticles in the PVP dielectric solution.

Figure_Apx G.1: Microscope images of PVP film cross-linked with HMBG at 130°C for 3 hours. Sample after acetone rinse (a). Sample etched using oxygen plasma (b). Reference sample (c).

Majority of the PVP layer is stripped off when cross-linking is performed at 130 °C. This is clearly seen by the distinct colour difference of the sample after acetone rinse

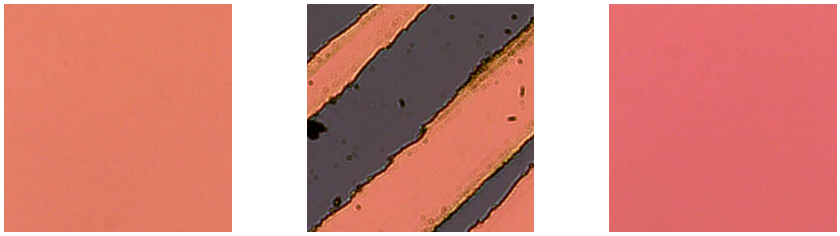
(Figure_Apx G.1a), compared to the reference sample (Figure_Apx G.1c). Figure_Apx G.1b shows a partially etched (bottom half) PVP layer after the acetone rinse, which reveals a slightly different colour shade compared to the un-etched portion. This suggests that only the PVP portion near the substrate-dielectric interface is resistant to the acetone rinse, in contrast with the good chemical resistance reported by IMEC.

The partially cross-linked PVP film was hypothesised to be due to the low process temperature. Therefore, the experiment was repeated with a higher cross-linking temperature (150°C).



(a) (b) (c)

Figure_Apx G.2: Microscope images of PVP film crosslinked with HMBG at 150°C for 3 hours. Sample after acetone rinse (a). Sample scratched using cocktail stick (b). Reference sample (c).



(a) (b) (c)

Figure_Apx G.3: Microscope images of PVP film crosslinked with HMBG at 150°C for 6 hours. Sample after acetone rinse (a). Sample scratched using cocktail stick (b). Reference sample (c).

At 150 °C (3 hours cross-linking duration), PVP is still not fully cross-linked. However, the degree of cross-linking improved marginally. Noticeable colour change of PVP (Figure_Apx G.2a) was observed after acetone rinse where a dull yellow film is obtained. Expectedly, the PVP layer scraped off easily when prodded with a cocktail stick, as shown in Figure_Apx G.2b. In contrast, conventional cross-linking using PMF would produce PVP films with good physical resistance. Similar results are observed even after doubling the cross-linking duration to 6 hours. The colour of the PVP layer becomes close to the reference device after acetone rinse (Figure_Apx G.3a), suggesting that the degree of cross-linking improved even further. However, the PVP film is still easily scratched in the cocktail stick test (Figure_Apx G.3b).

In this set of experiments, the processing steps are similar to that of IMEC's procedures, with the exception of using a nitrogen hotplate for the thermal annealing (cross-linking) step instead of a vacuum oven. It is plausible that HMBG can only effectively cross-link PVP at 130 °C under reduced atmospheric pressures. Otherwise, it can be deduced that the results published by IMEC were too optimistic. Even after increasing the suggested cross-linking temperature by 20 °C and doubling the cross-linking duration, the PVP + HMBG combination was unable to deliver the same degree of chemical and physical resistance as PVP + PMF. Although the increase in temperature and duration was found to improve the degree of cross-linking, extended cross-linking durations were not investigated as such lengthy processing are not practical. The cross-linking temperature was also limited to 150 °C as it is the typical threshold for compatibility with polymeric substrates.

Appendix H : Maximum Theoretical Gain for The Diode-Load Inverter

$$A_{max} = \frac{g_{m\,driver}}{g_{m\,load}}$$

The equation for transconductance, g_m

$$g_m = \frac{2I_D}{V_{gs} - V_{th}}$$

From the drain current equation for a transistor in saturation,

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2$$

$$V_{gs} - V_{th} = \sqrt{\frac{I_D}{\frac{1}{2}\mu C_{ox}\frac{W}{L}}}$$

Hence,

$$g_m{}^2 = \frac{4{I_D}^2}{\frac{I_D}{\frac{1}{2}\mu C_{ox}\frac{W}{L}}} = 2I_D\mu C_{ox}\frac{W}{L}$$

$$g_m = \sqrt{2I_D\mu C_{ox}\frac{W}{L}}$$

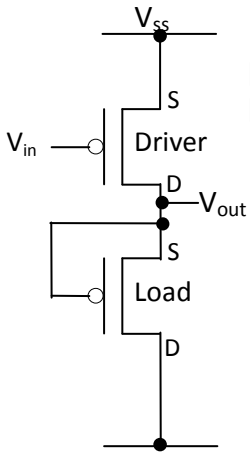
Substituting g_m back into the gain equation,

$$A_{max} = \frac{g_{m\,driver}}{g_{m\,load}} = \frac{\sqrt{2I_D\mu C_{ox}\frac{W_{driver}}{L_{driver}}}}{\sqrt{2I_D\mu C_{ox}\frac{W_{load}}{L_{load}}}}$$

Since the current flowing in the driver and load transistors is equivalent,

$$A_{max} = \sqrt{\frac{W_{driver}L_{load}}{W_{load}L_{driver}}}$$

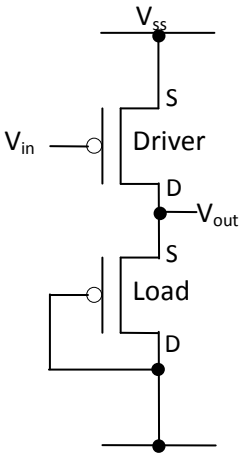
Appendix I : Circuit Designs



[Large driver] W=125 μm L=10 μm
[Small driver] W=20 μm L=10 μm

[Large load] W=1 mm L=10 μm
[Small load] W=160 μm L=10 μm

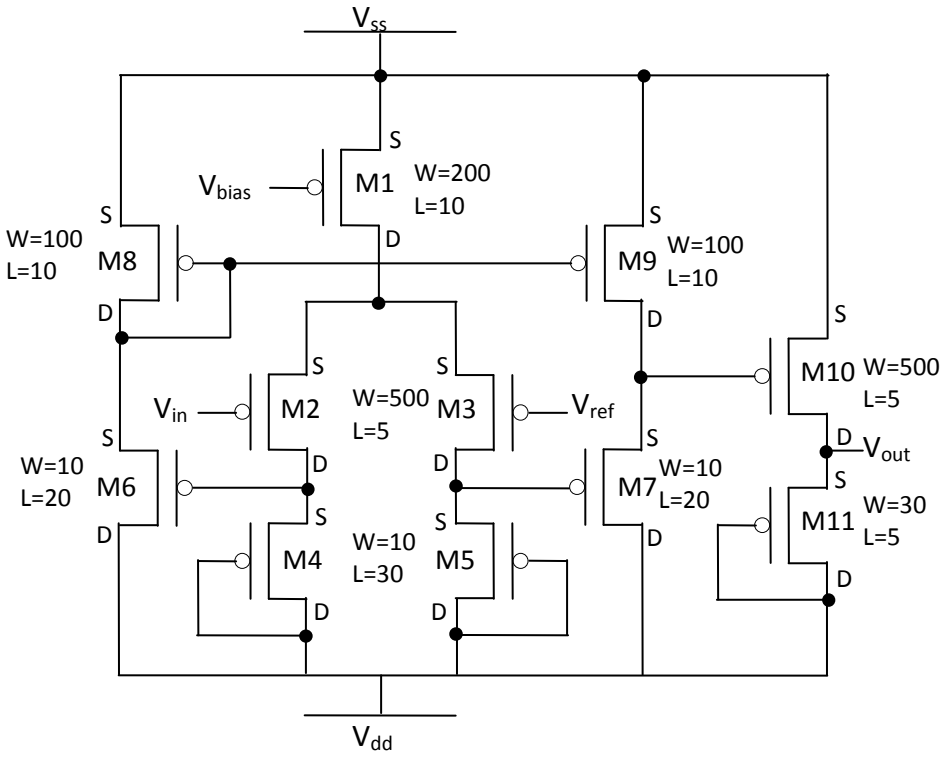
Figure_Apx I.1: Zero-V_{gs} inverter.



[Large driver] W=1 mm L=10 μm
[Small driver] W=160 μm L=10 μm

[Large load] W=125 μm L=10 μm
[Small load] W=20 μm L=10 μm

Figure_Apx I.2: Diode-load inverter.



Figure_Apx I.3: Comparator circuit. Length unit is in micrometers.

Appendix J : AIM-Spice Simulation

This appendix consists of two sections. The first section defines the fitting parameters used in the AIM-Spice level 15 amorphous silicon transistor model. The second section reviews the important equations used by the model. The discussion in this appendix is compiled from the AIM-Spice manual as well as [1-3].

Name	Symbol	Parameter	Units	Default Value
ALPHASAT	-	Saturation modulation parameter. It accounts for the variation of depletion charge across the channel	-	0.6
CGDO	-	Gate-drain overlap capacitance per meter channel width	F/m	0.0
CGSO	-	Gate-source overlap capacitance per meter channel width	F/m	0.0
DEF0	-	Dark Fermi level position	eV	0.6
DELTA	-	Transition width parameter	-	5
EL	-	Activation energy of the hole leakage current	eV	0.35
EMU	-	Field effect mobility activation energy	eV	0.06
EPS	-	Relative dielectric constant of substrate	-	11
EPSI	-	Relative dielectric constant of gate insulator	-	7.4
GAMMA	γ	Power law mobility parameter	-	0.4
GMIN	-	Minimum density of deep states	$m^{-3}eV^{-1}$	1E23
IOL	-	Zero bias leakage current. The minimum leakage current.	A	3E-14
KASAT	-	Temperature coefficient of ALPHASAT	1/°C	0.006
KVT	-	Threshold voltage temperature coefficient	V/°C	-0.036
LAMBDA	λ	Output conductance parameter	1/V	0.0008
M	M	Knee shape parameter	-	2.5
MUBAND	μ_0	Conduction band mobility	m^2 / Vs	0.001
RD	-	Drain resistance	Ω	0.0
RS	-	Source resistance	Ω	0.0
SIGMA0	-	Minimum leakage current parameter	A	1E-14
TEMP	-	Operating temperature of the circuit.	°C	27
TNOM	-	Parameter measurement temperature	°C	27
TOX	-	Thin-oxide thickness	m	1E-7
V0	-	Characteristic voltage for deep states	V	0.12
VAA	-	Characteristic voltage for field effect mobility (determined by tail states)	V	7.5E3
VDSL	-	Hole leakage current drain voltage parameter	V	7
VFB	-	Flat band voltage	V	-3
VGSL	-	Hole leakage current gate voltage parameter	V	7
VMIN	-	Convergence parameter	V	0.3
VTO	-	Zero-bias threshold voltage	V	0.0

The drain current for the level 15 AIM-Spice transistor model is composed of two contributions,

$$I_{ds} = I_{ab} + I_{leakage}$$ Equation_Apx J.1

where I_{ab} is from the accumulation of charge carriers while $I_{leakage}$ is due to intrinsic conductivity of the semiconductor material. I_{ab} for the above and below threshold region is given by Equation_Apx J.2.

$$I_{ab} = g_{ch} V_{dse} (1 + \lambda . V_{ds})$$ Equation_Apx J.2

where g_{ch} is the effective channel conductance and V_{dse} is the effective drain-source voltage. The equations for g_{ch} and V_{dse} are given by Equation_Apx J.3 and Equation_Apx J.5.

$$V_{dse} = \frac{V_{ds}}{\left[1 + \left(\frac{V_{ds}}{[ALPHASAT + KASAT(TEMP - TNOM)].V_{gte}}\right)^{M}\right]^{\frac{1}{M}}}$$ Equation_Apx J.3

where

$$V_{gte} = \frac{VMIN}{2}\left[1 + \frac{V_{gs} - [VTO + KVT(TEMP - TNOM)]}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gs} - [VTO + KVT(TEMP - TNOM)]}{VMIN} - 1\right)^2}\right]$$ Equation_Apx J.4

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)}$$ Equation_Apx J.5

where

$$g_{chi} = e\, n_s\, \mu_{FET} \frac{W}{L}.$$ Equation_Apx J.6

In the equations, e is the elementary charge, n_s is the charge carrier concentration and μ_{FET} is the field effect mobility, W is the width and L is the length of the channel.
For the above threshold region, the field effect mobility is a function of gate bias and is described by a power law given by Equation_Apx J.7.

$$\mu_{FET} = \mu_0 \left(\frac{V_{gs}-V_{th}}{V_{AA}}\right)^{GAMMA}$$ Equation_Apx J.7

where μ_0 is the MUBAND parameter and is defined as the intrinsic band mobility. A value of 10 cm^2/Vs is usually selected for the amorphous silicon semiconductor [1]. Gamma and V_{AA} are fitting parameters that are obtained from parameter extraction. Fjeldly *et al.* commented that 10^5 is a typical value for V_{AA}. [2]

The carrier concentration given by Equation_Apx J.8 is composed of the free carrier concentration n_{sa} and the carriers from deep traps n_{sb}.

$$n_s = \frac{n_{sa}.n_{sb}}{n_{sa}+n_{sb}},$$ Equation_Apx J.8

where

$$n_{sa} = \frac{EPSI.V_{gte}}{e.TOX}\left(\frac{V_{gte}}{V_{AA}\exp\left[\frac{EMU}{e.GAMMA}\left(\frac{1}{V_{th}}-\frac{1}{V_{tho}}\right)\right]}\right)^{GAMMA}$$ Equation_Apx J.9

and

$$n_{sb} = \left(3\times10^{25}\sqrt{\frac{EPS}{2e.GMIN}}\frac{2.V0.V_{tho}}{2.V0-V_{th}}\frac{1}{\mathrm{V0}}\exp\left(-\frac{DEF0}{V_{th}}\right)\right)\times \left(\frac{\sqrt{\frac{EPS}{2e.GMIN}}}{TOX}\frac{V_{gfbe}}{V0}\frac{EPSI}{EPS}\right)^{\frac{2.V0}{\left(\frac{2.V0.V_{tho}}{2.V0-V_{th}}\right)}}$$ Equation_Apx J.10

where

$$V_{gfbe} = \frac{VMIN}{2}\left[1+\frac{V_{gs}-VFB}{VMIN}+\sqrt{DELTA^2+\left(\frac{V_{gs}-VFB}{VMIN}-1\right)^2}\right],$$ Equation_Apx J.11

$$V_{tho} = \frac{k_B.TNOM}{e}$$ Equation_Apx J.12

and

$$V_{th} = \frac{k_B.TEMP}{e}.$$ Equation_Apx J.13

TEMP is a user specified parameter (during simulation) and not a parameter extracted from the transistor characteristics.

[1] M. Hack, *et al.*, "Physical models for amorphous-silicon thin-film transistors and their implementation in a circuit simulation program," Electron Devices, IEEE Transactions on, vol. 36, pp. 2764-2769, 1989.

[2] T. A. Fjeldly, T. Ytterdal, and M. Shur, "Introduction to device modeling and circuit simulation," John Wiley & Sons, New York, 1998, ISBN 0-471-15778-3.

[3] M. S. Shur, *et al.*, "SPICE Models for Amorphous Silicon and Polysilicon Thin Film Transistors," Journal of The Electrochemical Society, vol. 144, pp. 2833-2839, 1997.

Appendix K : Calculation of Dielectric Constant Values Using Series, Parallel And Logarithmic Mixing Equations

PVP
Density = 1.16 g/mL
ε = 5.4

BST
Density = 4.91 g/mL
ε = 50

PVP-BST8 solution with 10 wt% PVP and 8 wt% BST

Volume of PVP = $\frac{mass}{density} = \frac{10}{1.16} = 8.62mL$

Volume of BST = $\frac{mass}{density} = \frac{8}{4.91} = 1.63mL$

Volume fraction of PVP = $\frac{8.62}{8.62+1.63} = 0.84$

Volume fraction of BST = $\frac{1.63}{8.62+1.63} = 0.16$

Using series mixing equation,

$$\frac{1}{\varepsilon} = \frac{V_1}{\varepsilon_1} + \frac{V_2}{\varepsilon_2} = \frac{0.84}{4.4} + \frac{0.16}{50} = 0.194$$

$$\varepsilon = 5.15$$

Using parallel mixing equation,

$$\varepsilon = V_1\varepsilon_1 + V_2\varepsilon_2 = 0.84(4.4) + 0.16(50) = 11.696$$

Using Lichtenecker's logarithmic mixing equation,

$$\log \varepsilon = V_1 \log \varepsilon_1 + V_2 \log \varepsilon_2 = 0.84 \log 4.4 + 0.16 \log 50 = 0.812$$

$$\varepsilon = 6.49$$

For 50% BST loss,

Volume of PVP = $\frac{mass}{density} = \frac{10}{1.16} = 8.62mL$

Volume of BST = $\frac{mass}{density} = \frac{4}{4.91} = 0.81mL$

Volume fraction of PVP = $\frac{8.62}{8.62+0.81} = 0.914$

Volume fraction of BST = $\frac{0.81}{8.62+0.81} = 0.086$

Using series mixing equation (50% loss),

$$\frac{1}{\varepsilon} = \frac{V_1}{\varepsilon_1} + \frac{V_2}{\varepsilon_2} = \frac{0.914}{4.4} + \frac{0.086}{50} = 0.2094$$

$\varepsilon = 4.77$

Using parallel mixing equation (50% loss),

$\varepsilon = V_1\varepsilon_1 + V_2\varepsilon_2 = 0.914(4.4) + 0.086(50) = 8.32$

Using Lichtenecker's mixing logarithmic equation (50% loss),

$\log \varepsilon = V_1 \log \varepsilon_1 + V_2 \log \varepsilon_2 = 0.914 \log 4.4 + 0.086 \log 50 = 0.734$
$\varepsilon = 5.42$

PVP-BST16 solution with 10 wt% PVP and 16 wt% BST

Volume of PVP = $\frac{mass}{density} = \frac{10}{1.16} = 8.62mL$

Volume of BST = $\frac{mass}{density} = \frac{16}{4.91} = 3.26mL$

Volume fraction of PVP = $\frac{8.62}{8.62+3.26} = 0.73$

Volume fraction of BST = $\frac{3.26}{8.62+3.26} = 0.27$

Using series mixing equation,

$$\frac{1}{\varepsilon} = \frac{V_1}{\varepsilon_1} + \frac{V_2}{\varepsilon_2} = \frac{0.73}{4.4} + \frac{0.27}{50} = 0.171$$

$\varepsilon = 5.83$

Using parallel mixing equation,

$\varepsilon = V_1\varepsilon_1 + V_2\varepsilon_2 = 0.73(4.4) + 0.27(50) = 16.7$

Using Lichtenecker's logarithmic mixing equation,

$\log \varepsilon = V_1 \log \varepsilon_1 + V_2 \log \varepsilon_2 = 0.73 \log 4.4 + 0.27 \log 50 = 0.928$

$\varepsilon = 8.48$

For 50% BST loss,

Volume of PVP = $\frac{mass}{density} = \frac{10}{1.16} = 8.62mL$

Volume of BST = $\frac{mass}{density} = \frac{8}{4.91} = 1.63mL$

Volume fraction of PVP = $\frac{8.62}{8.62+1.63} = 0.84$

Volume fraction of BST = $\frac{1.63}{8.62+1.63} = 0.16$

Using series mixing equation (50% loss),

$$\frac{1}{\varepsilon} = \frac{V_1}{\varepsilon_1} + \frac{V_2}{\varepsilon_2} = \frac{0.84}{4.4} + \frac{0.16}{50} = 0.194$$

$$\varepsilon = 5.15$$

Using parallel mixing equation (50% loss),

$$\varepsilon = V_1\varepsilon_1 + V_2\varepsilon_2 = 0.84(4.4) + 0.16(50) = 11.696$$

Using Lichtenecker's logarithmic mixing equation (50% loss),

$$\log \varepsilon = V_1 \log \varepsilon_1 + V_2 \log \varepsilon_2 = 0.84 \log 4.4 + 0.16 \log 50 = 0.812$$

$$\varepsilon = 6.49$$

PVP-BST24 solution with 10 wt% PVP and 24 wt% BST

Volume of PVP = $\frac{mass}{density} = \frac{10}{1.16} = 8.62mL$

Volume of BST = $\frac{mass}{density} = \frac{24}{4.91} = 4.89mL$

Volume fraction of PVP = $\frac{8.62}{8.62+4.89} = 0.64$

Volume fraction of BST = $\frac{4.89}{8.62+4.89} = 0.36$

Using series mixing equation,

$$\frac{1}{\varepsilon} = \frac{V_1}{\varepsilon_1} + \frac{V_2}{\varepsilon_2} = \frac{0.64}{4.4} + \frac{0.36}{50} = 0.152$$

$$\varepsilon = 6.55$$

Using parallel mixing equation,

$\varepsilon = V_1\varepsilon_1 + V_2\varepsilon_2 = 0.64(4.4) + 0.36(50) = 20.81$

Using Lichtenecker's logarithmic mixing equation,

$\log \varepsilon = V_1 \log \varepsilon_1 + V_2 \log \varepsilon_2 = 0.64 \log 4.4 + 0.36 \log 50 = 1.023$

$\varepsilon = 10.55$

For 50% BST loss,

Volume of PVP = $\frac{mass}{density} = \frac{10}{1.16} = 8.62mL$

Volume of BST = $\frac{mass}{density} = \frac{12}{4.91} = 2.44mL$

Volume fraction of PVP = $\frac{8.62}{8.62+2.44} = 0.78$

Volume fraction of BST = $\frac{2.44}{8.62+2.44} = 0.22$

Using series mixing equation (50% loss),

$\frac{1}{\varepsilon} = \frac{V_1}{\varepsilon_1} + \frac{V_2}{\varepsilon_2} = \frac{0.78}{4.4} + \frac{0.22}{50} = 0.181$

$\varepsilon = 5.5$

Using parallel mixing equation (50% loss),

$\varepsilon = V_1\varepsilon_1 + V_2\varepsilon_2 = 0.78(4.4) + 0.22(50) = 14.43$

Using Lichtenecker's logarithmic mixing equation (50% loss),

$\log \varepsilon = V_1 \log \varepsilon_1 + V_2 \log \varepsilon_2 = 0.78 \log 4.4 + 0.22 \log 50 = 0.876$

$\varepsilon = 7.51$