

CURRENT SOURCE INVERTERS FOR PM MACHINE CONTROL

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ABSTRACT

Current Source Inverters for PM Machine Control.

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Brushless permanent magnet (PM) drive systems offer a high efficiency over a wide power/torque-speed operating envelope, however, there are a number of problems that may limit, or complicate, their operation particularly in automotive and aerospace vehicular applications, i.e. the loss of control of the power silicon gate drive circuitry during flux-weakening operation, control of high-speed low-inductance machines and the presence of large electrolytic capacitors on the inverter DC link. Current Source Inverters (CSIs) could potentially address some or all of the above issues. However, they have found little application to date due to the wide use of the Voltage Source Inverter (VSI) circuit topology.

This thesis investigates feasibility of utilising Current Source Inverters (CSIs) to control permanent magnet synchronous machines in automotive and aerospace actuation systems. CSIs, switching at the fundamental frequency, were used in some of the first semiconductor based, electronic variable speed drive systems that utilised the simple, low maintenance AC induction motor. However, the rapid progress of semiconductors and discovery of Pulse Width Modulation (PWM) techniques soon resulted in the Voltage Source Inverter (VSI) replacing the CSI in all but the highest power applications. Modern power electronics and (micro-processor based) control systems mean that the advantages of VSI systems may no longer be significant and combined with the unique environmental conditions that automotive and aerospace applications present, could allow the CSI to offer advantages over VSIs in these applications.

The thesis presents the switching and control logic for CSIs and mapping to the more conventional VSI logic. Analysis is made of the various loss mechanisms in VSI and CSI power circuitry. Simulation models of the VSI and CSI structures are presented and representative drive systems designed, built and tested to validate the model developed. Comparisons are made of the two inverter topologies based on power conversions and loss audits of the test validation hardware.

DECLARATION

No portion of the work referred to in this thesis has been submitted in support of an application for another degree or qualification of this or any other place of learning.

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CHAPTER 1

CURRENT SOURCE INVERTERS FOR PM MACHINE CONTROL

1.1 Introduction

The efficient conversion and utilisation of energy is possibly one of the most challenging issues for the future progress of humankind. Given the correlation between energy usage and societal development [1], the requirement for more efficient and less polluting energy conversion and utilisation is becoming more apparent, not only in the UK and an expanding European Union, but in emerging economies world-wide, India and China being clear examples. The reduction of carbon emissions linked with more fuel efficient propulsion for air and land based transport vehicles is a significant research challenge and a subject area actively researched within the Power Conversion Research Group at the University of Manchester. The research challenge of more/all-electric road and air vehicles, for example; all- and hybrid-electric road vehicles, more-electric conversion systems for aircraft, specifically electro-hydrostatic (electro-hydraulic) and electro-mechanical flight control surface actuation systems are among some of the research topics.

The research presented in this thesis is supported by the University of Manchester Alumni Fund which provided a broad remit in the subject area centred around the improved conversion and utilisation of energy. The research is also closely linked to a European Framework 6 Integrated Project, CESAR, “Cost Effective Small AiRcraft” [2] which provided benchmark specification requirements for the power electronic inverter that forms the main subject area of this thesis research.

A key element for the conversion of energy in more-electric system power trains is a brushless machine based drive-system comprising of an electro-magnetic machine, associated power electronic inverter (or converter) and control there-of. Although there are a number of electro-magnetic machine technologies, this research is solely related to brushless permanent magnet machine based systems, a technology choice arising from studies undertaken as part of the CESAR project [2]. To-date, the majority of these drive-systems are voltage source (VSI) based. This is exclusively so for automotive applications, although matrix converter systems [3,4] are receiving much interest in the aerospace sector.

In automotive and aerospace vehicular applications there are a number of operational problems encountered with variable speed brushless permanent magnet drive systems that significantly impact on system design, for example: the inverter may be electronically disabled with the machine in high-speed flux-weakening mode [5,6] control of high speed low-inductance machines [6], electrolytic capacitors on the inverter DC link [24,29] – particularly at high temperatures (100°C) and altitudes commensurate with aircraft operation.

Current Source Inverters (CSIs) could potentially address some or all of the above issues and are hence worthy of study for these vehicular applications. Traditionally, CSIs have found little usage in industry in general due to the much simpler, in terms of current control [7], structure of the Voltage Source Inverter (VSI) circuit topology. Indeed, nearly all inverter drives are of the VSI topology, with only a few reported publications investigating CSI structures over the last 15 years, as will be discussed later.

The CSI can produce a voltage boost function and hence there has been some research interest in their application as a fuel cell-to-AC interface. Fuel cells have poor voltage regulation at full-load power [8] and it is preferable to operate them with regular, non-pulsed, uni-polar load current. It will be reported in subsequent chapters that there is DC link current ripple for the CSI system studied and the voltage boost feature only equates to $\sqrt{3/2}$ p.u. voltage gain (1.46 p.u. required for a typical fuel cell application). CSIs for fuel cell interface applications are summarised but not studied in any depth in this thesis.

The primary subject area of this thesis is the design of a CSI and the comparison there of with a reference VSI benchmark design for an aerospace application provided via the

CESAR project. The remainder of chapter 1 investigates the historical development of variable speed drive systems to illustrate system components and present terminologies. Since CSIs formed a core of early drive systems, these will be discussed, along with recent system studies, to establish prior work and state of the art development.

Sections 1.4 to 1.6 have discussed the issues associated with high speed, flux-weakening operation of brushless permanent magnet machines and present analysis and example results that highlight the over-rating necessary for such schemes. The control of high speed, low inductance machines and the issues associated with electrolytic capacitors in automotive and aerospace applications will also be covered.

Chapter 1 concludes with a review of CSIs for fuel cell applications. Chapter 2 discusses evolution of standard VSI switch and control schemes for CSI applications. Consideration of the pre-charge is presented and mapping of VSI to CSI logic discussed. Chapter 3 develops analytic equations for the estimation of VSI and CSI losses and proposes a drive system specification that forms the basis of the VSI and CSI comparative study Chapters 4 and 5. Chapter 4 develops circuit simulation models for both the VSI and CSI topologies and presents simulation results that compare their relative performance. Chapter 5 presents a circuit and test facility hardware design to validate the analysis of Chapter 3 and simulation study of Chapter 4. Finally, Chapter 6 draws conclusions from all Chapters and suggests the scope for further research.

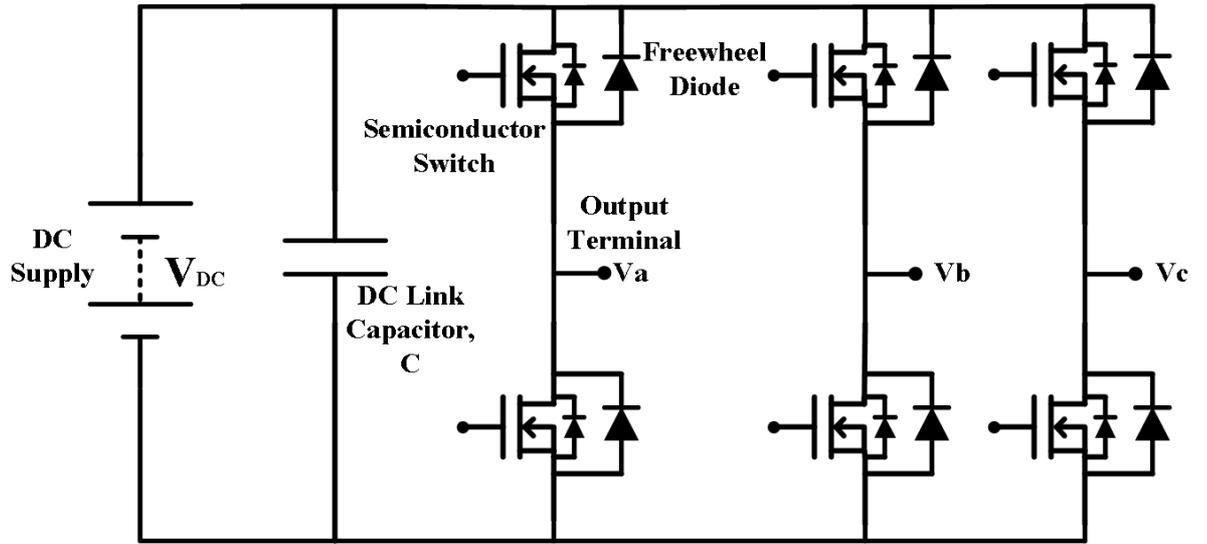
1.2 Development of Variable Speed Drive Systems

The reference to the voltage and current source for inverter circuit topologies essentially refer to the supply and how the load connected to the inverter affects the supply. The inverter is classed as voltage source if it has a ‘stiff’ DC voltage supply and the output voltage waveforms are not affected by the load, conversely, a current source if it has a ‘stiff’ DC current supply and the output current waveforms are not affected by the load [9].

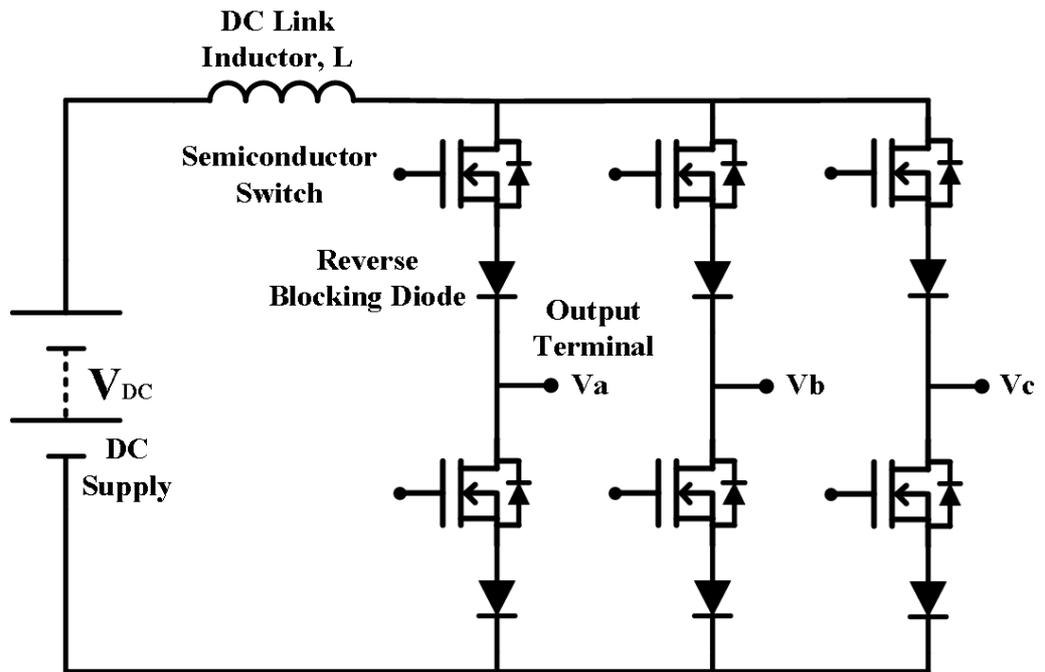
Connecting a large capacitor across the DC link is the usual method for creating a ‘stiff’ DC voltage supply, while connecting an inductor in series in the DC link is the usual method for creating a ‘stiff’ current supply [10].

The presence of a capacitor or inductor in the DC link is normally the basis for differentiating between a VSI from a CSI topology, although some VSIs incorporate an inductor in addition to the capacitor to form a filter, if, for example, the input supply is not via a smooth DC source, as in the case of a simple full-bridge rectified AC supply. Figure 1.1 illustrates the topology of a voltage source inverter (a) and current source inverter (b) for control of three-phase machine (outputs, V_a , V_b and V_c) via a fixed DC supply (V_{dc}). The main circuit elements are highlighted, i.e. DC link capacitor (VSI), link inductor (CSI), semiconductor switching devices, free-wheel (VSI) and reverse blocking (CSI) diodes. For this study, the semiconductor switches are insulated-gate-bipolar-transistors (IGBTs) due to the system voltage levels of interest.

The aim of most variable speed drives is to provide a controlled torque and speed to the load of the inverter. For many automotive and aerospace actuation systems, the load torque-speed envelope has a maximum (or near maximum) torque from zero speed to a full-voltage base speed, followed by an extended speed region where torque reduces from the maximum but power is maintained up to some load dictated maximum speed, as illustrated in Figure 1.2. Such a torque-speed characteristic is commonly referenced as a ‘traction’ characteristic. Brushed DC drive systems can readily achieve the power or torque profile above base-speed by reduction of the machine field current. Brushless machines, i.e. induction, permanent magnet, switched or synchronous reluctance, have no direct field current control mechanism. However, these machine topologies can be operated in the flux-weakening region by suitable excitation of the stator windings via the power converter, provided they are suitably designed [11].



(a) Voltage source inverter



(b) Current source inverter

Fig. 1.1 Circuit topologies for the voltage and current source inverters.

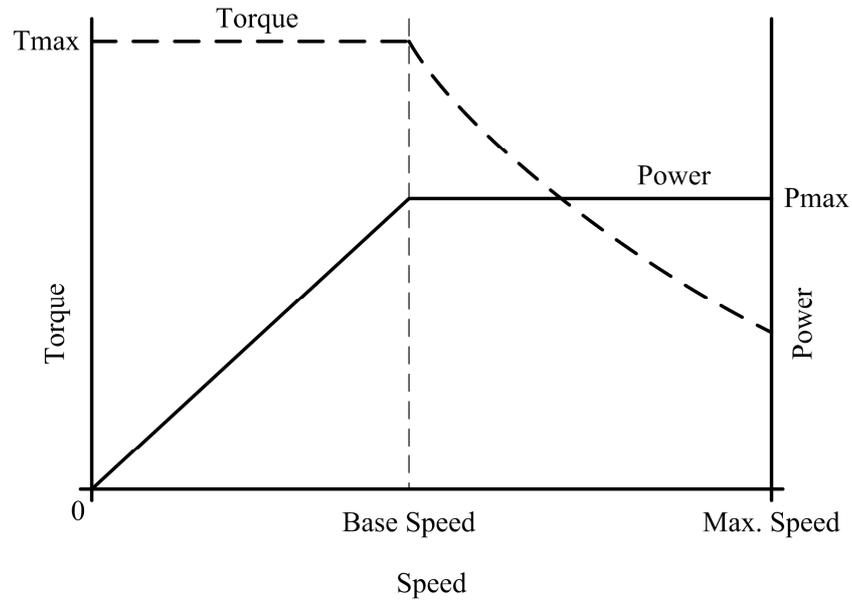


Fig. 1.2 Typical traction torque-speed characteristic.

Electric variable speed drives were traditionally realised via brushed DC machines with resistive armature and field voltage control or Ward-Leonard schemes [12]. The invention of the thyristor, or silicon controlled rectifier (SCR) as it was also known by General Electric in 1958 [13], allowed the control of the conduction point on an AC waveform. By varying the firing angle, as it is known, the magnitude of the resulting rectified DC voltage can be controlled. SCRs are not without limitations, although their voltage and current ratings are good, compared to MOSFETs and IGBTs, they can not be ‘turned-off’ by application of a signal. SCRs only turn-off if the turn-on signal is removed and the current stops flowing by another means, either via the connected load or circuits providing forced commutation. This lack of turn-off capability means SCRs cannot be used on DC circuits without additional commutation (turn-off) methods, limiting their practical application. To produce a low DC voltage from an AC supply the firing angle of the SCR has to be increased so that the device only conducts for a short time in each half cycle, this delay creates currents that are out of phase with the supply voltage and hence undesirable low power factors.

The brushed DC drive system generally has a good traction characteristic, shown in Figure 1.2. However, these machines require regular maintenance of the brush-gear, the ratings are limited by the ratings of the brush-gear and some applications are not possible due to the sparking of the commutator.

The induction motor, with its brushless design and general ruggedness, is ideal for harsh environments. The first electronic variable speed induction machine drives used SCRs to create a variable AC voltage at the required (variable) supply frequency. To create the performance similar to that of a brushed DC drive system a variable frequency inverter drive system provides a constant voltage to frequency ratio from zero to base speed, where-after a constant (maximum) voltage but increasing frequency control effectively flux-weakens the induction machine. Figure 1.3 illustrates induction machine torque-speed characteristics. Switching four, for single phase operation, or six, for three phase operation, devices in a predetermined pattern, creates the AC output. The inverter can be classed as either voltage or current source, as defined, each type having its advantages and disadvantages.

Although not considered as a machine option in this thesis, the induction machine is discussed here since early inverters were generally current source [14], due to the good voltage and current ratings that allowed them to be used on medium and high power applications, 100's of kW upwards, with the inclusion of simple commutation circuitry to commutate the SCRs. A typical CSI is the auto-sequentially commutated inverter (ASCI), as illustrated in Figure 1.4 (a). The ASCI was fed from a controlled rectifier, and utilised a six pulse controlled rectifier with unidirectional control capabilities and a smoothing inductor. The inverter circuit power stage components, Figure 1.4 (b), consist of SCRs, diodes and capacitors. The capacitors are necessary to aid commutation. The capacitor between two phase legs charges when the next SCR in the sequence is turned on, once the required voltage across the capacitor is reached; it changes the bias of the diode stopping the diode and its associated SCR from conducting.

During the 1970's CSI systems were popular due to their simplicity, controllability and regenerative capabilities [15]. Typical CSI output waveforms from research publications of the time, illustrated in Figure 1.5, for a synchronous machine [15] (a) and a linear inductor motor [16] (b), showing the essentially rectangular phase currents and near sinusoidal phase voltage. The 6x fundamental ripple in the phase voltage, and consequential phase current transients arise from the SCR switching. In the 1970's and early 1980's CSI research mainly focussed on improved control schemes for better dynamic control [17] and reducing torque pulsations [18]. In the mid-1980's low frequency PWM techniques emerged for CSIs promising a reduction in harmonics and torque pulsations [19,20], Figure 1.6 illustrates the inverter waveforms for an induction machine based CSI drive system reported by Nonaka et al [20].

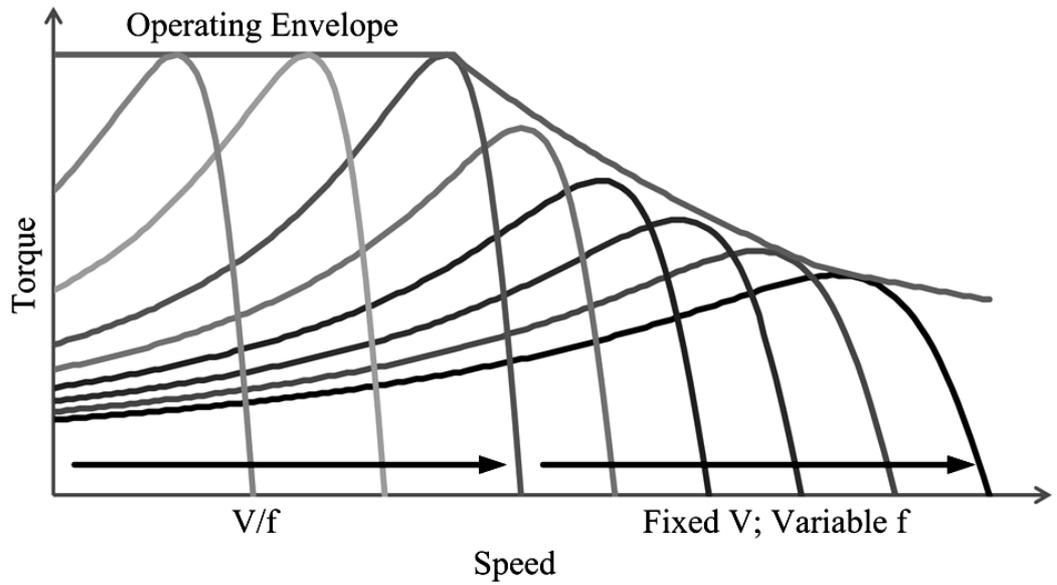


Fig. 1.3 Induction machine torque-speed characteristics.

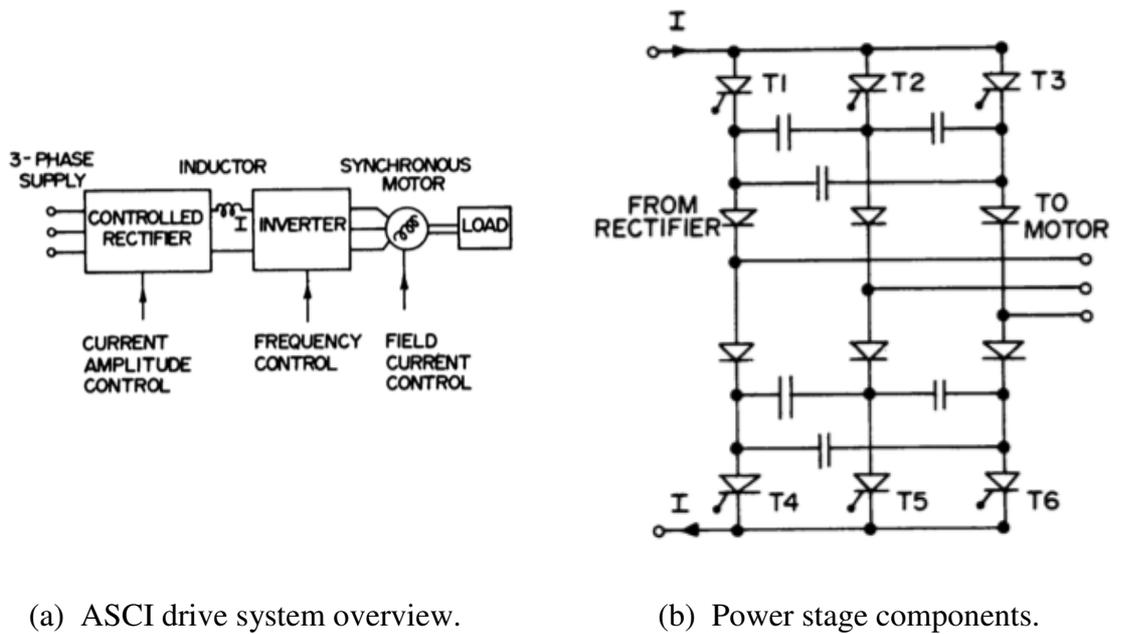
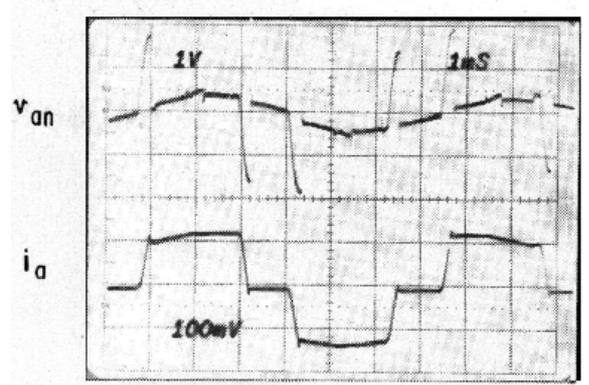


Fig. 1.4 Early A.C. machine drive system [17].

In the mid-1990's CSI research increased with and much effort was directed at reducing the voltage stress induced in the machine cable runs [21] and machine windings, reducing induced bearing currents [22] and control of low impedance static loads [23], Figure 1.7 illustrates the VSI (a) and CSI topologies (b) discussed by Delli Colli et al [24].



(a) Synchronous machine [15].



(b) Linear inductor machine [16].

Fig. 1.5 Typical ASCII output waveforms.

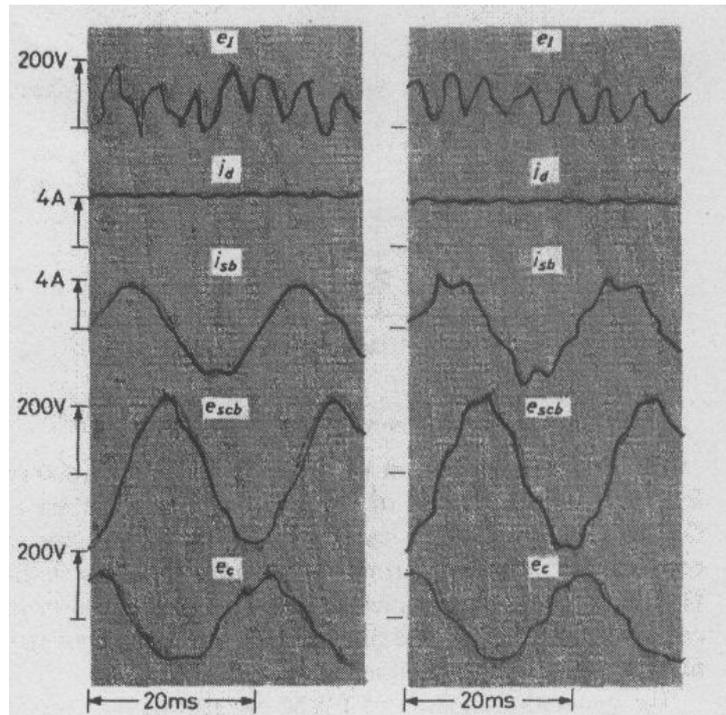
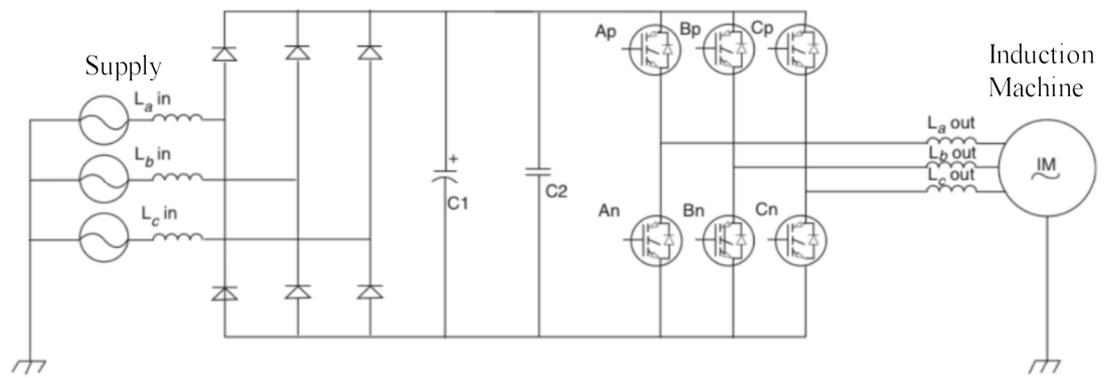
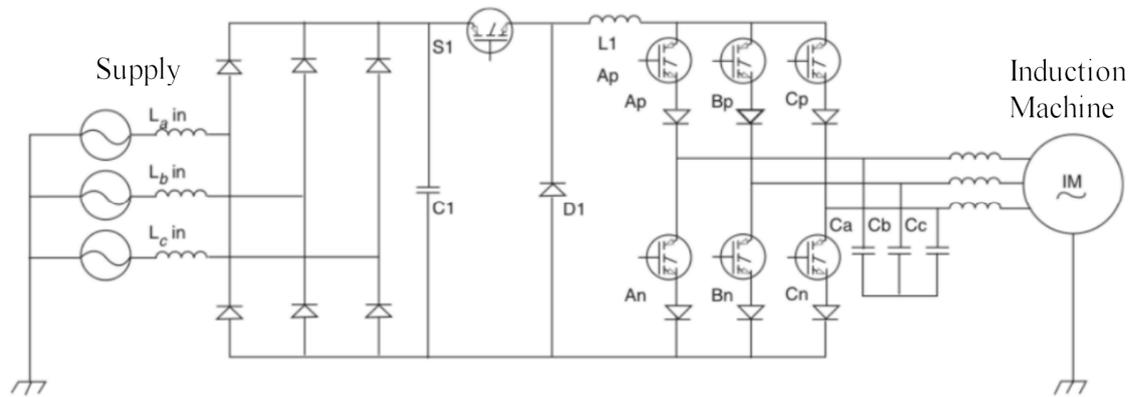


Fig. 1.6 ASCII output waveforms [22].



(a) VSI topology.



(b) CSI topology.

Fig. 1.7 Circuit topologies for the voltage and current source inverters [24].

During the early evolution of power electronic inverter drive systems, VSI systems were initially not as popular as CSI systems, although the reason is not clear. Semiconductors of the required voltage and current ratings were not available and commutation circuitry generally relied on the back-EMF or DC link voltage to operate correctly. For the ASCI system, the extra capacitors and diodes created additional losses and restricted the switching speed, and hence rotational speed of the drive system. Another popular method of commutation was load commutation, implemented by creating a leading power factor load where the switching devices could turn-off with additional circuitry. To achieve this with an induction motor a VAR generator has to be attached to the inverter output to supply the induction machine VARs and present a leading power factor load to the inverter. This implementation becomes difficult with varying frequency since the VAR generator would have to vary to prevent resonance and oscillations.

As the switching speeds of semiconductor devices increased they allowed PWM switching schemes to be introduced at significantly higher frequencies than achievable with SCR drives, i.e. in the region of 1-10kHz for IGBT based drive systems. The increased PWM switching speeds lead to improved harmonic performance reducing losses in the machine at the expense of some additional silicon switching losses. The PWM scheme also allowed a fixed voltage DC link, improving the efficiency and power factor of the input rectifier. Low to medium power VSIs thus became popular with the availability of power transistors; MOSFETs and IGBTs since these devices do not require commutation circuitry. As power levels increased VSIs were used in increasingly larger power and higher DC voltage applications reducing the market for CSI systems [25]. To date no silicon devices with the required voltage blocking capability are available; therefore PWM CSIs have to be assembled from discrete diode units in series with non-blocking switches. This creates additional losses over VSI systems since twice as many devices conduct at one time and thus the CSI is generally less attractive than VSI systems.

1.3 Recent Research

Recent research into CSIs, 1996 to 2009, can be categorised into several groups;

- hybrid topology machine control applications,
- non-machine applications, and
- CSI machine control applications.

Hybrid, dual, topology drives have been studied by several researchers including [26,27,28] but this research is of little interest in applications where the elimination of the DC link capacitor is required. The hybrid systems utilise a CSI topology using fundamental frequency switching in parallel with a small VSI system to aid the commutation of the CSI or to remove the output filter capacitors. The advantages, for the applications studied, include; the simplicity of the CSI, robustness, and high power capabilities, 100's of kW.

Non-motor applications such as Uninterruptable and Programmable Power Supplies (UPPS) [23], Superconducting Magnetic Energy Storage Systems (SMES) [21], fuel cell interface [29] and general CSI operation [21] have been studied. Loh et al. [21] investigated a modified PWM scheme for CSIs in SMES systems, where the CSI topology shows possible advantages over VSI systems, in particular, short circuit protection and the control of low impedance loads. The modified PWM scheme utilises controlled

freewheeling of the inductor to separate the input and output of the inverter, improving system control. Bendre et al. [25] studied a method for utilising high power SCRs in a PWM inverter, as opposed to fundamental frequency switching, through the use of a single gate turn-off device across the DC link. This removes the need for gate turn-off devices in series with diodes in the inverter. The proposed scheme is shown to allow PWM operation with SCRs, although the switching frequency is limited due to the time required for the reverse recovery of the SCRs. The upper limit of the switching frequency is estimated to be between 3kHz and 5kHz. Rivas and Rufer [29] investigate the use of a PWM CSI for interfacing fuel cells to the AC grid. They present a modified PWM scheme for reducing losses and harmonics and present a loss comparison between the CSI and an equivalent VSI system with Boost Converter (BC). They conclude that the CSI has lower switching losses but higher conduction losses, overall the VSI+BC is marginally more efficient.

CSI research in machine control applications has predominantly focused on use with induction machines [24,30,31,32,33,34,35,36]. Only two applications of the CSI with a brushless permanent magnet synchronous machine (PMSM) have been noted to date [7,37]. For IM applications several papers [22,23,24,36] have investigated the use of the CSI topology to reduce voltage stress on the motor cable and winding insulation along with reducing bearing currents. Salo et al [33] also present the CSI as a simpler topology in terms of measurements as it is possible to use the DC link current measurement instead of multiple phase currents. Colli et al [23] concludes that the CSI reduces voltage stress and bearing current but offers a lower efficiency. Several papers [31,34,38] investigate the dynamic performance of the CSI compared to equivalent VSI systems, while Suh et al [35] compare efficiency. Suh et al, investigate medium voltage applications (for MW systems) and concludes that there is less than 1% difference between VSI and CSI systems, however he claims to use a “relatively simple engineering method of calculating losses” along with failing to include the losses associated with the line side passive components in the comparison. Klönne et al, [30] compare the dynamic performance of complete rectifier/inverter CSI systems while investigating the factors that influence the inductor size, with view to improving the mass and volume of the system, they present measured results for an improved dynamic response of an induction machine. Nikolic et al [34] investigate a modified control scheme to eliminate errors, improving torque ripple and other characteristics, in a system switching the machine at the fundamental frequency (i.e. over-modulated) with an active rectifier providing the controlled DC link current.

In PMSM applications, Hinrichsen [7] investigates the use of a fundamental frequency switching CSI system with low inductance PM machines, where VSI solutions require extremely high switching frequencies to control current and can lead to EMI and system overvoltage problems. It is concluded that the CSI address the VSI problems, although, as with Nikolic et al [34], a current controlled active rectifier is required for fundamental frequency switching. PWM techniques in combination with a PMSM have been found in one single paper, Cancelliere et al [37], who investigate the use of a soft switching CSI for an axial flux PMSM in an electric vehicle wheel drive. The axial flux motor is proposed to have greater efficiency with its direct drive capability, instead of the traditional gearbox-driveshaft assemblies, and the low axial length tends to fit with current vehicle design for integration within the wheel hub. The CSI is of interest due to the reduced voltage stress on the cable and winding insulation and the greater efficiency of the sinusoidal phase currents afforded by the CSI topology. Soft switching is proposed to further increase the efficiency of the system by reducing the voltage stress further and reducing the switching losses within the inverter power electronics. These benefits are, however, at the expense of additional circuit components, in this case three power electronic, four passive, and much more complex control. The proposed control scheme performs a “first guess” for the switching timing, followed by multi-stage checking of the calculated, and possibly adjusted, values to ensure correct zero current operation. A major weakness of the paper is that it is purely a simulation based study providing no test validation.

1.4 CSI Benefits – Flux-weakening Control

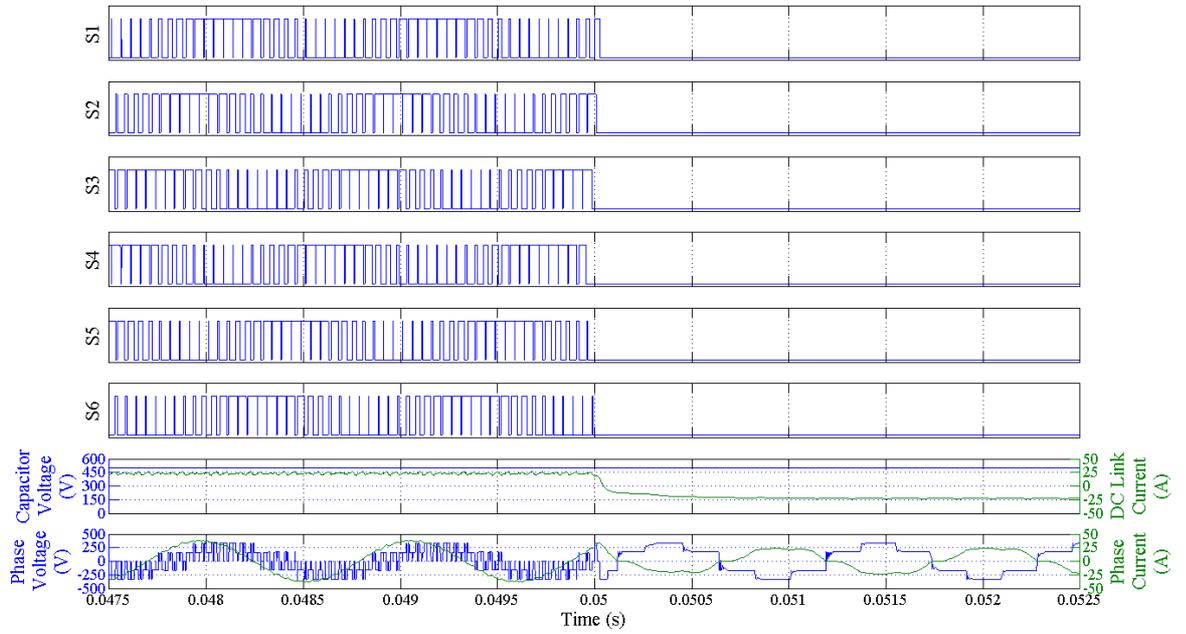
Flux-weakening is a well publicised method of controlling brushless machines to realise a reduced torque, extended speed operating region with a near constant power, Figure 1.2, within the machine supply voltage and current constraints. As discussed previously, such a traction characteristic is desirable in many applications, in particular automotive and marine traction, but also in aerospace where activation of aircraft flight surfaces often require such performance envelopes.

Flux-weakening operation should allow for drive system design optimisation, leading to improving the utilisation of the power supply, electronics, machine electro-magnetics and a reduction of the motor mass/volume of the machine and/or the VA rating of the inverter components [11]. A lower VA rating of the inverter components will inevitably lead to a lower cost and lower mass/volume inverter. Note, in aerospace mass and volume of systems are key design optimisation criteria.

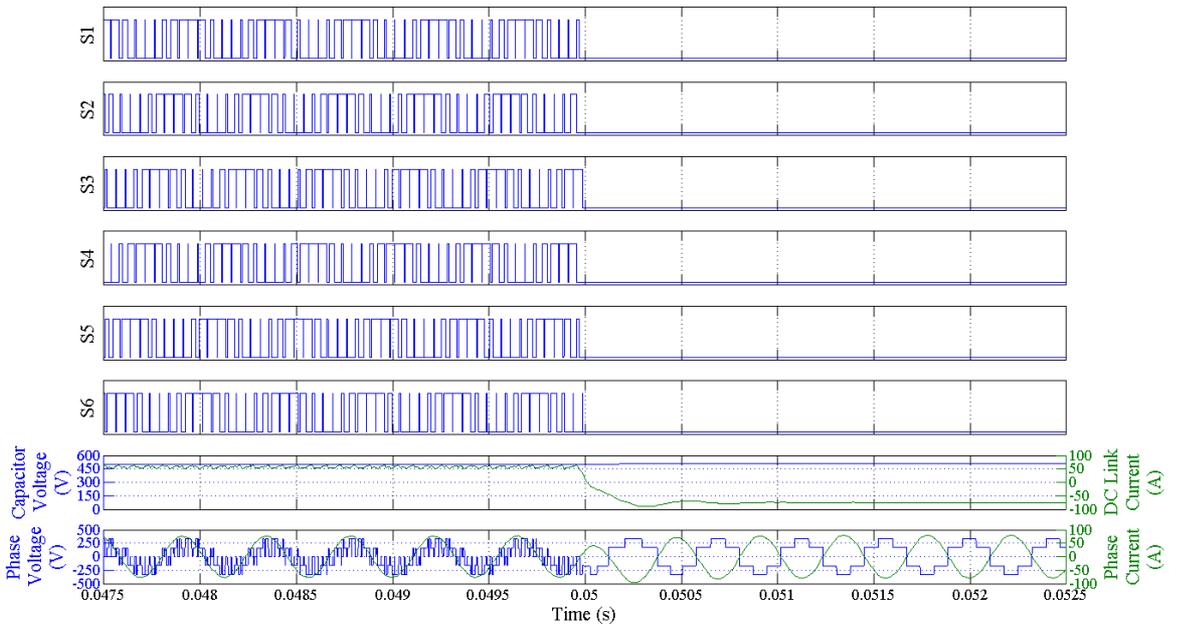
Brushless permanent magnet machines can only yield constant power in the flux-weakened region if their electro-magnetics are designed appropriately – so called 1.0 per unit inductance machines [11]. Here, some back-EMF is compromised and a higher than normal phase inductance is realised.

The operation in the flux-weakening mode results in the machine back-EMF being larger than the supply phase voltage. This is of great concern for PM machine based drive systems since the rotor magnetisation is fixed; it may or may not be an issue with other machine technologies depending upon the transient excitation conditions. For example, the operation of PM machines above base speed poses no problems when operating during steady operation. However, should the control signals to the power electronic devices fail or be disabled above base speed, the inverter fly-back diodes will function as an uncontrolled 3-phase bridge rectifier to the machine back-EMF [5,39] until the machine coasts down to below base speed. The excessive overvoltage will potentially over charge the DC link capacitor. The current flowing through the semiconductor devices may also exceed their maximum operating level. Usually a crowbar circuit is used to dissipate the excess energy. However, any crowbar circuit would need to be independent from the main control system to ensure operational integrity. Figure 1.8 illustrates the loss of VSI switching control at full load base speed (a) and at 3 times full load base speed (b). There is a lack of understanding regarding failures of PM machine drive systems during flux-weakening operation as identified in [5]. Thus, a case study was undertaken to assess the impact on VSI and CSI inverter component rating due to drive system failure during high speed, flux weakening operation. An aerospace drive system was redesigned to facilitate flux-weakening operation.

A trade study was carried out by researchers in the Power Conversion Group of the University of Manchester into improving the drive system optimisation of an aerospace actuation PMSM drive system. The original PMSM specification is detailed in Table 1.1, torque and power-speed profiles illustrated in Figure 1.9.



(a) Loss of switching at 1p.u. base speed.



(b) Loss of switching at 3p.u. base speed.

Fig. 1.8 Loss of VSI switching control during base and extended-speed operation.

Speed (max.)	23000 rpm
Poles	4 -
Power (mech)	16 kW
Torque (max.)	8 Nm
DC Supply	550 V
I_{ph} (max.)	46 A

Table 1.1 Aerospace actuation PMSM specification.

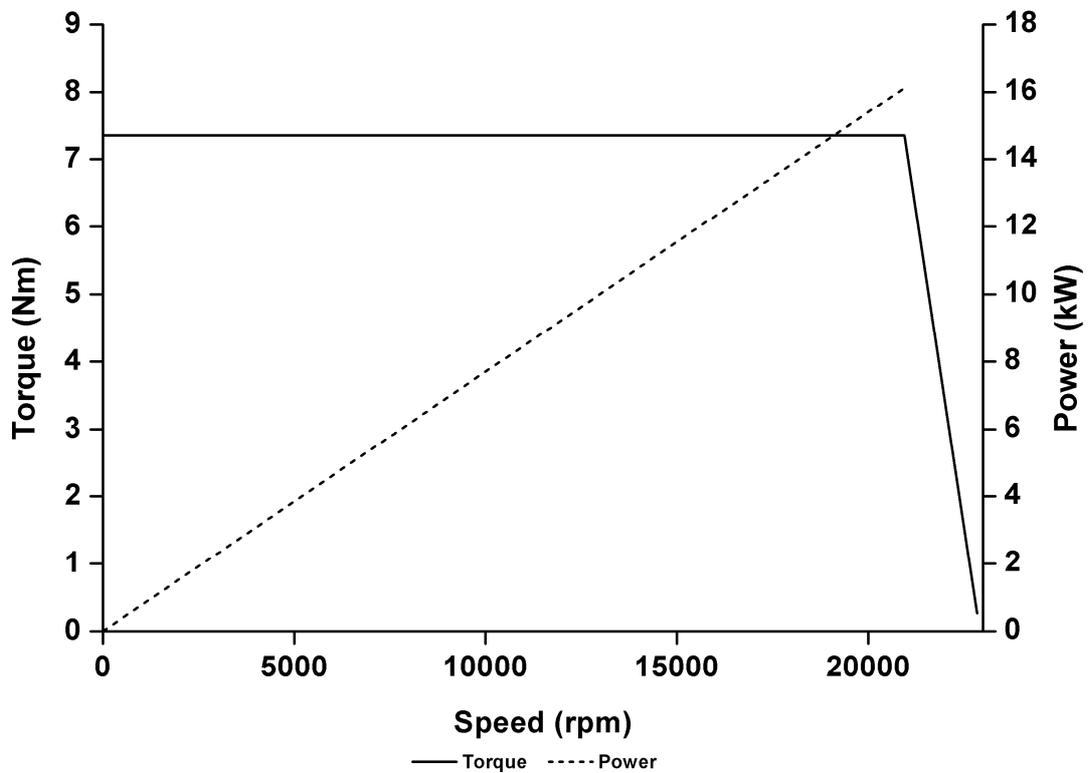


Fig. 1.9 Drive system performance characteristic.

It should be noted that the drive system performance is only a transient duty with operational manoeuvres lasting in the order of minutes. The actual flight surface operating points are overlaid on the drive system performance characteristic in Figure 1.10 showing that the drive system is considerably overspecified in terms of peak power capability if a constant torque (no flux-weakening) control philosophy is adopted. Analysis of the required operating envelope suggested a flux-weakening ratio of 4:1 with a base speed of 5000 rpm, yielding a peak power reduction of almost 75% and machine phase current reduction of 26%. Given the new operating envelope, the inverter components VA ratings

were optimised to take advantage of the modified design. The optimised machine specification is detailed in Table 1.2. Confidentiality issues restrict publication of the actual and modified machine parameters.

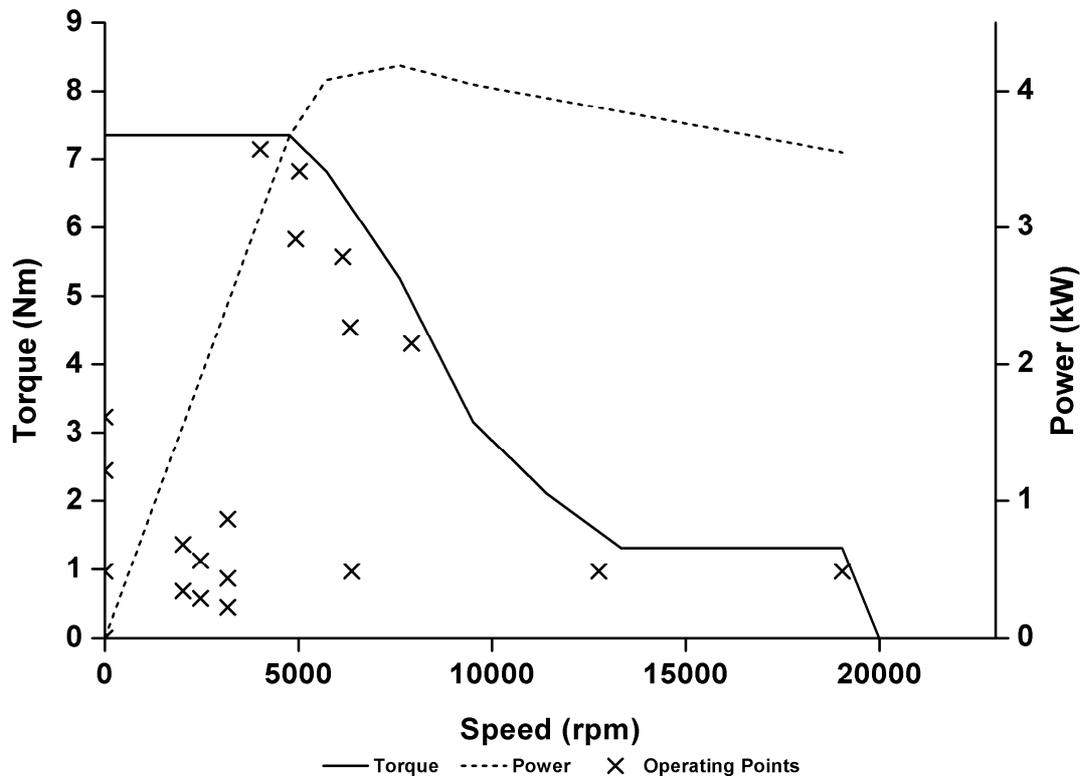


Fig. 1.10 Optimised PMSM drive system torque and power-speed characteristics employing flux-weakening operation.

Speed (max.)	20000 rpm
Poles	4 -
Power (mech)	4.2 kW
Torque (max.)	8 Nm
DC Supply	550 V
I_{ph} (max.)	12 A

Table 1.2 Optimised PMSM specification.

Utilising the new machine design a SABER™ simulation model was developed and used to investigate the consequences of loosing control of the inverter power electronic switches while operating at full-speed, i.e. 4 times base-speed. Figure 1.11 illustrates the predicted DC link voltage and the current conducted through the diodes within the VSI and by the

DC link capacitor, while Table 1.3 details a summary of the results. It can be seen that a very large transient current flows at the instant of the control failure. Thus the VSI power electronics and DC link capacitor would have to be rated accordingly to prevent damage. The peak current of each flyback diode within the VSI will depend on the electrical position of the PMSM at the point of failure. The worst-case condition arises if the failure occurs when one phase of the machine EMF is at either its maximum or minimum. Here, maximum current will flow through a diode in that phase-leg, For the drive system considered, this could result in a fault current of 30 p.u. The large transient current also charges the DC link capacitor to approximately 3 p.u. voltage if no method for control of the DC link voltage is utilised. Obviously, all devices would require rating for the maximum transient voltages and currents possible.

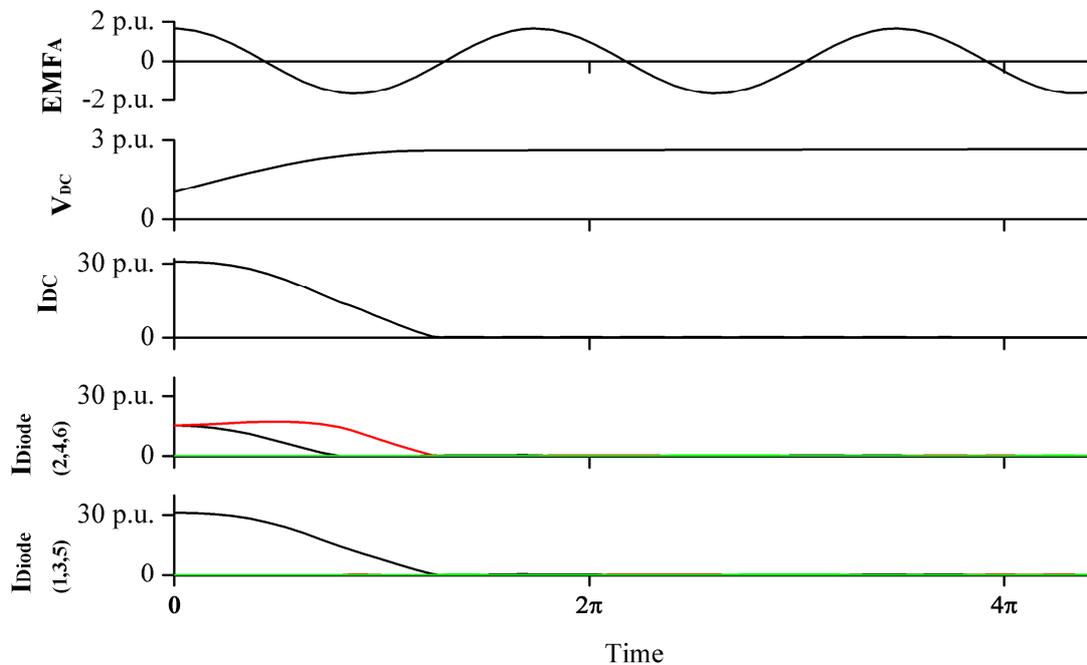


Fig. 1.11 VSI voltage and current profiles during a drive system control failure when at 4 p.u. base speed.

Diode	EMF _{ph-rms} @ base speed	1 p.u.
	EMF _{ph-rms} @ full speed	3.6 p.u.
	Conduction current (max)	31 p.u.
Capacitor	Current (max)	31 p.u.
Capacitor	Voltage rating	3 p.u.

Table 1.3 Predicted VSI voltages and currents during a drive system control failure when at 4.0 p.u. base speed.

By way of comparison a CSI based model was created to determine the required drive system voltage and current ratings due to CSI control failure. The voltage profiles, across each device in one phase-leg, are detailed in Figure 1.12 while the results are summarised in Table 1.4, The results illustrate that voltage rating of the power electronics need to be that of the peak line voltage of the machine EMF at full speed when operating at high speed, i.e. 4x base speed, flux-weakening operation via a CSI, i.e. the voltage rating increases by the flux-weakening factor.

Table 1.5 summaries drive system rating requirements when using flux weakening to operate at 4 times base speed with a representative PMSM. Although both VSI and CSI topologies require an increase of the inverter rating, the CSI topology only requires an increase (above normal operating conditions) in voltage rating that is essentially the same value as that of the VSI, whereas the VSI requires a very significant increase in the current handling capabilities of the fly-back diodes. The increase in voltage rating of both systems should be considered standard when operating a system using flux weakening, since the normal method for determining the voltage rating of the inverter components, (the nominal DC link voltage), is no longer the dominating factor, being replaced by the peak line EMF of the PMSM at the maximum operating speed. The VSI topology also requires the addition of a fail-safe (i.e. control independent) DC link protection circuit, rated appropriately for the peak overvoltage and maximum fault current.

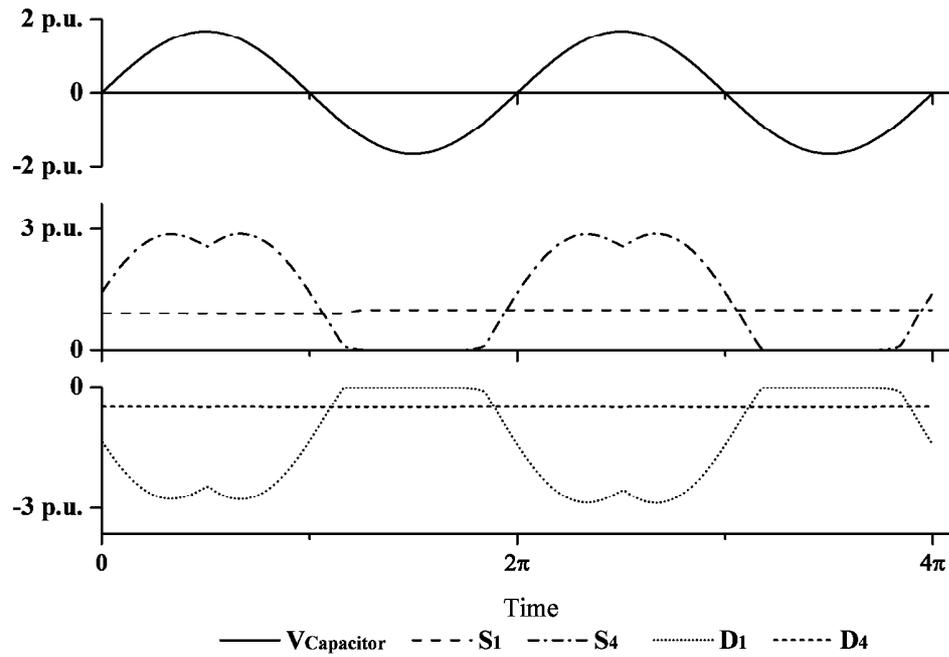


Fig. 1.12 Voltage profiles for CSI power electronic devices during a flux-weakening fault.

	EMF _{ph-rms} @ base speed	1 p.u.
	EMF _{ph-rms} @ full speed	3 p.u.
Switch	Forward blocking (max)	2.9 p.u.
Diode	Reverse blocking (max)	2.9 p.u.
Capacitor	Voltage rating	1.2 p.u.

Table 1.4 Predicted CSI voltages during during a drive system control failure when at 4.0 p.u. base speed.

The requirement of the VSI system to have such a large increase in current rating (31 p.u.) is likely to cause a significant increase in the mass and volume, but more importantly the cost of the VSI system. This factor coupled with the DC link protection circuit should give CSI systems a significant advantage when designing inverter systems to operate PMSMs with significant levels of flux-weakening.

VSI		CSI	
Switching device voltage rating	3 p.u.	Switching device voltage rating	3 p.u.
Diode current rating	31 p.u.	Switching device current rating	1 p.u.
DC link protection circuit voltage rating	3 p.u.	DC link protection circuit	NA
DC link protection circuit current rating	31 p.u.	Filter capacitor voltage rating	1.2 p.u.
DC link capacitor; current rating voltage rating	31 p.u. 3 p.u.	NA	
1 p.u. $V = EMF_{ph-rms}$ @ base speed.		1 p.u. $V = EMF_{ph-rms}$ @ base speed.	
1 p.u. $I = \text{Machine full load current}_{ph-rms}$.		1 p.u. $I = \text{Machine full load current}_{ph-rms}$.	

Table 1.5 Effects of flux-weakening faults on VSI and CSI systems.

There are many scenarios for the failure of a PM machine during flux weakening operation. These include, but are not limited to; failure of the gate drive circuits power supply; failure of the microprocessor system; interruption of the main power supply. Each scenario will result in the same outcome, an extremely large current for a short duration, which must be dealt with to prevent components from being damaged. As controlled PWM rectifiers are a common method of obtaining a DC link, it seems obvious that utilising the rectifier to transfer the power back to the AC source would suffice, however this is not without problems, not least the current capability of the rectifier which could be expected to deal with a current of 30 p.u. (for a VSI system). Also, the fault may have also disabled the PWM rectifier, or the AC source may also have been disabled and therefore cannot accept the power transfer. Therefore relying on a PWM rectifier is unlikely to be an acceptable solution for fault critical applications. The case is similar when the VSI supply is a common DC bus. For the fault current to be managed, without causing failure, another system must accept the fault current or the DC bus must be rated for the voltage rise on the bus. As with the PWM rectifier, it cannot be assumed that other systems linked to the DC supply have not also been disabled during the fault.

The simplest methods for mitigating the fault are likely to be based on systems that operate additional switches during fault conditions, either shorting the motor terminals together or

activating a crow-bar type circuit on the DC link. The PMSM terminal option would have the advantage of preventing the fault current from flowing in the VSI but requires more switches and safe guards to prevent its operation under normal conditions. Note, should an inadvertent operation of the protection circuit occur when the VSI is healthy, a short circuit trip of the inverter power devices should clear the fault. The crow-bar method would only require a single switch, although the DC link supply would require disconnecting during such a fault to ensure it is only the motor induced currents that need to be dealt with. Thus, the CSI could offer a potential, more robust drive system solution providing the component ratings meet the transient fault specification requirements.

1.5 CSI Benefits - Control of High Speed Low Inductance Machines

One consequence of designing a high performance, efficient high-speed (tens of thousands of rpm) PM machine is that, in general, they have a phase inductance that is lower than a machine with a more typical (up to 3krpm) speed range. The cause of this low inductance can be attributed to many factors [7], but generally arises from the design considerations for high speed. The low inductance machine will create control problems as the low impedance path that the inverter and motor present to the DC link capacitor will result in large current transitions but low average current levels if the PWM frequency is not high. Moreover, high PWM and current sensor sampling times make accurate control of the machine current difficult; the switching devices must also be rated sufficiently to operate reliably with the high peaks. Increasing the switching frequency could improve the performance of the machine, but the frequency will be limited by the device specifications and control system capabilities. This phenomenon will be exaggerated at low or zero speed, when the back-EMF is negligible. Poor control of phase current results in a greater phase current ripple, which will create torque ripples on the machine shaft, and induce additional machine losses [18].

A CSI system may address the current control issues by utilising the DC link inductance to limit the rate of change of the machine phase current, although this will obviously have an affect on the dynamic performance of the drive system. However, if the equivalent VSI results in large torque and current ripples, the dynamic performance of the VSI will also be compromised. A CSI system has previously been suggested for control of low inductance machines [7], although the utilisation of six-step switching at the output fundamental frequency, fails to benefit from the previously mentioned PWM advantages.

A case study was undertaken to investigate the issues associated with control of a high speed-low inductance PMSM in an aerospace application. The motor currents were simulated for the VSI topology to highlight the associated problems and to provide a benchmark for comparison with a CSI system.

A project investigating Large Electro-Mechanical Actuation Systems (LEMAS) resulted in the design of PMSM machine with significantly lower per unit resistance and inductance when compared to a typical 3000 rpm industrial PMSM. This resulted in significant effort being focused on controlling the machine current to reduce the ripple current therefore improving the torque ripple and high frequency related losses. The parameters of interest are listed in Table 1.6, the torque-speed requirement of the actuator demanded a high torque at low speed and a negligible torque at full speed, a typical traction drive characteristic. This resulted in a predicted phase current of 200A (1 p.u.) at 1krpm (0.05 p.u.), given that current ripple depends to a great extent on the average current, the high current demanded was likely to cause a significant and problematic amount of ripple.

Speed (max.)	20000 rpm
Inductance (Phase)	60 μ H
Resistance (Phase)	2.75 m Ω
EMF _{ph-rms}	0.038 V/rads ⁻¹
I _{ph} (max.)	200 A
V _{DC}	270 V
Switching frequency	20 kHz

Table 1.6 LEMAS machine and inverter parameters.

System models were created in SABER™ to estimate the magnitude of the phase current ripple for both the VSI and CSI topologies. To reduce implementation and simulation times, and reduce problems due to complete systems or full drive models failing to solve, the models were simulated for a period of a few switching cycles with DC voltage sources representing the PMSM back-EMF. Given that the switching period of the inverter is several orders of magnitude smaller than the PMSM period, the errors caused by approximating the PMSM as a DC source should be negligible. Figure 1.13 illustrates the VSI model, while Figure 1.14 illustrates the CSI model. The inverter specifications for each system are given in Table 1.7.

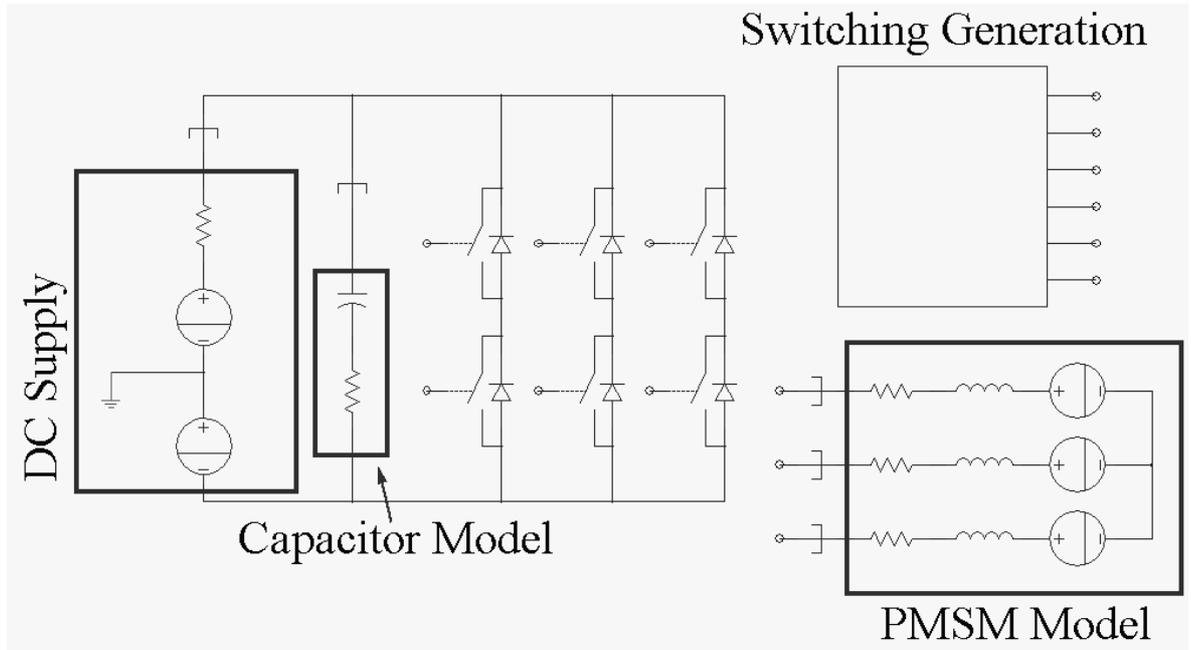


Fig. 1.13 Simplified model of the LEMAS system with a VSI.

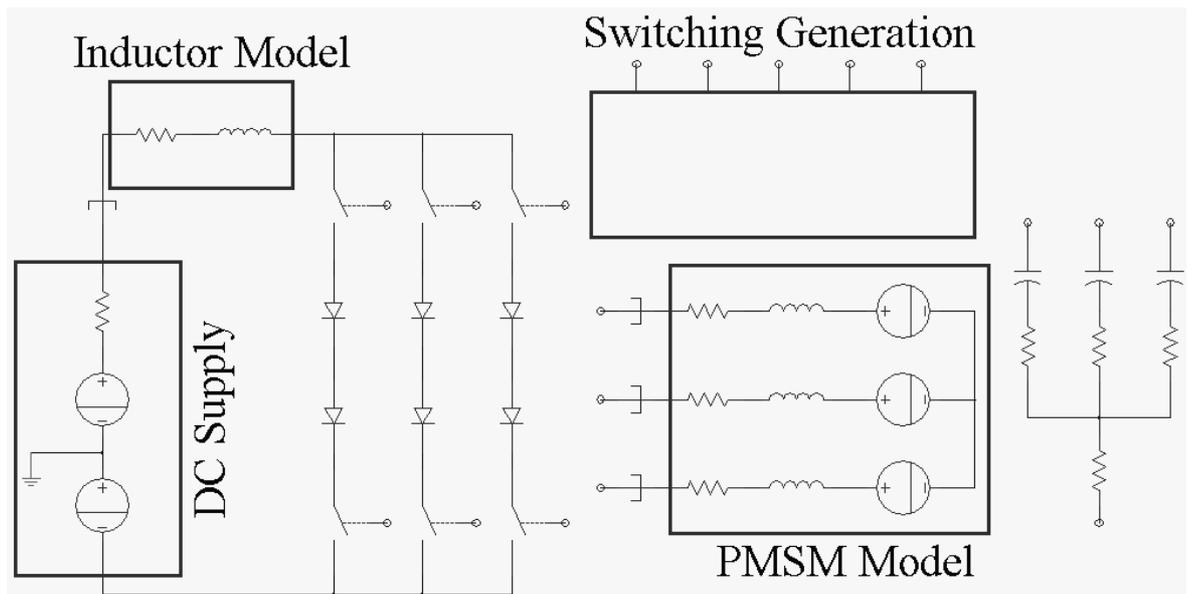


Fig. 1.14 Simplified model of the LEMAS system with a CSI.

VSI	
Switching frequency	20 kHz
Capacitor	1000 μ F
CSI	
Switching frequency	20 kHz
Inductor	300 mH
Filter capacitor	5 μ F

Table 1.7 Inverter model specifications for LEMAS machine study.

The phase and DC current waveforms for the VSI and CSI systems are illustrated in Figures 1.15 and 1.16 respectively. It can be seen that for the VSI system, attempting to achieve a 200A phase current results in a 470A peak to peak current ripple. Operating in this mode would obviously cause problems with machine control and device ratings, therefore either a different control method or topology would be required. It should be noted that in this simple model the PWM frequency has been reduced by the controller due to the current being significantly higher than the set point for an extended time, i.e. the ‘on’ signals are blocked due to the reference being higher than the set point.

In the CSI system, a ripple current is still present, however it has been reduced by almost a factor of 6 to 80A, this being a vast improvement on the VSI system. The scale of the reduction of the phase ripple current is only limited by the compromise that as the link inductor increases, the response time of the system to a step load, will increase. Using equation (3.30) it is possible to calculate the response time for a step change of 0.5 p.u. to 1 p.u. at 1krpm for the system with a 300mH inductor to be 135ms. Should the inductor be increased to 500mH, the response time increases to 250ms. It should be noted that these are the theoretical response times and therefore a slightly slower response time should be expected.

This study is by no means extensive and further research is required to develop greater design criteria for the control of high speed low inductance machines via CSIs. However, these results confirm other authors comments [7] and show a favourable attribute of the CSI system.

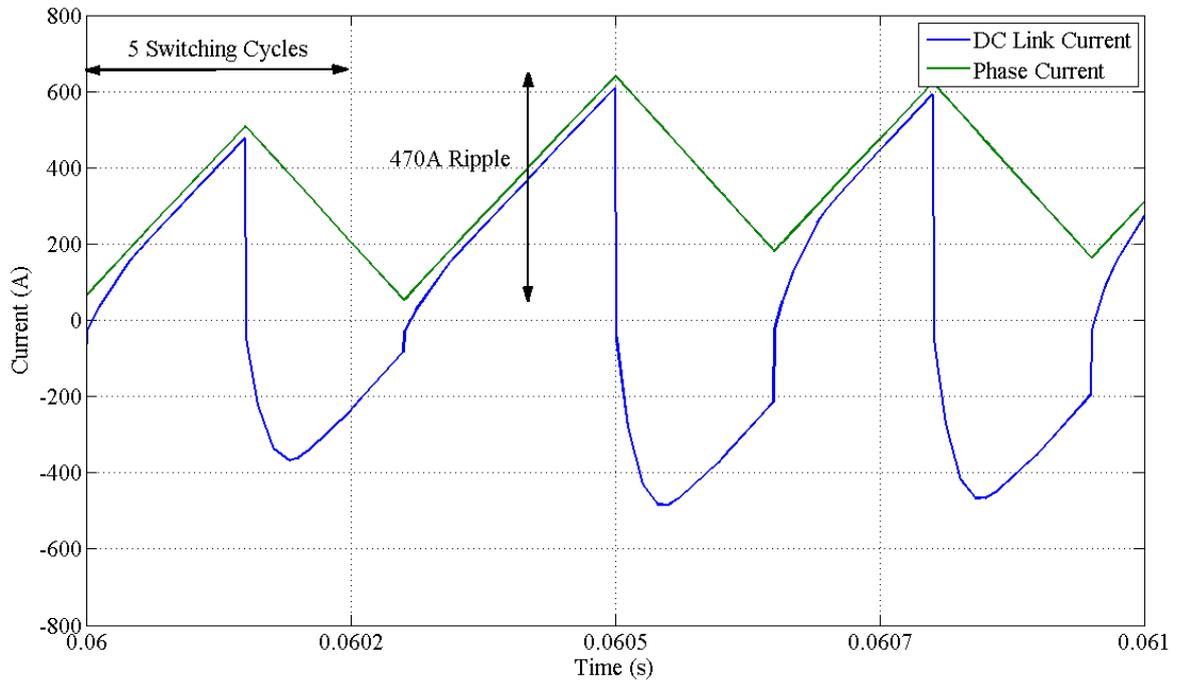


Fig. 1.15 Phase and DC current for the LEMAS machine with a VSI.

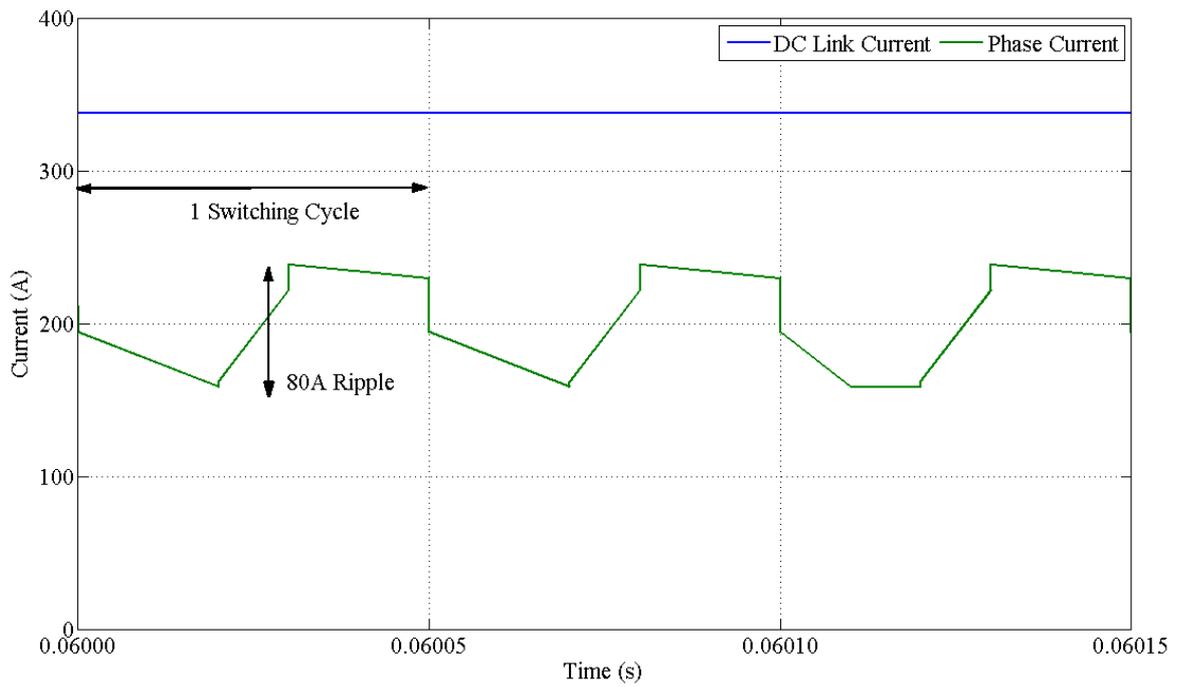


Fig. 1.16 Phase and DC current for the LEMAS machine with a CSI.

1.6 Electrolytic Capacitors

The large, usually electrolytic, capacitor at the heart of a VSI can potentially cause problems if the inverter is used in certain environments. The capacitors are generally packaged in a sealed aluminium can which, when subjected to low atmospheric air pressures (typical of flying at altitude), as is the case in aircraft, the containment can become distorted, usually causing catastrophic failure. Existing solutions involve sealing or maintaining the atmosphere around the capacitor at ground level ambient or removing it from the system completely.

The capacitor has also been identified in several papers [24,29] as being unreliable and the subject of investigation. It has also been known for several years, through the release of documentation by manufacturers, that electrolytic capacitors require measures to be taken if the devices are stored non-operational. ABB document “Capacitor Reforming Inspection Instruction” [39] details the preventative measures that must be employed to prevent damage to the DC link capacitors on ABB drive systems that have been left non-operational, i.e. disconnected, for more than a year. The capacitors require a limited current power supply to allow the capacitor electrolyte to reform without breaking down and damaging the capacitor catastrophically. Research papers into the exact cause of the problem have so far not been found, however, several internet resources, have stated that the problem is associated with the oxide layer of the capacitor degrading when a electric field is absent from the capacitor for a substantial period of time, though these sources are not traceable.

The CSI topology does not have an electrolytic capacitor on the DC link, although practical implementations of CSI drives utilise ceramic filter capacitors on the output of the inverter to improve the quality of the waveforms and reduce motor harmonics [30]. The use of filter capacitors on VSI systems has been suggested, if not already implemented, to improve VSI performance [31] therefore inclusion of filter capacitors would not necessarily be an added complication of the CSI system over the VSI system.

1.7 Boost Capability and Ripple Current

A typical fuel cell stack voltage is in the region of 200V [29], however, typical electricity supplies and machine phase voltages far exceed this. For VSI systems the DC link voltage must exceed the phase-to-phase voltage to allow the full rated voltage to be applied. The CSI however, through the inductor in the DC link, can act as a limited boost converter. This could allow the fuel cell stack to be connected directly to the CSI without the added complexity and expense of an additional boost converter (BC).

Research has been carried out in this area, by Rivas & Rufer [29] and Mohr et al [38], with differing results. Both investigations focus on the losses within the semiconductor components in a VSI+BC and a CSI system. Mohr et al [38] compare the typical systems for connecting a fuel cell stack to AC mains, each system is designed using commercially available components and the losses in each system are calculated. Although the results show the VSI+BC system to have fewer losses, several important points are noted. The large output voltage range of the fuel cell system requires substantially more installed semiconductor power rating in the CSI system, as the low output voltage creates large currents in the devices. This can only be solved by careful calculation of the lower limit of the input. In the future, reverse blocking (RB) IGBTs should reduce conduction losses in the CSI due to removal of series diodes, this should bring substantial benefits to the CSI topology.

Rivas & Rufer [29] compare the VSI+BC and CSI topologies for fuel cell stack-electricity network connections. They conclude that the losses in both topologies are very similar, but slightly in the favour of the CSI system. However, again, it is noted that RB-IGBTs should improve performance once available. In both research papers no account is made of the losses within the passive components required for each system, an inductor for the CSI and an inductor plus capacitor for the VSI+BC.

Fuel cell operation is a chemical reaction and as such the current available from the cell depends on the availability of the reactants in sufficient quantity. Gemmen [41] investigated the effects of ripple currents on fuel cell stack operation and the possible implications on cell life longevity and reliability due to ripple currents generating low reactant levels in the fuel cell. Gemmen concludes that ripple frequencies should be above 120Hz or ripple magnitudes below 4% to ensure negligible impact on the fuel cell.

CSIs show promise for fuel cell interface, but further research is required on this aspect.

1.8 Summary

This thesis investigates feasibility of utilising Current Source Inverters (CSIs) to control permanent magnet synchronous machines in automotive and aerospace actuation systems. CSIs, switching at the fundamental frequency, were used in some of the first semiconductor based, electronic variable speed drive systems that utilised the simple, low maintenance AC induction motor. However, the rapid progress of semiconductors and discovery of Pulse Width Modulation (PWM) techniques soon resulted in the Voltage Source Inverter (VSI) replacing the CSI in all but the highest power applications. Modern power electronics and (micro-processor based) control systems mean that the advantages of VSI systems may no longer be significant and combined with the unique environmental conditions that automotive and aerospace applications present, could allow the CSI to offer advantages over VSIs in these application.

CHAPTER 2

VSI AND CSI SWITCHING AND CONTROL SCHEMES

2.1 Introduction

In this Chapter background textbook theory on rotating electromagnetic machine control and associated power electronic switching will be presented for VSIs, with reference to [42,43,44,45] unless otherwise stated, since this theory forms the basis of progression to CSI schemes. The VSI schemes will then be modified and adapted for application to the CSI. The CSI switching and pre-charge algorithms are presented and discussed and mapping of the VSI to CSI logic presented for ease of comparison

2.2 Variable Speed Drive Systems

Servo performance from variable speed drive systems refer to drives with position feedback and control that deliver highly responsive, dynamic torque, speed and position control. They are often implemented on actuation systems for aircraft and robotics, producing fast, accurate movements of the controlled surface or arm. To achieve servo performance in an AC machine advanced control techniques are required [45], such as vector control [44]. For a PMSM with sinusoidal back EMF, sinusoidal currents are required to produce a constant, ripple free, torque [46]. Failure to provide the sinusoidal currents results in noise and a lower efficiency, as well as other undesirable effects, in addition to the torque ripple.

The control of brushed DC motors is the simplest to implement, with 2 coils maintained orthogonally to each other (via the commutator) producing torque, it can be represented as in Figure 2.1. The axes are referred to as the direct (d-axis) and the quadrature (q-axis),

with the d-axis, by convention, representing the flux from the field coil. Therefore I_q is the armature current and I_d is the field current. Torque, being proportional to the armature current for a given field excitation, is also on the q-axis. Flux-weakening (also known as field-weakening) a brushed DC machine, by reducing the field current, will cause an increase in speed at the expense of torque to give a constant mechanical power output [11].

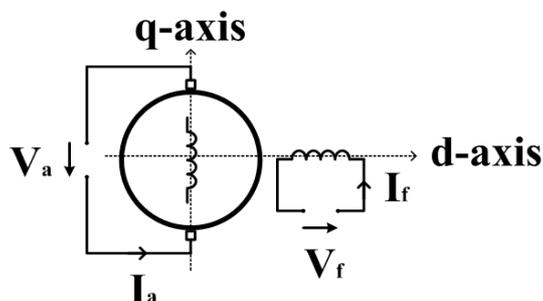


Fig. 2.1 Brushed DC machine coil representation [42].

Control of an AC machine using a system similar to that of a brushed DC machine is desirable due to the simplicity and correlation between q- and d-axes with torque and field control respectively. A three phase machine is represented in Figure 2.2, having three stator coils, each with its own flux equation and resulting in three electrical dynamic equation. It should be noted that in a synchronous machine there will be a rotating coil (or permanent magnet) on the rotor, adding to the complexity. A mathematical transform allowing a change from the three coil system to a two coil system is equivalent if, at any time, the resulting field is the same.

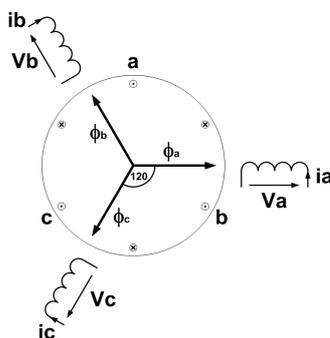


Fig. 2.2 Three phase machine, coil representation [42].

If at time instant t , the flux resulting from the three phase coils, $\phi_a(t), \phi_b(t), \phi_c(t)$, can be transformed to a two axis, $\alpha \beta$, orthogonal system, where α is conventionally aligned to phase a. The resulting two axis flux value will be [42]:

$$\phi_\alpha = \phi_a + \phi_b \cos(120) + \phi_c \cos(-120) = \phi_a - \frac{1}{2} \phi_b - \frac{1}{2} \phi_c \quad (2.1)$$

$$\phi_\beta = \phi_b \cos(30) - \phi_c \cos(30) = \frac{\sqrt{3}}{2} \phi_b - \frac{\sqrt{3}}{2} \phi_c \quad (2.2)$$

This can be represented as in Figure 2.3.

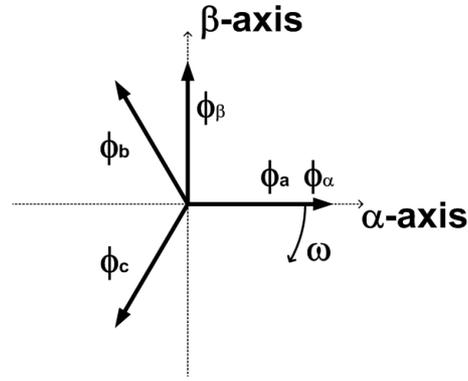


Fig. 2.3 Two coil representation of a three coil system [42].

Flux is the product of the current and the number of turns, where there is an equivalent number of turns for the two coil system, therefore [42]:

$$N_\alpha i_\alpha = N_a i_a - \frac{1}{2} N_b i_b - \frac{1}{2} N_c i_c \quad (2.3)$$

$$N_\beta i_\beta = \frac{\sqrt{3}}{2} N_b i_b - \frac{\sqrt{3}}{2} N_c i_c \quad (2.4)$$

For a balanced three phase system $N_a = N_b = N_c = N_3$ and a balanced two phase system [42]:

$$N_\alpha = N_\beta = N_2 \quad (2.5)$$

Therefore [42]:

$$N_2 i_\alpha = N_3 \left(i_a - \frac{1}{2} i_b - \frac{1}{2} i_c \right) \quad (2.6)$$

$$N_2 i_\beta = N_3 \left(\frac{\sqrt{3}}{2} i_b - \frac{\sqrt{3}}{2} i_c \right) \quad (2.7)$$

This allows the creation of a matrix form equation for the transformation from a three phase system to a two phase system, a transform back to the three coil system may be required, this, however, would not be possible, as the matrix dimensions would not allow transposition. To allow this an extra variable, γ , is required and three constants, k . γ is usually defined as the zero-sequence. Equation (2.8) [42] details the three to two coil transform equation, known as the Clarke Transform and is also applicable to voltages.

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_\gamma \end{bmatrix} = \begin{pmatrix} N_3 \\ N_2 \\ k \end{pmatrix} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ k & k & k \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = C \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2.8)$$

The values N_2 and k are unknown, this can be solved by using the ‘invariance of power’, i.e. the power input in the three coil model is the same as the power input to the two coil model.

Therefore [42]:

$$P_{abc} = [V_{abc}][i_{abc}]^T \quad (2.9)$$

and [42],

$$P_{\alpha\beta} = [V_\beta][i_{\alpha\beta}]^T = C[V_{abc}]C^T[i_{abc}]^T \quad (2.10)$$

This condition will be fulfilled if $\left(\frac{N_3}{N_2}\right) = \sqrt{\frac{2}{3}}$ and $k = \frac{1}{\sqrt{2}}$, giving Equation (2.11) [42];

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_\gamma \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2.11)$$

The inverse transform is detailed in Equation (2.12) [42]. Now the inverse matrix form equation is known, the zero sequence component and the additional constants are normally not required and often are not shown in the Clarke and Inverse Clarke transforms.

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_\gamma \end{bmatrix} \quad (2.12)$$

The two coil $\alpha\beta$ system still rotates at the frequency ω , not lending itself to simple control methods, to rectify this a second transform involving a time function is needed, using the flux values again, the direct and quadrature flux can be calculated using [42]:

$$\phi_d = \phi_\alpha \cos \theta_r + \phi_\beta \sin \theta_r \quad (2.13)$$

$$\phi_q = -\phi_\alpha \sin \theta_r + \phi_\beta \cos \theta_r \quad (2.14)$$

This can be represented as in Figure 2.4.

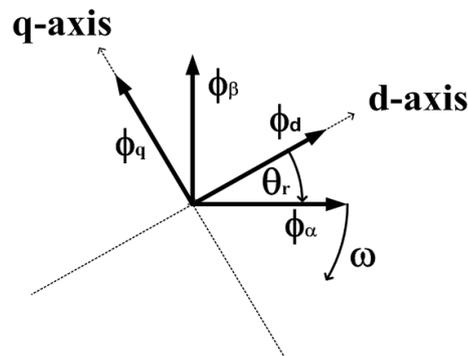


Fig. 2.4 Two coil rotary reference system [42].

Again, a component, γ , is required to determine the reverse transformation. The matrix from Equation is detailed in Equation (2.15) [42], and the inverse detailed in Equation (2.16) [42]. The γ component and associated constants, again, are often not included for simplicity.

$$\begin{bmatrix} i_d \\ i_q \\ i_\gamma \end{bmatrix} = \begin{bmatrix} \cos \theta_r & \sin \theta_r & 0 \\ -\sin \theta_r & \cos \theta_r & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_\gamma \end{bmatrix} \quad (2.15)$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_\gamma \end{bmatrix} = \begin{bmatrix} \cos \theta_r & -\sin \theta_r & 0 \\ \sin \theta_r & \cos \theta_r & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_\gamma \end{bmatrix} \quad (2.16)$$

2.3 Voltage Source Inverters

The power-electronic stage of the voltage source inverter, illustrated in Figure 2.5, consists of six semiconductor switches (S_1 to S_6), with gate-turn off control, and their associated freewheel diode, usually incorporated within the device package in modern devices. Gate drive and snubber circuitry is not shown. The six devices create three separate phase legs (a,b and c) within the inverter, the centre point of each leg being a connection point for the load being driven. The switch activation signals for S_1 to S_6 , can be applied either at the output frequency, for six-step operation, or using a high frequency pulse width modulation scheme.

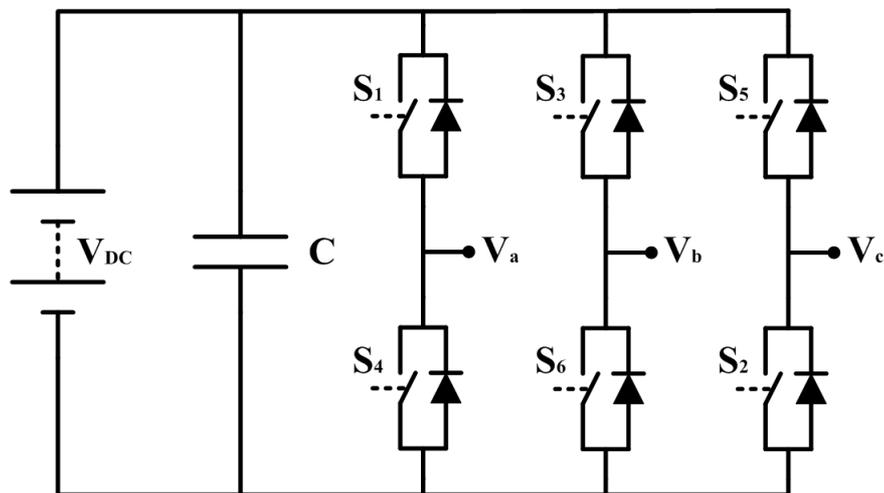


Fig. 2.5 Voltage source inverter topology.

2.3.1 Six-Step Switching

Six-step operation is switching at the frequency of the inverter output, i.e. each switch turns on and off once during the output period, 2π , and has an 'on' duration of π radians. Each phase leg is offset by $\pi/3$ radians creating six equal intervals (I to VI) during one output period. The switching order is the number order of the switches and results in there always being one switch from each leg conducting, except for a small time period to allow the conducting switch to turn off before the switch from the same leg is turned on. The delay period is known as the blanking time and is required to prevent both switches within a leg conducting simultaneously, shorting the DC link and causing a shoot-through fault, where current rises rapidly and is likely to cause device(s) with the inverter to fail. Figure 2.6 details the control signals for each switch (excluding blanking time) along with the resulting output voltage, V_{an} , referenced to the load star point.

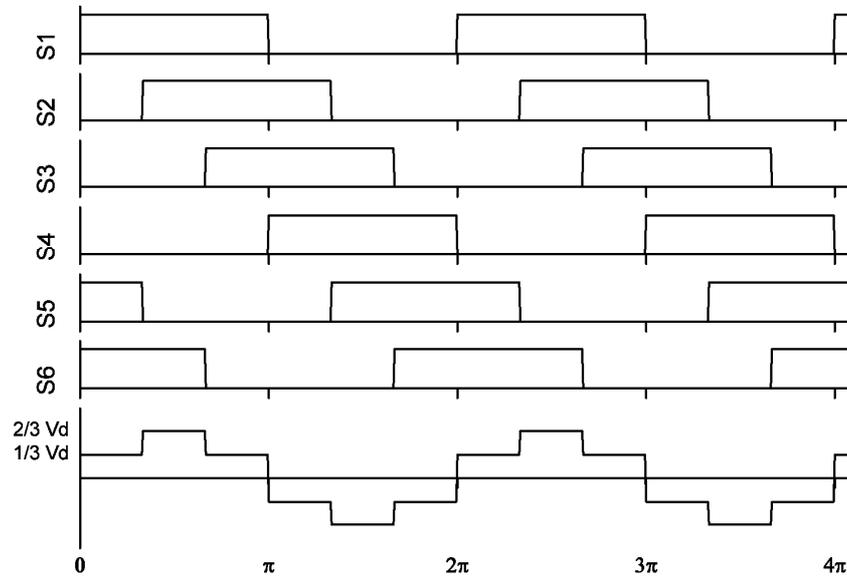


Fig. 2.6 VSI six-step switching.

Frequency control is achieved by the controlling time of one period, however, induction machines and PMSMs also require the voltage to be controlled with the frequency in an almost linear manner. Voltage control in a six-step system is only achievable by varying the DC link voltage unless multiple inverters are used. Control of the DC link voltage depends on the source of the DC, this can be achieved with a DC chopper when used with a DC source (such as a battery) or an uncontrolled rectifier with an AC source, or by using a controlled rectifier from an AC source. Controlling the DC link voltage is not without its drawbacks, a controlled DC link requires a separate DC link for each inverter, preventing the cost/size/efficiency gains associated with having a common DC link, varying the DC voltage can have one or more of the following consequences; low power factor on the AC supply; low frequency harmonics on the inverter input voltage increasing motor losses and creating low speed torque pulsations; and additional power stages, i.e. DC choppers, reducing the efficiency while increasing the cost and complexity of the system.

2.3.2 PWM Switching

A solution to the previously described problems, when controlling the DC link voltage, is to use PWM, turning each switch within the inverter on and off multiple (usually thousands) of times within one period, effectively reducing the voltage at the output terminal while maintaining a fixed DC link voltage. The system will now be free mostly from all the problems that are present in variable DC link voltage systems.

Multiple PWM schemes exist, with differences being designed to optimize the switching efficiency and/or reduce the harmonic content of the output voltage and so on. The basic principles of PWM are the same in all schemes; sinusoidal PWM is achievable using analogue techniques and is simple to demonstrate while most advanced techniques require microprocessor implementation. Sinusoidal PWM compares a triangular carrier wave against a reference sine-wave (per phase), i.e. the sine-wave reference represents the frequency and magnitude desired to be output from the inverter. Figure 2.7 details a sinusoidal reference wave with magnitude A and a triangular carrier wave with magnitude A_m , the ratio of the two amplitudes is known as the modulation index, as in Equation (2.17).

$$m = \frac{A}{A_m} \quad (2.17)$$

For phase A (S_1 and S_4) when $V_{ref} > V_t$, S_1 receives a control signal and turns on, S_4 is the opposite of S_1 (except during the blanking time) and receives a control signal when $V_{ref} < V_t$. If $m > 1$ then the output of the comparator is over-modulated, i.e. the number of pulses per period reduces, eventually, beyond a certain value of m , six-step operation is reached. During normal operation ($m < 1$), the output waveform contains harmonics which are odd multiples of the carrier frequency, f_c , and harmonics in the sidebands around multiples of f_c . If we define the ratio of reference to carrier, p , shown in Equation (2.18)

$$p = \frac{f_c}{f} \quad (2.18)$$

When p is large, the frequency of the harmonics are large compared to the fundamental frequency of the output, and the normal leakage inductance of the motor will filter out the harmonics so the current appears sinusoidal. To minimise harmonics p is normally chosen to be an integer that is an odd multiple of 3, such as 9 as in Figure 2.7. This condition results in the phase relationship of V_{ref} and V_t being fixed and the pulse pattern repeated every cycle, for a fixed V_{ref} , and the inverter output harmonics will be reduced to odd multiples of f_c and the sidebands.

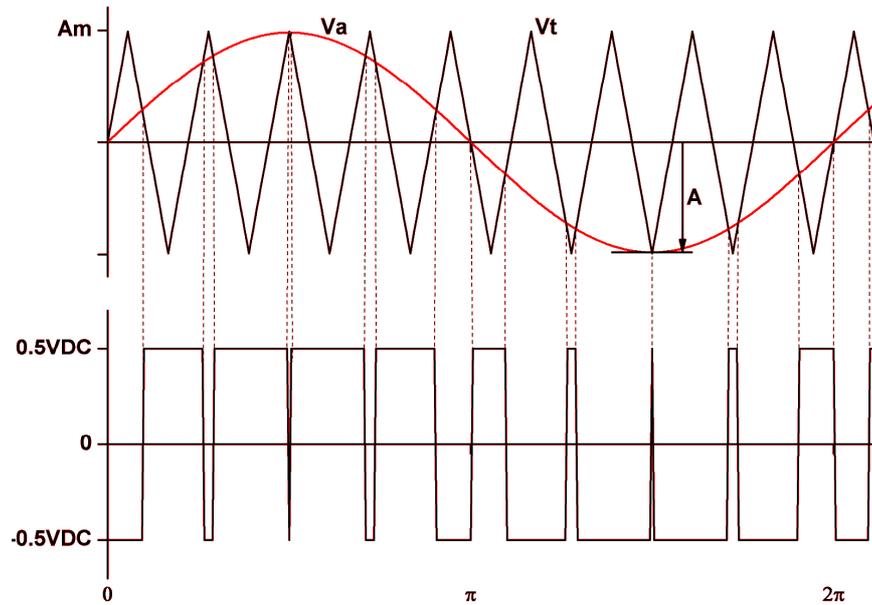


Fig. 2.7 VSI PWM modulation waveforms.

2.3.3 Space Vector PWM Switching

Space Vector PWM (SV-PWM) is an advanced modulation technique that is normally implemented using microprocessors, it is based on the eight possible switch combinations of a VSI. Of the combinations, six (SV_1 to SV_6) are ‘on’ (active) states and two (SV_0 and SV_7) are ‘off’ (zero) states, with zero states being all the top or bottom switches conducting, shorting the connected load. The eight states can be represented as stationary vectors on the d-q plane, as shown in Figure 2.8. An output reference vector can be formed by the addition of two or more vectors where the amplitude of each vector can be controlled by the time over which it is applied. For example, to create a reference vector, \bar{V}_0 , located between SV_1 and SV_2 , Equation (2.19) can be used. Assuming T is the switching period;

$$\bar{V}_0 = V_0 \angle \theta_0 = T_1 SV_1 + T_2 SV_2 \quad \text{where } 0 \leq T_1 + T_2 \leq \frac{T}{2} \quad (2.19)$$

The vectors are applied over half the switching period and then repeated over the second half of the switching period with the reverse operation, creating symmetrical switching. Should the total time for which the two vectors are applied not equal half the switching period, then one of the zero vectors is applied. In practice, at the start of each switching period, the inverter is outputting one of the zero vectors, switches to the first active vector, followed by the second and returns to a zero vector, the sequence is then reversed exactly.

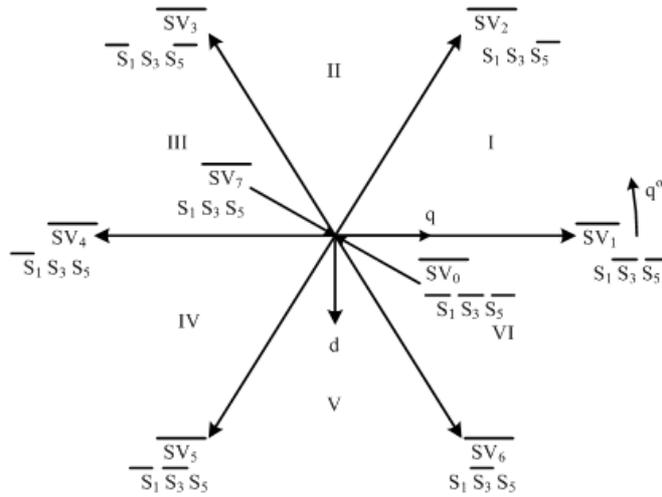


Fig. 2.8 VSI space vector diagram.

The particular zero vector that is used in the sequence will depend on the modulation scheme (optimization) in use but is generally chosen to be the one that requires the minimum switch transitions to change from the current active vector to a zero vector. Figure 2.9 details the switching sequence for vector \overline{V}_0 . If T_0 , the zero vector duration, is chosen to split equally between the two zero vectors the switch sequence becomes the same as that of the sinusoidal PWM with a triangular carrier reference. The maximum output voltage is $V_{0,max} = \frac{2}{\sqrt{3}}V_{DC}$ or $1.15V_{DC}$, a significant increase over six-step switching.

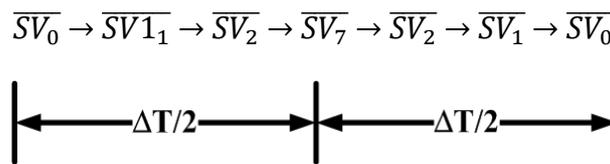


Fig. 2.9 SV-PWM switching sequence.

Much work on harmonic elimination has been performed [44] [47] and optimum switching patterns resulting in a variety of switching schemes based on the scheme just covered. Ultimately the choice of SV-PWM scheme will be decided by the running costs (motor and inverter efficiency and/or life expectancy) versus implementation cost, i.e. available control hardware.

2.4 Current Source Inverters

The power-electronic stage of the current source inverter, detailed in Figure 2.10, consists of six semiconductor switches (S_1 to S_6), with gate-turn off control, and six diodes. Gate drive and snubber circuitry is not shown. The six device pairs create three separate phase legs (a,b and c) within the inverter, the centre point of each leg being a connection point for the load being driven. In practical systems, the constant current source is replaced by a DC voltage supply and a DC link inductor, as detailed in Figure 2.11. Switch activation signals for S_1 to S_6 can be applied either at the output frequency, for six-step operation, or using a high frequency pulse width modulation scheme.

2.4.1 Six-Step Switching

Six-step operation of a CSI is similar to that in a VSI system with each switch operating once during the output period, 2π , except with an 'on' duration of $\frac{2\pi}{3}$ radians. Each phase leg is offset by $\pi/3$ radians, again, creating six equal intervals (I to VI) during one output period. The switching order is the number order of the switches and results in there always being one switch from top row and one switch from the bottom row conducting at all times. Figure 2.12 details the control signals for each switch along with the resulting output voltage, V_{an} , for a static load referenced to the load star point. Without filter capacitors, the output voltage, V_{an} , will have voltage spikes at the switch transitions. The filter capacitors allow gradual transfer of the current between phases. Frequency control is again via the control of the time for one period, to maintain a constant I_{DC} from a DC voltage supply a controlled rectifier or DC chopper is used to control the voltage, and hence current, in the inductor. Six-step switching in a CSI results in the same low frequency harmonics as the six-step switched VSI.

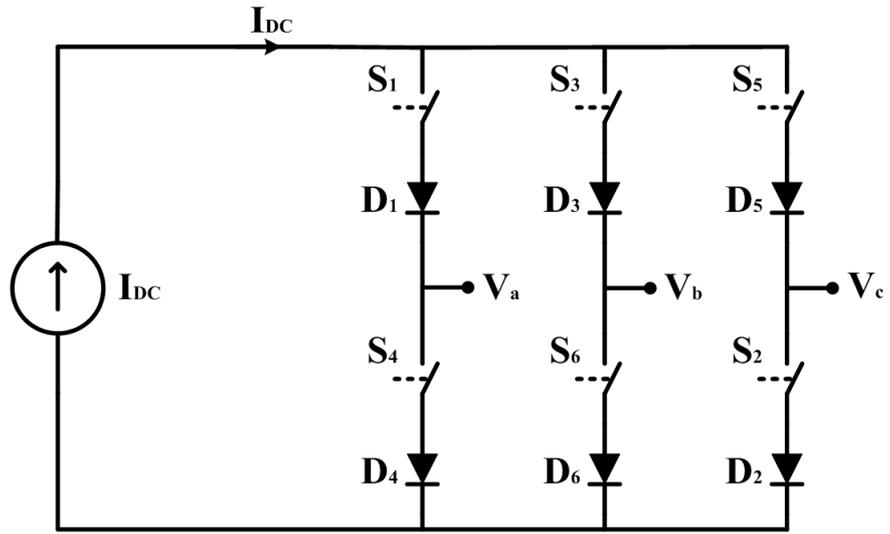


Fig. 2.10 Current source inverter topology.

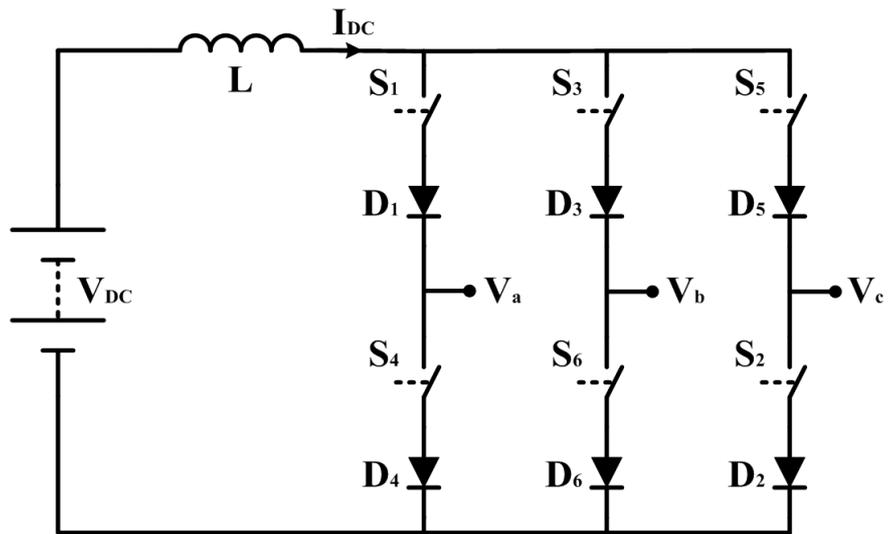


Fig. 2.11 Practical implementation of a current source inverter.

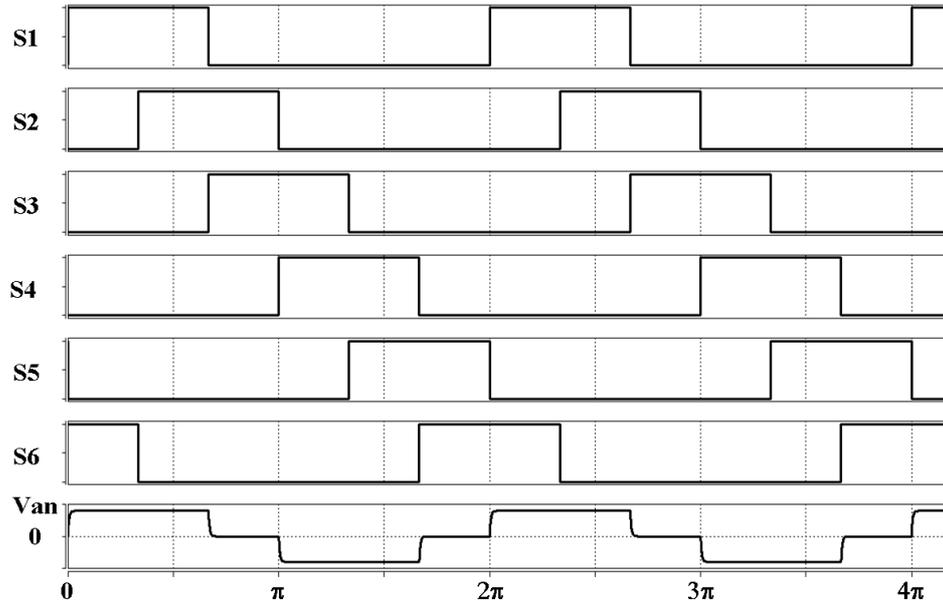


Fig. 2.12 CSI six-step switching.

2.4.2 PWM Switching

To eliminate the low frequency harmonics a PWM scheme is required, by modulating the first and last 60° (of a half cycle) the low frequency harmonics can be reduce to such a level that they can be considered to have been eliminated. The number of harmonics eliminated is directly related to the number of pulses per half cycle, for example, three pulses results in the lowest harmonic being eliminated, while seven pulses results in the elimination of the lowest three harmonics. Implementation is usually achieved by a trapezoid-triangle comparison, detailed Figure 2.13, resulting in PWM operation for electrical angles 0 to $\frac{\pi}{3}$ and $\frac{2\pi}{3}$ to π (with a continuous high for $\frac{\pi}{3}$ to $\frac{2\pi}{3}$) for S1, S4 repeats this pattern for π to 2π . Each phase leg is offset by $\frac{2\pi}{3}$, note; this results in the switching no longer being the 120° switching of the six-step CSI and the rule that there are always (and only) two simultaneously active switches is no longer true.

The modulation index is again calculated as the ratio of amplitude of the reference wave, A , and the amplitude of the carrier wave, A_m , as in Equation (2.6). The optimum modulation index has found to be $m = 0.82$ [9]. Controlling the magnitude of the output current still requires a controlled current source as the supply to the inverter.

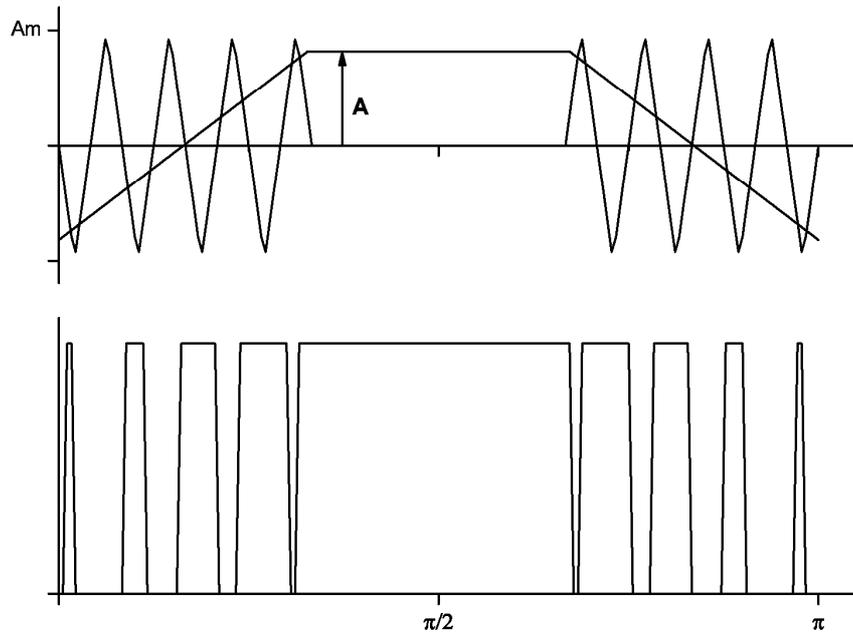


Fig. 2.13 CSI PWM switching.

2.4.3 Space Vector PWM Switching

Current source space vector pulse width modulation (CS-SV-PWM), like SV-PWM, is based upon the possible switch combinations, for a CSI there are also six active states (SC_1 to SC_6) but three zero states (SC_7 to SC_9), although in this case, the zero states are the activation of both switches within one leg, this is to ensure a continuous current through the DC link inductor. As before they can be represented as stationary vectors on the d-q plane, as shown in figure 2.14. The CSI space vector mapping shows a 30° phase lag on the vectors, this is due to vector SC_1 results in the maximum of the line-to-line voltage V_{ac} , which lags V_a by 30° .

The 30° phase shift can be implemented in the control system when determining the output vector. This allows direct mapping of the active vectors with those from the VSI, i.e. $SC_1 = SV_1$, etc. The mapping of the zero vectors, assuming that minimum switch transition is to be implemented, is based upon the current interval that the reference vector is currently located, as each interval has a common switch in the two active vectors that mark the boundaries. i.e. in interval I, S2 is common to both active vectors so the zero vector for the minimum switch transitions will be SC_9 . Obviously when the reference vector transitions an interval boundary, the zero vector at the start of the PWM period will be incorrect, this is however unavoidable and will only occur on six occasions per period. Using a truth table, the individual switch mappings required to convert SV-PWM to CS-SV-PWM can

be determined, allowing standard controllers to implement CS-SV-PWM with a small modification of the output control signals. Table 2.1 details the control signal mapping for VSI to CSI, Table 2.2 details the Null vector mapping. Provided signals representing the current interval can be output by the controller implementing the SV-PWM, it is possible to implement CSI-SV-PWM through discrete logic circuits or programmable logic devices.

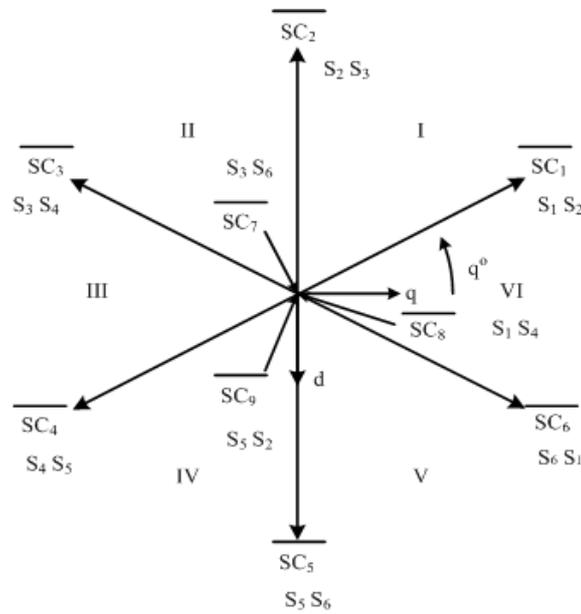


Fig. 2.14 CSI space vector diagram.

Switch	Active VSI Vectors	VSI Active Switches	VSI Logic	VSI Logic (without inversion)
S ₁	SV1 + SV6	$\overline{135} + \overline{135}$	$1 \cdot \overline{3}$	1 · 6
S ₂	SV1 + SV2	$\overline{135} + \overline{135}$	$1 \cdot \overline{5}$	1 · 2
S ₃	SV2 + SV3	$135 + \overline{135}$	$3 \cdot \overline{5}$	2 · 3
S ₄	SV3 + SV4	$\overline{135} + \overline{135}$	$\overline{1} \cdot 3$	3 · 4
S ₅	SV4 + SV5	$\overline{135} + \overline{135}$	$\overline{1} \cdot 5$	4 · 5
S ₆	SV5 + SV6	$\overline{135} + \overline{135}$	$\overline{3} \cdot 5$	5 · 6

Table 2.1 VSI to CSI control signal mapping.

Interval	Active CSI Vectors	Null Vector	Active switches
I	SC1 + SC2	SC9	2 · 5
II	SC2 + SC3	SC7	3 · 6
III	SC3 + SC4	SC8	1 · 4
IV	SC4 + SC5	SC9	2 · 5
V	SC5 + SC6	SC7	3 · 6
VI	SC6 + SC1	SC8	1 · 4

Table 2.2 CSI null vector mapping.

2.4.4 Modified Space Vector PWM Switching

CSI-SV-PWM with DC link shorting during the null vector has been identified as reducing the harmonic benefits that make PWM schemes attractive [48] and increasing the complexity of the current control scheme by requiring DC link current control system [49]. Referring to Figure 2.11, it is obvious that, unless a current controlled source is used, during the null vector period the DC link current will rise, unless the inductance of the DC link inductor is of a sufficient value. Such a DC link inductor would have the effect of severely reducing the dynamic response of the system as there would be no method to increase the DC link current sufficiently quickly to respond to a step change on the load. To overcome this problem it has been suggested [21,49] to modify the CSI topology and switching by adding an additional switch and series diode, allowing the controlled free-wheeling of the DC link inductor. This results in the inductor current to being maintained while any of the possible switch combination could be implemented, including, all inverter switches off. Control of the load where the current is low can now be achieved by increasing the time of the null vector as is in the case for the VSI, this solution also allows the full advantages of PWM to be realised by utilising modes where all switches are off [48]. Figure 2.15 details the modified CSI (MCSI) topology, the control signal for the free-wheeling circuit is determined from the null vector of the SV-PWM signals, where activation of either of the null vectors, all top or all bottom switches on, results in the free-wheeling circuit being activated. Table 2.3 details the control signal mapping for modified CSI-SV-PWM (MCSI-SV-PWM).

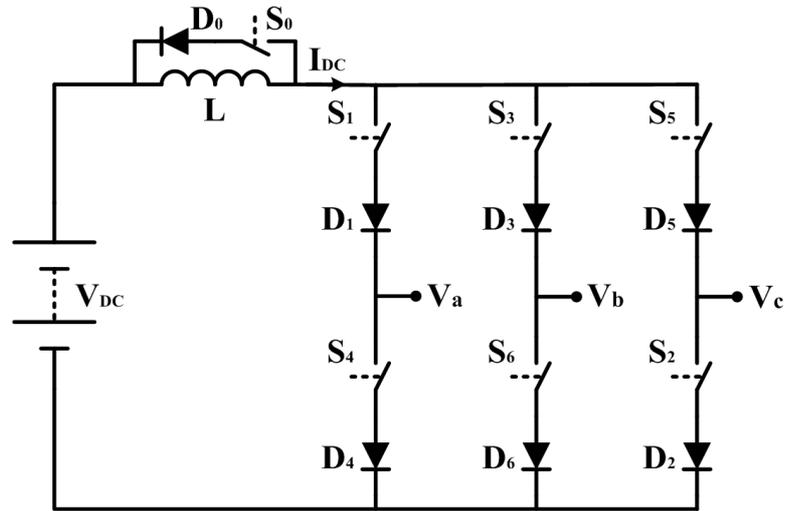


Fig. 2.15 Modified CSI topology.

Switch	Active VSI Vectors	VSI Active Switches	VSI Logic	VSI Logic (without inversion)
S_1	$SV1 + SV6$	$\bar{1}\bar{3}\bar{5} + \bar{1}3\bar{5}$	$1 \cdot \bar{3}$	$1 \cdot 6$
S_2	$SV1 + SV2$	$\bar{1}\bar{3}\bar{5} + 13\bar{5}$	$1 \cdot \bar{5}$	$1 \cdot 2$
S_3	$SV2 + SV3$	$13\bar{5} + \bar{1}3\bar{5}$	$3 \cdot \bar{5}$	$2 \cdot 3$
S_4	$SV3 + SV4$	$\bar{1}\bar{3}\bar{5} + \bar{1}35$	$\bar{1} \cdot 3$	$3 \cdot 4$
S_5	$SV4 + SV5$	$\bar{1}35 + \bar{1}\bar{3}5$	$\bar{1} \cdot 5$	$4 \cdot 5$
S_6	$SV5 + SV6$	$\bar{1}\bar{3}5 + 1\bar{3}5$	$\bar{3} \cdot 5$	$5 \cdot 6$
S_0	$SV0 + SV7$	$135 + \bar{1}\bar{3}\bar{5}$	-	$(1 \cdot 3 \cdot 5) + (2 \cdot 4 \cdot 6)$

Table 2.3 Modified CSI control signal mapping.

2.5 Other Considerations

2.5.1 Digital Implementation

Digital implementation of space vector switching can be accomplished using microprocessor based systems interfaced with the appropriate analogue to digital conversion (ADC) and PWM systems. Measured phase currents, a minimum of two, and rotor position are used to calculate I_d and I_q , reference currents are generated via proportional plus integral (PI) controllers based on the control methodology in use, such as current control, speed control or position control. The reference I_d and I_q values are used to digitally plot (i.e. calculate in the microprocessor) the desired output vector for the next

PWM period, the vector is used to determine the active switches and the switching times, T_0 , T_1 and T_2 , which can then be applied to the PWM hardware during the next PWM period. Using alternative measurement systems and calculations it is possible to implement digital control with speed or position feedback, however, the complexity and accuracy of the system depends on the machine being controlled, i.e. synchronous or asynchronous.

2.5.2 Start-up and Shutdown

When energising a VSD system, consideration of the possible inrush current is required to ensure correct and safe start up of the system. The large, usually electrolytic, capacitor present on the DC link will begin charging as soon as a DC voltage is applied. If the supply is not controlled or current limited the low impedance of the capacitor will result in a current surge during the initial start-up. This surge will be severe, possibly damaging other components. The susceptible components include the input rectifier, in an AC:DC:AC system, the capacitor itself and protection devices on the supply side of the VSD. Operation of supply fuses, or circuit breakers, to interrupt inrush currents are nuisance trips that should be avoided, since the owner/operator of the drive system will tend to incorporate higher rated and hence less effective protection devices. The inrush current may also cause problems for other equipment on the same electrical supply, for example voltage perturbations, such as on aircraft, where strict rules apply to the electrical power system and that connecting equipment.

The rectifier, on an AC:DC:AC system, if uncontrolled or without a suitable ramp up method, could be subjected to an over-current that causes permanent damage to the device, resulting in instantaneous failure or producing a cumulative effect that causes the failure rate of the device to increase substantially. The effects of the current surge on the capacitor are also likely to reduce the life expectancy of the component, manufacturers supply extensive documentation regarding lifetime calculation based on current ripple, temperature etc. A large inrush during energisation is likely to cause both these effects and could even result in the component rupturing in a catastrophic failure, especially when the device is near the end of its working life.

Should the VSD be of the DC:AC type, the ability to control the current using a controlled rectifier is obviously not available, therefore additional components will be required to limit the inrush current. The additional components create a resistive charging circuit [50] on the DC link, enabled at energisation, it limits the current to safe levels before being

disabled. The charging circuit utilises a current limiting resistor and a shorting contactor, the contactor being energised after a sufficient amount of time has passed or voltage sensing circuits determine that the capacitor has charged sufficiently to prevent an inrush when the resistor is shorted. Which ever method is chosen for controlling the contactor, the effect of a supply voltage dip should be considered [51] to ensure that the charging circuit is re-enabled if it is necessary to limit the current once more.

In a CSI system there should not be a large inrush current when the system is energised, due to there being no path for current to flow when the inverter is not active. There will however be an inrush when current is demanded by the inverter, the machine speed is zero and no current is flowing in the inductor (through the shorting bridge). The magnitude of the current will depend on the inductance value of the circuit (DC link and machine). Should the inrush be larger than desired, or permitted, modulation of the power electronic switches in one leg of the inverter could be used to ‘pre-charge’ the inductor in the time between energising the system and the machine rotating. The modulation could be as simple as activating switch 4 and modulating switch 1 (with the inductor bridge switch modulated in opposition) until the required current is flowing through the inductor. A possible alternative solution, provided the starting torque (and therefore current) is low, is to control the DC link voltage when starting the machine. The ramp up from zero volts as the machine starts would also limit any inrush current.

2.5.3 Dead-banding

Dead banding PWM signals is required to prevent shoot through faults, a dead time is necessary due to the non-ideal characteristics of the semiconductor switches. The non-ideal characteristics result in the turn on and turn off of the device not being instantaneous; this characteristic has been studied in detail [52] and well understood. Figure 2.16 details a typical switching characteristic of a semiconductor device, the parameters of interest when determining dead banding requirements are:

- $t_d(\text{on})$ – the time delay between the gate signal turning on and the device beginning to conduct.
- $t_c(\text{on})$ – the time for the current to rise from zero to rated.
- $t_d(\text{off})$ – the time delay between the gate signal turning off and the device current beginning to reduce.
- $t_c(\text{off})$ – the time for the current to fall from rated to zero.

These parameters are usually supplied by the device manufacturer and due to the parameters being function of the current flowing through the device, they are provided in graphical form so that the total turn-on and turn-off times can be accurately calculated for the particular application.

The dead banding inserted in the PWM signal should be no less than that of the worst case, often a safety factor is applied to ensure system reliability. Introducing a dead time does affect the performance of the drive system [46], reducing the stability of the system and increasing low order harmonics, these factors increase as the dead time is increased. Careful consideration of the safety factor is required if maintaining the performance of the drive system is a priority.

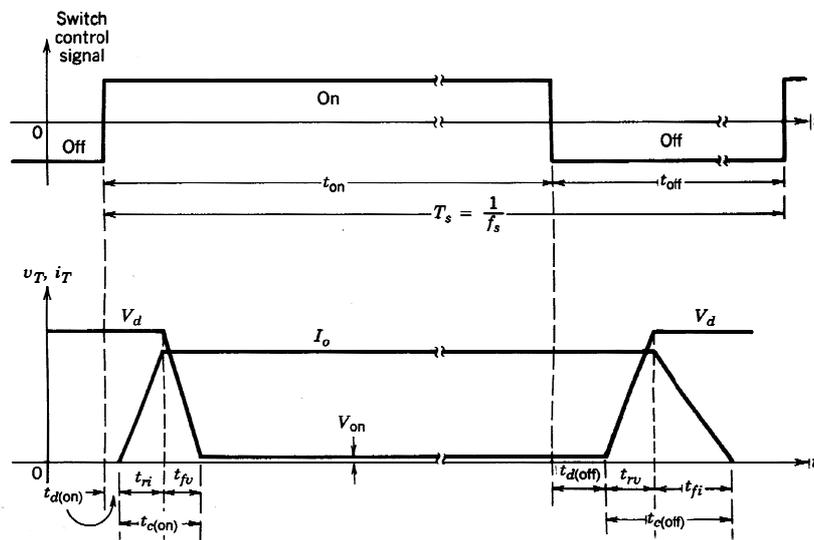


Fig. 2.16 Semiconductor switching characteristics [52].

For a CSI system the dead time has a duality in the overlap time, to achieve a continuous conduction path for the DC link current, it may be necessary to extend the ‘on’ signal for each device. This will ensure that the device turning on is fully conducting before device turning off interrupts the current flowing through it, although devices tend to turn on faster than they turn off, this may appear to be unnecessary, however, the consequences of interrupting the current path could be catastrophic for the inverter silicon devices as a rapidly changing current will induce a voltage across the DC link inductor which could be transiently very large, damaging devices.

2.6 Summary

Background theory on rotating machine control and associated power electronic switching has been presented for space vector modulation VSI converters as a baseline reference for development of a CSI scheme. Detailed information, not commonly found in standard switching literature, has been presented, on the standard CSI switching scheme that is generally implemented via the use of a large DC link inductance. A modified CSI PWM switching scheme that allows the full benefits of PWM techniques to be achieved in CSI systems, i.e. allowing the inverter bridge to be switched in an all device-off mode, is presented. This mode of switching allows a comparable strategy to VSI scheme to be realised.

Methods for pre-charging the DC link inductor to allow for the safe start-up of CSI PWM systems, have been discussed and one procedure is presented that facilitates drive operation.

Mapping of the VSI to CSI switching logic is presented in Table 2.3. This has not been previously published.

CHAPTER 3

VSI AND CSI LOSS ESTIMATION

3.1 Introduction

An early intention of this research study was to ultimately design and build hardware to test validate the precursor analysis and simulation thereof. The objectives of the chapter are therefore to develop suitable analysis for the prediction of inverter losses and to finalise VSI and CSI specification requirements for further simulation study (in CHAPTER 4) and hardware validation (in Chapter 5).

3.2 Power Supply and Test Machine Specification

The basic outline specification for a test prototype system evolved from the aerospace actuation systems researched in the EU CESAR project [2]. Two actuation systems were studied a 50W electro-mechanical actuator (EMA) and a 1KW electro-hydrostatic actuator (EHA). The 1kW EHA system specification was chosen since it represented reasonable power levels for sensible test validation measurements. The DC power used for the test rig was determined by an available 150V, 1.5kW, adjustable power supply and the PMSM will be an available, industrial 3kW, 3krpm AC servo machine manufactured by Control Techniques [53]. A nominal voltage of $150V_{DC}$ will result in the maximum machine speed being limited to approximately 800rpm.

The operation of the CSI results in a voltage boost of approximately $\sqrt{\frac{3}{2}}$ [38]. Therefore to achieve the same operating speed point (where the maximum speed at full modulation is

800rpm), the CSI system requires a supply voltage of approximately 120V at full load, to be confirmed during simulation. Thus the CSI system will be designed to take this into account, and the chosen power supply has the ability to operate at 120V at this load.

3.3 Silicon Devices

Using the PMSM specification [53] the mechanical power output can be estimated using Equation (3.1) [11]. At 1krpm, although not attainable using the available power supply, the phase current will be $5.9A_{RMS}$. The silicon devices should therefore be rated for 150V and 6A, although as devices are manufactured in stepped voltage and current levels, the actual device selection will be a combination of voltage and current that exceeds the calculated requirements, often voltage ratings are approximately doubled to provide security of operation during small over-voltage transients.

$$P_{mech} = 3 \cdot EMF_{phase,RMS} \cdot I_{Phase,RMS} \quad (3.1)$$

To allow direct comparison of the VSI and CSI topologies, both were built using individual components instead of using a standard six-switch integrated power electronic module (PEM) for the VSI. The devices will also be chosen to allow use in either topology, ensure other system components, such as gate drive systems, will function regardless of the topology. The chosen devices are detailed in Table 3.1 along with the parameters of interest from the manufacturer's data sheets [54,55].

IGBT	Part Number	IRGB4056
	Voltage Rating	600 V
	Current Rating	12 A
Diode	Part Number	STTH1210
	Voltage Rating	1200 V
	Current Rating	12 A

Table 3.1 Test rig power electronic device specifications.

3.4 VSI Silicon Losses

Semiconductor losses within VSI and CSI systems have previously been studied by [56] and [38], the analytic techniques used do not take into account the non-linear effects of semiconductor power devices and no test measurements have verified the results. Also, the PWM scheme used for the CSI system studied is a standard system and not the MCSI-SV-PWM that will be implemented in hardware, therefore the losses will be calculated using equations from Casanellas [57] for the VSI and the principles used in will be adapted to produce loss equations the CSI system.

Power losses in the IGBTs of VSIs when switching sinusoidal currents have previously been studied by Casanellas [57], the losses fall into three categories; conduction, switching, reverse recovery and applied to the IGBT itself and/or the internal free-wheeling diode. The losses are as follows:

- P_{C-IGBT} ; the losses associated with the conduction of current through the main switch, which is not a perfect conductor, and is based upon the linear approximation of the diode equation.
- $P_{C-DIODE}$; the losses associated with the conduction of current through the free-wheeling diode, again based upon the linear approximation of the diode equation.
- $P_{SWITCH-ON}$; the losses associated with the transition from blocking current to conduction current where the voltage across the C-E junction has not yet fallen to its 'fully-on' state, yet current has started to flow through the device.
- $P_{SWITCH-OFF}$; the losses associated with the transition from fully conducting current to blocking the current flow current through the device.
- P_{RR} ; the losses associated with the diode changing from a conducting state to a blocking state.

These loss mechanisms are based upon parameters that change with operating temperature of the device junction. The models developed in [57] use linear approximations for temperature related effects and those models have been verified by calorimetric testing and found to be accurate to within 5-10% [58].

Using [57] the conduction losses through the IGBT switch can be calculated using:

$$P_{C-IGBT} = \left(\frac{1}{8} + \frac{2\sqrt{3}}{9\pi} M \cos \theta - \frac{\sqrt{3}}{45\pi} M \cos 3\theta \right) \left(\frac{V_{CEN} - V_{CO}}{I_{CN}} \right) I_{CM}^2 + \left(\frac{1}{2\pi} + \frac{\sqrt{3}}{12} M \cos \theta \right) V_{CO} I_{CM} \quad (3.2)$$

The conduction losses associated with the diode within the IGBT device can be calculated using:

$$P_{C-DIODE} = \left(\frac{1}{8} + \frac{2\sqrt{3}}{9\pi} M \cos \theta - \frac{\sqrt{3}}{45\pi} M \cos 3\theta \right) \left(\frac{V_{CEN} - V_{FO}}{I_{CN}} \right) I_{CM}^2 + \left(\frac{1}{2\pi} + \frac{\sqrt{3}}{12} M \cos \theta \right) V_{FO} I_{CM} \quad (3.3)$$

The switch-on losses can be calculated using:

$$P_{SWITCH-ON} = \frac{1}{8} V_{CC} t_{rN} F_S \left(\frac{I_{CM}^2}{I_{CN}} \right) \quad (3.4)$$

The switch-off losses can be calculated using:

$$P_{SWITCH-OFF} = V_{CC} I_{CM} t_{fN} F_S \left(\frac{1}{3\pi} + \frac{1}{24} \frac{I_{CM}}{I_{CN}} \right) \quad (3.5)$$

The reverse recovery losses can be calculated using:

$$P_{RR} = F_S V_{CC} \left[\left(0.28 + \frac{0.38 I_{CM}}{\pi I_{CN}} + 0.015 \left(\frac{I_{CM}}{I_{CN}} \right)^2 \right) Q_{rrN} + \left(\frac{0.8}{\pi} + 0.05 \frac{I_{CM}}{I_{CN}} \right) I_{CM} t_{rrN} \right] \quad (3.6)$$

3.5 CSI Silicon Losses

Semiconductor loss mechanisms within CSIs have the same basis as those in VSI systems but must be adapted to incorporate the differences in topology, modulation system and current waveforms. The loss mechanisms for the inverter IGBTs of the CSI will be the same as the CSI with the exception of the diode conduction loss ($P_{C-DIODE}$) and reverse recovery loss (P_{RR}), although the IGBTs do incorporate fly-back diodes, the series diodes will prevent

current from flowing through the fly-back diodes therefore there will be no losses associated with the fly-back diodes. Additional to the inverter IGBT losses, there will also be losses associated with the series diodes, conduction and reverse recovery, and also IGBT and diode losses for the inductor shorting circuit.

Using [57] as a basis, equations have been formed to predict the semiconductor losses for a CSI system. CSI conduction losses for each IGBT ($P_{C-IGBT-CSI}$) can be calculated from the Equation (3.7) taken from [59] and adapted for the CSI modulation and current functions.

$$E_C = V_{CE} i_c \delta \tau \quad (3.7)$$

Where:

- E_C is the conduction energy.
- V_{CE} is the Collector-Emitter voltage of the IGBT.
- i_c is the current flowing through the IGBT.
- δ is the modulation function.
- τ is the conduction time.

The modulation function for a single IGBT in a CSI system is significantly different from that in a VSI system, firstly the IGBT will only be modulated for half of the cycle, the other half it will be off, i.e. each leg of the CSI will have one switch modulate while the other is off before reversing roles in the second half of the cycle. The modulation function for an IGBT in a CSI system is detailed in Equation (3.8).

$$\delta = M \sin(\omega t) \quad \text{for } 0 < \omega < \pi \quad (3.8)$$

Where:

- M is the modulation index.
- ω is the electrical position.

Given the previous stipulation that voltage and current waveforms in a CSI system are line-to-line values, the current conducted by the IGBT must be the same as that in the DC Link inductor during the conduction time, using [52] the line-to-line nature of the waveform can be defined in Equation (3.9) as:

$$I_{dc} = \sqrt{2}i \cos \omega t \quad \text{for } -\frac{1}{6}\pi < \omega t < \frac{1}{6}\pi \quad (3.9)$$

However, to calculate the power loss, E_C must be integrated over the same period as the modulation function, 0 to π . Therefore an approximation must be used. Equation (3.10) represents an approximation of the DC link current.

$$I_{DC} \approx \hat{I} \left(0.95 - \frac{\cos(6\omega t)}{16} \right) \quad (3.10)$$

Where:

- \hat{I} is the peak motor phase current.

The approximation was determined using an iterative approach in graphing software, Figure 3.1 details the DC link current, as defined by Equation (39) and the approximation as defined by equation (3.10) for operating points of 1 p.u., 0.5 p.u. and 0.05 p.u.

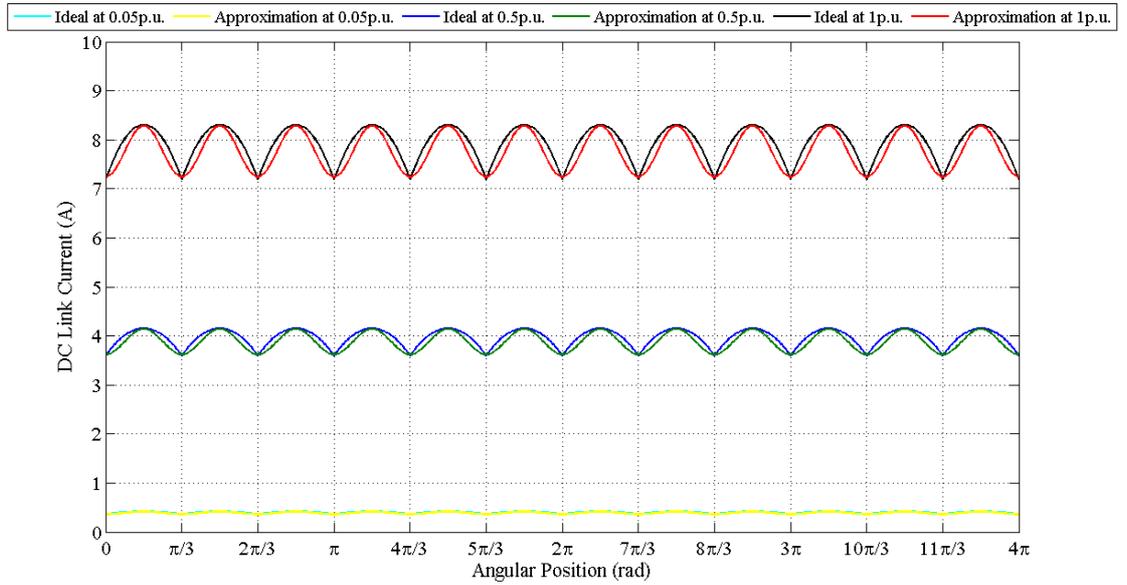


Fig. 3.1 Calculated and approximate DC link current waveforms.

As in [57] the power dissipated can be calculated by integrating the conduction energy over the period of repetition, 0 to π and dividing it by the cycle time, 2π , as in Equation (3.11).

$$P_{C-IGBT-CSI} = \frac{1}{2\pi} \int_0^{\pi} E_{C-IGBT-CSI} d\omega \quad (3.11)$$

Solving Equation (3.11) leads to Equation (3.12), which allows the calculation of IGBT conduction losses based on the operating point of interest and the device parameters as stated by the device manufacturer.

$$P_{C-IGBT-CSI} = \frac{\hat{I}M}{2\pi} \left[1.7533\hat{I} \left(\frac{V_{CEN} - V_{CO}}{I_{CN}} \right) + 1.9035V_{CO} \right] \quad (3.12)$$

Given the condition that the series diode conducts during the same period as the IGBT, Equation (3.12) can be re-written with the diode specific parameters replacing those of the IGBT, resulting in Equation (3.13) to calculate $P_{C-DIODE-CSI}$.

$$P_{C-DIODE-CSI} = \frac{\hat{I}M}{2\pi} \left[1.7533\hat{I} \left(\frac{V_{FN} - V_{FO}}{I_{CN}} \right) + 1.9035V_{FO} \right] \quad (3.13)$$

Incorporating the CSI current, Equation (3.10), with the equation from [59] for switch on losses (detailed in Equation (3.14)), the equation for $P_{SWITCH-ON-CSI}$ at the inverter switching frequency F_S can be shown to be Equation (3.15).

$$E_{ON} = \frac{1}{2} V_{CC} i_C t_{rN} \left(\frac{i_C}{I_{CN}} \right) \quad (3.14)$$

$$P_{SWITCH-ON-CSI} = \frac{0.2272 V_{CC} t_{rN} \hat{I}^2}{\pi I_{CN}} F_S \quad (3.15)$$

Similarly, the equation for switch off loss, Equation (3.17), can be determined using Equation (3.10) and the equation for turn off loss from [57] (detailed in Equation (3.16)).

$$E_{OFF} = \frac{1}{2} V_{CC} i_C t_{fN} \left(\frac{i_C}{I_{CN}} \right) \quad (3.16)$$

$$P_{SWITCH-OFF-CSI} = \frac{0.2272 V_{CC} t_{fN} \hat{I}^2}{\pi I_{CN}} F_S \quad (3.17)$$

Reverse recovery losses can be determined using Equations (3.18) and (3.19) from [57] and Equation (3.10), resulting in Equation (3.20)

$$E_{RR} = V_{CC}t_{rrN} \left(0.8 + \frac{0.2i_C}{I_{CN}} \right) \left(0.35I_{rrN} + \frac{0.15i_C}{I_{CN}}I_{rrN} + i_C \right) \quad (3.18)$$

$$P_{RR} = \frac{F_S}{2\pi} \int_0^{\pi} E_{RR} d\theta \quad (3.19)$$

$$P_{RR} = \left(\frac{V_{CC}F_S}{2\pi} \right) \left[\left(0.28 + \frac{0.114\hat{I}}{I_{CN}} + \frac{0.0665\hat{I}}{I_{CN}} + 0.02727 \left(\frac{\hat{I}}{I_{CN}} \right)^2 \right) Q_{rrN} + \left(\frac{0.76}{I_{CN}} + \frac{0.3925\hat{I}}{I_{CN}} \right) \hat{I}t_{rrN} \right] \quad (3.20)$$

Conduction losses within the inductor shorting circuit can be determined using the DC link current and the modulation function for the inductor shorting bridge. The modulation function for the inductor bridging circuit will be the difference between the envelope average of the inverter switches and 1, it can be approximated by Equation (3.21), determined using the same method as for Equation (3.10)

$$\delta_{SHORT} = 1 - 0.95M - 0.1313M|\cos(3\omega t)| \quad (3.21)$$

To calculate the dissipated power the integration required is not possible as the period of Equation (3.21) does not match that of the DC link current, Equation (3.10), and contains a magnitude function. To allow the calculation of dissipated power, Equation (3.21) must be approximated using a function of the same period as Equation (3.10). This results in Equation (3.22) for the modulation function of the inductor shorting bridge.

$$\delta_{SHORT} = 1 - 0.95M + 0.1313M \cos(6\omega t) \quad (3.22)$$

The power dissipated due to IGBT conduction losses in the inductor shorting circuit IGBT ($P_{C-IGBT-S-CSI}$) can be determined using Equations (3.10), (3.11) and (3.22), resulting in Equation (3.23).

$$P_{C-IGBT-S-CSI} = \frac{1}{2\pi} \left[\left\{ \left(\frac{V_{CEN} - V_{CO}}{I_{CN}} \right) \left(0.9025\hat{I}^2(1 - 0.95M) + \left(\frac{\hat{I}^2\pi}{768} \right) - (1.299 \times 10^{-3}\hat{I}^2M\pi) \right) \right\} + 0.95\hat{I}V_{CO}(1 - 0.95M) + 0.6839 \times 10^{-3}\hat{I}M\pi V_{CO} \right] \quad (3.23)$$

As with the inverter diode losses, the inductor shorting circuit diode losses can be determined by replacing the IGBT specific parameters in Equation (3.23) with the parameters for the diode, resulting in Equation (3.24)

$$\begin{aligned}
P_{C-DIODE-S-CSE} &= \frac{1}{2\pi} \left[\left(\frac{V_{FN} - V_{FO}}{I_{CN}} \right) \left(0.9025 \hat{I}^2 (1 - 0.95M) + \left(\frac{\hat{I}^2 \pi}{768} \right) \right. \right. \\
&\quad \left. \left. - (1.299 \times 10^{-3} \hat{I}^2 M \pi) \right) \right] + 0.95 \hat{I} V_{FO} (1 - 0.95M) \\
&\quad \left. + 0.6839 \times 10^{-3} \hat{I} M \pi V_{FO} \right] \tag{3.24}
\end{aligned}$$

The losses associated with switching and reverse recovery will be the same for the inductor shorting circuit as for the inverter.

3.6 VSI Passive Components

In a VSI system, the purpose of the DC Link capacitor is to provide a stiff voltage source to the load, i.e. the DC Link voltage does not change as the load. An approximation of this is achieved by choosing a capacitance value that reduces the DC Link voltage ripple to a level that is insignificant to the operation of the system; this is often specified to be no greater than 5%. The stiff DC link voltage allows the control system of the inverter to achieve good torque and speed control, if the voltage ripple was too large, the system could become unstable.

Several papers have shown that the capacitance in the dc link capacitor is usually determined by the effective capacitor current stress and not by a given maximum admissible value of the amplitude of the dc link voltage ripple [59]. Hence, simple mathematical equation is obtained in [52], as in Equation (3.25).

$$I_{C(rms)} = I_{L(rms)} \sqrt{2M \left\{ \frac{\sqrt{3}}{4\pi} + \cos^2(\Phi) \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} M \right) \right\}} \tag{3.25}$$

Where:

- $I_{C(rms)}$ is the capacitor RMS current.
- $I_{L(rms)}$ is the load RMS current.
- M is the modulation index.
- Φ is the phase angle.

It can be shown [52] that the maximum current will occur when the phase shift is zero and the modulation index satisfies equation (3.26).

$$M = \frac{8 \cdot \sqrt{3}}{9} \left(1 + \frac{1}{4 \cdot \cos^2 \Phi} \right) \quad (3.26)$$

The maximum will be approximately 0.6

To analytically size the required dc link capacitor in the considered VSI system, a percentage ripple of the dc source is assumed to be 5% and the PWM carrier switching frequency is set to 20 KHz, see Chapter 5. Therefore, the required dc link capacitor value, which meets the specified initial constraints, is calculated by Equation (3.27).

$$C = \frac{I_{c(peak)} dt_c}{dU} \quad (3.27)$$

Where:

- dt_c is the period of the switching frequency.
- dU is dc link voltage ripple.

Solving Equation (3.25) results in a capacitor current of $3.1A_{RMS}$, utilising the previously discussed system specification the required DC link capacitance is calculated to be $27\mu F$, for a maximum of 5% voltage ripple. Utilising manufacturers' specifications, a capacitor with a voltage rating in excess of 150V, and current rating in excess of 3.1A, requires the capacitor specifications detailed in Table 3.2.

Capacitance	1000 μF
Voltage Rating	200 V
Voltage Rating (Surge)	250 V
RMS ripple current	3.25 A

Table 3.2 DC link capacitor specification.

The losses within the DC link capacitor can be determined using the manufacturers stated equivalent series resistance (ESR) and the capacitor current. When utilising PWM switching the capacitor current has a different magnitude at each harmonic and the ESR varies with frequency. The variation of ESR with frequency is a device specific function and [59] states the equation as:

$$ESR_f = \frac{ESR_{120}}{(Mf)^2} \quad (3.28)$$

Where:

- ESR_f is the ESR at the desired frequency, f .
- ESR_{120} is the manufacturer stated ESR at 120Hz.
- Mf is the frequency multiplier for f .

The total power loss is the sum of the power losses at all significant frequencies, as in Equation (3.29), a harmonic analysis of the capacitor current allows calculation of the loss.

$$P_{CAP} = \sum_{n=1}^{n=k} (I_{nf}^2 ESR_{nf}) \quad (3.29)$$

Where:

- P_{CAP} is the total power loss in the capacitor.
- n is the harmonic number.
- k is the highest significant harmonic.
- I_{nf} is the capacitor current at harmonic nf .
- ESR_{nf} is the ESR at the harmonic nf .

3.7 CSI Passive Components

In a CSI system the purpose of the DC Link inductor is to provide a stiff current source to the load. The DC link current will depend on the load operating point at any given time and therefore the definition ‘stiff’ applies over a small time-scale, this results in the DC link inductor being sized according to prevent large changes of the DC link current over a single switching event.

Using the same 5% rule as the VSI, applying it to the full load current of a CSI system, results in a 300mA maximum current change over one switching event. A CSI system using tri-state SVPWM has two operating modes per switching cycle, during which the DC link current will change. In the ‘on’ mode, when the inverter switches create a current path from the DC link to the motor, the inductor current will rise, during the ‘off’ mode, the inductor current ‘freewheels’ through the freewheel bridge and the inductor current falls. A DC model of the DC Link, inverter and machine is detailed in Figure 3.2, SW1 represents the change from ‘on’ to ‘off’ mode.

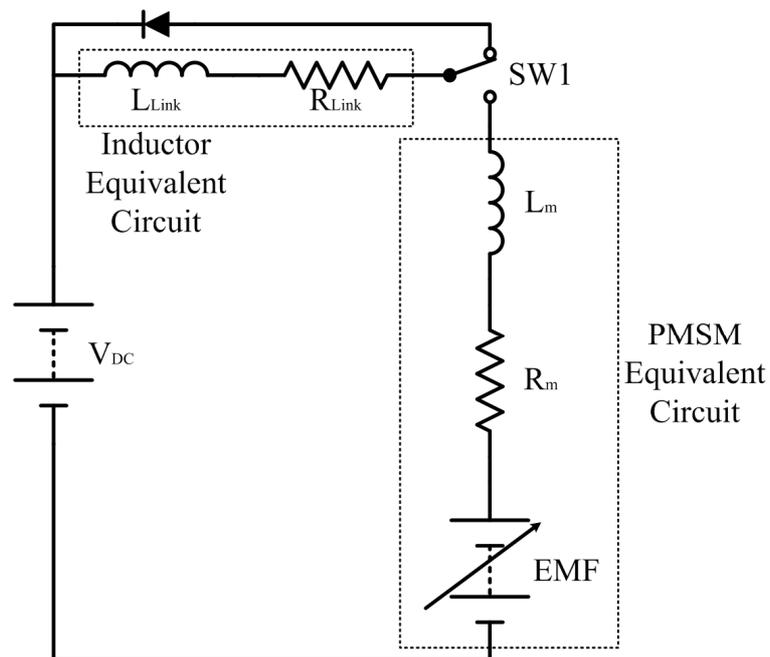


Fig. 3.2 DC model of a CSI and PMSM.

During the ‘on’ mode the current rise in the DC link inductor is shown in Equation (3.30), whereas the current fall in the DC link inductor during the ‘off’ mode is described in Equation (3.31):

$$\Delta I_{rise} = \left\{ \frac{V_{dc} - E}{R_{total}} \right\} \left[1 - e^{-\left(\frac{R_{total} t_{on}}{L_{total}} \right)} \right] \quad (3.30)$$

$$\Delta I_{fall} = I_{(0)} \left[1 - e^{-\left(\frac{R_{Ldc} t_{off}}{L_{Ldc}} \right)} \right] \quad (3.31)$$

Where:

- E is the motor EMF_{L-L,RMS}.
- $R_{total} = R_{Link} + R_m$.
- $L_{total} = L_{Link} + L_m$.
- $I_{(0)}$ is the inductor current flowing at $t=0$.
- F_s is the switching frequency.
- $t_{on} = \frac{M}{F_s}$.
- $t_{off} = \frac{(1-M)}{F_s}$.

The maximum ΔI_{rise} will occur when the EMF is at its minimum and t_{on} is at its maximum, whereas the maximum ΔI_{fall} will occur when $I_{(0)}$ and t_{off} are their maximum values. Specifying a maximum current rise of 5% of full load current per switching event and an operating point when the motor is starting at maximum torque ($E=0$, $t_{on} = \max$ and $\Delta I_{rise} = 300\text{mA}$), using Equation (3.30), the target DC link inductor is determined to be 16mH. At the same operating point the current fall during the ‘off’ mode is determined, using Equation (3.31), to be 49.7 μA .

The worst-case current fall in the inductor will occur at full load and a low motor speed, from circuit analysis, the operating point is determined to be a motor speed of 50rpm at full torque. Using Equation (3.31), this results in a current fall of 17.1mA, which is significantly lower than the maximum current rise.

The inductor inductance was designed by modifying an existing laboratory soft-iron cored circuit for which the magnetic characteristics were well documented. This enabled fine tuning of the inductance, and also quick test of the circuit sensitivity to this component value. The size of the DC link inductance will determine the minimum time response of the system when subjected to a step change in output torque, the time response will be its maximum when motor is operating at full speed with a low output torque and a change to

full torque is demanded. Using Equation (3.30), with an initial torque of 0.2 p.u., the time response of the system is determined to be 2.4ms.

The changing current in L_{Link} will result in an EMF across the inductor, that must be within the device specifications of the components in the freewheel bridge; the maximum inductor voltage during current rise will be 95V and -300mV during current fall, with the inverter side of the inductor being the reference. The inductor voltages should pose no problems to devices rated appropriately for this system.

The DC link inductor losses are determined by using Equation (3.32) and the rms value of the inductor current.

$$P_{Link} = I_{Link-RMS}^2 R_{Link} \quad (3.32)$$

The filter capacitor on a CSI system aids commutation, however, the presence of the capacitor, combined with the machine and DC link inductance and resistance will create a resonance effect, where the machine could become unstable and/or components, insulation, etc damaged. The capacitor value should be chosen so that the resonance frequency does not coincide with the fundamental frequency, switching frequency or significant harmonics of either frequency. The capacitors are required to be non-polarised, have sufficiently high voltage rating, considerations of the cost and availability of the capacitors should also be considered when determining the size.

If the resonant frequencies to avoid are chosen to be those below $20f_1$, 1kHz for a $50\text{Hz}_{(max)}$ output and those of approximately 10kHz , $\frac{f_c}{2}$, then a frequency sweep in a circuit simulation package can determine the resonant frequency based upon the parameters for the DC link inductor and PMSM. It is found that if the capacitor value is limited to the range $0.1\mu\text{F}$ to $1\mu\text{F}$, the resonant frequency will be in the range 2.74kHz to 8.65kHz . A readily available capacitor, recommended for motor filter applications, has been selected; it is a $0.47\mu\text{F}$, 1000V metal film capacitor manufactured by EPCOS.

The capacitor losses, as with the DC link capacitor, can be determined using Equation (3.29), the manufacturers' specifications [60] and ESR calculation, as in Equations (3.28) and (3.29).

3.8 Topology Loss Comparison

The parameters for Equations (3.2) to (3.6) have been taken from the manufacturer data sheet for the selected IGBT and diode, and are listed in Table 3.3.

Parameter	Definition	Value	Units
V_{CEN}	rated V_{CE}	1.9	V
V_{CO}	threshold V_{CE}	1	V
I_{CN}	rated I_C	12	A
V_{FO}	diode threshold voltage	0.7	V
t_{rN}	rated rise time	18	ns
t_{fN}	rated fall time	41	ns
Q_{rrN}	rated recovery charge	800	nC
t_{rrN}	Rated recovery time	68	ns

Table 3.3 Device parameters for semiconductor loss equations.

For the VSI system, the worst-case operating parameters, full load at full speed, have been detailed in Table 3.4.

Parameter	Value	Units
V_{CC}	150	V
I_{CM}	5.9	A
$\cos \theta$	1	p.u.
F_S	20	kHz
M	0.95	p.u.

Table 3.4 VSI full load operating parameters.

Using Equations (3.2) to (3.6), (3.29) and (3.30), the parameters in Tables 3.8 and 3.9, the losses for the VSI semiconductors have been calculated and are detailed in Table 3.5. The DC link capacitor loss, detailed in Table 3.5, has been determined using Equations (3.28) and (3.29), the manufacturers' specifications and a harmonic analysis of the capacitor current from the simulation in Chapter 4.

Element	(W)
P_{C-IGBT}	2.59
$P_{C-DIODE}$	0.95
$P_{SWITCH-ON}$	0.02
$P_{SWITCH-OFF}$	0.09
P_{RR}	1.16
Device total	4.80
Inverter Total	28.8
P_{Cap}	4.64
System total	33.46

Table 3.5 VSI system power electronic and DC link losses.

For the CSI system the worst-case operating parameters, full load at full speed, have been detailed in Table 3.6. The DC link inductor loss has been determined using Equation (3.32), while the filter capacitor loss has been determined using Equations (3.29) and (3.30), the manufacturers' specifications and a harmonic analysis of the filter capacitor current from the simulation in Chapter 4. The CSI inverter and DC link losses are detailed in Table 3.7.

Parameter	Value	Units
V_{CC}	150	V
\hat{I}	8.3	A
$\cos \theta$	1	p.u.
F_s	20	kHz
M	0.95	p.u.

Table 3.6 CSI operating parameters.

CSI element	W
$P_{C-IGBT-CSI}$	3.76
$P_{C-DIODE}$	2.74
$P_{SWITCH-ON}$	0.02
$P_{SWITCH-OFF}$	0.05
P_{RR}	0.48
½ leg total	7.04
Inverter total	42.24
Inductor Short	
$P_{C-IGBT-S-CSI}$	0.19
$P_{C-DIODE-S-CSI}$	0.08
$P_{SWITCH-ON-S}$	0.02
$P_{SWITCH-OFF-S}$	0.05
P_{RR-S}	0.48
Inductor short total	0.82
Passive components	
P_{Ind}	31.46
$P_{Cap-filt-total}$	4.35
System total	78.87

Table 3.7 CSI system power electronic and DC link losses.

3.9 Summary

A set of equations have been developed to allow analytic estimation of the losses in a CSI system. The analytic results show an increase in losses over the VSI, which is to be expected due to the additional semiconductor devices in the main power circuit conduction path. The analytic results will be compared with test measurements in Chapter 5. Previously studied CSI loss calculations used simplistic, generalised loss equations for the semiconductors and did not take account of the modified switching scheme used in the MCSI-SV-PWM scheme. No previous CSI semiconductor loss analysis have presented measured data to allow verify the validity of the analysis.

A representative aerospace drive system application has been studied and used to develop VSI and CSI converter specifications. Appropriate semiconductor devices have been selected to construct VSI and CSI test hardware. A suitable DC link inductor has been specified and designed for the CSI and specifications for the capacitors in the VSI and CSI systems have been determined.

Comparison of the VSI and CSI system losses show that they (including inductor shorting losses for the CSI) increase from 29W to 43W respectively. As there are additional devices in the conduction path, this is not unexpected. The passive component losses increase from 5W to 36W since the CSI DC link inductor is subject to full operational current, whereas the losses in the VSI system are due to the magnitude of the ripple current seen by the DC link capacitor. This leads to system losses of 34W and 84W for the VSI and CSI systems respectively. Comparison of these analytic results with simulation and experimental loss results, will allow the accuracy of the calculations to be validated in Sections 5.6.1 and 5.6.2 of Chapter 5.

CHAPTER 4

DRIVE SYSTEM CIRCUIT SIMULATION

4.1 Introduction

A SABER™ simulation model for the VSI system has been created to set a benchmark for accuracy when comparing the simulation study results against data from the hardware test rig. Building on the VSI model experience, a simulation model was created for the CSI system to give a better understanding of how a CSI operates aid future circuitual developments, determine the accuracy of some of the assumptions made in Chapter 3 when estimating the losses, and to estimate the power conversion efficiency of both the VSI and CSI systems.

4.2 Aims

The aim of the system simulation is to test and confirm ideas and methods presented in earlier chapters and to produce an indication of the expected operating condition of the hardware test rig. Modern simulation software suites can produce extremely accurate results, although this comes at the expense of time. Accurate models require significant amounts of time to implement, especially for complex systems. They will also require a significant amount of simulation time, for the purpose of this project, extremely accurate simulations are not a priority, although efforts should be taken to maximise the accuracy where possible. The models will therefore require simplification to reduce the implementation and simulation time. To that end, the SABER™ simulation package, a SPICE based product, will be used for simulations, steady state operating conditions will be simulated, reducing the model complexity and PWM switching schemes based on

analogue techniques will be used instead of modelling micro-processor based PWM implementation.

4.3 Method

To simulate the steady state operating, circuit parameters require solving to set the steady state conditions. An analytical model has been created in MATLAB to solve the operating point voltage and current vector. For operating speeds up to base speed, the operating speed and phase current are set and the model solves the supply voltage vector, therefore determining the PWM settings. Figure 4.1 (a) details the vector for below base speed operation, while (b) details the above base speed vector. Above base speed this is solved in an iterative approach, by adjusting the current angle until a voltage vector is found that does not exceed that maximum output voltage.

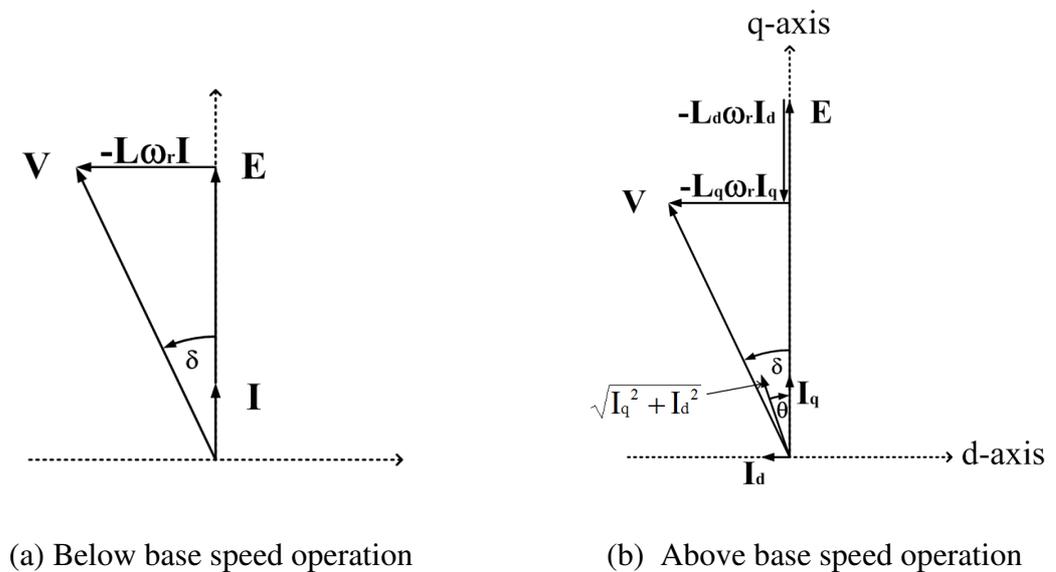


Fig. 4.1 System operating point vector.

The model includes basic motor parameters, switch and supply parameters and produces a starting point for operating the steady state model, the parameters are iteratively adjusted if the phase current characteristics do not match those desired.

4.4 Model Implementation

The system model will consist of PWM generation circuitry, the DC link, inverter model and PMSM. Visually complex parts of the model use a hierarchical system to simplify the overall system model.

4.4.1 VSI PWM Generation

Modelling micro-processor generated SV PWM is extremely time consuming in the SABER™ package, therefore analogue techniques are required. Traditional sine-triangle PWM results in under utilisation of the DC link voltage compare to SV PWM, as detailed in Chapter 2. Using [60] and [44] an analogue method for generating SV PWM signals was implemented, it is known as naturally sampled space vector PWM (NS-SV PWM). It uses zero sequence components to produce reference waveforms that emulate SV techniques. Figure 4.2 details the SABER™ sub model of the NS-SV PWM circuitry, while Figure 4.3 details the original sinusoidal reference, the zero sequence and PWM reference at a modulation of $\frac{2}{\sqrt{3}}$.

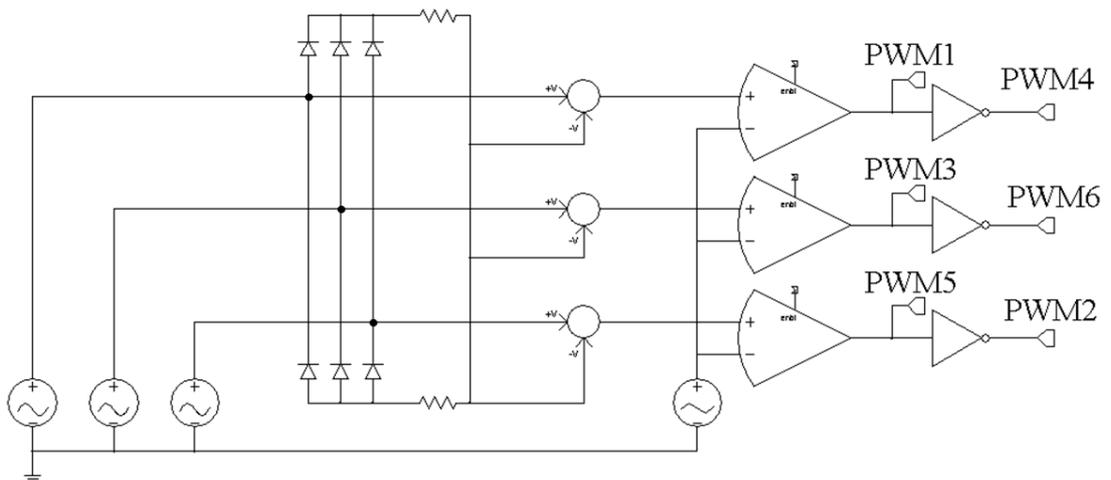


Fig. 4.2 Naturally sampled space vector model.

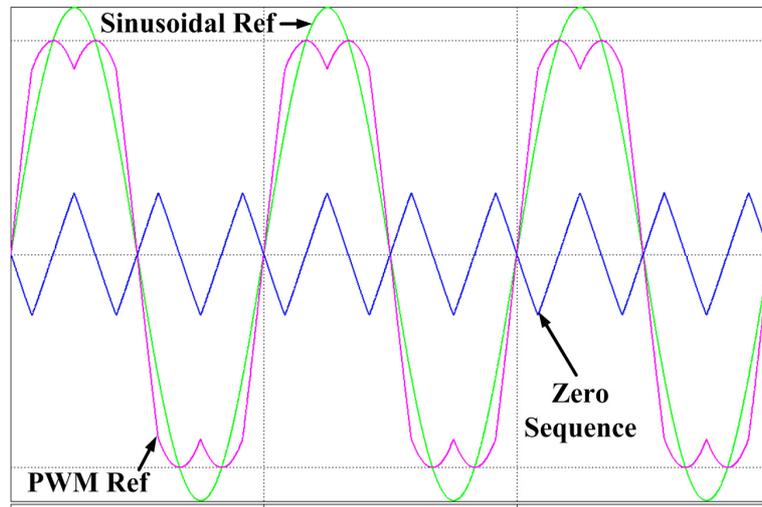


Fig. 4.3 Naturally sampled space vector reference waveforms.

The PWM signals, 1, 3 and 5 over two switching periods are detailed in Figure 4.4, also detailed, the carrier waveform and the state outputs.

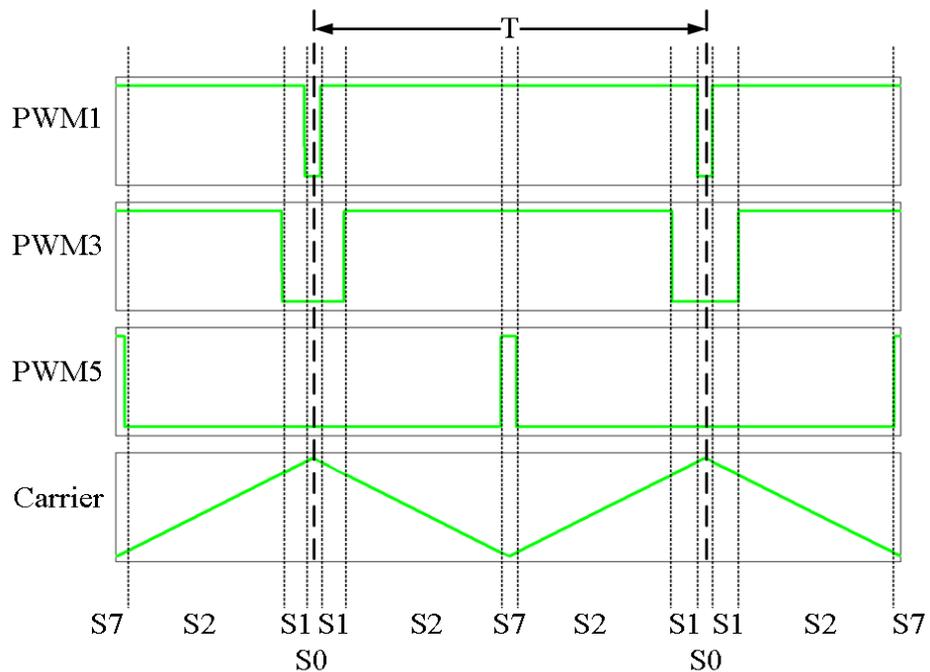


Fig. 4.4 Naturally sampled space vector PWM output.

4.4.2 CSI PWM Generation

Using the NS-SV PWM detailed previously, the CSI PWM simulation requires implementation of the CSI conversion logic detailed in Chapter 2. Logic implementation of this in SABER™ should pose no problem, in terms of complexity or simulation time,

however, checks are required to ensure correct operation before implementation of the full system simulation. Correct implementation of the logic conversion should result PWM signal 1 having an average sinusoidal output over half of the reference cycle. Each subsequent output, 2 to 6, will be successively offset by 1 sector, 60° . To ensure a sinusoidal average, a low pass filter will be implemented on a PWM test model. Obviously this will affect the phase and magnitude of the signal, however, the differences will be small and if the output is very close to the expected output then the logic conversion was a success. Figure 4.5 (a) details mathematically generated PWM output averages, while (b) details the simulated, filtered PWM outputs, confirming the operation of the VSI to CSI conversion of PWM signals 1 to 6. PWM 0, for the inductor shorting circuit will be active whenever PWM signals 1 to 6 generate a zero state output, averaging PWM0 results in the waveform being the difference between the combined operating envelope of PWM1 to 6 and modulation magnitude 1. The CSI conversion logic is implemented as a sub model on the CSI simulations.

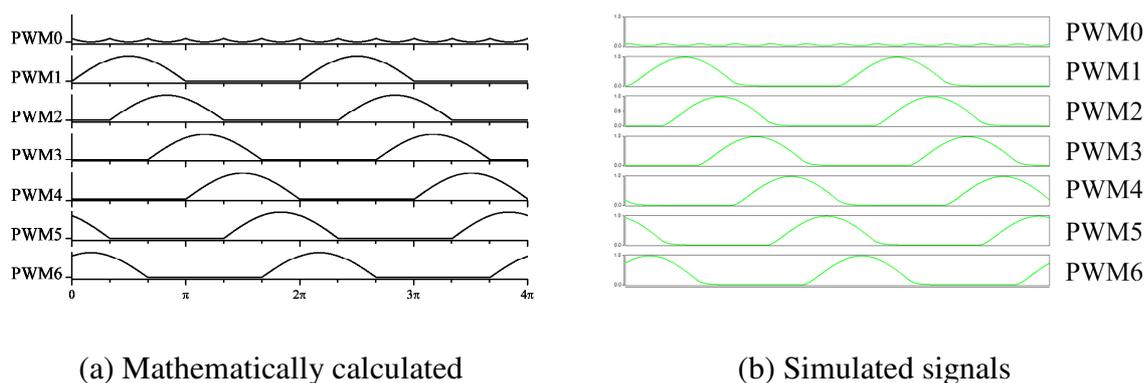


Fig. 4.5 CSI PWM switching signal averages.

4.4.3 PMSM Modelling

The PMSM is modelled using an equivalent circuit consisting of a single phase resistance, single inductance and an EMF, for simplicity, mutual inductance has not been modelled. The PMSM model includes voltage and current measurements to allow, for example, the mechanical power to be estimated. Figure 4.6 details the PMSM model, the PMSM is modelled as three phase inductance, resistance and EMF, with the details being taken from the manufacturers' product manual [53] and detailed in Table 4.1. The measured voltage and current signals are connected to sum and product functions, not detailed to allow estimation of the power etc. The analogue ground, Agnd, connection, provides a reference

for simulation, without which the simulation fails. The analogue ground is independent of the main system reference, gnd(node 0), and prevents errors due to floating nodes.

The EMF constant requires implementation manually as the amplitude, A_m , and frequency, f , of the AC output for the simulated motor speed. The $\frac{2\pi}{3}$ phase relationship is also maintained using the phase angle parameter for each phase sinusoidal source.

L_{ph}	4.3 mH
R_{ph}	0.7 Ω
f	0.477 Hz/rads ⁻¹
A_m	1.6f V
ϕ_a	From operating point analysis
ϕ_a to ϕ_b	120 degrees
ϕ_a to ϕ_c	240 degrees

Table 4.1 PMSM model specifications.

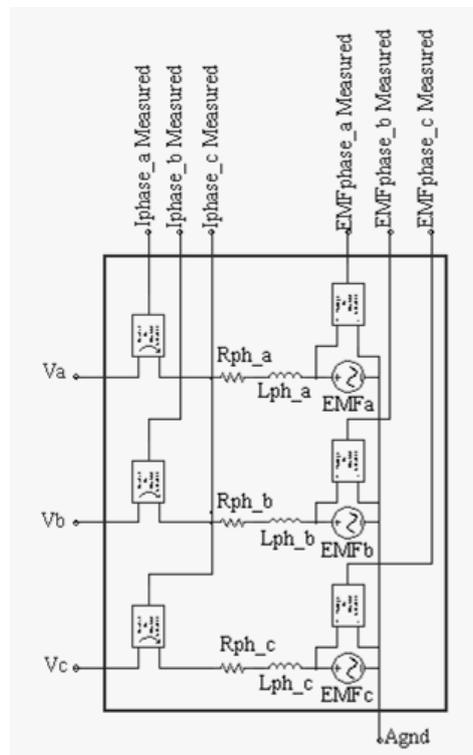


Fig. 4.6 PMSM model.

4.4.4 Passive Components

The DC link inductor has been modelled as an inductance with a series resistance (as a separate component) as shown in Figure 4.7 (a). The properties of components are set using the component property window, each window varies according to the particular component type and modelling level, Figure 4.7 (b) details the properties for the inductance component of DC link inductor. This inductor component is able to model many properties, some of which obsolete other values. For example, if n (number of turns), μ_r (relative permeability), l_{en} (magnetic path length) or area (cross sectional area) are specified then the L parameter is ignored and the model calculates the inductance using the user supplied details. Parameter i_c , is an initial condition for the current flowing in the inductor. Temperature ratings, $temp$, rth_ja etc, allow temperature characteristics to be modelled. For simplicity the effects of temperature will not be modelled for any component. A full explanation of each property of each component is available in the help files associated with each component within the SABER™ software. The series resistance of the inductor has been modelled as 0.6Ω . Once the actual inductor has been assembled, the series resistance will be determined and if there is a significant difference it may be decided to perform additional simulations. The DC link inductor parameters are summarised in Table 4.2.

Inductance	16 mH
Series resistance	0.6 Ω

Table 4.2 DC link inductor model specification.

The capacitors are modelled using the standard linear capacitor component; ESR details have been included from the manufacturers' data sheets for both the DC link capacitor, detailed in Table 4.3, and the filter capacitors, detailed in Table 4.4. The filter capacitors star point requires connection to a reference point to prevent the simulation from failing. This is achieved through the use of a $10M\Omega$ resistor to the PMSM star point.

Capacitance	1000 μF
ESR	0.2 Ω

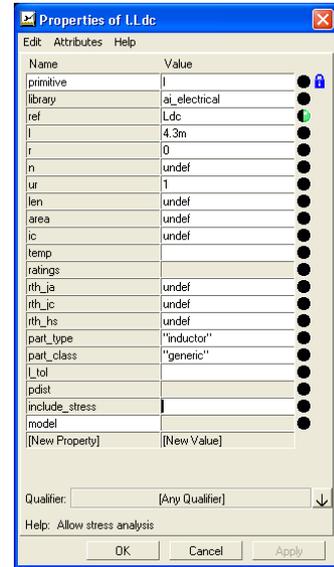
Table 4.3 DC link capacitor model specification.

Capacitance	0.47 μF
ESR	0.27 Ω

Table 4.4 Filter capacitor model specification.



(a) Schematic representation of the inductor.



(b) Component property page.

Fig. 4.7 DC link inductor model.

4.4.5 Semiconductor Modelling

To reduce implementation and computation time the semiconductors (IGBTs and diodes) were initially modelled as ideal devices. Once the operation of the system had been confirmed the ideal devices were replaced with data sheet driven models, as no specific device models were available for the devices to be used in the test rig. The data sheet driven models require specification of a set of characteristic values to allow a non linear model of the device to be implemented. The device models include a help file [61] explaining how to read the values from the manufacturers' datasheets, [54,55], to obtain the required parameters. For example, the 'vge1' parameter is listed as the V_{CE} value at the point 'P1' on the output characteristic curve (V_{CE} vs. I_{CE}), while parameter 'ic1' is the collector current at point 'P1'. The example included in the help file [61] is detailed in Figure 4.8. The process of parameter extraction is repeated for all parameters in the IGBT

and diode models, the fly-back diode within the IGBT device is modelled as a data sheet driven device for the VSI system, using parameters from the IGBT datasheet [54]. Although present in the CSI test rig, the fly-back diode has not been modelled for simplicity, the diode itself cannot conduct due to the presence of the series diode in the CSI system, and therefore errors caused by not including it should be negligible.

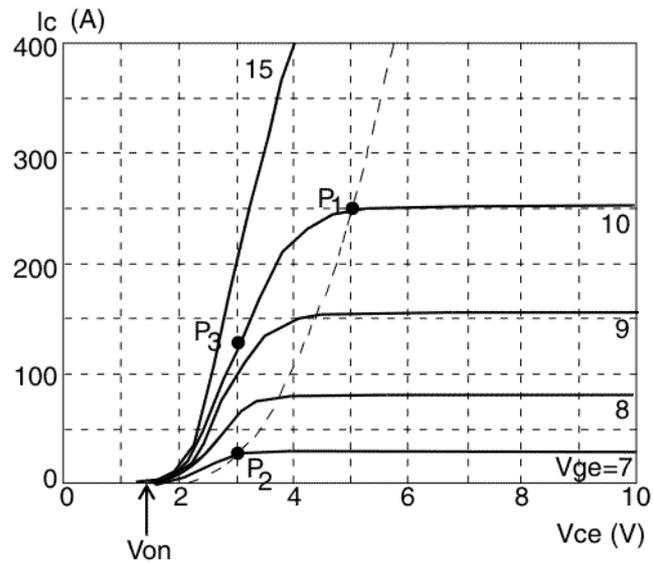


Fig. 4.8 IGBT model parameter example [61].

Table 4.5 details the parameters for the IGBTs, while Tables 4.6 and 4.7 details the VSI fly-back diode parameters and series diode parameters respectively, where NS is a parameter not specified by the manufacturer and the model default value.

Parameter	Value	Description
vce1	5 V	Co-ordinate P1 on static characteristic
vge1	12 V	Vge at co-ordinate P1
ic1	40 A	Co-ordinate P1 on static characteristic
vce2	2 V	Co-ordinate P2 on static characteristic
vge2	8 V	Vge at co-ordinate P2
ic2	4 A	Co-ordinate P2 on static characteristic
vce3	2 V	Co-ordinate P3 on static characteristic
vge3	12 V	Vge at co-ordinate P3
ic3	18 A	Co-ordinate P3 on static characteristic
vt	6 V	Channel threshold voltage
von	1 V	Collector-emitter threshold voltage
crss1	350 pF	Reverse transfer capacitance for vce=0, vge=0
crss2	20 pF	Reverse transfer capacitance for vce=4, vge=0
coss1	700 pF	Output capacitance for vce=0, vge=0
coss2	40 pF	Output capacitance for vce=vce4, vge=0
vce4	40 V	Vce voltage corresponding to (crss2,vce4)
vge4	9 V	Gate voltage corresponding to the Miller plateau
q1	7 nC	Charge corresponding to beginning of Miller plateau
q2	17 nC	Charge corresponding to the end of the Miller plateau
q3	25 nC	Total on-state gate charge
vge5	15 V	On-state gate voltage
vce5	1.9 V	On-state Vce voltage
vce6	600 V	Off-state Vce voltage
tau	NS s	Time constant related to turn-off tail current
itail1	NS A	Collector current before turn-off
itail2	NS A	Maximum tail current in hard turn-of commutation
rg	NS Ω	Internal gate resistance
m	NS -	Miller capacitance coefficient
n	NS -	Smoothness transition

Table 4.5 IGBT model parameters.

Parameter	Value	Description
ron	63 m Ω	On-state resistance
roff	250 k Ω	Off-state resistance
von	2.1 V	Knee voltage
ifo	15 A	On-state current before turn off process
dirdt	600e ⁶ A/s	Current slope at turn-off
irrm	19 A	Peak reverse recovery current
trr	60 ns	Reverse recovery time
qrr	NA C	Recovery charge (not required if trr and irrm specified)
cj	23 pF	Junction capacitance
r_snap_off	NS Ω	Snap_off resistance
n	NS -	Smoothness transition

Table 4.6 VSI fly-back diode model parameters.

Parameter	Value	Description
ron	115 m Ω	On-state resistance
roff	260 k Ω	Off-state resistance
von	1.4 V	Knee voltage
ifo	15 A	On-state current before turn off process
dirdt	200e ⁶ A/s	Current slope at turn-off
irrm	20 A	Peak reverse recovery current
trr	67 ns	Reverse recovery time
qrr	NA C	Recovery charge (not required if trr and irrm specified)
cj	10 pF	Junction capacitance
r_snap_off	NS Ω	Snap_off resistance
n	NS -	Smoothness transition

Table 4.7 CSI series diode model parameters.

4.4.6 Dead-banding and Overlap Modelling

The dead-banding, or overlap, is implemented using logic gates and an RC circuit to create a time difference between the rising or falling edges of the gate inputs. For dead-banding, an AND gate is used, the RC circuit delays the second input by τ , preventing the output from changing and therefore creating a turn-on delay. The overlap circuit uses the same principle with an OR gate, holding the output high for the additional time τ and resulting in a turn-off delay. The dead-banding sub model is detailed in Figure 4.9, the overlap sub model, not shown, has an additional channel for the inductor bridge circuit.

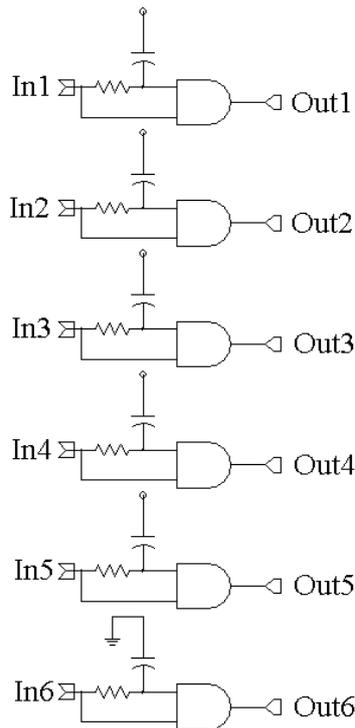


Fig. 4.9 Dead-banding sub model implementation.

4.4.7 Gate Drive Modelling

The gate drive circuitry has not been modelled as a functionally complete system. The gate drive sub model simply converts the logic format PWM signal to a voltage output, with reference, to allow connection to the IGBT gate and emitter terminals. A gate source resistance has been included as a small value to allow successful simulation when using characterised switched, ideal switches simulate properly without a gate source resistance. Figure 4.10 details the gate drive sub model.

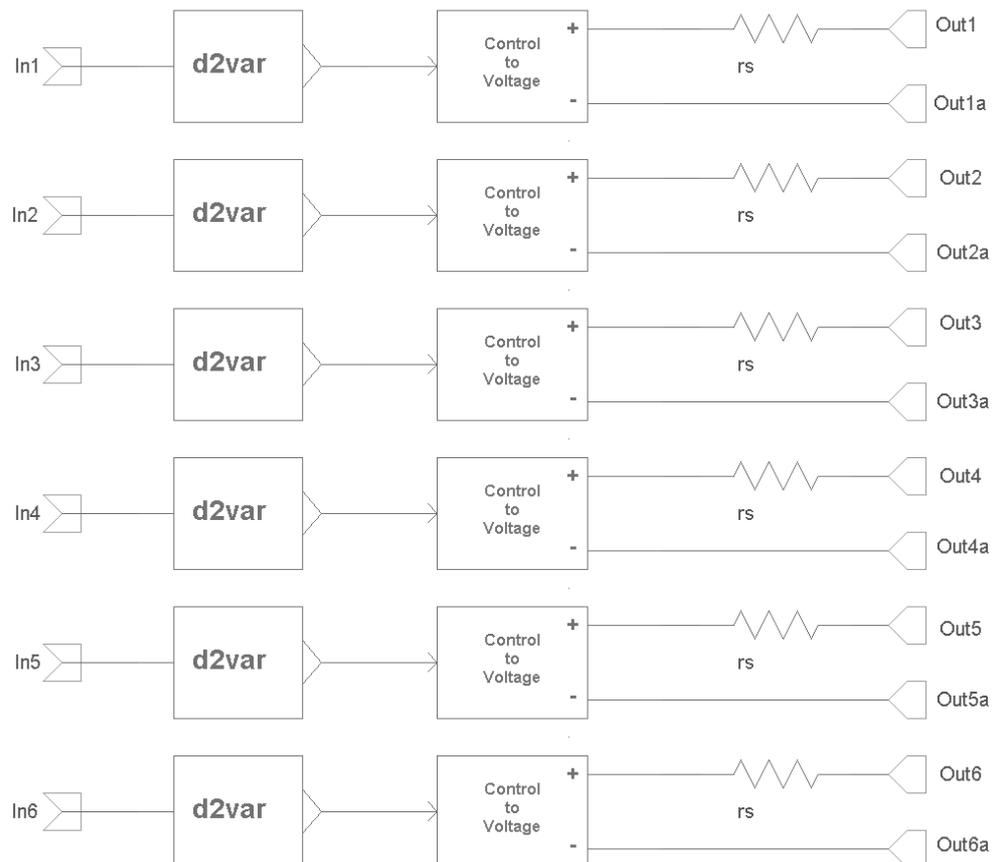


Fig. 4.10 Gate drive sub model implementation.

4.4.8 System Models

Figure 4.11 details the full model for the VSI simulation. Measurement systems have been included in the model to allow automatic computation of the predicted mechanical power output, using Equation (3.1a). Figure 4.12 details the full model for the CSI simulation.

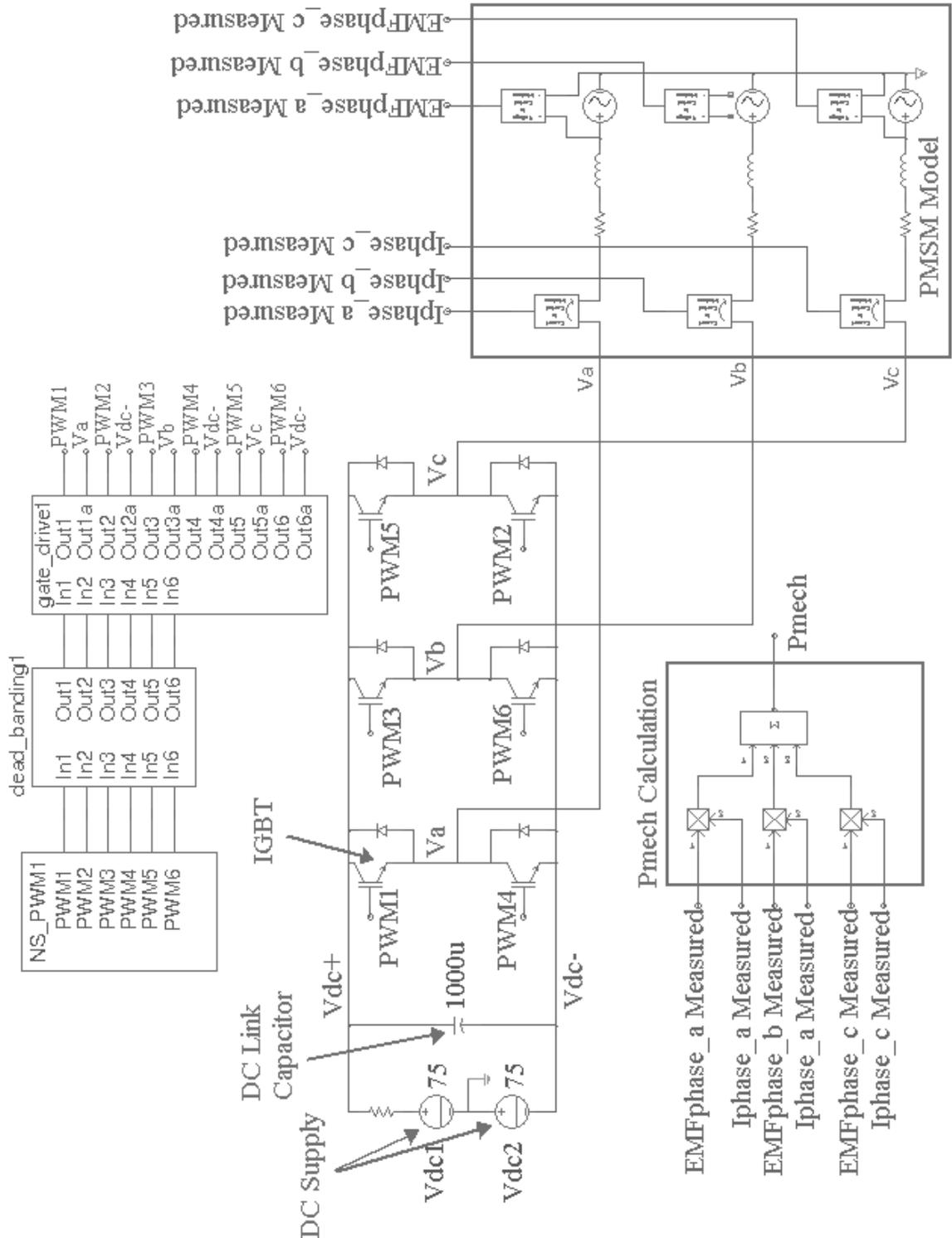


Fig. 4.11 VSI system simulation schematic.

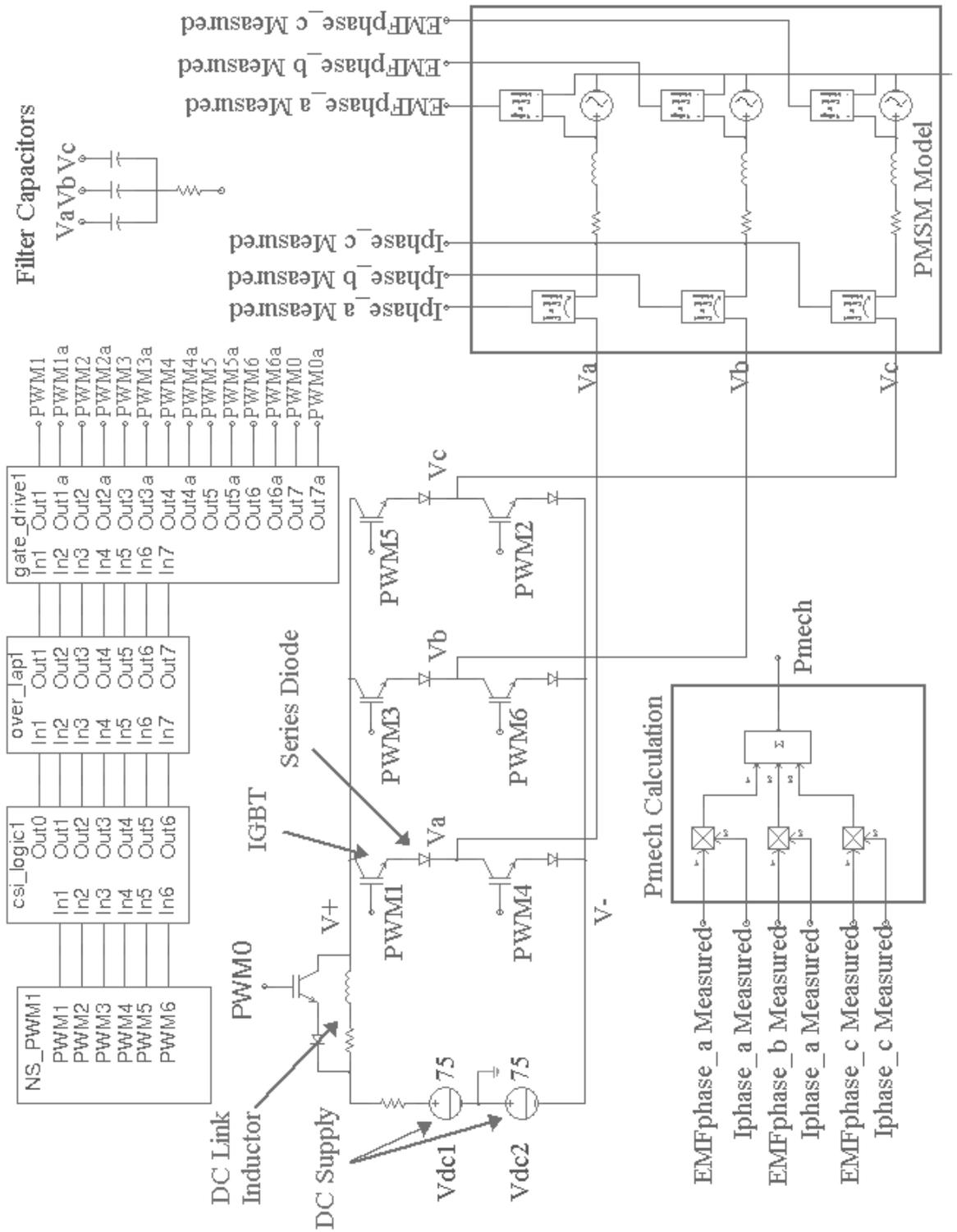


Fig. 4.12 CSI system simulation schematic.

4.4.9 Simulation Issues

When testing the CSI simulation, several problems were discovered. Firstly, the filter capacitors for the CSI system produced errors as soon as they were introduced. The problem was a floating reference at the star point, this created an equation that SABER™ could not solve. The only solution was to include a large, 10MΩ, resistor, connecting the capacitor star point to the PMSM star point. The problem of the floating reference was also encountered with the PMSM model, although there was an option of using another reference point to solve this problem. Once the additional reference had been used, no more were available for solving other reference issues.

Although the SABER™ package solves VSI systems well, with results matching closely with analytic and experimental system, simulating CSI systems is not straight forward. The CSI model is very sensitive to operating point; voltages, phase angles, modulation index etc, a small change often results in a failure to solve the circuit problem. Two different simulation errors are often encountered when simulating CSI systems;

- Failure to solve the equations, i.e. the inability to solve one or more of the equations that represent a node or loop; and
- Failure of the iterative routines to converge on a valid answer.

The suggested method for overcoming the ‘failure to solve’ error is to remove voltage sources and inductors in parallel. Given the nature of the CSI topology and the PMSM this is not an appropriate solution. When the equations fail to solve there are a few options for adjusting parameters in an attempt to achieve a successful simulation: reducing the simulation time-step beyond a setting that the circuit may be expected to require, can have positive results. However, below a certain value further reduction is detrimental to the outcome. Another option is to set initial conditions with inductors and capacitors. This can help, but care must be taken when assigning a value, especially with polarity. Even the initial conditions can be sensitive to change, it has been witnessed that changing the current in the DC link inductor by 10mA can result in simulation failure.

To overcome the convergence error, there are two options; reduce the model complexity or increase the maximum number of iterations. Adjustment of the number of iterations has a dramatic affect on the simulation time, and even small increases in the number of iterations can result in the simulation requiring well in excess of one hour to simulate 100ms. The

results file created by such a simulation often spans many gigabytes of information, causing problems viewing and manipulating the results.

4.5 Simulation Study

Simulations have been performed to gain an understanding of the waveforms to expect when operating the hardware rig. Simulation of the VSI system will provide a basis for comparison, allowing the simulated performance of the CSI to be compared against the simulated performance of the VSI. A comparison of the simulated to actual performance of the VSI will give an indication of any differences between these results.

To simulate the loading parameters of the CESAR specifications, please see Chapter 2, the simulation and hardware test will be operated at full speed and the performance of the system evaluated at the 0, 0.25, 0.5, 0.75 and 1 p.u. operating points. This will demonstrate the performance of the VSI and CSI systems on the far edge of the torque-speed characteristic, see Figure 4.13. The no load operating point has arbitrarily been chosen to be an operating point 0.05 p.u. This should account for the power required to rotate the PMSM and dynamometer. Losses will be estimated for both the DC to AC power conversion and the electrical to mechanical power conversion. All measurements, for the purpose of power estimation have been taken over two cycles of the output fundamental.

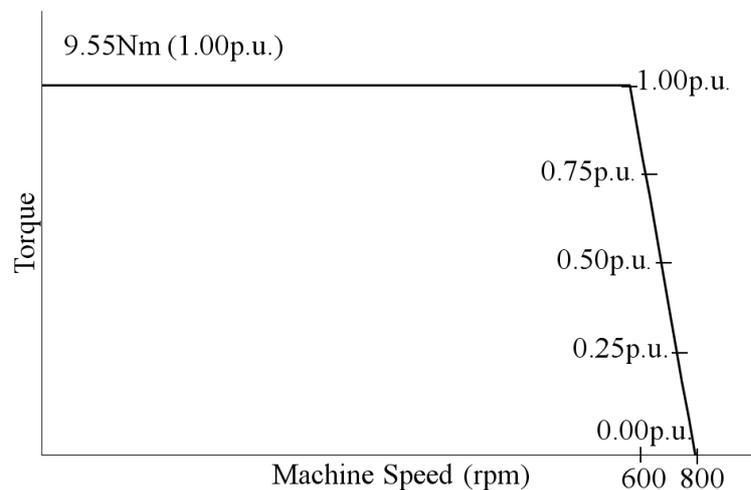
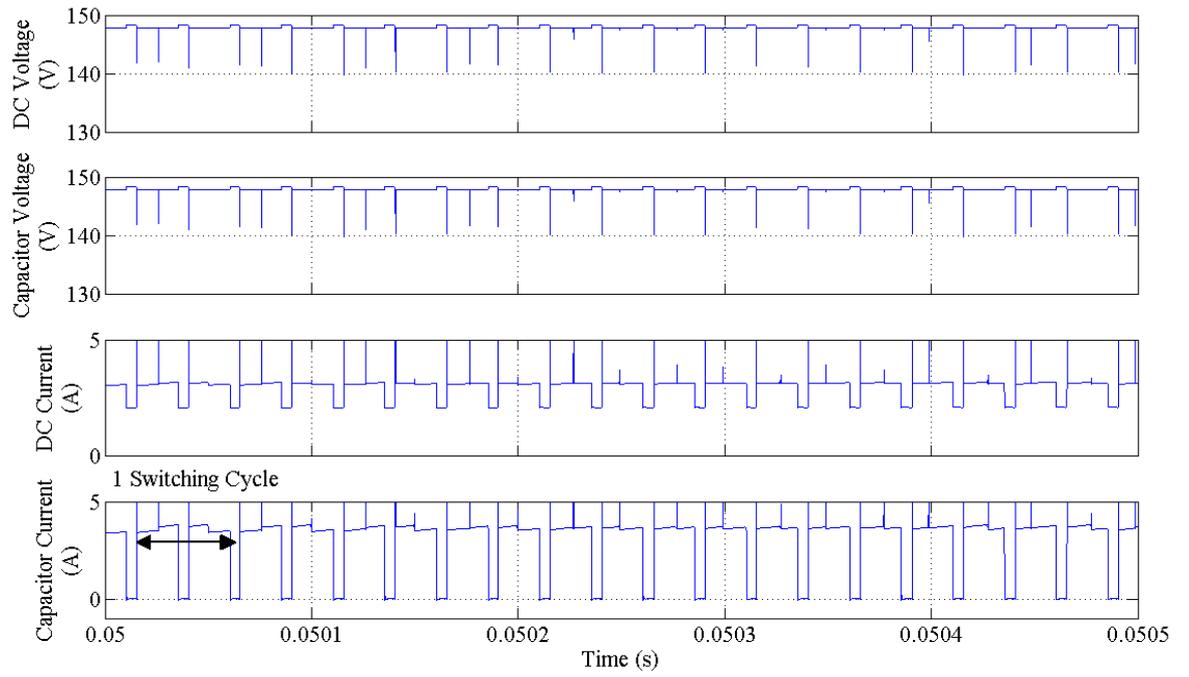


Fig. 4.13 Machine torque-speed characteristic used through the studies.

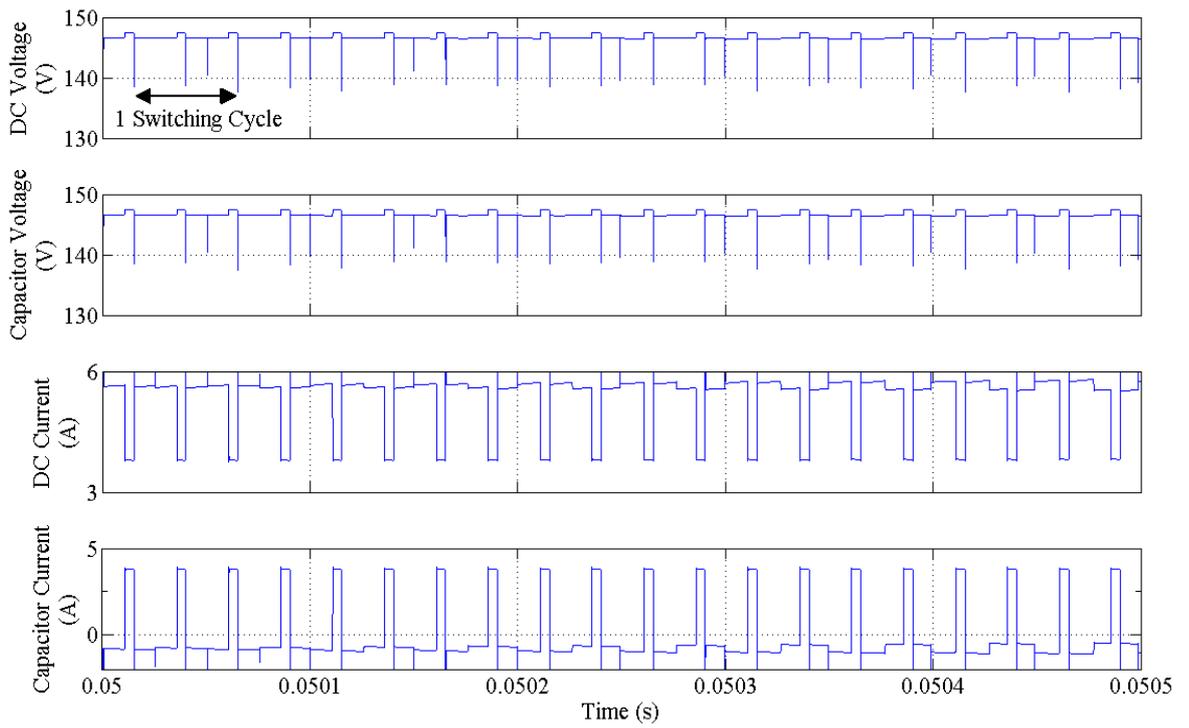
4.5.1 VSI Results

Figures 4.14 to 4.16 detail the DC link, motor phase and magnified PMSM phase waveforms respectively at the load points 0.5 p.u. and 1 p.u. The waveforms are representative of a standard six-step, space-vector PWM VSI. The DC link current waveforms, Figure 4.14, show very short transients of a very large magnitude. This is due to the limitations of the model. The DC current waveforms on the hardware system are expected to be of longer duration and lower magnitude. This will be demonstrated in Chapter 5 and comparisons between simulated and measured results will also be made in Chapter 5. The results give confidence that the results from the CSI simulation will be closely related to the performance of the hardware test rig.

Table 4.8 summarizes the results for the VSI simulations. Measurements have been taken over two output cycles, while the DC and power measurements have been averaged over the same cycles.

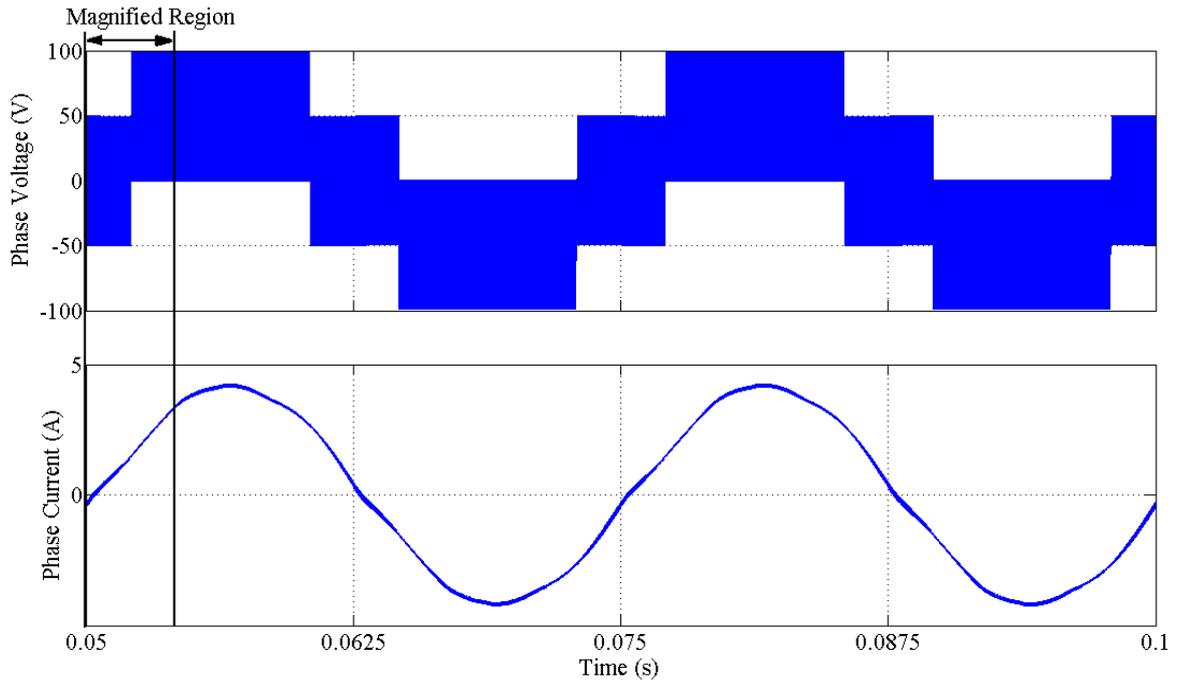


(a) 0.5 p.u. operating point.

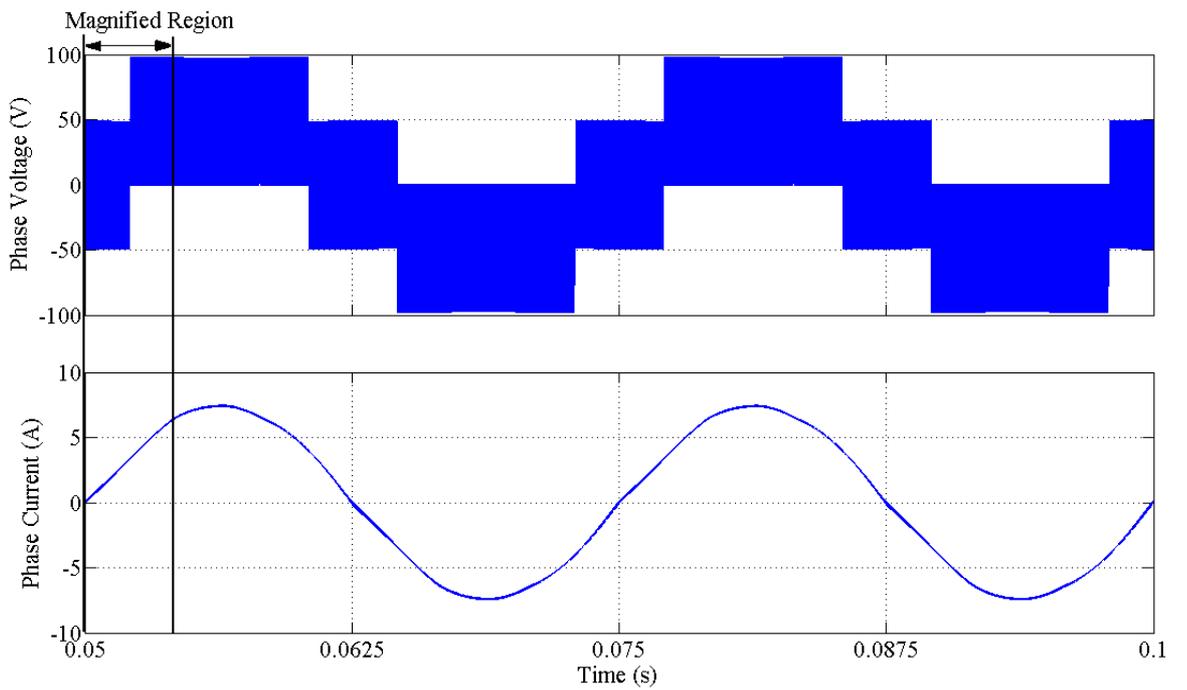


(b) 1 p.u. operating point.

Fig. 4.14 VSI DC link waveforms.

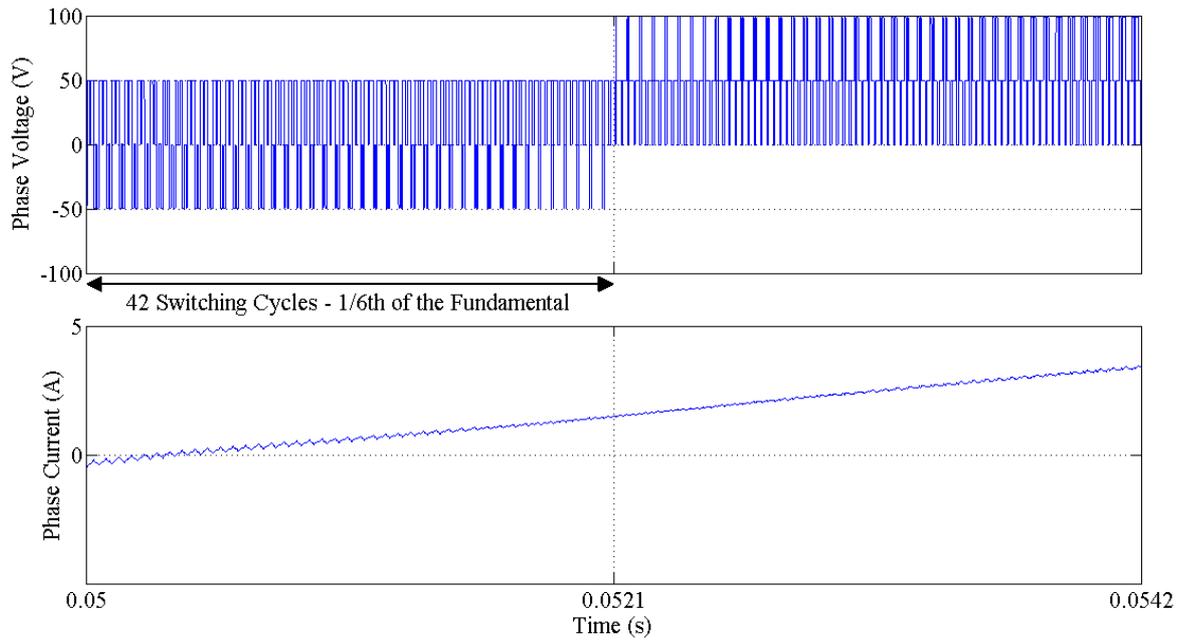


(a) 0.5 p.u. operating point.

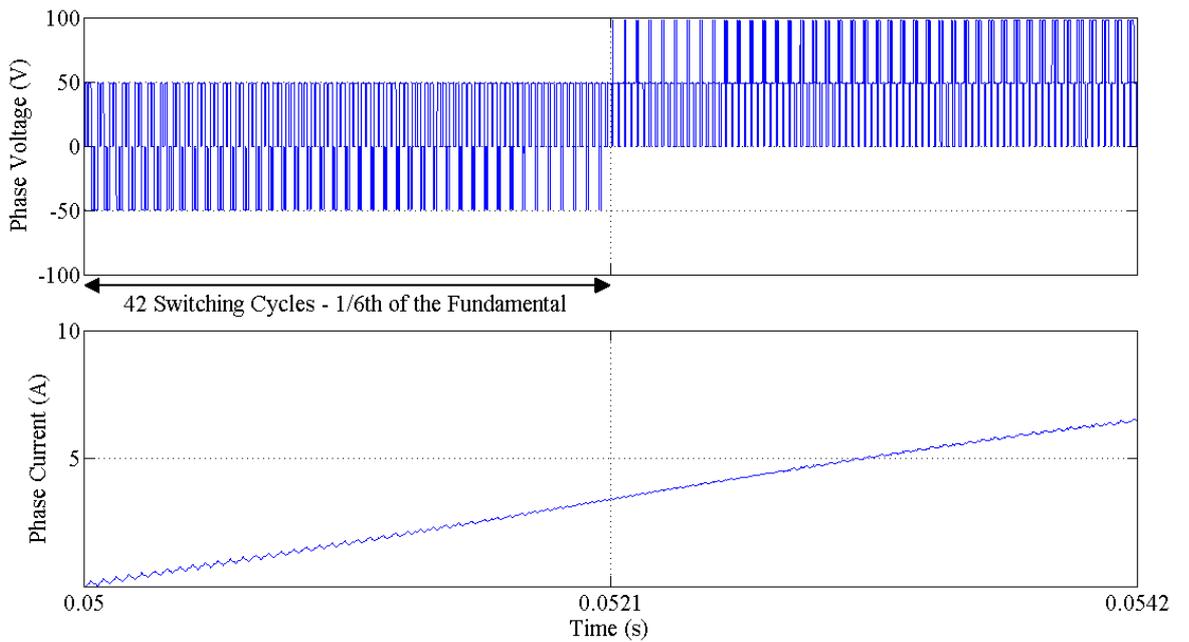


(b) 1 p.u. operating point.

Fig. 4.15 VSI voltage and current phase waveforms; 2 cycles of the fundamental.



(a) 0.5 p.u. operating point.



(b) 1 p.u. operating point.

Fig. 4.16 VSI voltage and current phase waveforms; magnified region from Fig 4.15.

Load (%)	V_{dc} (V)	I_{dc} (A)	P_{dc} (W)	V_{rms} (V)	I_{rms} (A)	P_{elec} (W)	P_{mech} (W)	η ($P_{dc}:P_{elec}$) (%)	η ($P_{elec}:P_{mech}$) (%)
0	149.36	0.30	44.54	59.39	0.27	42.25	41.87	94.9	99.2
25	149.34	1.46	218.1	60.07	1.48	207.88	202.79	95.3	97.6
50	149.32	3.01	449.24	60.73	2.95	420.11	401.04	93.5	95.5
75	149.30	4.65	697.37	61.7	4.52	655.29	612.32	94.0	93.4
100	146.69	6.26	919.12	61.0	5.25	865.65	793.78	94.2	91.7

Table 4.8 Simulated VSI results summary.

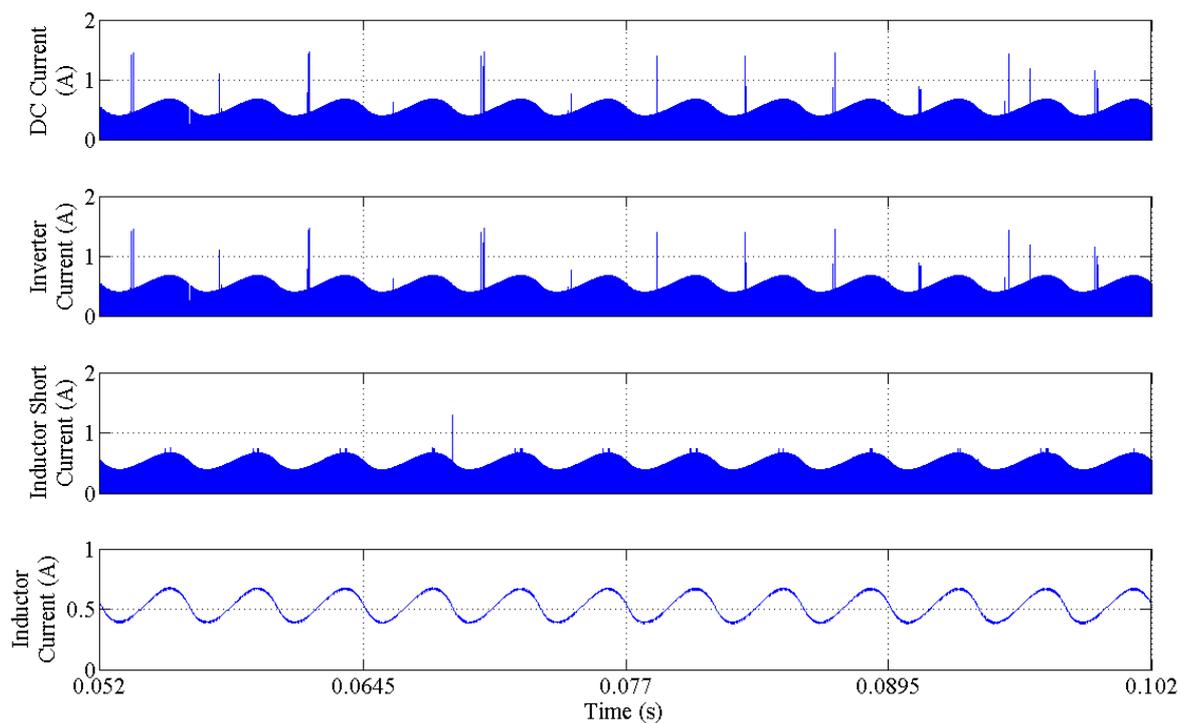
The tabulated results confirm the VSI model is representative, when compared with similar published material on VSI operational waveforms. The efficiency of the system is high, although it should correlate with the hardware system close to the margin of error.

4.5.2 CSI Results

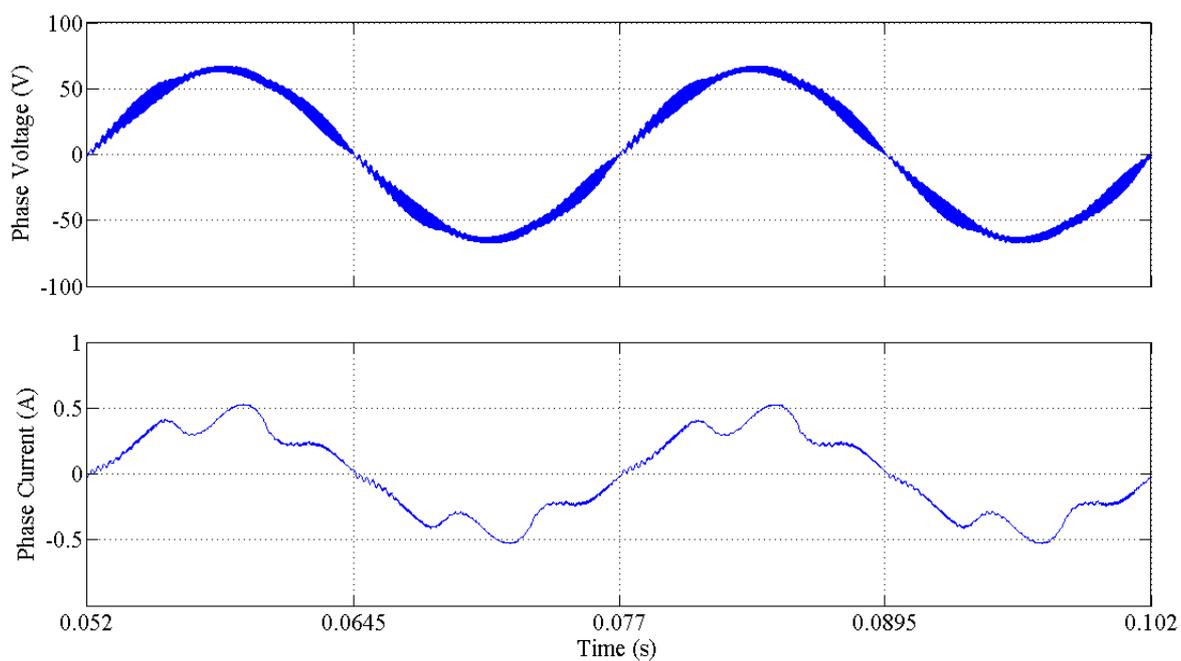
Figures 4.17 to 4.20 detail the DC and PMSM phase waveforms for the operating points at no load, 0.25 p.u., 0.5 p.u., 0.75 p.u. and 1 p.u. respectively. At the no load operating point, Figure 4.17, there is significant distortion in the phase current. This is due to the magnitude of the phase current being small compared to the current ripple. At higher power levels this would be expected to become insignificant, as is shown in Figures 4.18 to 4.20. The harmonic content of the load points, with the exception of no load, was found to be low. Figures 4.17 to 4.20 also show that the voltage waveform for a CSI does not have the same six-step envelope as the VSI, although it can be clearly seen that there are six distinct sectors within each fundamental period, as is the case with the VSI. In Figure 4.14 the inductor current ripple can be seen to be significant compared to the magnitude of the current, in the same way that the phase current ripple is significant.

Figures 4.21 and 4.22 detail the DC link currents over a small time period. The high frequency switching of the current can clearly be seen in all but the inductor current. This is as expected in a CSI system. The high frequency switched currents show very idealised waveforms. In the hardware rig it would be expected that the current rise and fall would occur over a longer period and that the peaks and troughs would be reduced. This will be

demonstrated in Chapter 5. The results presented give confidence of the operation of the CSI hardware system in Chapter 5.

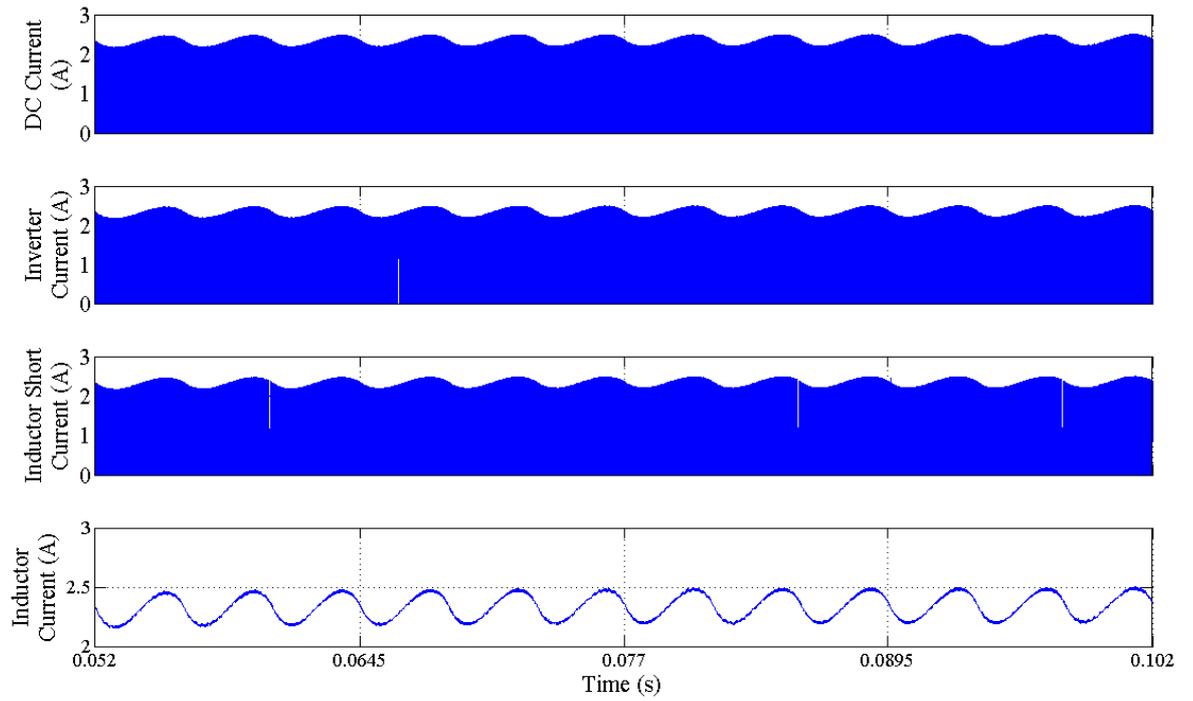


(a) DC link waveforms.

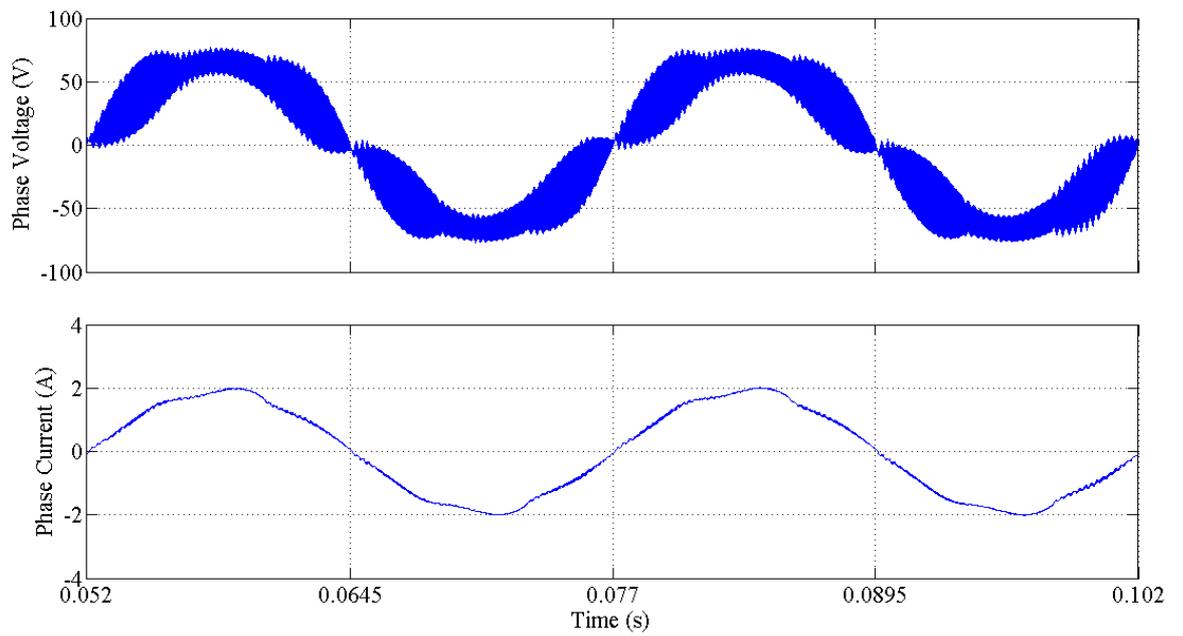


(b) PMSM phase voltage and current.

Fig. 4.17 CSI Waveform overview; 2 cycles of the fundamental, no load operating point.

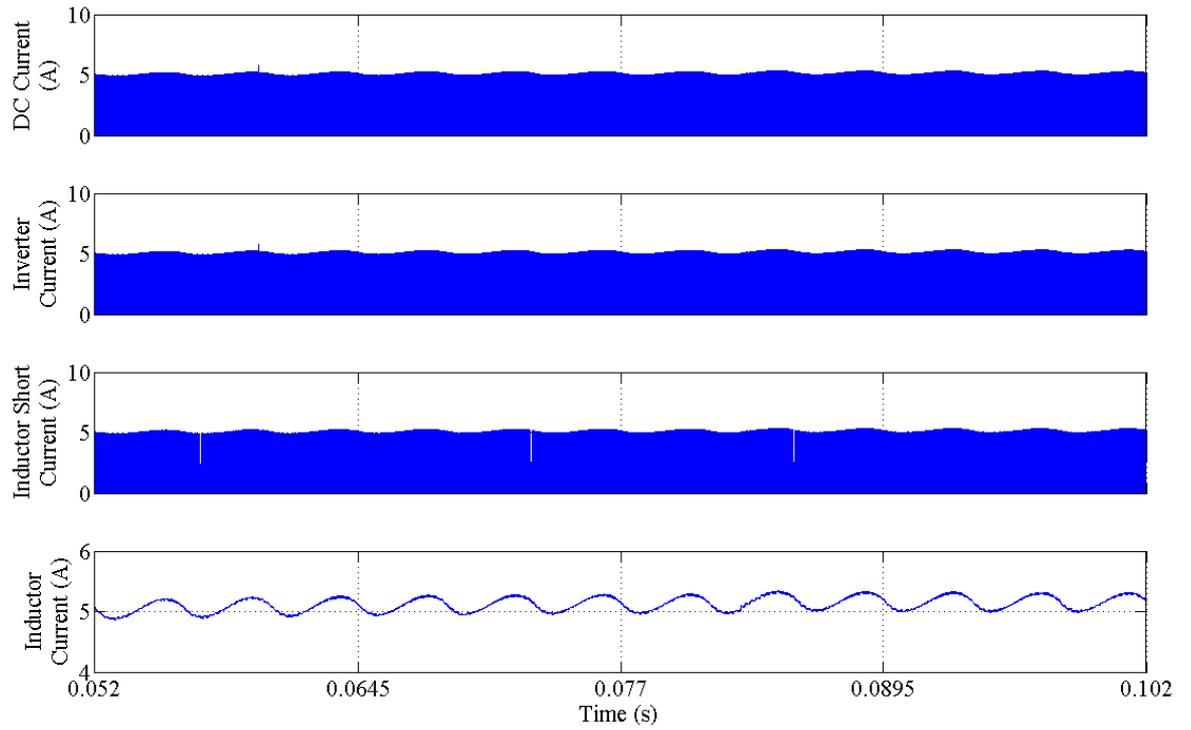


(a) DC link waveforms.

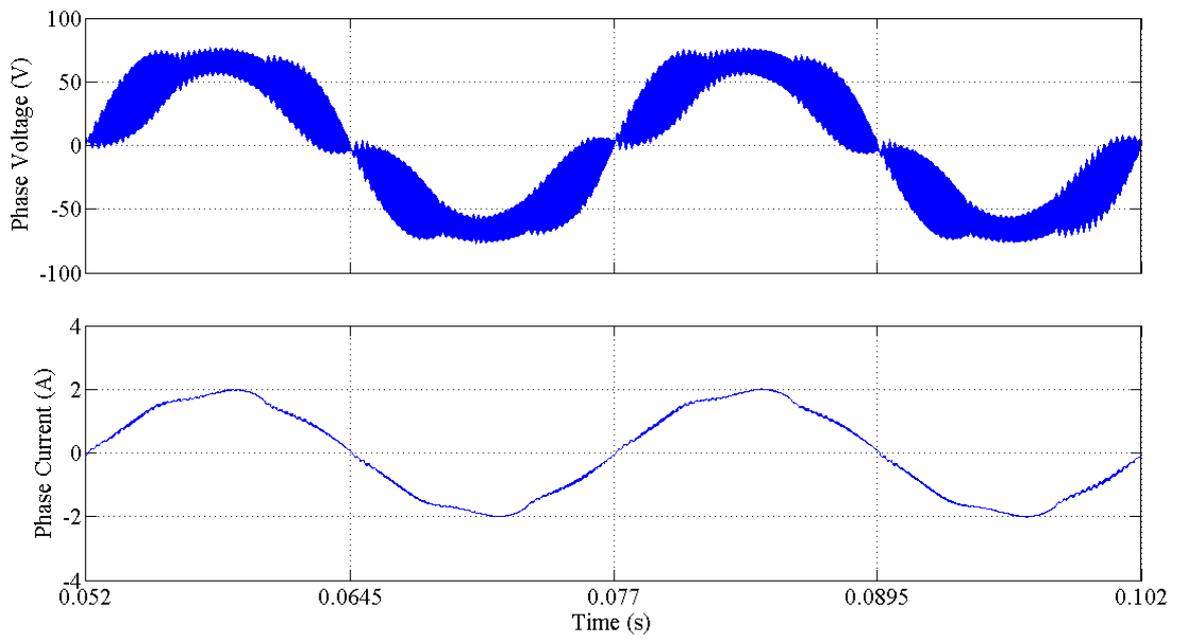


(b) PMSM phase voltage and current.

Fig. 4.18 CSI Waveform overview; 2 cycles of the fundamental, 0.25 p.u. operating point.

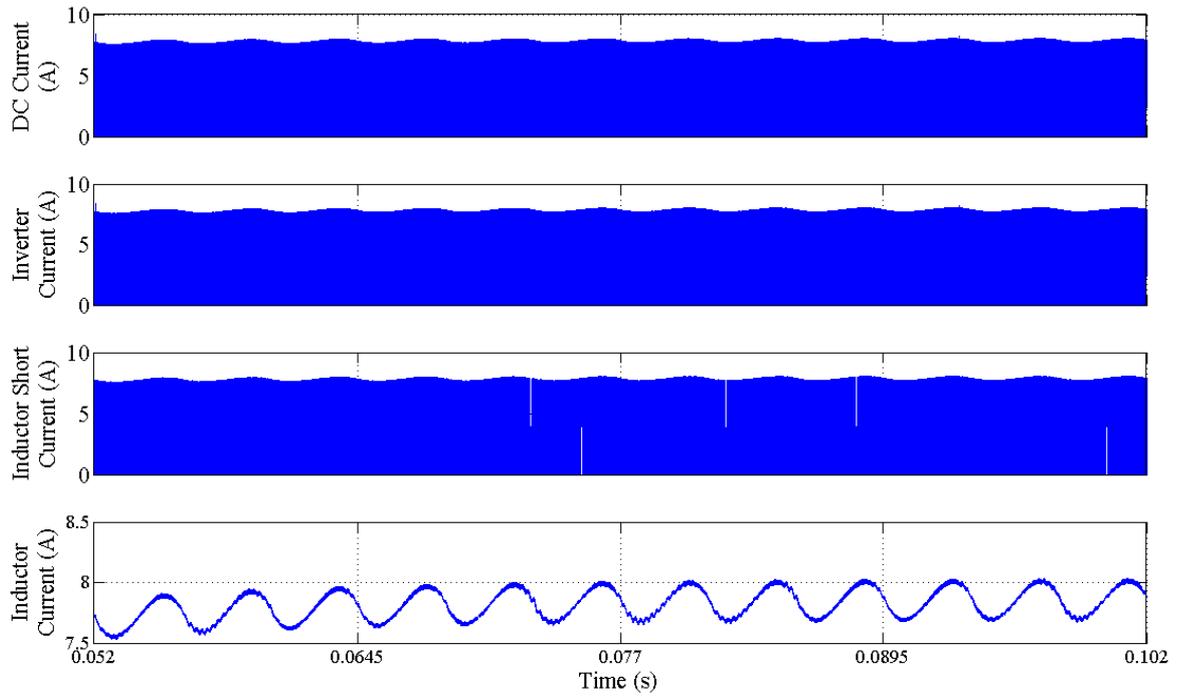


(a) DC link waveforms.

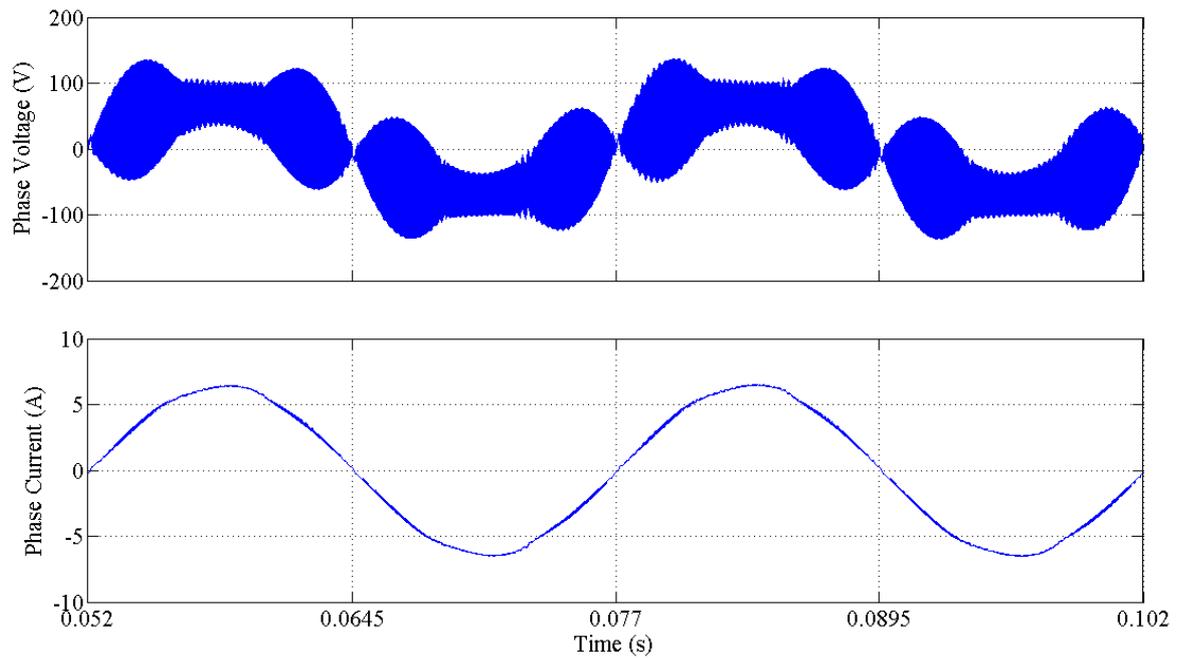


(b) PMSM phase voltage and current.

Fig. 4.19 CSI Waveform overview ; 2 cycles of the fundamental, 0.5 p.u. operating point.

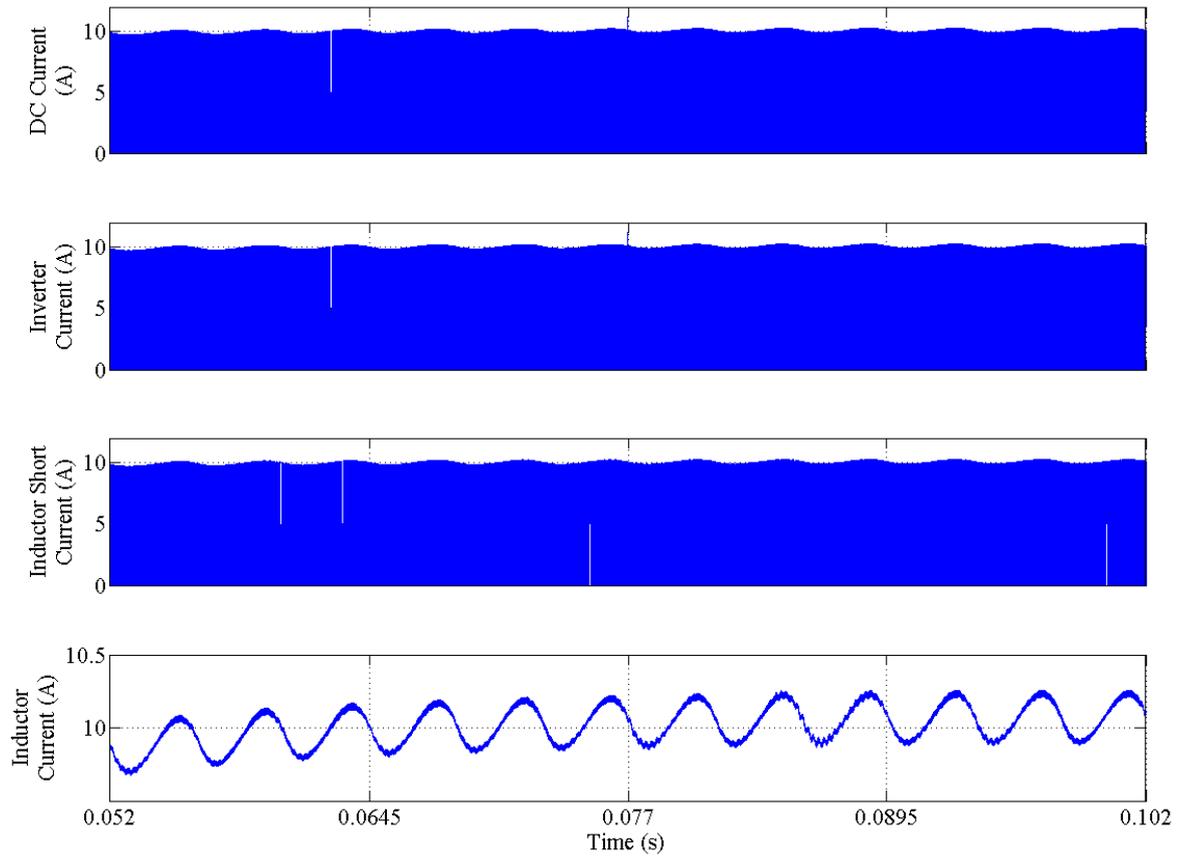


(a) DC link waveforms.

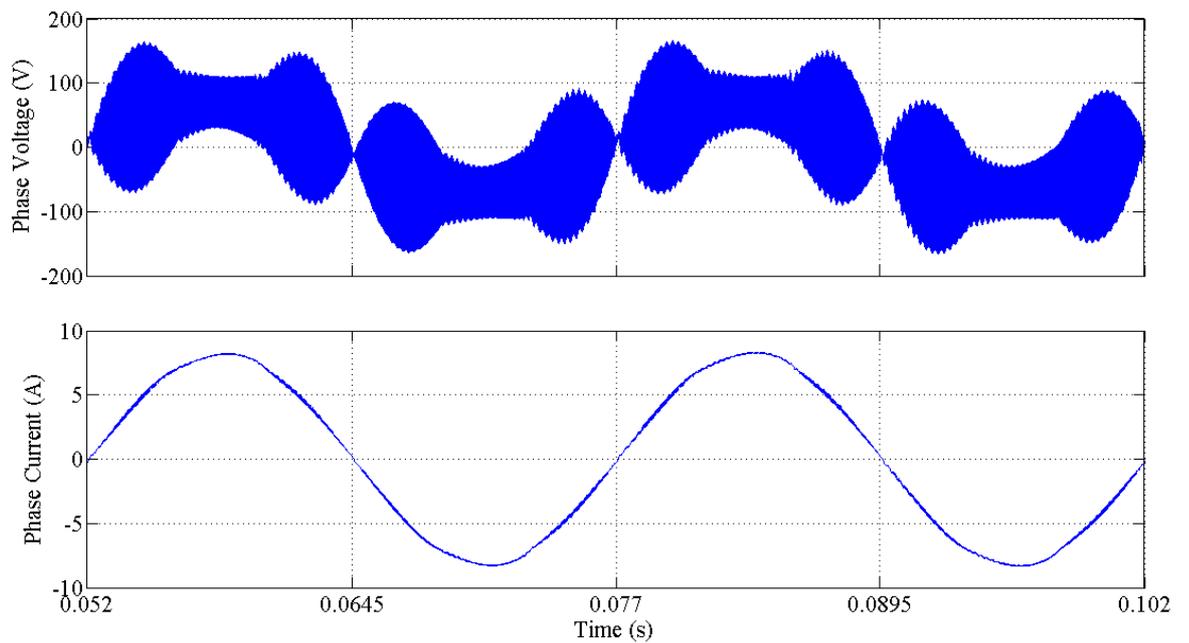


(b) PMSM phase voltage and current.

Fig. 4.20 CSI Waveform overview; 2 cycles of the fundamental, 0.75 p.u. operating point.

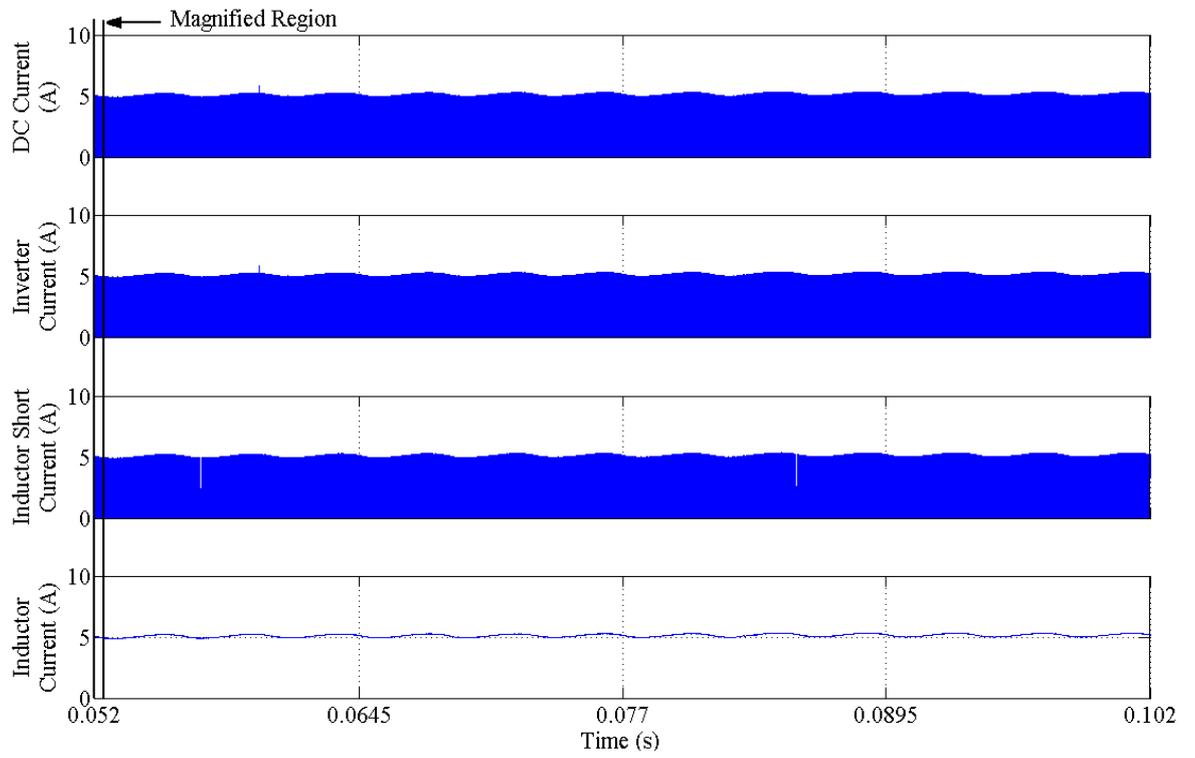


(a) DC link waveforms.

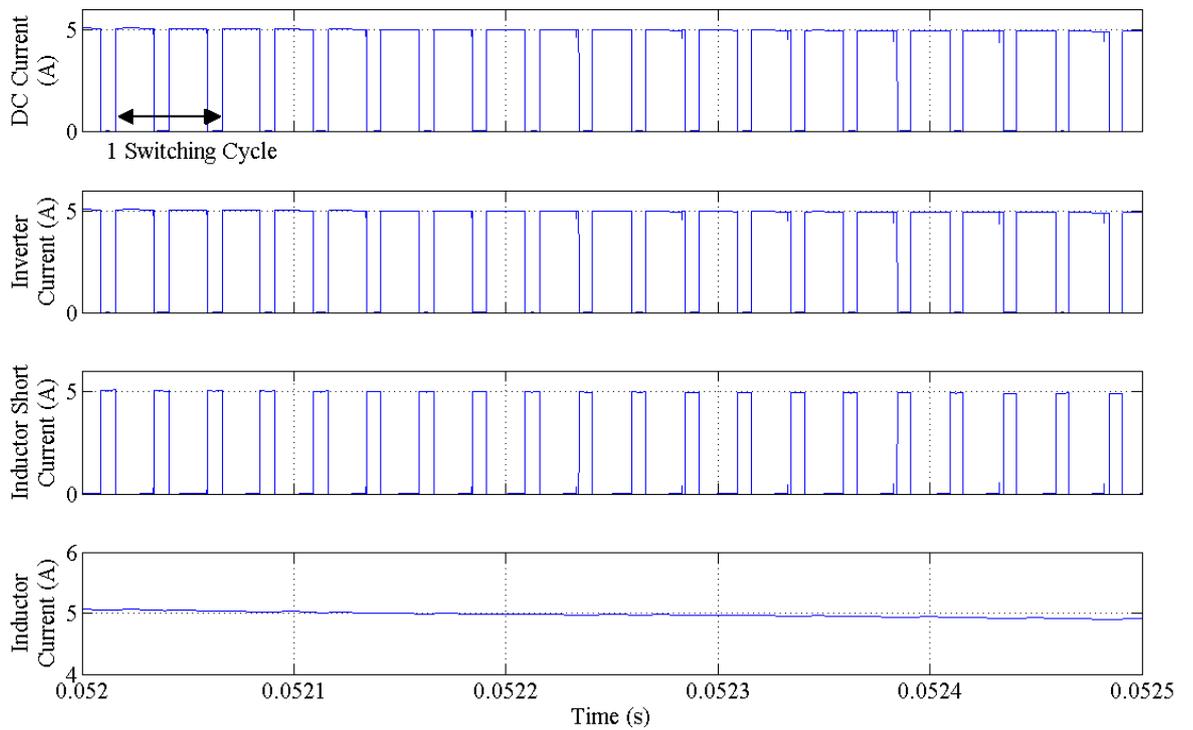


(b) PMSM phase voltage and current.

Fig. 4.21 CSI Waveform overview; 2 cycles of the fundamental, 1 p.u. operating point.

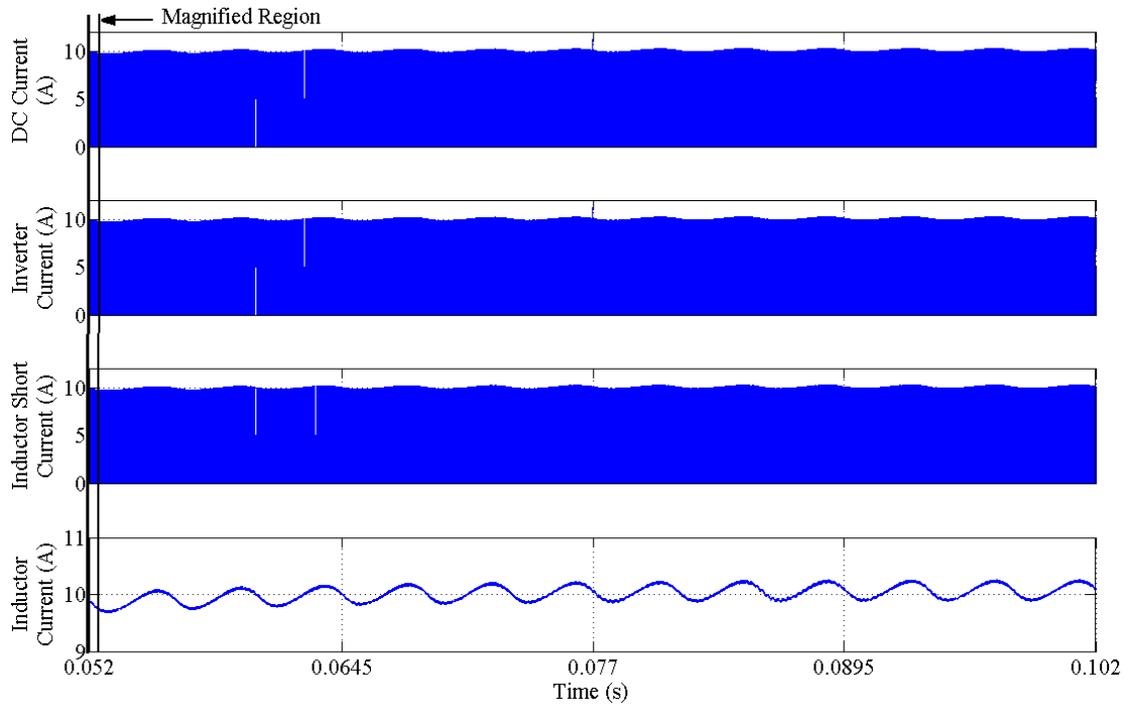


(a) Two cycles of the fundamental.

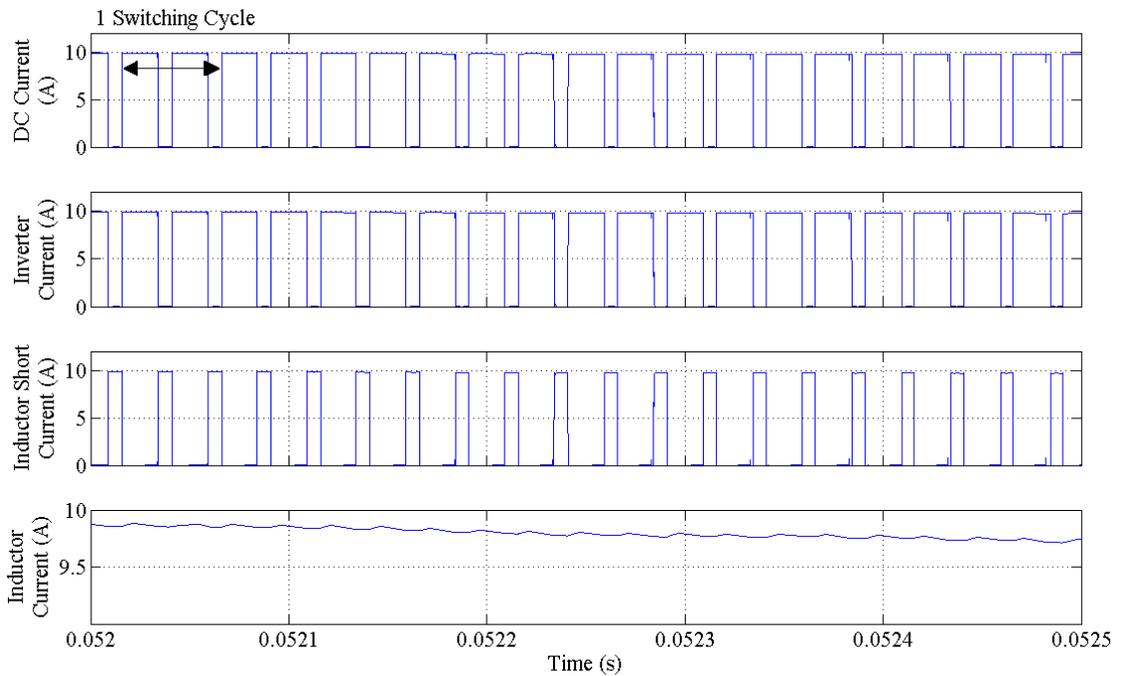


(b) Magnified region from (a).

Fig. 4.22 CSI DC link waveforms; 2 cycles of the fundamental, at 0.5 p.u. operating point.



(a) Two cycles of the fundamental.



(b) Magnified region from (a).

Fig. 4.23 CSI DC link waveforms; 2 cycles of the fundamental, at 1 p.u. operating point.

Table 4.9 summarizes the results for the CSI simulations. Measurements have been taken over two output cycles, while the DC and power measurements have been averaged over the same cycles.

Load (%)	V_{dc} (V)	I_{dc} (A)	P_{dc} (W)	V_{rms} (V)	I_{rms} (A)	P_{elec} (W)	P_{mech} (W)	η ($P_{dc}:P_{elec}$) (%)	η ($P_{elec}:P_{mech}$) (%)
0	109.82	0.42	42.73	45.54	0.31	41.44	41.23	96.98	99.49
25	114.56	1.84	195.56	47.42	1.36	188.7	184.7	96.49	97.88
50	119.62	4.04	450.11	52.62	2.98	424.22	404.75	94.25	95.41
75	124.94	6.15	717.85	59.66	4.55	662.45	617.14	92.28	93.16
100	127.97	7.87	952.1	64.2	5.44	864.66	790.32	90.82	91.40

Table 4.9 Simulated CSI results summary.

The tabulated results show that the efficiency of the CSI, although lower in most cases, is not significantly lower than the VSI. The reduction in efficiency as the load increases is to be expected due to the copper loss of the inductor. The limitations of the model are likely to result in lower efficiency than predicted, especially at high load conditions where current magnitude is high.

4.6 Summary

The VSI model has been used to simulate the example PMSM discussed in Chapter 3, to gain confidence in the software tool, circuit components and the parameter values. The VSI results are typical of published VSI drives implementing space vector PWM. The validity of both the VSI and CSI simulations will be presented in Chapter 5.

Simulation models of the VSI and CSI systems have been created using the SABER™ software package. The VSI simulation can now be used as a benchmark for the comparison of simulated to measured results, presented in Chapter 5, for both the VSI and CSI systems. A software model for MCSI-SV-PWM, presented in Chapter 2, has been created and tested from the limited literature on CSI PWM switching. It has subsequently been used to simulate the CSI drive system, and the CSI output waveforms have been observed to verify the operating characteristics of the CSI system against published results. The tabulated results for the VSI and CSI systems suggest that the inverter efficiency is higher for the VSI system than that of the CSI. However, the voltage and current waveforms in the PMSM and the predicted electrical-to-mechanical power conversion suggests that the two topologies are comparable in terms of machine performance. The software package appears to be sensitive to the operating parameters of the CSI and the mathematical parameters of the iterative routines used, but once a stable combination is found, the simulation appears to produce valid results.

CHAPTER 5

HARDWARE DESIGN, BUILD AND VALIDATION

5.1 Introduction

The preceding Chapters 2-4 have discussed the switching, losses and detailed simulation of VSI and CSI drive systems. This chapter aims to provide test validation of these studies via the design, build and test of comparative VSI and CSI systems.

5.2 Hardware

The hardware will consist of many modules including; programmable controller and external interface, Power Electronic Module (PEM), gate drive circuits, measurement transducers and signal conditioning, driven machine and a load machine. Each module requires designing and/or interfacing to the other modules. The entire system will be designed to allow switching from a VSI system to a CSI system with a minimum of hardware changes. An overview is detailed in Figure 5.1. Changing from VSI to CSI will require swapping the PEM, reconfiguring the control algorithm (changing the program to a CSI version), reconfiguring the signal routing on the interface board and connection of any required DC link voltage a current measurements. The computer (PC) interface is used to manage start-up and control of the system via the debugging interface of the controller. It is possible for the system to be run autonomously, however, the PC allows nearly-real time monitoring of the system status and computed values, as well as control of the system, greatly improving the flexibility of the system.

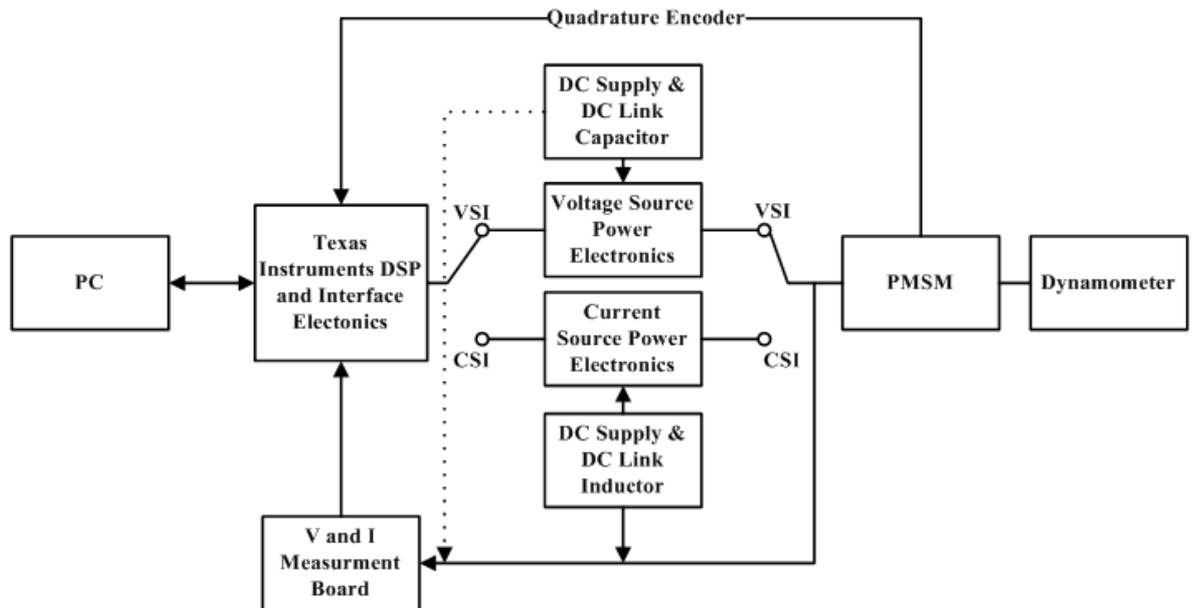


Fig. 5.1 Overview of the VSI-CSI hardware.

5.2.1 Control System

The chosen control system is a Texas Instruments (TI) C2000 series 32bit Digital Signal Processor (DSP) in the form of a development kit, referred to by TI as an eZdsp.

A DSP is a type of microprocessor, designed to process data in real time [62]. Peripherals are incorporated into the DSP to increase the performance of the device for certain tasks. The DSP will include a CPU, memory and peripherals. The CPU consists of math components, logical components along with the usual array of cache memory and registers. The memory will include RAM and ROM and possibly flash memory for semi-permanent storage of the program to be executed. The peripherals will be application specific, allowing the DSP to perform common tasks without the need to interface with and control external hardware. This will improve the speed and size of the entire control system and allows the device to be marketed as a single device solution. Peripherals for motor control and power conversion systems usually include, but are not limited to; PWM, Analogue to Digital Conversion (ADC) and communications systems. These peripherals are designed to be semi-autonomous, requiring initial configuration by software and then servicing, such as result collection, as the control algorithm requires.

The eZdsp is a fully functional system incorporating power management, clocking signals and programming/debugging interface. It comes ready to connect to a motor control (or similar) system to allow familiarisation and design testing. The C2000 DSP has many

The hardware PWM allows the operation of the PWM outputs to be independent of the control software, removing the need for critical timing within the software. The principle is based upon a symmetric triangular wave. A hardware counter is configured to be incremented by an internal clock signal. The combination of the configured maximum value and the clock frequency determines the duration of half the PWM period, $T/2$. On reaching the maximum value the counter changes direction and a count down begins, back to zero. This creates a symmetric triangular waveform at the switching frequency, F_s . Hardware compare units are used to change the state of outputs when the counter values crosses the value set in the compare unit, in both the up and down direction. These outputs are the PWM signals. Three compare units, one for each phase, are programmed, by the software control loop with the value for the next PWM period. A buffering system allows the automatic transfer of this value from a buffer to the active value each time the counter reaches zero. The buffering allows the software to act independently of the PWM, provided the new values are calculated before the next PWM period, i.e. the next set of compare values takes less than one PWM period to calculate. Figure 5.3 details the triangular wave generated by the counter, the switching events taking place when the compare units trigger and the resulting vector outputs.

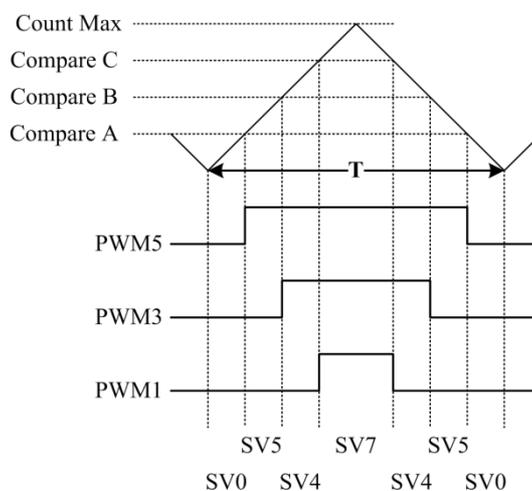


Fig. 5.3 Hardware PWM operation.

The signals for PWM2, PWM4 and PWM6 are created at the same time as PWM1, PWM3 and PWM5, as complement signals. All signals can optionally be configured with dead-banding.

The hardware analogue to digital converter does not have the speed and accuracy of some dedicated devices, it is designed to be more than adequate for motor control and power

conversion systems and allow minimal software intervention for its correct operation, freeing the CPU within the DSP to execute the control algorithm. The C2000 ADC hardware is a 16 channel, 12bit single conversion module, i.e. it uses a single analogue to digital module and a 16 channel multiplex to function as a multichannel ADC. The configurable hardware allows the ADC to run a sequence of conversions without the need for servicing by the CPU, allowing the DSP to freely execute the control algorithm and fetch the ADC results when necessary. Using a more advanced, external ADC, it would be possible to capture more accurate conversions; this however would require connecting the ADC via a communication channel that would require servicing by the CPU on receipt of each result. This would greatly increase the operations required by the CPU and, unless accurately timed and controlled, the arrival of a new result could interrupt the calculation of the next PWM cycle switching points, causing switching faults.

The hardware quadrature encoder allows the calculation of the rotor position with a minimum of complexity; the A and B signals are transformed into a single clock signal and direction flag. The clock signal is used to drive a hardware counter, with the Index signal triggering the control software to reset the counter on each revolution, a simple and fast operation. Using the counter value, direction flag and the encoder properties, the software can easily calculate the speed, position and direction of the motor.

The C2000 DSP uses 3.3V (5V intolerant) for all external interfaces, whereas, it is common for gate drive interfaces to use a 5V system, such as the Powerex VLA500 Integrated Power Supply and Drive unit or the Powerex BP7B IPM Power Supply and Interface unit. A choice of 3.3V would appear to be far from ideal for motor control. TI detail the decision in an Application Report [64], summarising, the operating voltage is the result of a shrink in the integrated circuit manufacture process, smaller transistors result in higher performance, lower energy usage and small packages, it also results in a reduction in the insulation value used within the integrated circuit. This makes it necessary to reduce the operating voltage. Common peripherals (communications, speed/position) are often available in 3.3V options and level conversion systems are easily implemented when compatible systems are not available.

5.2.2 Gate Drive Circuits

Gate drive circuits for VSI systems usually consist of four isolated power supplies with six switched outputs. Four power supplies are required as the voltage is applied across the

gate-emitter terminals. For switches 1, 3 and 5, the emitter is connected to the inverter output terminal (a, b or c). Failure to isolate the power supplies for these switches would result in shorting the inverter output through the gate drive power supply, therefore an individually isolated supply is required each switch (1, 3, 5). Switches 2, 4 and 6 have the emitter terminals connected to the negative of the DC link and therefore do not require to be isolated from each other. They do, however, need isolating from switches 1, 3 and 5. On a CSI system there are no common connections for the switches, therefore individually isolated supplies are required for all switches. The isolation level is usually several kV, even for 600V systems. This is to prevent failure during switching faults.

The use of the same IGBTs for both the VSI and CSI system allows the use of the same gate drive system. This results in the gate drive circuitry for the VSI system being larger than a standard gate drive system. However, it ensures that active signal polarity is maintained the same for the both the VSI and CSI system. Gate drive circuits can either be ‘active high’ or ‘active low’, with a high logic signal or low logic signal, respectively, used to set the gate drive output high (on). The selection of the polarity of the active signal is by the gate drive manufacturer and is sometimes used to implement failsafe control, i.e. ensure that the lack of a signal (control failure) is not confused with a signal state that could result in a switching event leading to a fault. Utilising the same gate drive system ensures that no adjustments are required when changing from the VSI to CSI system and vice-versa. It also helps keep the costs of the system down.

The JGPL MT24 gate drive circuit has been selected. Each unit consists of a pair of independent, isolated gate drive circuits. They incorporate short-circuit sensing, protection and indication, as well as negative turn off of the IGBTs. The negative turn off capability drives the gate terminal negative with respect to the emitter, ensuring the device is turned off, instead of assuming a zero volt bias on the gate-emitter junction will result in the expected turn off characteristics, for example, fully off in the specified time.

The gate drive circuit application notes and circuit diagrams are included in the Dual Topology Test Rig Manual [65], the details of which are in Appendix A.

5.2.3 Measurements

A low cost system is required to allow the ADC within the DSP measure the appropriate parameters for motor control, the minimum requirements are:

- Two phase currents.
- Bandwidth in excess of the 20kHz (chosen to be above the natural audible range) control loop of the DSP. A higher bandwidth on the measurement system will ensure the system can provide measurements as fast as the DSP can process them.
- 0-3V signals for interfacing with the ADC, including a 1.5V offset for bipolar signals.

The system should also be flexible enough to allow current and future development of the motor control system, useful features for consideration are:

- Voltage measurement for system status, startup/shutdown routines and future work.
- Configurable measurements to allow the use with a range of currents and voltages.

To keep the costs to a minimum, widely available, industry standard transducers and signal conditioning circuits have been chosen.

The configuration of the ADC, incorporation of the offset for bi-polar signals and scaling of the measurement result, 12-bit to 16-bit (for efficient usage of the 32 bit memory locations), results in the possibility of performing the measurement circuit calibration within the DSP software. Therefore it was decided to use a signal conditioning system with fixed values for amplification/attenuation, reducing the complexity of the system.

The LEM LA 55-P has been selected for the current measurement, it is a widely available hall-effect transducer designed for power converters and similar systems, features include:

- 50A_{rms} maximum current.
- 200kHz bandwidth
- 2.5kV isolation.

The large current range, although far in excess of that required for a 1kW system, has been chosen due to its extensive availability, and therefore, competitive price. It will allow the use of the transducer in many systems and through the use of additional turns around the sensor coil, the current range can be reduced. A measurement circuit based around the LV 55-P produces a bipolar voltage signal that can be scaled, to some extent, by the selection

of an appropriate measuring resistor, R_m . However, the restrictions placed upon the value of R_m , to ensure correct operation of the transducer, prevent the signal from being scaled appropriately for the DSP analogue inputs and it does not incorporate a system for introducing the required DC offset. To condition the transducer output to a suitable format for the DSP a programmable instrument amplifier, with optional DC offset, was utilised, the TI AD628. The measurement circuit has been configured for a maximum measurement current of 6.25Arms, resulting in 92% of the ADC input range being utilised. A single phase measuring circuit is detailed in Figure 5.4 (a).

The LEM LV 25-P has been selected for the voltage measurement, it is a widely available hall-effect transducer designed for power converters and similar systems, features include:

- 10 – 900V range.
- 200kHz bandwidth
- 2.5kV isolation.

The use of this transducer allows the same signal conditioning system as the current measurement to be used, with the correct scaling and amplification. A current proportional to the measured voltage is passed through the device and an external resistor. The resistor value is chosen so that at V_{max} , 10mA flows through the transducer. Recommended operating procedure is to split the resistance either side of the transducer inputs, as shown in Figure 5.4 (b). This also results in the dissipated power within each resistor reducing. The resistance can be split across multiple components if necessary. A four-way split was chosen as this would allow two different value resistors to be used on each side of the transducer, increasing the voltage range possibilities while keeping the circuit balanced.

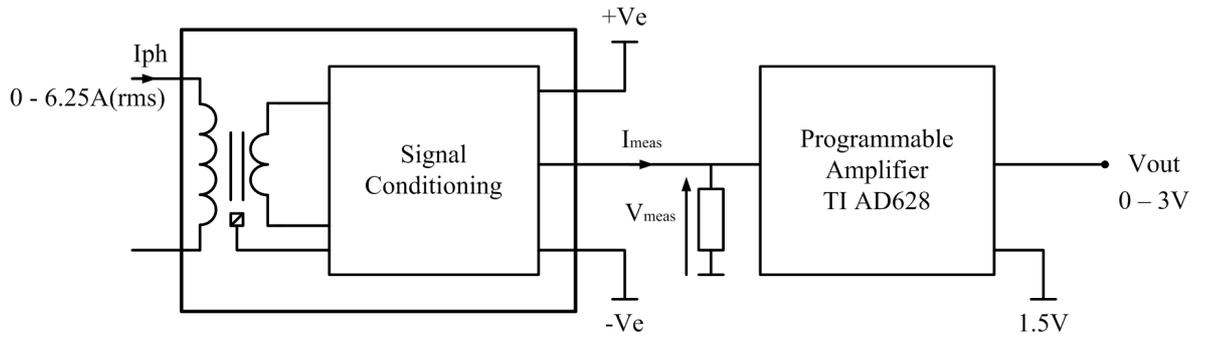
As the DC voltage measurement is included for system status and future work, it has been configured for 600V operation, allowing it to be used on standard three phase rectified supply systems.

Calibration of the measurement and ADC system was performed using known voltage and current sources prior to connection to the test rig hardware.

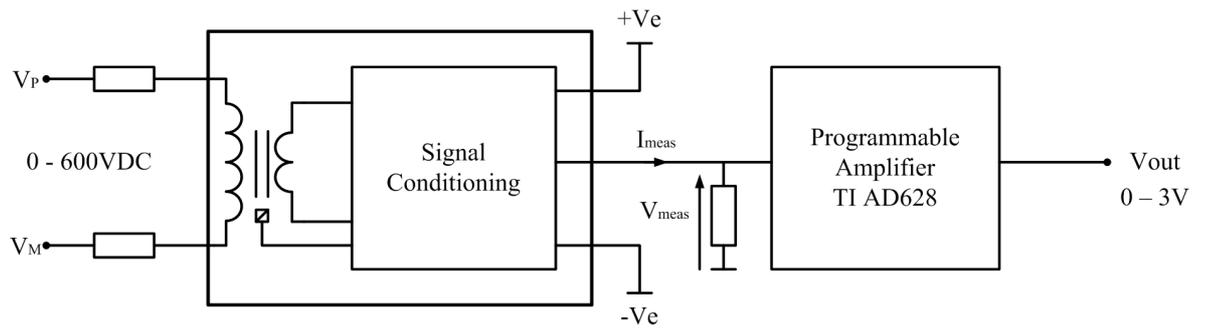
A multi-measurement board has been created for use with the test rig using the above voltage and current measurement circuits. The board has been designed to make full use of a single, standard size PCB by incorporating additional circuits for voltage and current

measurements for a total of five of each type, as detailed in Figure 5.4 (c). Currently two voltage and three current circuits have been populated, due to the design of the measurement circuits. The spare circuits can be configured for a multitude of extra voltages and currents via the correct selection of components, allowing the use on future developments or future projects.

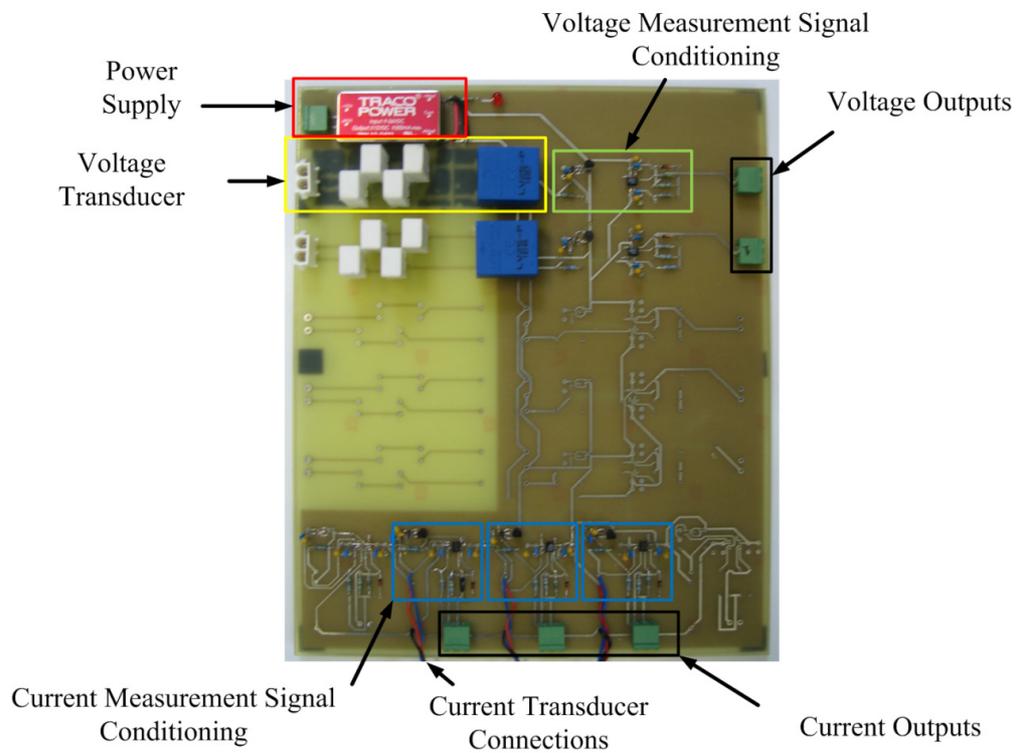
The multi-measurement board schematics, PCB diagrams and sensor data sheets are included in the Dual Topology Test Rig Manual [65], the details of which are in Appendix A.



(a) Current transducer and signal conditioning circuit.



(b) Voltage transducer and signal conditioning circuit.



(c) Measurement board.

Fig. 5.4 Voltage and current measurement system.

5.2.4 Power Module layout

The CSI PEM will require designing and building from discrete components as it is not available as an IPM. To allow comparison of the VSI and CSI topologies without biasing the results with an optimised, high developed commercial IPM, the VSI PEM will be built in the same way. The main considerations for the PEMs are; minimise the parasitic effects (e.g. stray inductance), allow access for measurements and to conform to the recommendations of the electronic component and gate drive manufacturer. The modules will use a heatsink-fan unit as a base, allowing forced cooling during high power tests. The DC link bus bars are to be stacked on top of each other, with suitable insulation separation, to allow the electronic components to be mounted to the heatsink without needing to increase the terminal length, as well as reducing parasitic inductance. The gate drive circuit application notes recommend keeping the leads to the gate terminal as short as possible. The gate drive circuits will be mounted to the side. Above the IGBTs would result in the shortest distance but hinder measurements. Using this method, the leads have been kept within the 100mm limit set out in the application notes. Figure 5.5 details a single phase of the layout of the VSI PEM, the CSI will follow the same layout basis, with the addition on the diodes.

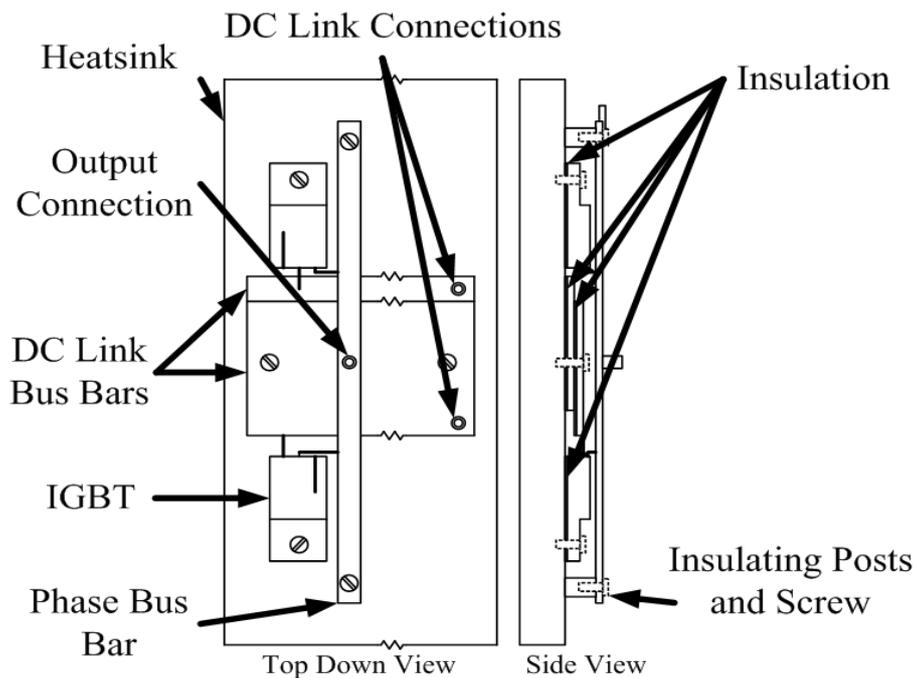


Fig. 5.5 PEM layout schematic for VSI.

The inductor shorting bridge also requires mounting for the CSI topology, although as this is a separate circuit, its position relative to the PEM is of no significance. Figure 5.6 and 5.7 detail the completed VSI PEM and the VSI PEM, with gate drive circuits, respectively.

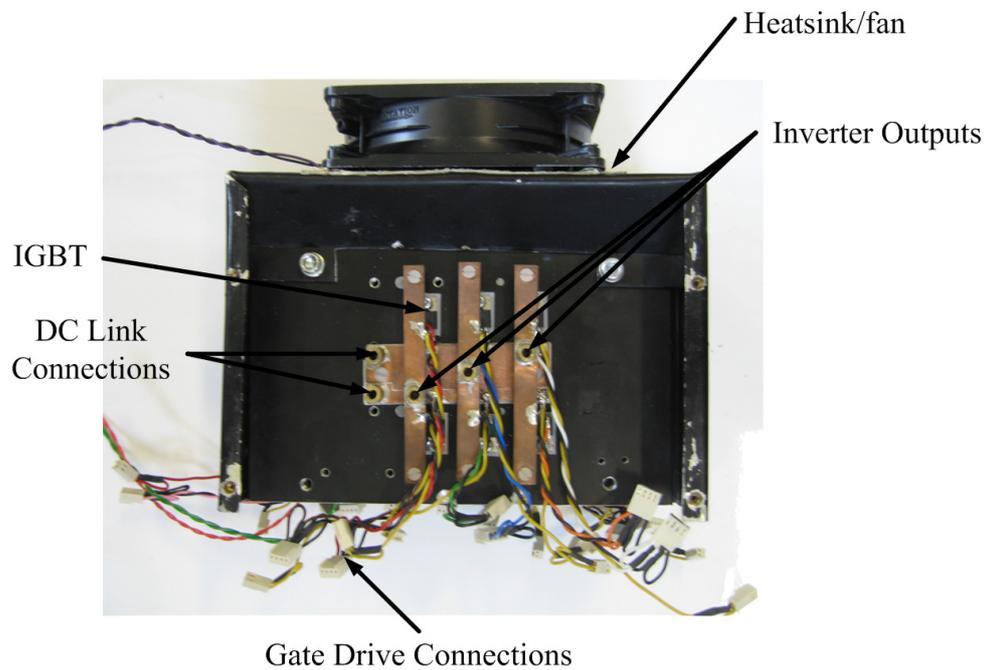


Fig. 5.6 VSI PEM mounted to a heat-sink fan unit.

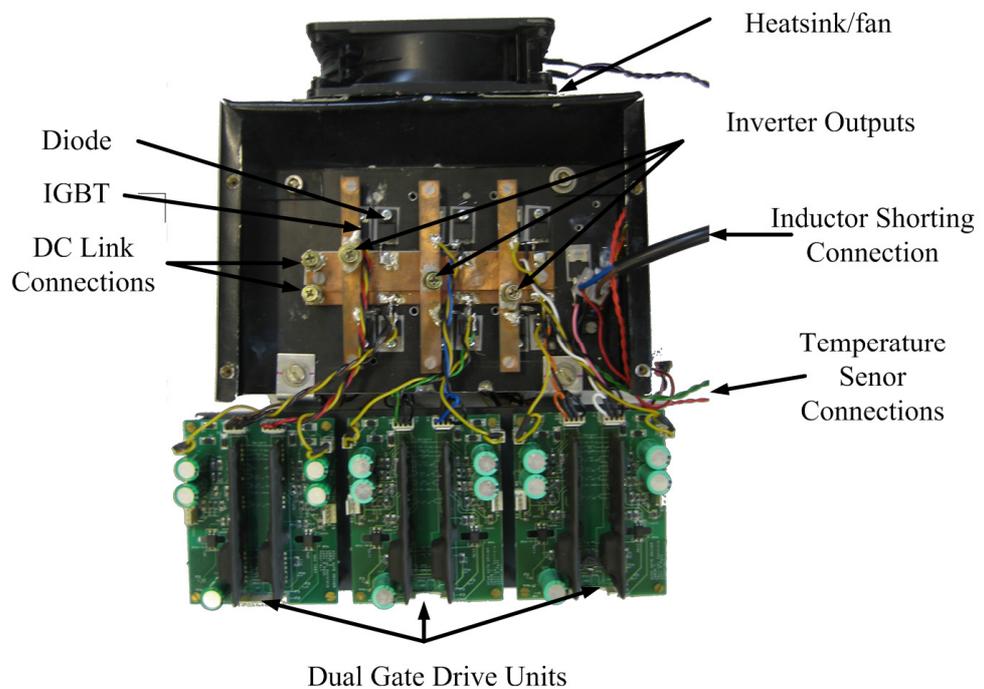


Fig. 5.7 CSI PEM mounted to the opposite side of the heat-sink fan unit.

The VSI and CSI PEM component data sheets are included in the Dual Topology Test Rig Manual [65], the details of which are in Appendix A.

5.2.5 DC Link Inductor

The DC link inductor has been constructed using an available standard E-core kit, as described Chapter 3. An LCR meter was used to confirm the correct inductance had been achieved; Figure 5.8 illustrates the wound core.

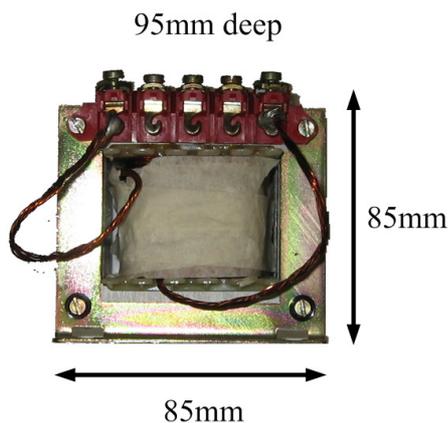


Fig. 5.8 DC link inductor.

5.2.6 Dynamometer

A controlled, variable, mechanical loading system is required to allow the investigation of the VSI and CSI system performance. An available 1500W DC motor was selected as the load machine and field control was implemented to allow the control of the load applied to the PMSM. The PMSM-Load system is detailed in Figure 5.9.



Fig. 5.9 The PMSM and Dynamometer set-up.

5.2.7 DSP Interface Board

To allow the interface of the eZdsp board to the hardware required to build a motor test rig, an interface board was designed. The requirements are;

- Power the eZdsp board.
- Interface the DSP 3.3V system to the voltage required by the external components.
- Provide the option for hardware dead-banding or overlap.
- Provide a means to incorporate the CSI conversion logic hardware.
- Provide a reliable connection for the encoder cable.
- Provide analogue outputs to aid system debugging and development.
- Provide potentiometer based analogue inputs.

The encoder, integrated into the PMSM, gate drive circuits and eZdsp board all operate at 5Volts. The interface board provides a 5V supply, with fuse protection for the eZdsp separate from the external hardware.

The chosen 3.3V interface is the TI SN74CB3T3245 8-Bit Bus Switch. This is a bi-directional switch that limits the output voltage to its supply voltage, in this case 3.3V. This device can therefore be used with the PWM outputs, and digital IO regardless of their configuration, resulting in a highly flexible system.

Hardware dead-banding and overlap is provided by the use of RC time delay components and logic gates. Simple dead-banding can be implemented by delaying the 'on' signal, where as overlap can be implemented by delaying the off signal. A two input AND gate with inputs of the PWM signal and a time delayed version of the same signal will result in the output low-to-high transition being delayed. The delay time will be τ , of the RC components, as the exponential voltage rise will reach the logic switching level at after that time. Hardware overlap is achieved by the same method, utilising an OR gate to delay the high-to-low transition. To allow the dead-banding time to differ from the overlap time, multiple selectable paths for the PWM signal will be utilised to allow the multiple RC values to be implemented during board assembly, thus allowing dead-banding or overlap time to be modified by selecting a different path for the signals and not by replacing RC

components on the circuit board. The logic integrated circuits will also be socketed to allow them to be changed as required. Using the IGBT parameters, as supplied on the manufacturers' data sheet the dead-time and overlap time have been determined and the chosen dead time and overlap times chosen for the test rig are detailed in Table 5.1.

Parameter	Time (ns)
td(on)	20
tc(on)	30
td(off)	150
tc(off)	40
Dead time	500
Overlap time	150

Table 5.1 Dead time and overlap time parameters.

The CSI conversion logic will interface to the DSP board through a selectable socket system, this allows the CSI conversion logic to be developed independently from the DSP system.

The encoder input utilises the 15-way D-type connector that comes as standard on the PMSM encoder, ensuring a reliable connection.

The analogue output is provided through the use of a TI DAC7614, four channel, 12bit digital-to-analogue converter. It utilises the serial peripheral interface (SPI) protocol for serial communication and is compatible with the C2000 DSP communication peripherals. It is a 5V device, therefore it will utilise the previously mentioned level converters. As the device outputs are not required for control, they are implemented as test points for the connection of an oscilloscope.

Figure 5.10 illustrates the DSP interface board

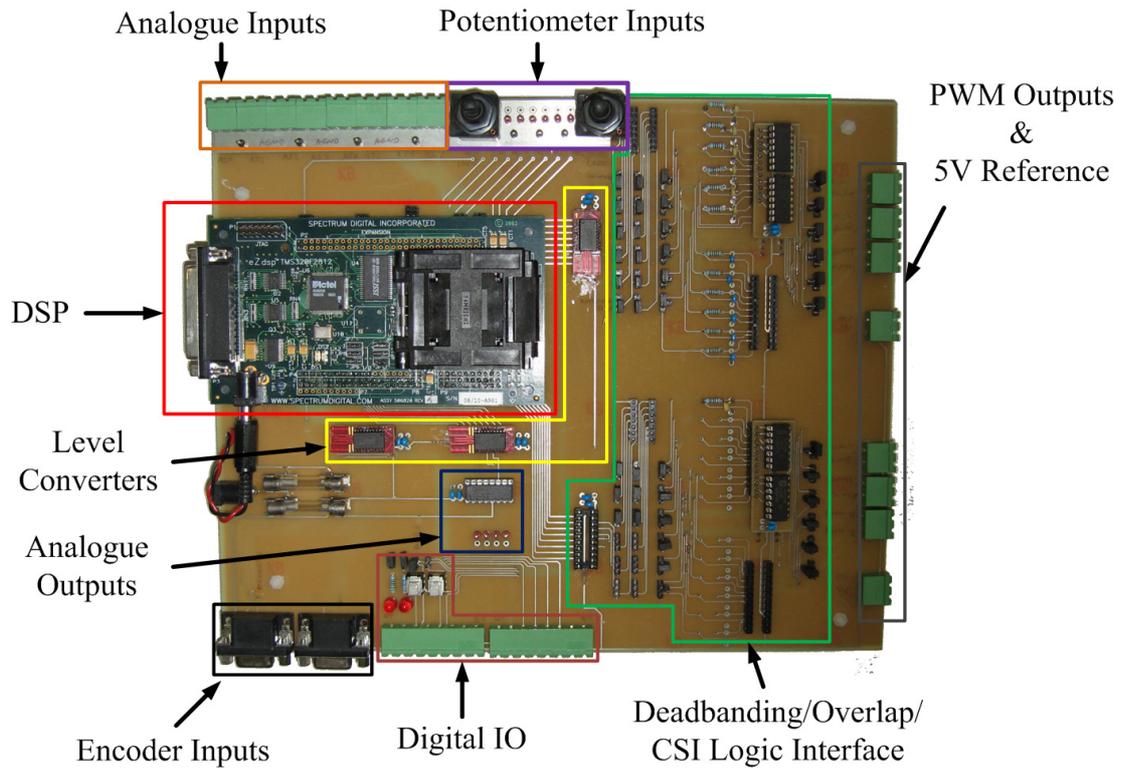


Fig. 5.10 DSP interface board.

The DSP interface board schematics, PCB diagrams and component data sheets are included in the Dual Topology Test Rig Manual [65], the details of which are in Appendix A.

5.2.8 CSI Conversion Logic

To convert the VSI PWM switching signals to the CSI format the logic conversion detailed in Chapter 2 requires implementation. The CSI system would achieve maximum flexibility if the conversion was implemented by a programmable logic device (PLD). This would dramatically increase the complexity of the conversion as well as increase the cost. To speed completion of the system the conversion logic has been implemented using integrated circuit logic components. Future development of the CSI system could allow the PLD option to be explored and the socketed interface to the DSP interface board allows this to be achieved without significant redesigning of the system. Figure 5.11 illustrates the CSI conversion logic board.

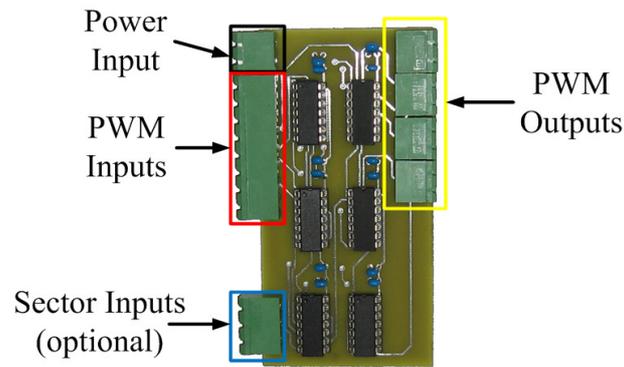


Fig. 5.11 CSI PWM conversion logic.

The CSI PWM conversion logic schematics and PCB diagrams are included in the Dual Topology Test Rig Manual [65], the details of which are in Appendix A.

5.2.9 Temperature Monitoring

To ensure the reliable operation of the CSI, thermistors have been attached to devices on the CSI PEM, the inductor shorting diode and an inverter leg IGBT. Thermistors were chosen due to their robustness to the high frequency switching present within PWM inverters. The thermistors have not been incorporated into the control algorithm at this point for simplicity and are monitored using digital multi-meters. Not all devices are monitored as the temperature monitoring gives an indication of system health. Should there be a sudden temperature rise or the case temperatures exceed 70°C , then the system will be manually shutdown before damage occurs. The manufacturers specifications [54,55] list a maximum device case temperature of 100°C . Should temperature rises be unexpected at the given operating point, investigations can be made to try and determine the cause. The thermistors used [66] are negative temperature coefficient devices with a nominal resistance at 25°C of $5\text{k}\Omega$. The device details and the resistance temperature profile has been plotted and is included in Appendix B.

5.3 Software

Texas Instruments provides software library of DSP instruction code, documentation, training and hardware to allow system developers, for example, white-goods designers, to familiarise themselves with the DSP hardware and test possible designs without needing to design the full hardware system during initial testing. The software library includes sample code to implement control of most motor types, from DC to switched reluctance. Each set of sample code has been designed to function with a Experimenters Kit, supplied separately, but is designed in such a way to be suitable for custom hardware without requiring a complete re-write.

5.3.1 VSI Control Algorithm

The supplied software (code) is built in a modular manner, allowing relatively simple reconfiguration of the code to implement different control strategies, machine types and applications. Figure 5.12 shows the complete control algorithm for a sensed, field orientated control system with a quadrature encoder position measurement system. Each block within the DSP unit is a separate software module and can be enabled or disabled at will. The documentation is designed to step the user through a commissioning sequence, confirming correct operation of the modules before including them in the control loop.

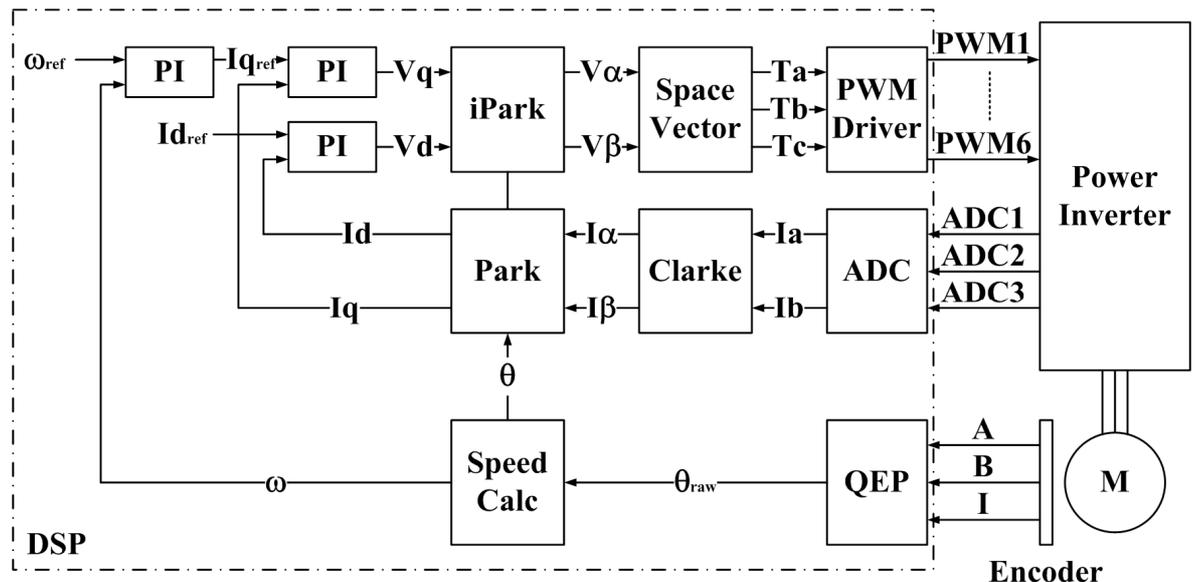


Fig. 5.12 TI DSP motor control scheme [67].

The first stage is V/Hz control without position feedback, for confirmation of the inverse Park transform, space vector and PWM modules. The final stage enables the speed or position control system (depending upon application). The control system is designed around the per-unit system, therefore requires the phase currents to be scaled accordingly upon acquisition.

An additional module is required for operation of the DAC. Although custom code, it is designed with the same principles as the supplied software to allow it to be easily incorporated into the existing system and future systems

As implemented by TI, the speed PI control loop uses the speed set point directly for the PI reference. This results in speed set point changes being implemented solely by the PI controller, which when tuned to allow accurate control of the rotation speed, could result in excessive acceleration being demanded of the motor. To prevent this situation occurring, modifications were made to make a buffer between the speed set point and the speed PI controller reference. The modifications set a maximum increase of the PI reference on each execution of the speed control loop. This allows a ramp rate to be set to limit the speed change to a particular rpm/second.

The TI software system documentation and main DSP code components are detailed in the Dual Topology Test Rig Manual [65] , the details of which are in Appendix A.

5.3.2 CSI Control Algorithm

To allow control of a CSI system, software modifications are required in addition to the hardware modifications already detailed. New code modules will be required to implement the rotor offset calculation for the CSI switching, along with a system to compensate for the switched nature of the phase current to allow the Clarke and Park transformations to function properly. The completion of the VSI commissioning allows the new modules to be created and tested, at least partially, on a functioning control system. They do not require inclusion within the control loop for their outputs to be tested. Viewing the results prior to incorporation within a CSI system reduces the likelihood of errors preventing the CSI system from operating.

Once the additional modules are complete, a testing and commissioning program is required, as with the VSI system. This will incrementally implement and test the CSI control loop. The commissioning program is detailed below. Initial testing will use an open loop, six-switch modulation scheme to confirm the operation of the PEM before introducing PWM switching and vector control methods. As with the VSI, resistive loads will be used initially, to allow confirmation of correct operation before progressing to the dynamic system of the PMSM. The commissioning program has been broken into nine stages, detailed below.

1. Six-switch operation with resistive load.
2. Six-switch operation with resistive load and position feedback.
3. Six-switch operation with the PMSM.
4. V/Hz control with resistive load, without position feedback
5. V/Hz control with resistive load and position feedback.
6. Current control with resistive load, without position feedback.
7. Current control with PMSM and position feedback.
8. Speed control.

Stage 1: A simple six-switch modulation scheme will be implemented, based on an artificially generated position signal. There will be no measurement of currents within the DSP, although they will be monitored with test equipment, and the system will operate open loop. This stage will allow the correct operation of the PEM to be confirmed.

Stage 2: The six-switch test is repeated utilising the actual encoder signal and calculated rotor angle. To achieve this the PMSM is driven by the DC motor. This will ensure that the phase relationship of the output voltage and the rotor angle is correct and that the 30° offset has not been applied in the wrong direction.

Stage 3: The PMSM is connected and the correct operation confirmed, in this test the speed of the PMSM will be controlled via the DC link voltage.

Stage 4: The PWM control scheme is used from now on, again utilising a three phase resistive load, and the artificially created rotor. The inverter output can now be controlled using voltage and speed set points in the DSP algorithm. Comparing the rotor position signal and output voltage on an oscilloscope, the phase relationship can be confirmed as in

stage 2 for the six-switch modulation. This test confirms the correct operation of the CSI SV logic and the CSI offset calculation.

Stage 5: The actual rotor position is used within the control loop, as in stage 2. This allows the phase relationship to be observed once more, with the addition of the PMSM EMF.

Stage 6: The resistive load and artificial rotor angle are used to confirm the correct operation of the current control modules; a satisfactory output from the measurement filter will result in stable outputs from Park transform and allow the PI controller to operate correctly.

Stage 7: The resistive load is replaced by the PMSM and filter capacitors to allow switching and current control with the PMSM is confirmed to operate correctly.

Stage 8: The speed control module is enabled to confirm the ability of the control loop to accurately control the speed of the PMSM.

The DSP code implementation of the CSI control algorithm is detailed in Appendix C, while the TI software system documentation and main DSP code components are detailed in the Dual Topology Test Rig Manual [65], the details of which are in Appendix A.

5.3.3 Current Measurement Filter

Due to the switched nature of the current in a CSI, the PI control modules will not function correctly. A filter to reduce the high frequency noise is an obvious solution to this problem and the DSP would allow it to be implemented digitally. However, complex filters are computationally expensive even for DSPs and could result in the time required to execute the control loop exceeding the PWM period, preventing the control system from functioning properly. The filter needs to remove the high frequency noise without introducing a significant phase shift that would result in errors during the Park transform. A possible solution is to implement moving average filter to average any switching noise over a number of samples [68], rather than a computationally more expensive, low pass filter. This, obviously, can be implemented using addition and divide functions. This is still not an ideal situation, due to divide operations also being computationally expensive [69]. In DSPs, there is an extremely efficient divide operation if the factor to divide by is a

binary power, i.e. 2^3 , this utilises logical operations on the binary data instead of maths operations and results in the same output as the mathematical divide functions.

When data is examined as the binary data within a CPU register, as in Figure 5.15, with the most significant bit (MSB) on the left, moving the contents one position to the right will result in a change in the value. The resulting value will be half of the original. Each subsequent shift right will further divide by 2. Figure 5.13 details a shift right by 3 on the number 88, the result can clearly be seen to be 11. This type of division can be performed in the least number of clock cycles, but is obviously limited to binary powers. It should be noted that the fixed point fractional number system used by the DSP simply requires the shift operation to be implemented on the integer component and fraction component separately and the results combined.

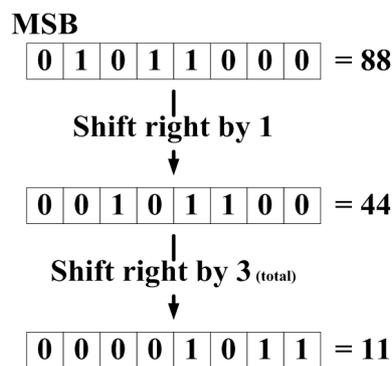


Fig. 5.13 Binary divide operation implemented on a DSP.

The choice of the window size, the number of samples to average, depends on several factors. A large window will maximise the noise reduction, however, on a periodic signal it will also smooth the output. A large window will also require many binary shifts on each result and require many additions per output result, greatly increasing the computation time. A window of 8 was chosen initially, with examination of the output determining if the windows size needed modification.

On each call to the moving average filter module, the most recent measurement is divided by eight and stored at the location of the filter pointer. All eight stored values are summed and the result output. The filter pointer is then incremented for the next operation. The process is repeated each time the filter is called; once eight values have been stored the

filter pointer resets and overwrites the oldest value, ensuring that the memory buffer always contains the eight most recent values.

The DSP code implementation of the moving average filter is detailed in Appendix C.

5.3.4 CSI Offset Calculation

The 30° offset required for correct CSI operation should be implemented in the PWM output of the control system, implementing the offset before the Park transformation would result in incorrect values for i_d and i_q being calculated. Therefore, the control loop will require two rotor positions: the rotor position, θ , and the offset position θ_{CSI} . This can be calculated at the same time as the actual rotor position using the same method as used to adjust the position index pulse with respect to the rotor angle. Testing can be accomplished by utilising the analogue outputs to measure the phase shift between θ and θ_{CSI} . The system can also be verified by observing the calculated values of i_d and i_q during commissioning stage 1. Correct operation will result in fixed value for both values when the phase currents are of fixed magnitude and the phase relationship with respect to the rotor position is correct.

The modified control loop for controlling a CSI is detailed in Figure 5.14.

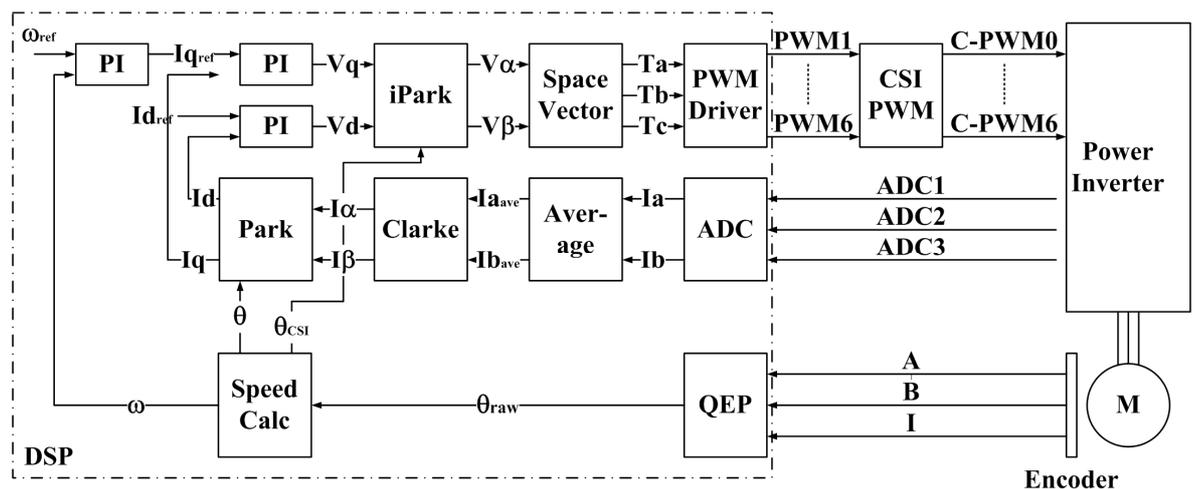
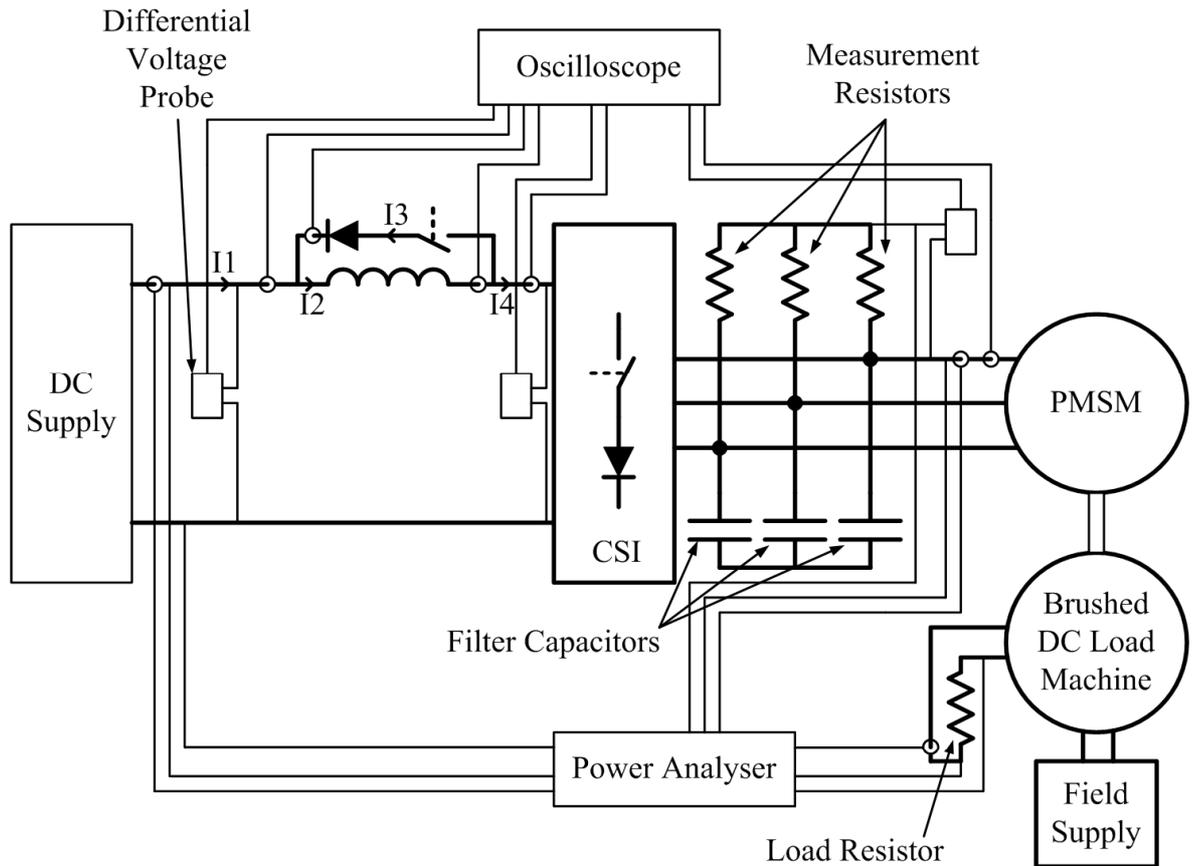


Fig. 5.14 Modified motor control scheme for the CSI.

The DSP code implementation of the CSI offset angle is detailed in Appendix C.

5.4 Test Measurements

To allow analysis of the performance of the VSI and CSI topologies, test measurements, detailed in Figure 5.15, will be taken using both an oscilloscope, for offline analysis of the waveforms, and by a 3 channel (voltage and current measurement) power analyser to give a real-time indication of the operating conditions. The power analyser results will be recorded to allow comparison with the oscilloscope results and to check for irregular readings.



Index	Description
I1	DC Current
I2	Inductor Current
I3	Inductor Short Current
I4	Inverter Current

Fig. 5.15 Measurement system for CSI topology.

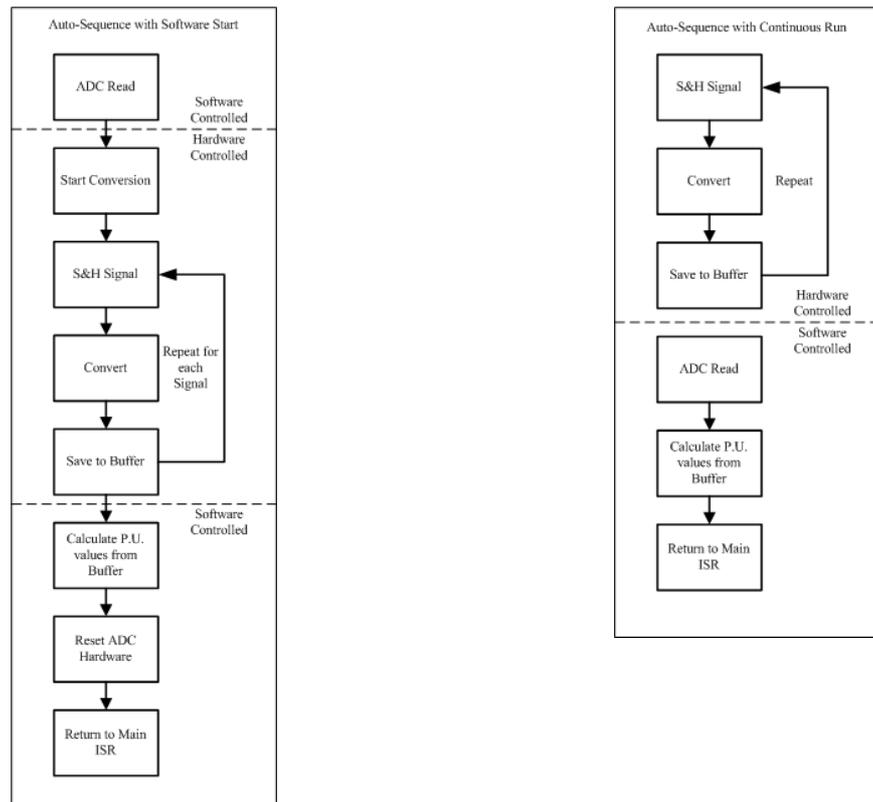
5.5 Commissioning

5.5.1 VSI System

Commissioning of the test rig was performed in multiple steps, initially with the VSI system, confirming correct operation of the hardware and the software before progressing to the CSI system.

The first stage of commissioning is to verify the encoder operation and rotor position calculation. To achieve this, the PMSM was driven by the DC motor, with the DSP active but the inverter not powered up. The PMSM motor connections were connected to a three phase resistive load (star configuration) to allow a small current to flow. Using an oscilloscope the back EMF of the designated ‘a’ phase, the index pulse and the phase current were compared, along with an analogue output of the calculated rotor angle. The encoder calibration parameter, within the DSP rotor angle calculation code module, was used to align the rotor angle with the EMF and current. The PC-DSP debugging interface was used to confirm the alignment of the current and rotor angle, ensuring that the analogue output of the rotor signal was not subject to a delay (phase shift) that would corrupt the results.

The next stage of commissioning was to verify the ADC operation. The resistive load was connected to the inverter output terminals to provide a safe, easily controlled load for the DSP and inverter. During testing it was discovered that the ADC produced errors on the first conversion of each control loop. The cause is due to a bug within the ADC hardware in the DSP. The bug results in the first conversion being subject to errors if there is an interval between conversions. The original configuration of the ADC performs one set of conversions during each execution of the control loop, triggered by a software call within the control loop. The operation of the ADC hardware is detailed in Figure 5.16 where (a) details the original configuration, the ADC operation was modified to run continuously (b), eliminating the error. The latest conversion results are stored automatically and the control loop retrieves the results at the required point within the loop.



(a) Original system.

(b) Modified system.

Fig. 5.16 ADC operating flowchart.

Figure 5.17 details the ADC conversion results on a switched signal (inverter output) and a non switched signal (mains current measurement) for the original configuration while Figure 5.18 details switched and non switched measurements for the modified configuration. It is clear that the original system produced erroneous conversion and that the modified system performs as would be expected.

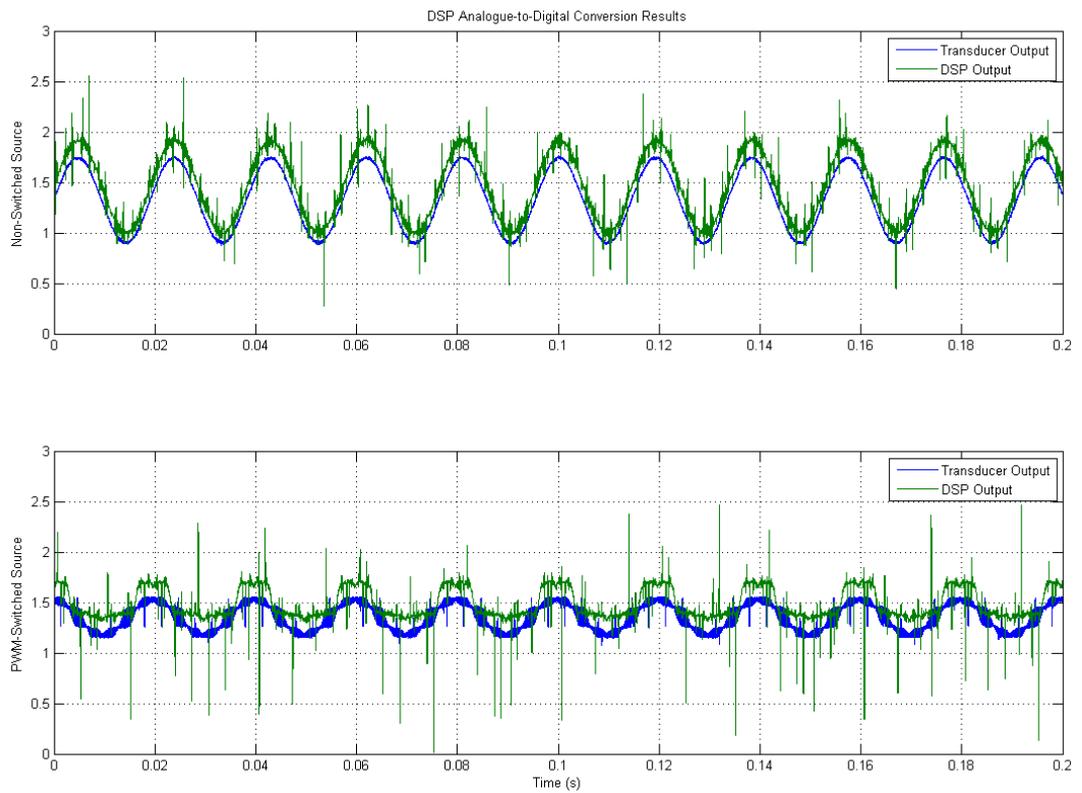


Fig. 5.17 ADC conversion, original operation results.

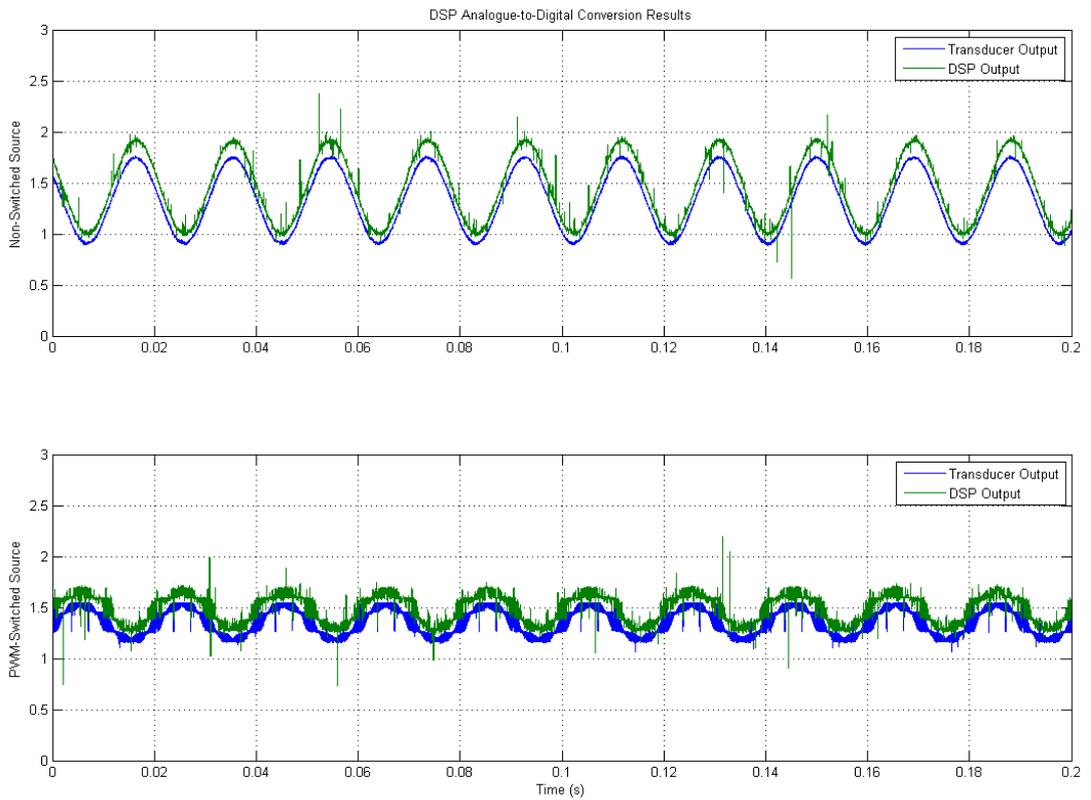


Fig. 5.18 ADC conversion, modified operation results.

With the encoder calibrated and the ADC operation confirmed, the PMSM was connected to the PEM and the TI commissioning sequence followed to produce a working VSI system.

The manufacturer supplied characteristics for the PMSM are detailed in Table 5.2. Mechanical power estimations will be based on the assumption that the PMSM EMF is sinusoidal, the supplied EMF constant is correct and that the EMF is in phase with the calculated rotor angle.

To determine the validity of these assumptions the brushed DC motor was used to rotate the PMSM while measurements were taken. Figure 5.19 details the phase EMF, generated by connecting the PMSM terminals to a high resistance start load, DSP generated rotor angle and a constant representing the peak phase EMF for the rotation speed, 400rpm (41.88 rads^{-1}). Table 5.3 details the k_o characteristic measurements of the PMSM.

PMSM Characteristics	
ω	3000 rpm
ω	314 rads^{-1}
R_{l-l}	1.4 Ω
L_{l-l}	8.6 mH
k_o	98 $V_{l-l-rms}/krpm$ As quoted by manufacturer
k_o	0.54 $V_{ph-peak}/rads^{-1}$

Table 5.2 PMSM manufacturer specifications.

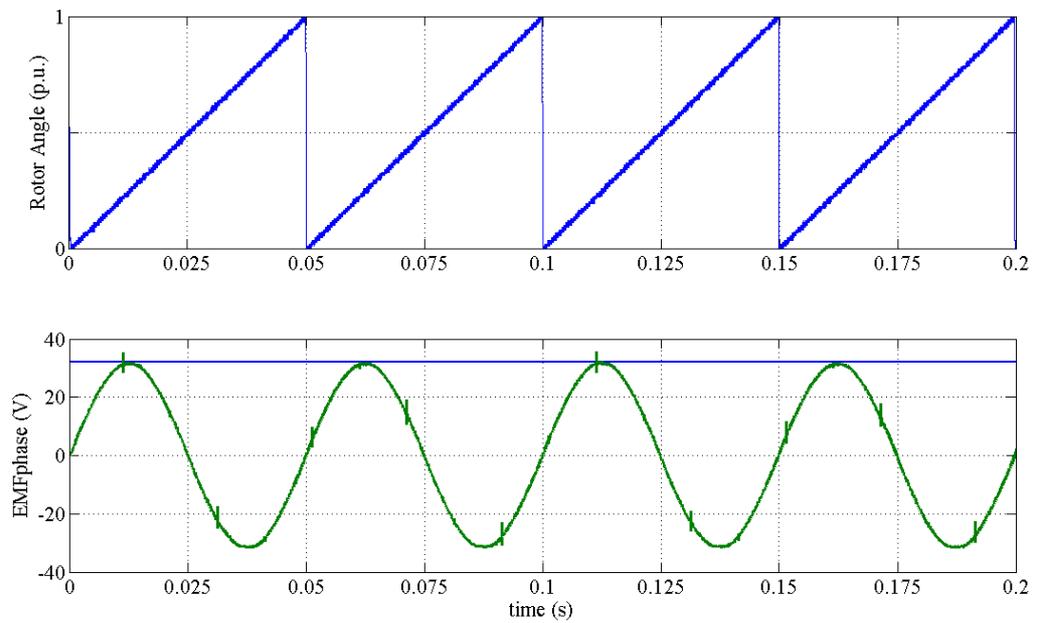


Fig. 5.19 PMSM EMF characteristic test results.

PMSM k_o Characteristic		
Speed (rads^{-1})	EMF _{phase-rms} (V)	k_o ($\text{V}_{\text{ph}}/\text{rads}^{-1}$)
0	0	0
10.47	5.6	0.53
20.94	11.1	0.53
31.41	16.7	0.53
41.88	22.3	0.53
52.35	27.7	0.53
62.83	33.2	0.53
73.30	38.7	0.53
83.77	44.3	0.53
94.24	49.8	0.53
104.71	55.3	0.53

Table 5.3 PMSM k_o characteristic measurements.

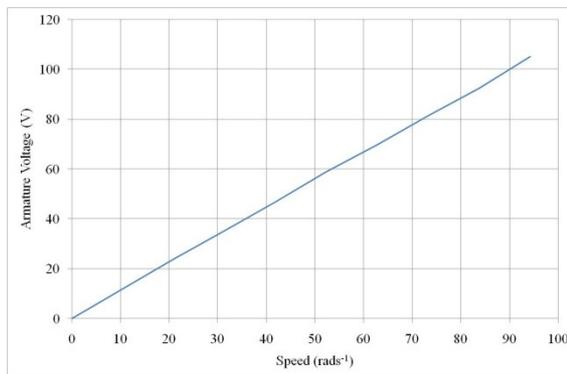
The k_o characteristics show that the manufacturer specified EMF constant is correct, within measurement errors.

The brushed DC machine characteristics are detailed in Table 5.4

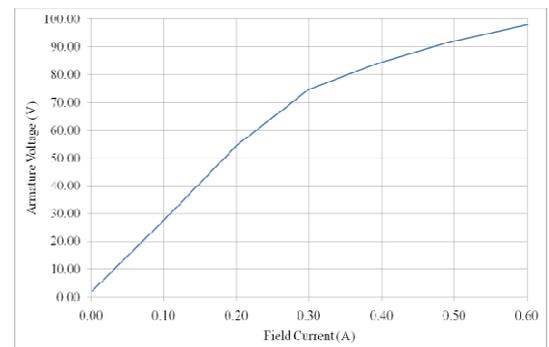
Brushed DC machine Characteristics	
P	1500 W
ω	1500 rpm
ω	157 rads^{-1}
V_a	180 V
V_f	210 V
I_a	9.8 A
R_a	1.725 Ω
I_f	0.5 A

Table 5.4 Brushed DC machine manufacturer specifications.

Confirmation of the brushed DC machine output voltage vs. speed and field excitation is detailed in Figure 5.20. This will allow calculation of the required parameters conditions to load the PMSM appropriately.



(a) Speed vs. armature voltage characteristic.



(b) Armature vs. field excitation characteristic at full speed.

Fig. 5.20 Brushed DC machine excitation characteristics.

To load the brushed DC motor output, variable field voltage control and a power dissipation system is required. For simplicity, 20Ω load bank resistors were chosen to dissipate the brushed DC machine output. The mechanical power on the brushed DC motor shaft can be approximated using Equations (5.1) and (5.2), assuming that windage and friction are negligible. An approximation of the field excitation and load resistance can be determined for load points of 0.25 p.u., 0.5 p.u., 0.75 p.u. and 1.0 p.u.

$$P_{mech} \approx P_{gen} + P_{copper-loss} \quad (5.1)$$

$$P_{mech} \approx i_a^2 R_l + i_a^2 R_a \quad (5.2)$$

As discussed in Chapter 4, the maximum load will be limited, due to power supply specification and designed inverter output currents, to 800W. Given a maximum armature voltage of approximately 90V at 800rpm, from Figure 5.20b, the load resistance requires calculating to ensure the voltage and current specifications of the DC motor are not exceeded. Table 5.5 details the armature current and voltage required for each load point, using Equation (5.2). For a single load resistor the required armature voltage is exceeded before a load 0.75 p.u. is reached. Therefore the load has been recalculated using two resistors in parallel. In this configuration the required field excitation is close to maximum for the 1.0 p.u. test, to ensure that the load point can still be reached if the motor speed drops an additional load resistor will be used for the full load test. These operating points will be used as a guide, for the VSI system, the mechanical torque can also be estimated using Equation (4.1) and therefore the PMSM phase current will be used to indicate the correct operating point. The machine speed, armature voltage and current will be recorded and used as the operating point for the CSI test to ensure the same operating condition are used.

	Load point (p.u.)	I_a	V_a
1 Resistor	0.25	3.03	60.68
	0.5	4.29	85.82
	0.75	5.26	105.11
	1.0	6.07	121.37
2 Resistors	0.25	4.13	41.30
	0.5	5.84	58.41
	0.75	7.15	71.54
	1.0	8.26	82.60
3 Resistors	1.0	9.76	65.09

Table 5.5 Brushed DC machine load parameters.

5.5.2 CSI System

The encoder calibration and modifications to the ADC operation were carried through to the CSI control algorithm; the six-switch operation of the CSI was implemented as a separate control algorithm, due to its simplicity compared to the space vector algorithm implemented in PWM system.

Stage 1 of commissioning the CSI resulted in the expected voltage and current waveforms, verifying the correct operation of the PEM. Stage 2 also produced the correct waveforms and confirmed the correct phase relationship between the PMSM back EMF and the inverter output. Completion of Stage 3 resulted in a working CSI PMSM system; Figure 5.21 details the measured phase voltage and current with the rotor position also shown to confirm the correct phase relationship. Figure 5.22 details a SABER simulation of the same operating conditions, it can be seen that there is a close correlation between the simulated and actual results. Phase angle control was tested during six-switch operation, Figure 5.23 details the measured phase voltage and current with the rotor position also shown to confirm the ability to adjust the phase relationship. Figure 5.24 details a SABER simulation of the same operating conditions, it can be seen that there is a close correlation between the simulated and actual results.

Stage 4 uses the TI motor control algorithm from the VSI system as a base with the CSI specific modifications. The inverter output waveforms confirmed the correct operation of the SV PWM logic and monitoring of the filtered phase currents showed a signal with a sinusoidal measurement with some switching noise. The switching noise on the current measurement, although clearly visible, was not anticipated to cause significant problems during the Clarke and Park transforms. Verification of this would be possible in later stages when the transform modules are enabled. If the noise on the current signal proved to be problematic at that stage, the measurement filter would be adjusted to produce satisfactory results. Figure 5.25 details the inverter output and voltage with i_d set to zero, while Figure 5.26 shows operation with a negative i_d , resulting in a phase advance of the current by 20° electrical. If the load was a PMSM instead of the resistive test load, the net value of flux would have been weakened by an amount that depends on the motor characteristics, specifically the $I_d L_d / k_o$ ratio.

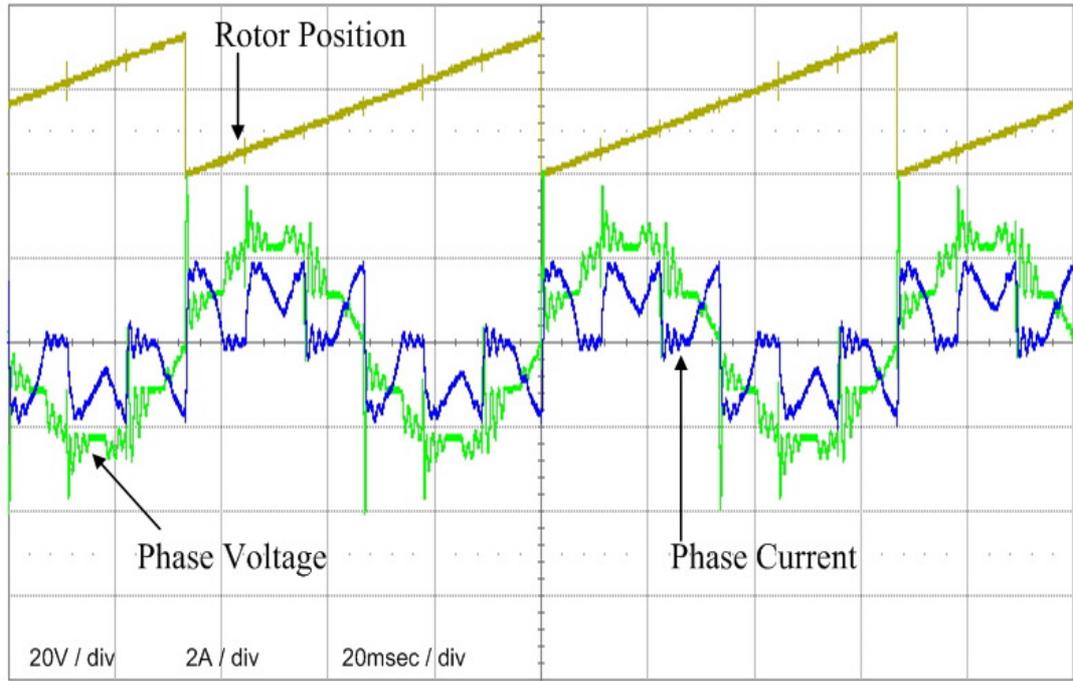


Fig. 5.21 Six-switch CSI operation with PMSM.

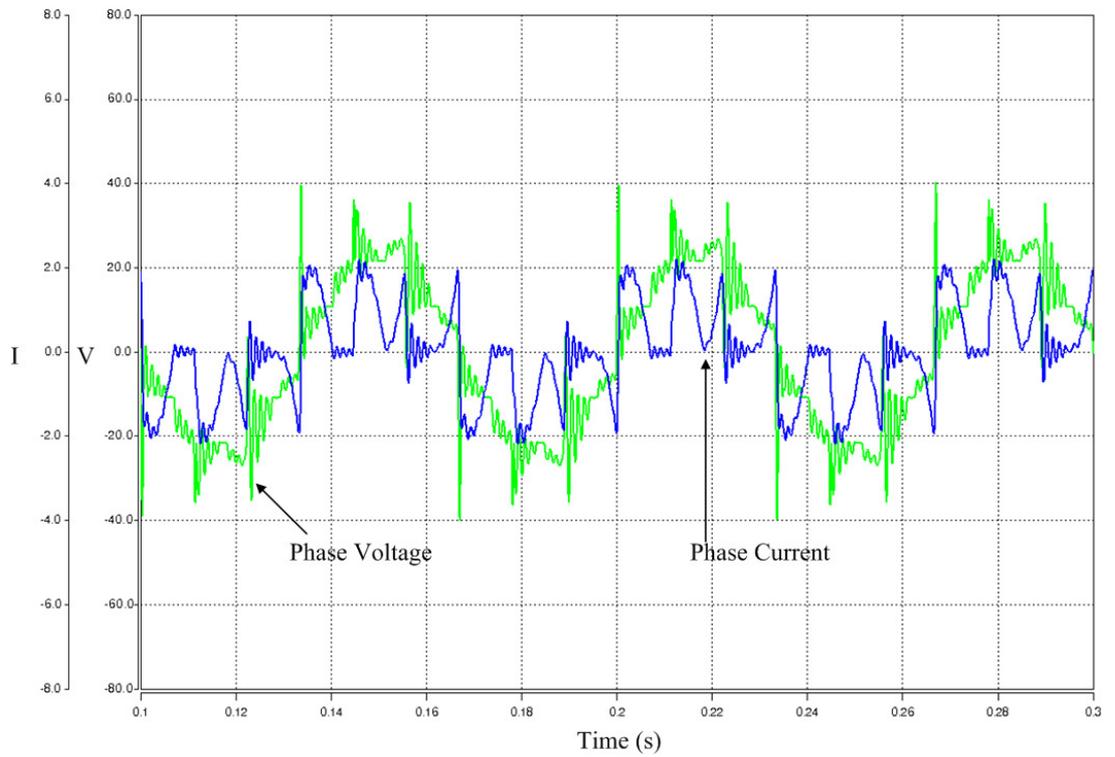


Fig. 5.22 Simulated six-switch CSI operation with PMSM.

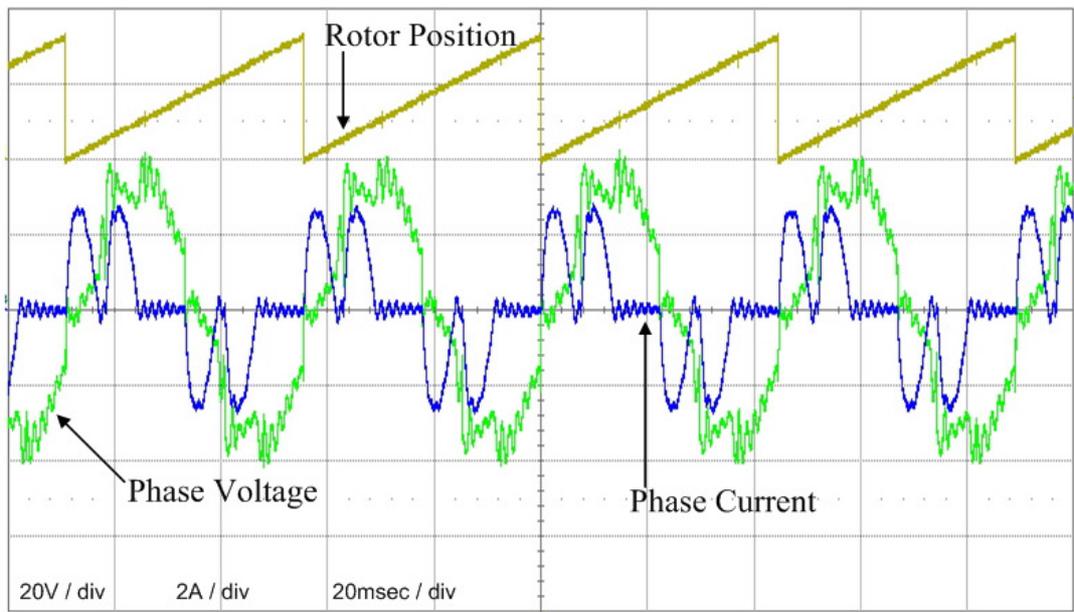


Fig. 5.23 Six-switch CSI phase shift operation with PMSM.

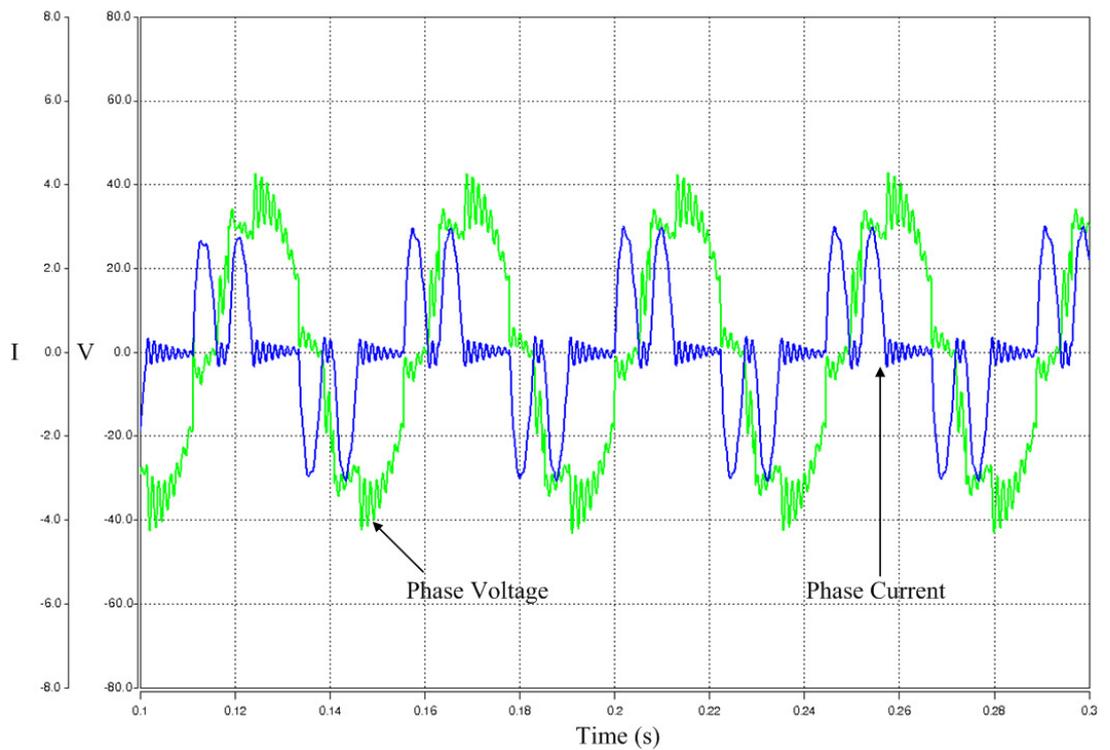


Fig. 5.24 Simulated six-switch CSI phase shift operation with PMSM.

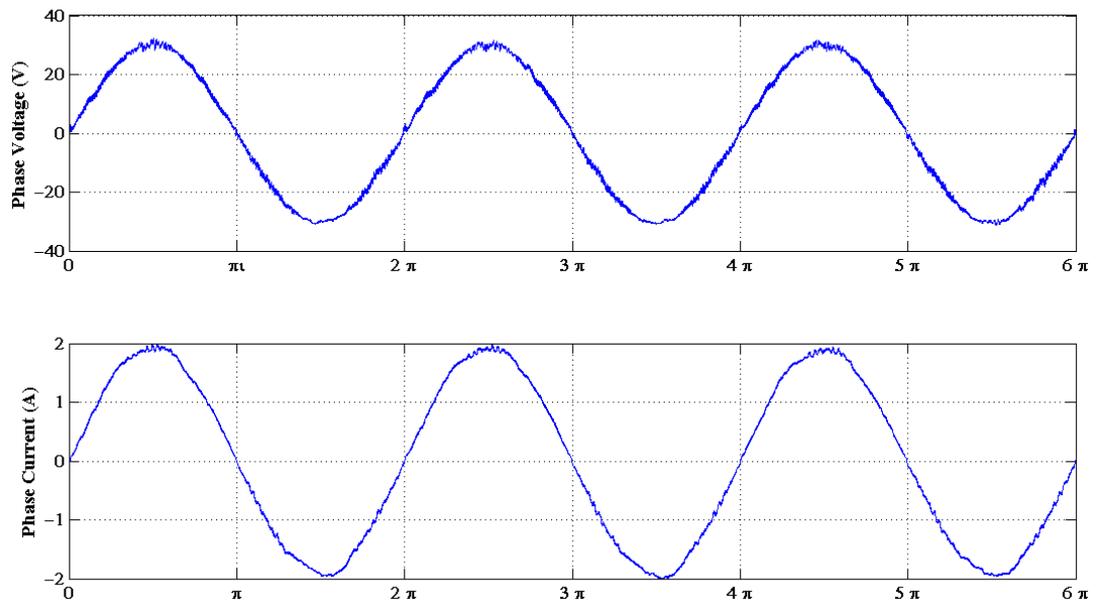


Fig. 5.25 PWM CSI with resistive load.

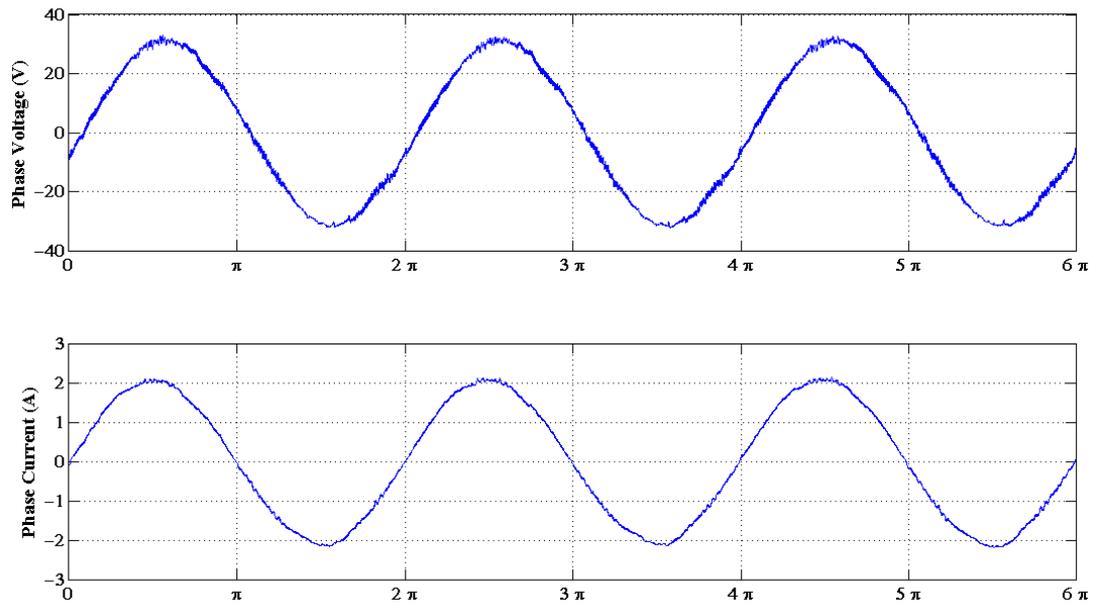


Fig. 5.26 PWM CSI flux-weakening with resistive load.

Stage 5, like Stage 4, confirmed the PWM logic with PMSM encoder signal as the reference. Stage 6 resulted in the i_d and i_q measured currents, as output from the Park transform, detailed in Figure 5.27. The small ripple, 0.06 p.u. on a 0.13 p.u. signal, although not ideal, is sufficiently small that the PI controller will not be adversely affected. It is expected that at higher load currents, where the signal magnitude is greater, the ripple will become less significant.

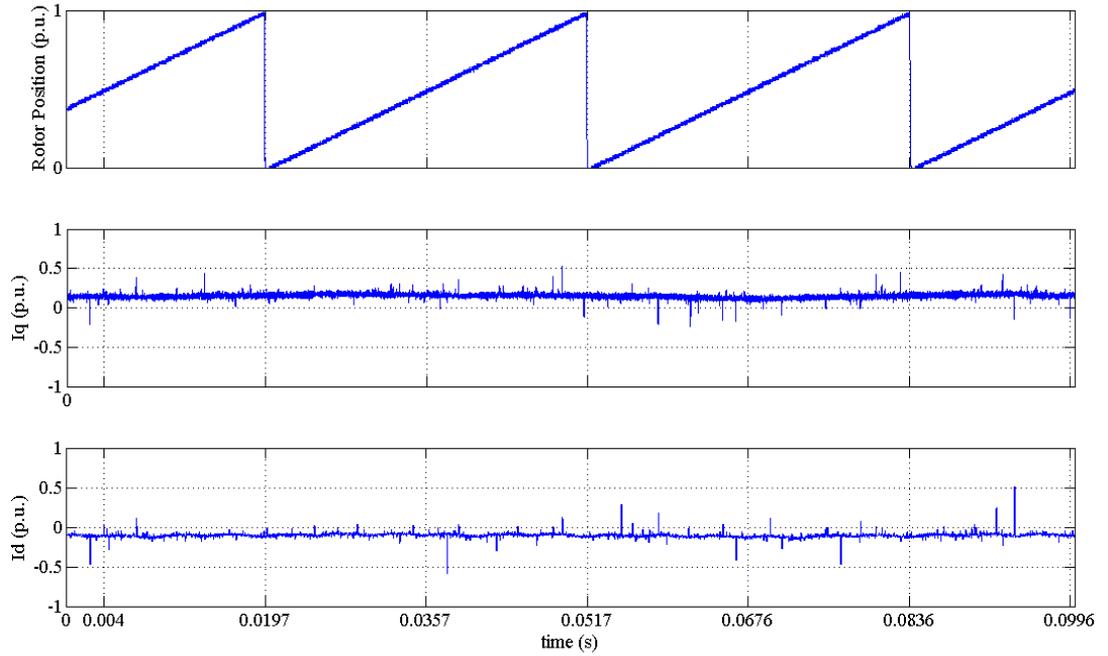


Fig. 5.27 Park transform outputs for resistive loaded CSI.

Stage 7 resulted in current control of the PMSM, the speed was controlled by adjustment of the DC link voltage until the current set point limited the PMSM output and the speed dropped. Figure 5.28 details a low load test of the PMSM at 400rpm.

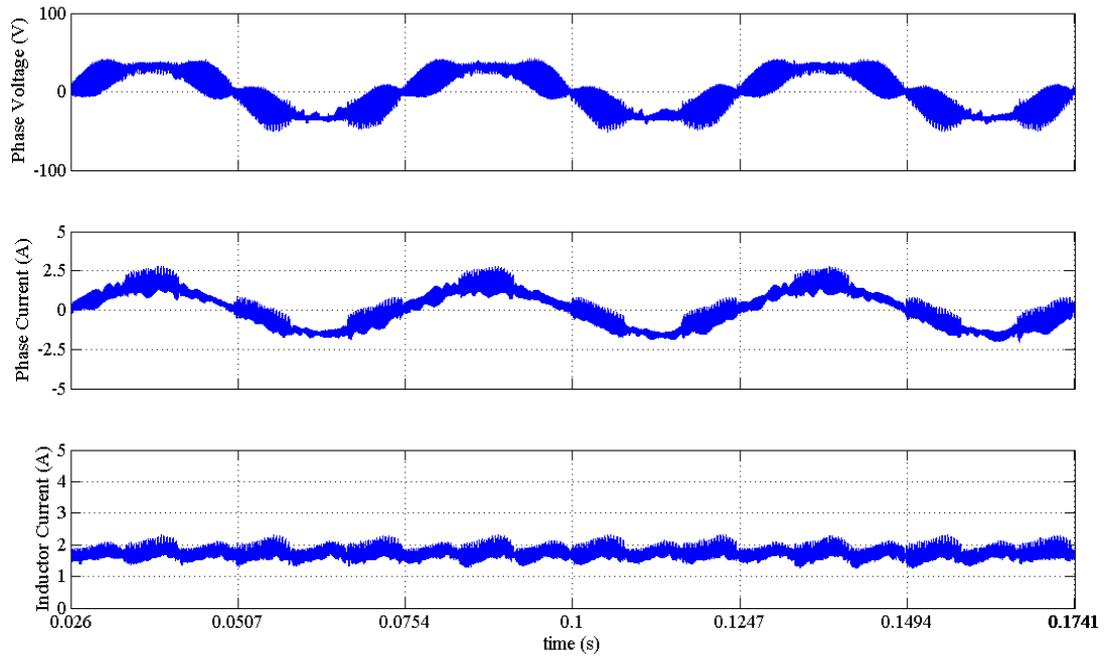


Fig. 5.28 CSI commissioning test, approx. 90W mechanical.

Stage 8 successfully implemented speed control of a PMSM, Figure 5.29 details an operating point of 700rpm with an approximate mechanical power of 400W.

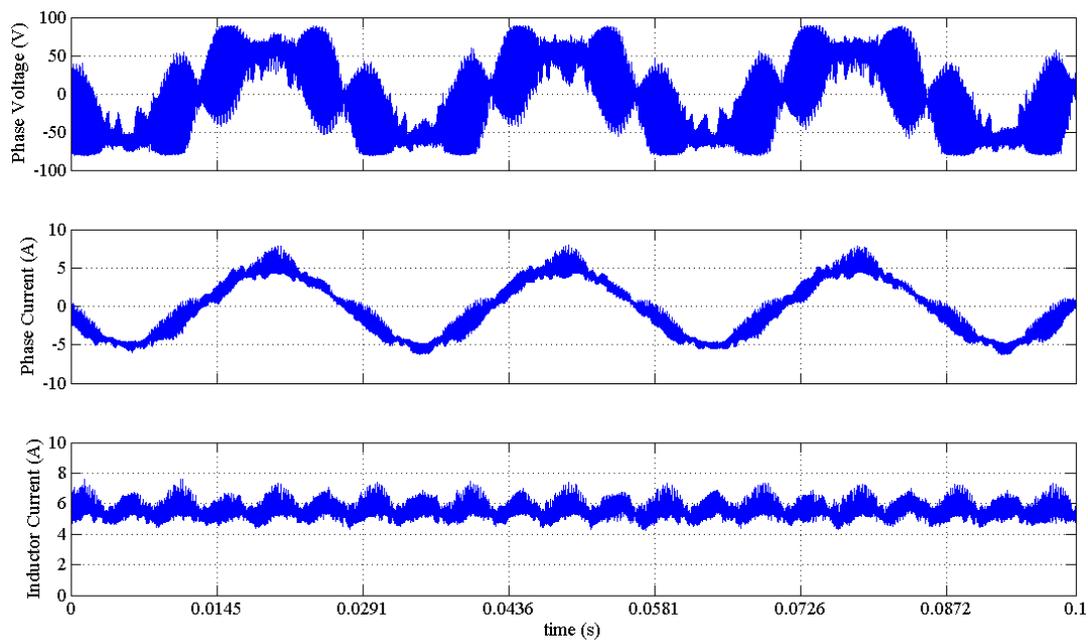


Fig. 5.29 CSI commissioning test, approx. 400W mechanical.

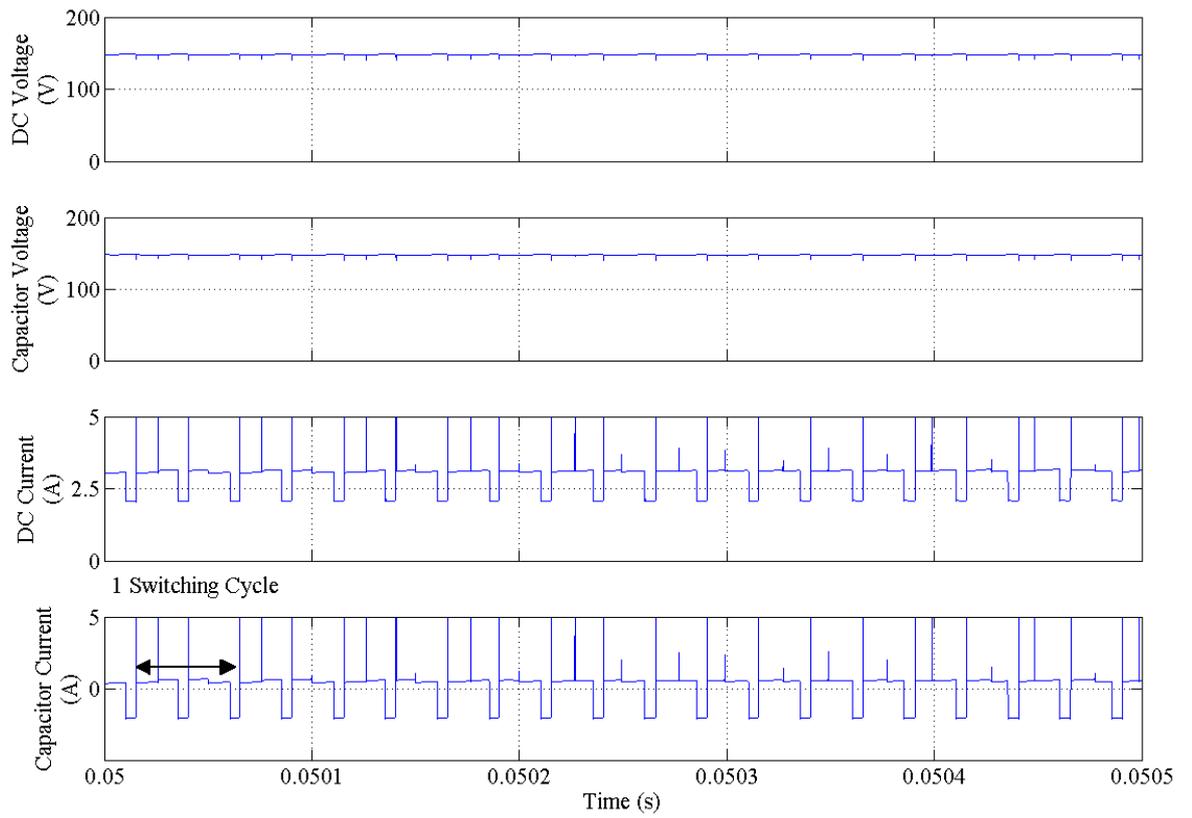
5.6 Test Results

The test hardware has been used to validate the analytical calculations and SABER simulations, from Chapters 3 and 4 respectively. VSI results will be presented for DC link and PMSM phase voltage and current waveforms at various load conditions. Similarly, for the CSI, the DC link and PMSM phase voltage and current waveforms will be presented at five load points, Figures 5.36 to 5.40. Further, the DC link will be illustrated over a reduced time period to show the PWM switching in detail at 0.5 p.u. and 1.0 p.u. load conditions. Simulated and measured results are compared, similarly PMSM phase voltage and currents are illustrate at 0.5 p.u. and 1 p.u. load conditions showing two full electrical periods and number of PWM cycles detailed. Measured data for the VSI and CSI is presented in Tables 5.5 and 5.6 respectively and relevant waveforms illustrated in Figures 5.51 and 5.52.

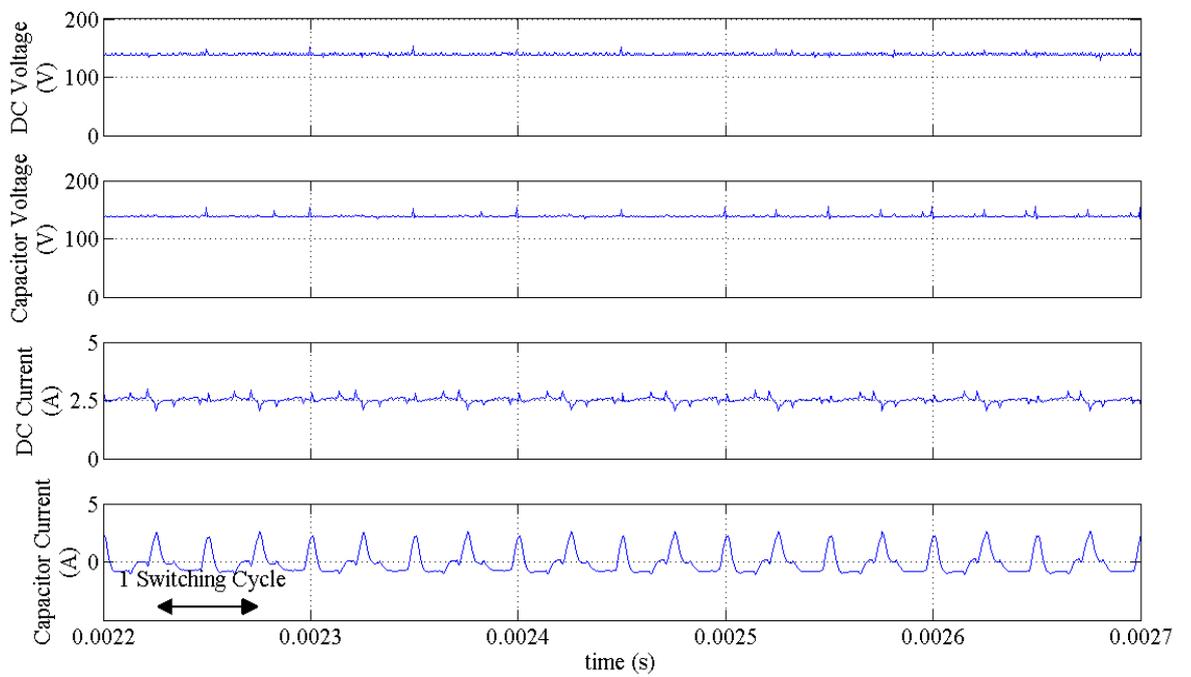
5.6.1 VSI

Figures 5.30 and 5.31 compare the DC link waveforms at 0.5 p.u. and 1.0 p.u. respectively, for simulated and measured results. The simulations show high current transients which are attributable to the numerical simulation. In Figure 5.32, both simulated and measured waveforms show the classic six-step space vector PWM modulation with additional noise on the measured waveforms arising from circuit parasitics. Figure 5.33 zooms in on the waveform transients, to highlight the problems indicative of measuring high frequency (20kHz) switched power electronic circuits. Figures 5.34 and 5.35 report the findings for the 1.0 p.u. load point and show the same trends as Figures 5.32 and 5.33. The VSI results show a good correlation between simulation and measured results. Table 5.6 lists the results for analytic, simulated and measured, where:

- P_{dc} is the DC power from the DC supply.
- P_{inv} is the DC power at the inverter terminals.
- P_{elec} is the three-phase electrical power as measured on the machine tails.
- P_{mech} is an estimation of the mechanical power based on the theoretical back-EMF and the instantaneous machine phase current.
- P_{gen} is the power generated into the load bank by the brushed DC machine.
- P_{gen} is the power generated into the load bank by the brushed DC machine.
- $P1_{Loss}$ is equal to $(P_{dc} - P_{inv})$.
- $P2_{Loss}$ is equal to $(P_{dc} - P_{elec})$.
- $P3_{Loss}$ is equal to $(P_{inv} - P_{elec})$.
- $P4_{Loss}$ is equal to $(P_{elec} - P_{mech})$.

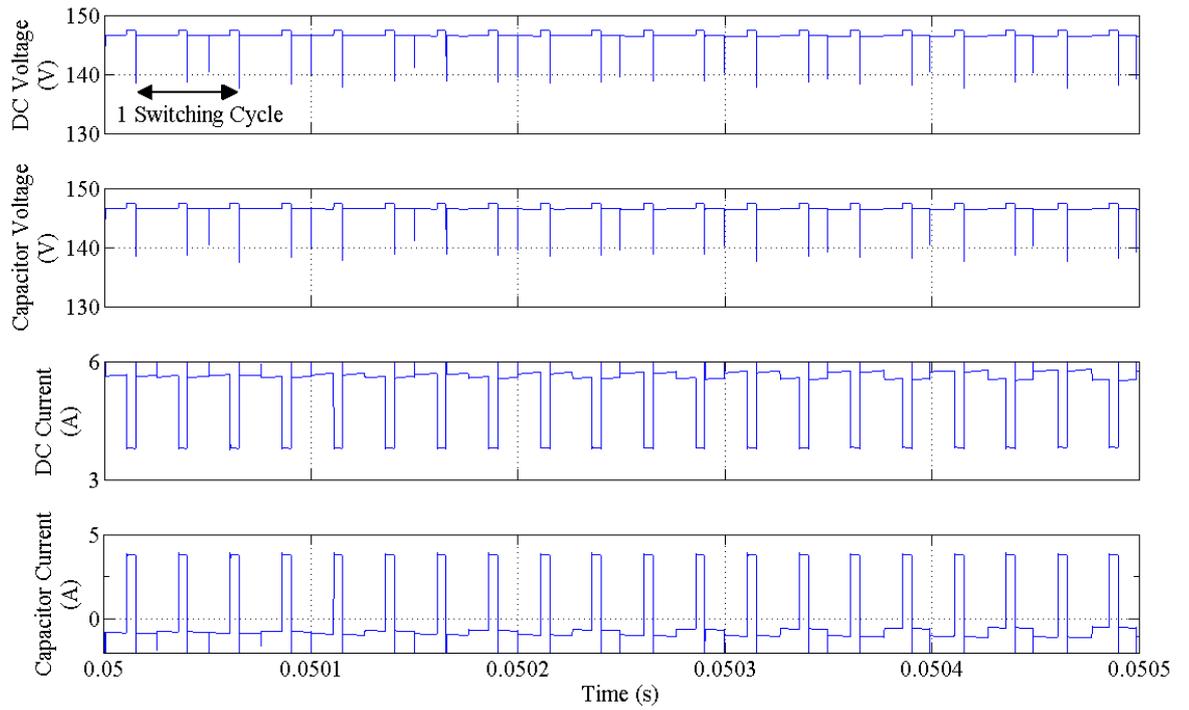


(a) Simulated waveforms (Fig 4.14 (a)).

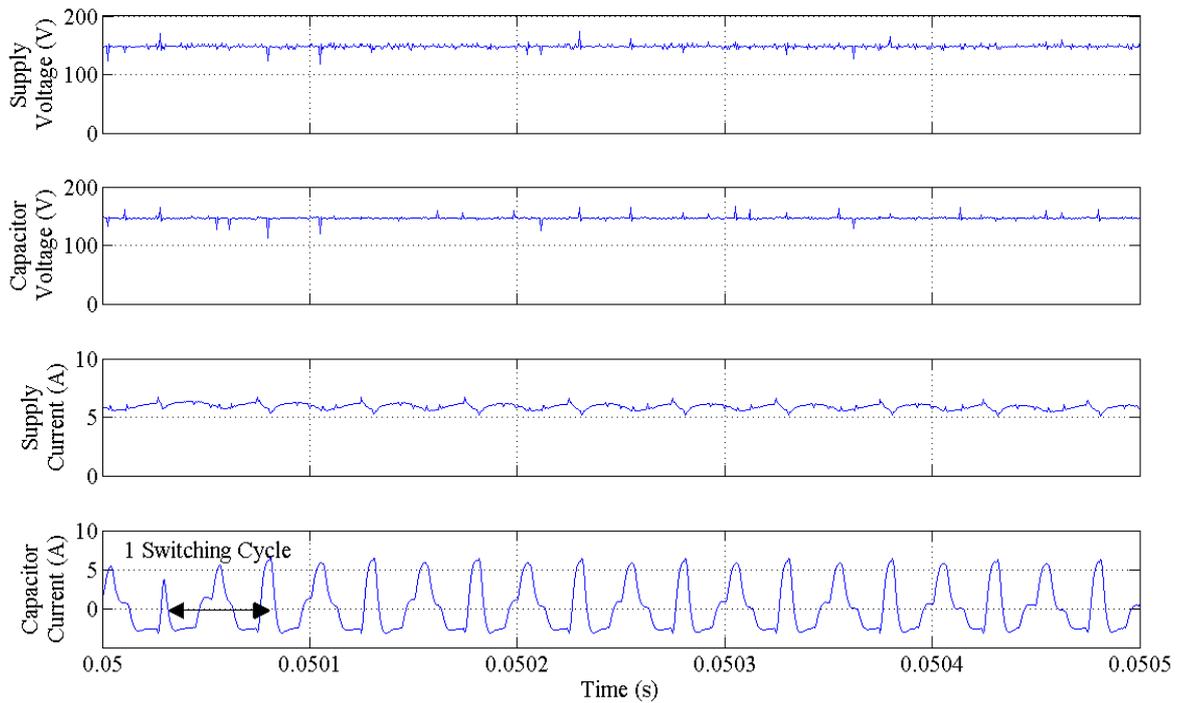


(a) Measured waveforms.

Fig. 5.30 Comparison of VSI DC link simulated and measured waveforms;
0.5 p.u load point.



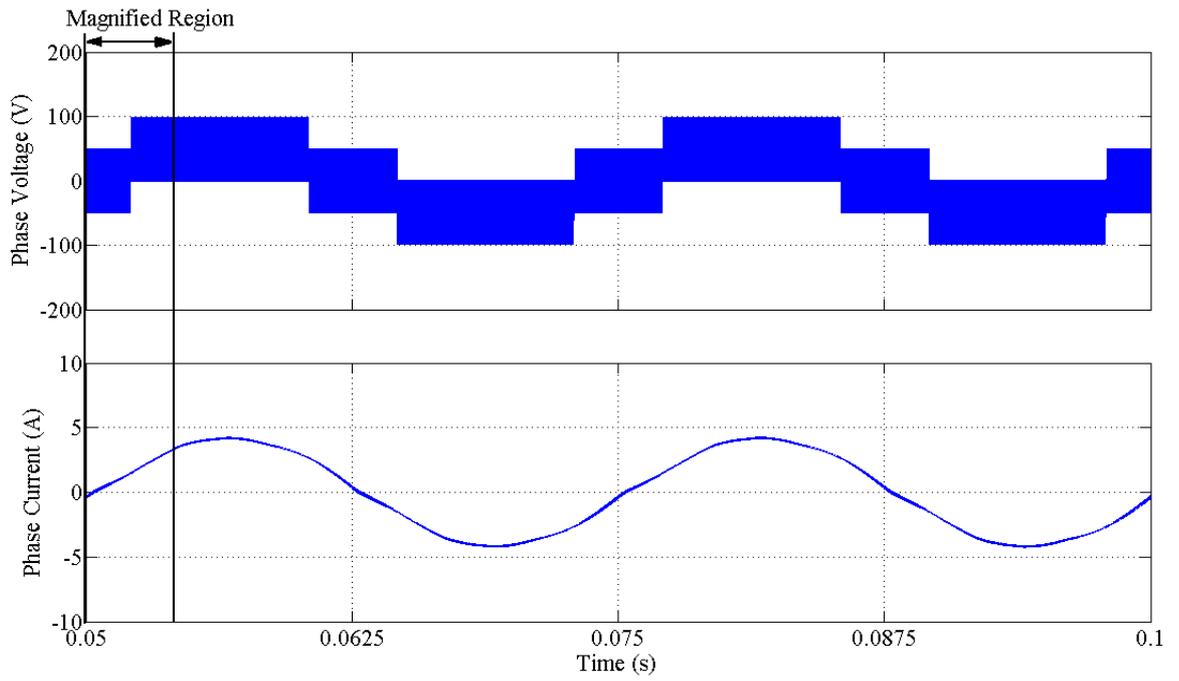
(a) Simulated waveforms (Fig 4.14 (b)).



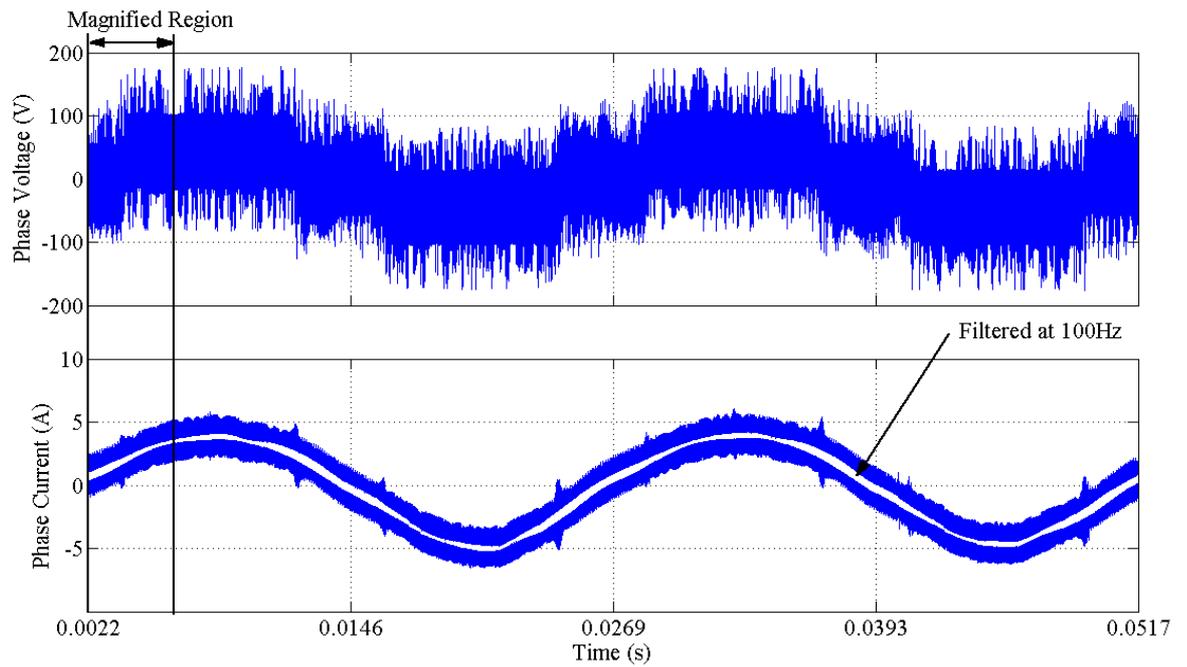
(b) Measured waveforms.

Fig. 5.31 Comparison of VSI DC link simulated and measured waveforms;

1 p.u load point.



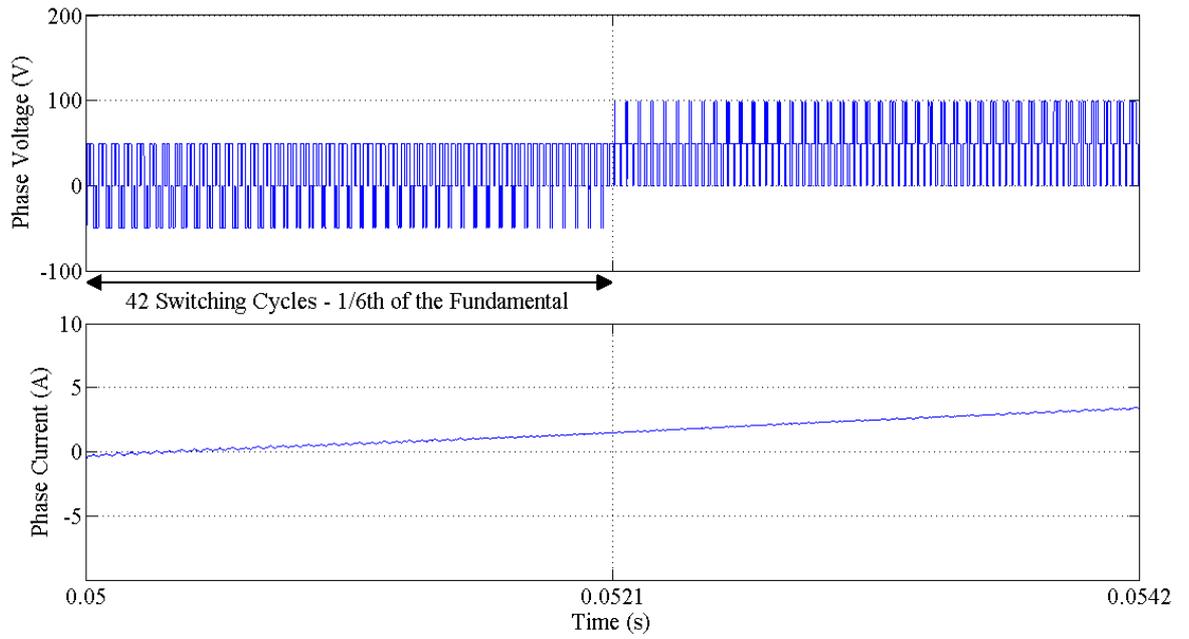
(a) Simulated waveforms (Fig 4.15 (a)).



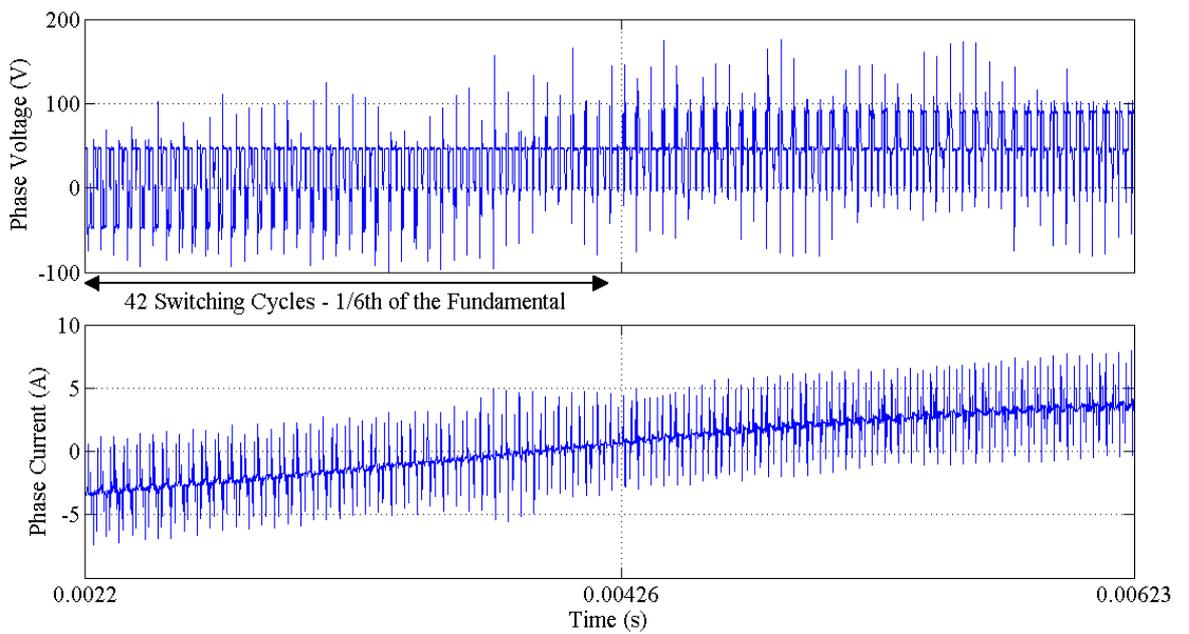
(b) Measured waveforms (white line superimposed on measured results).

Fig. 5.32 Comparison of VSI simulated and measured waveforms;

0.5 p.u load point.

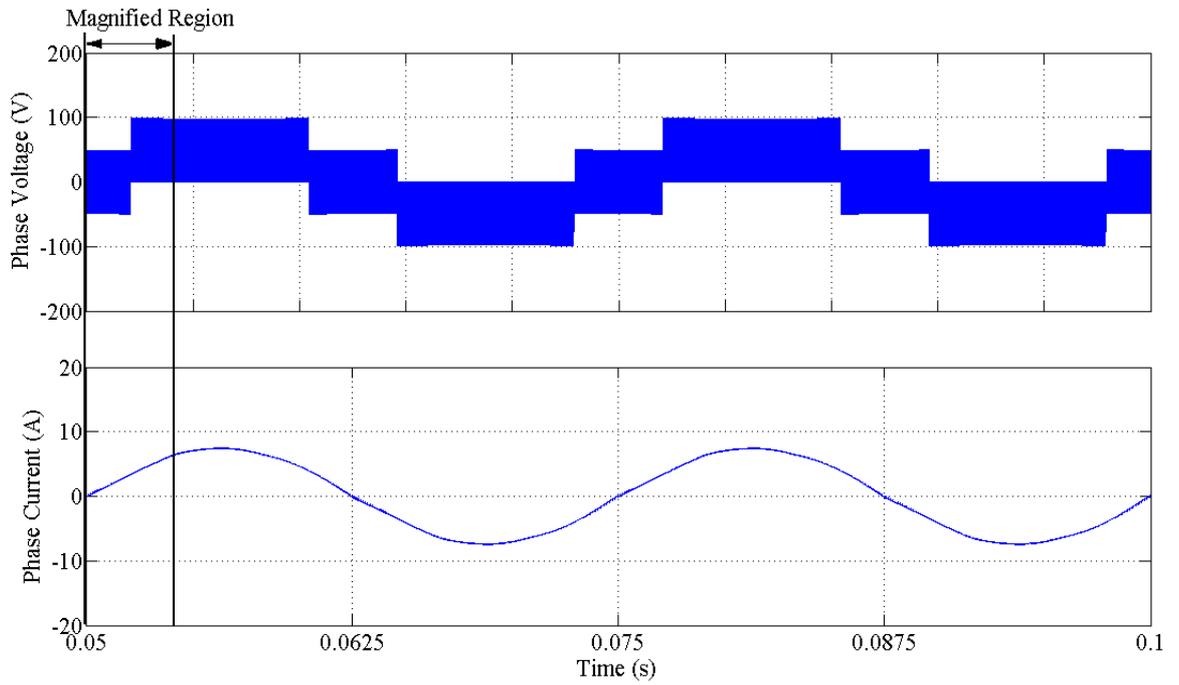


(a) Simulated waveforms (Fig 4.16 (a)).

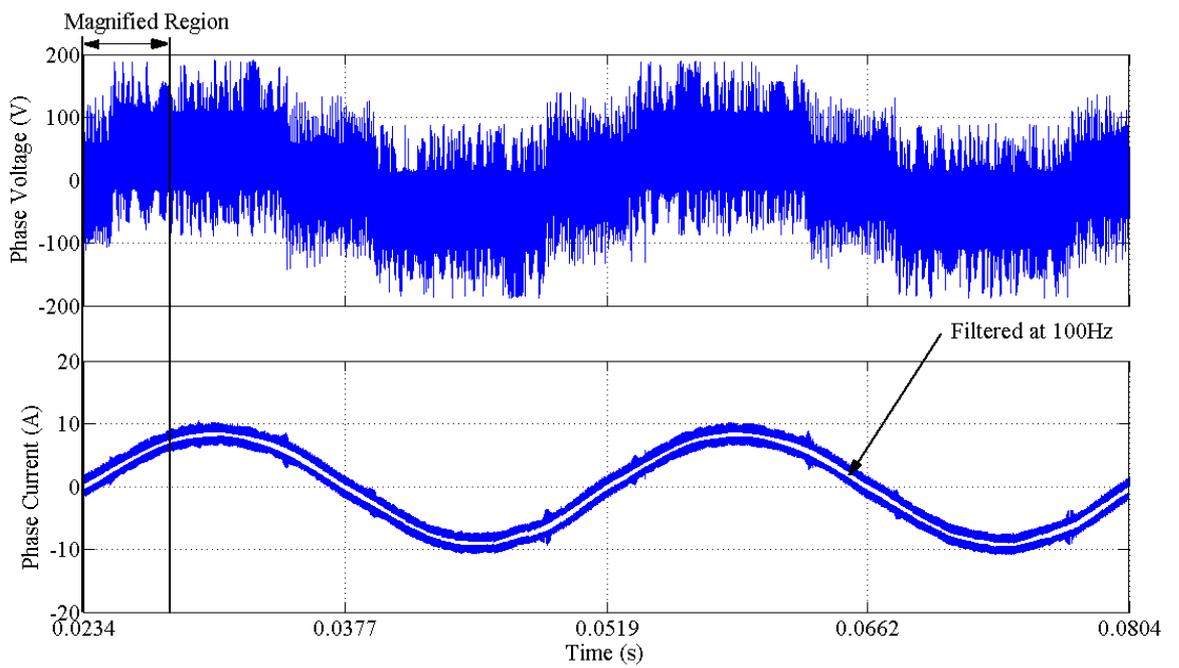


(b) Measured waveforms.

Fig. 5.33 Comparison of VSI simulated and measured waveforms; 0.5 p.u load point, magnified region highlighted in Fig. 5.32.



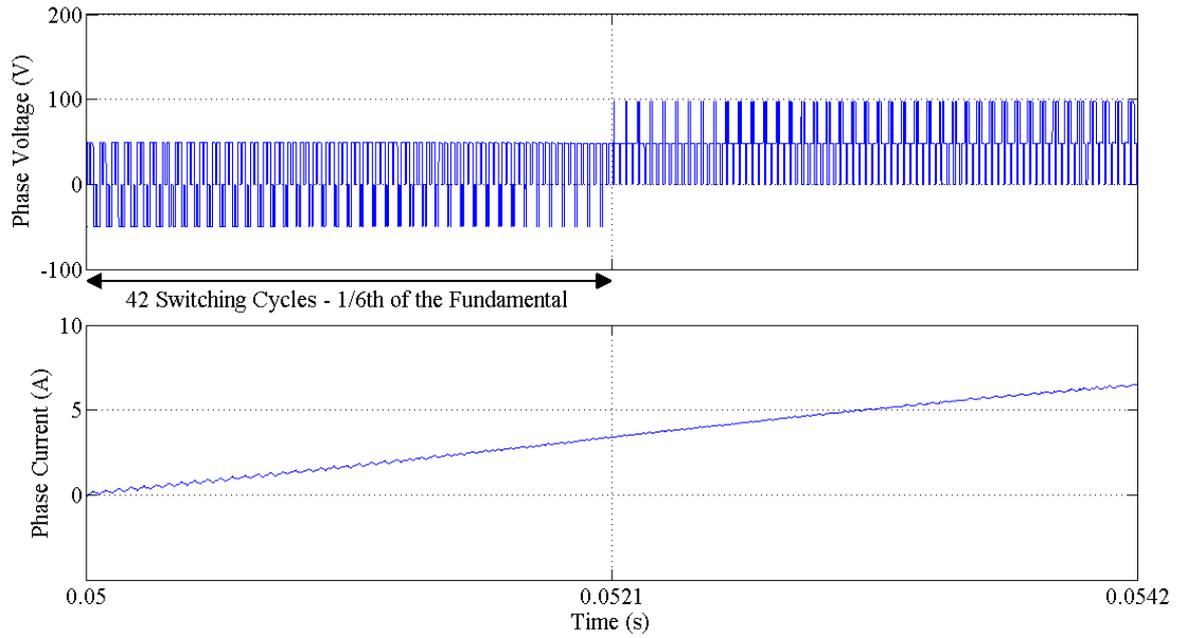
(a) Simulated waveforms (Fig 4.15 (b)).



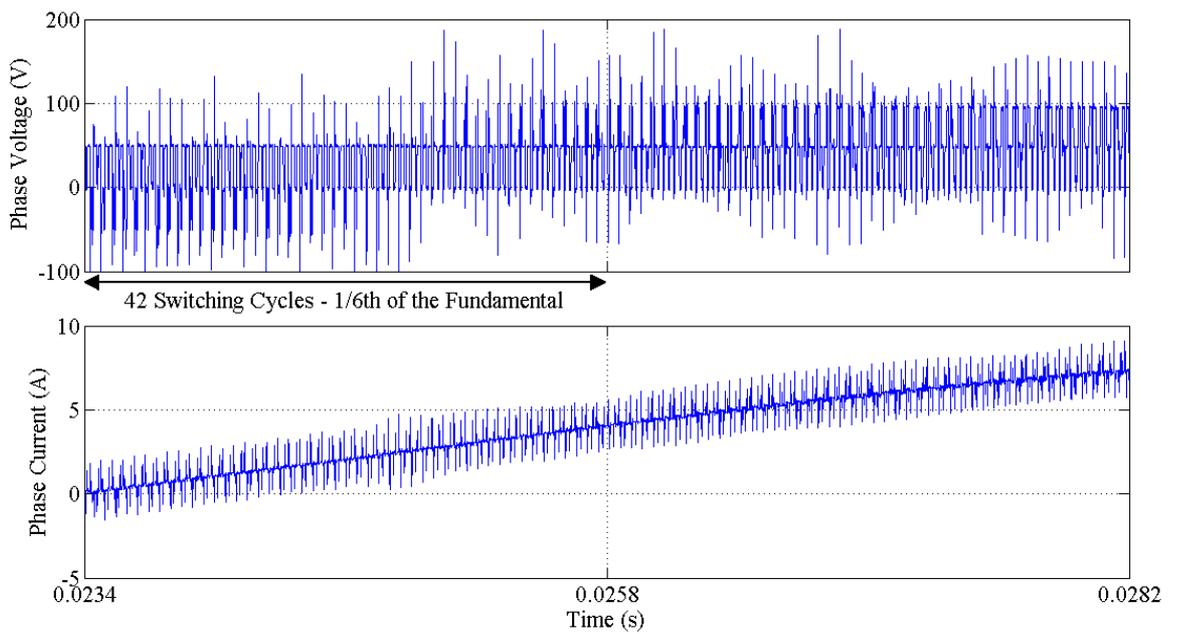
(b) Measured waveforms (white line superimposed on measured results).

Fig. 5.34 Comparison of VSI simulated and measured waveforms;

1 p.u load point.



(a) Simulated waveforms (Fig 4.16 (b)).



(b) Measured waveforms.

Fig. 5.35 Comparison of VSI simulated and measured waveforms; 1 p.u load point, magnified region highlighted in Fig. 5.34.

Analysers	Vdc	Idc	Pdc	Pinv	Pinv	Vrms	Irms	Pelec	P2Loss	P3Loss	Pmech (est)	P4Loss	Pgen
0	119.07	0.35	42.15	NA	NA	52.20	0.33	37.47	4.68	NA	44.46	-6.99	26.81
25	125.00	1.65	206.18	NA	NA	52.80	1.56	197.43	8.75	NA	210.78	-13.35	71.84
50	140.17	3.26	457.47	NA	NA	57.57	3.03	421.89	35.58	NA	416.07	5.82	133.77
75	148.95	4.46	663.72	NA	NA	59.08	4.43	624.39	39.33	NA	590.54	33.85	197.31
92	149.58	5.76	860.99	NA	NA	57.90	6.16	824.13	36.86	NA	732.30	91.83	239.86
Oscilloscope	Vdc	Idc	Pdc	Pinv	Pinv	Vrms	Irms	Pelec	P2Loss	P3Loss	Pmech	P4Loss	Pgen
0	118.63	0.34	47.38	NA	NA	53.23	113.78	39.74	7.65	NA	45.21	-5.48	26.81
25	124.09	1.76	218.14	NA	NA	54.95	102.86	210.11	8.03	NA	216.11	-6	71.84
50	138.41	3.16	436.71	NA	NA	59.16	98.73	423.53	13.18	NA	418.14	5.39	133.77
75	146.50	4.45	651.61	NA	NA	61.09	96.14	624.80	26.81	NA	600.68	24.12	197.31
92	146.71	5.74	842.82	NA	NA	59.41	92.82	791.79	51.03	NA	734.95	56.84	544.11
Simulation	Vdc	Idc	Pdc	Pinv	P1Loss	Vrms	Irms	Pe	P2Loss	P3Loss	Pmech	P4Loss	Pgen
0	149.2	0.33	48.64	48.51	0.13	59.4	0.3	42.25	6.39	6.26	41.87	0.38	NA
25	149.3	1.44	215.4	215.1	0.3	60.07	1.48	207.88	7.52	7.22	202.79	5.09	NA
50	149.3	2.87	428.74	428.16	0.58	60.73	2.95	420.11	8.63	8.05	401.04	19.07	NA
75	149.3	4.46	666.43	665.52	0.91	61.73	4.52	656.29	10.14	9.23	612.32	43.97	NA
100	146.69	5.31	779.08	778.03	1.05	61	5.25	767.66	11.42	10.37	709.67	57.99	NA

Note: P1Loss = (Pdc – Pinv); P2Loss = (Pdc – Pelec); P3Loss = (Pinv – Pelec); P4Loss = (Pelec – Pmech).

Table 5.6 VSI results comparison.

5.6.2 CSI

Figures 5.36 to 5.40 present the DC link currents of interest and the PMSM phase voltage and current measured waveforms from no-load to the 1.0 p.u. load point. The set of waveforms are included from no-load to 1.0 p.u. load at 0.25 p.u. increments to illustrate the trends of these waveforms and for general completeness of the thesis documentation. As can be noted, the DC link waveforms contain the expected 6th harmonic of the phase voltage fundamental in addition to PWM switching event components. Although relatively noisy, the phase current waveform is essentially a sinusoidal fundamental frequency plus switching related harmonics, confirmed by the FFTs of the phase current and voltage waveforms, as illustrated in Figure 5.41 and 5.42 respectively. The FFTs show that the magnitude of the fundamental frequency is significantly higher than the other frequencies, which are made up of the switching frequency and its harmonics. Methods have been reported [44,47] to minimise these effects but have not been considered in this thesis due to time constraints.

Figure 5.43 and 5.44 illustrate the DC link waveforms in more detail. For example, Figure 5.43 (a) and 5.44 (a) represent the DC link waveforms at the 0.5 p.u. and .01 p.u. load points respectively, each identifying regions of interest, shown in (b) and (c) of the respective figures. These figures illustrate the fundamentals of inductor current control, where the inductor current is essentially 5A and 11A at the respective load conditions. The figures also show that the short circuit current through the IGBT and diode, and the consequential impact on the DC input current and inverter input current. The high frequency (40kHz; i.e. two times the 20kHz PWM due to space vector modulation) and improvement of the DC link current is an area of interest for further study.

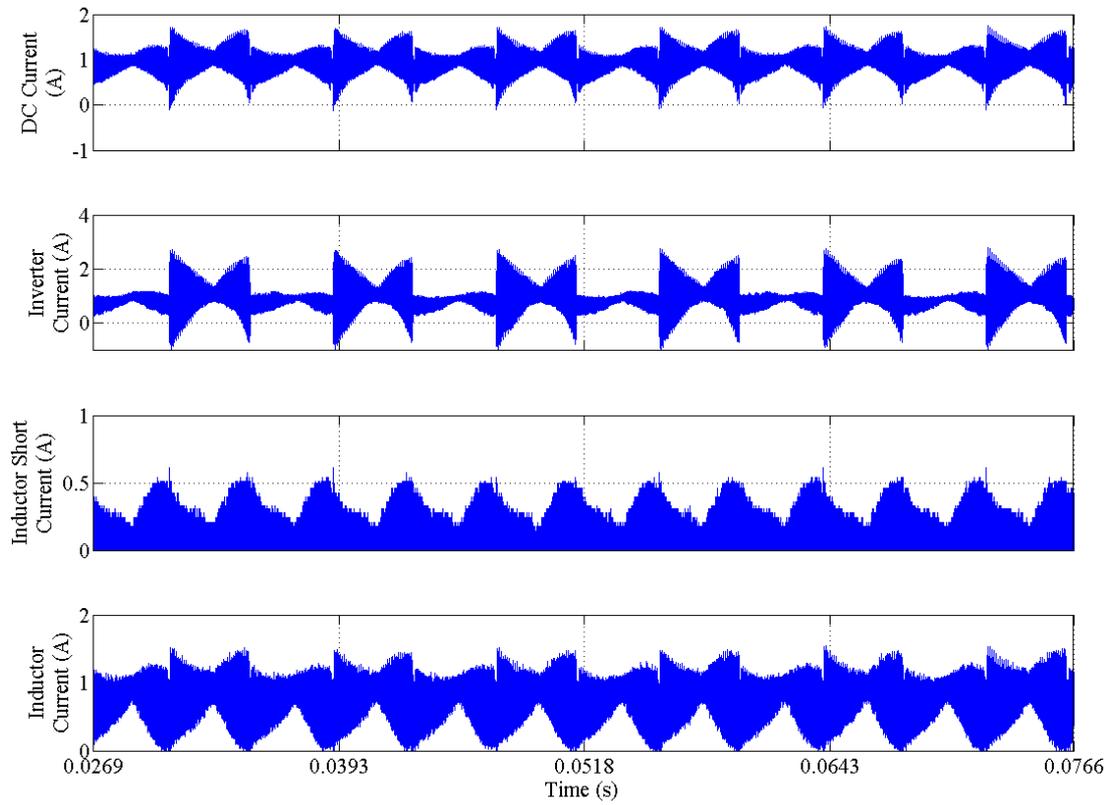
Comparison of the simulated and measured DC link waveforms are made in Figures 5.45 and 5.46. The square edges of the simulated waveforms are a result of the time-step and model limitations, however, they do not impact on the global link and phase RMS currents. Comparison of the simulated and measured phase voltage and current waveforms are made in Figures 5.47 to 5.50. The measured voltage and current waveforms show a good comparison to the simulated waveforms. Figures 5.47 and 5.49 have been superimposed with 100Hz low-pass filtered voltage and current waveforms on the measured results to illustrate the waveform fundamental for comparison with simulation. Again, good correlation is evident. Figures 5.48 and 5.50 detail the voltage and current waveforms

transients of the 0.5 p.u. and 1 p.u. load points respectively, showing the previously discussed problems with the measurements.

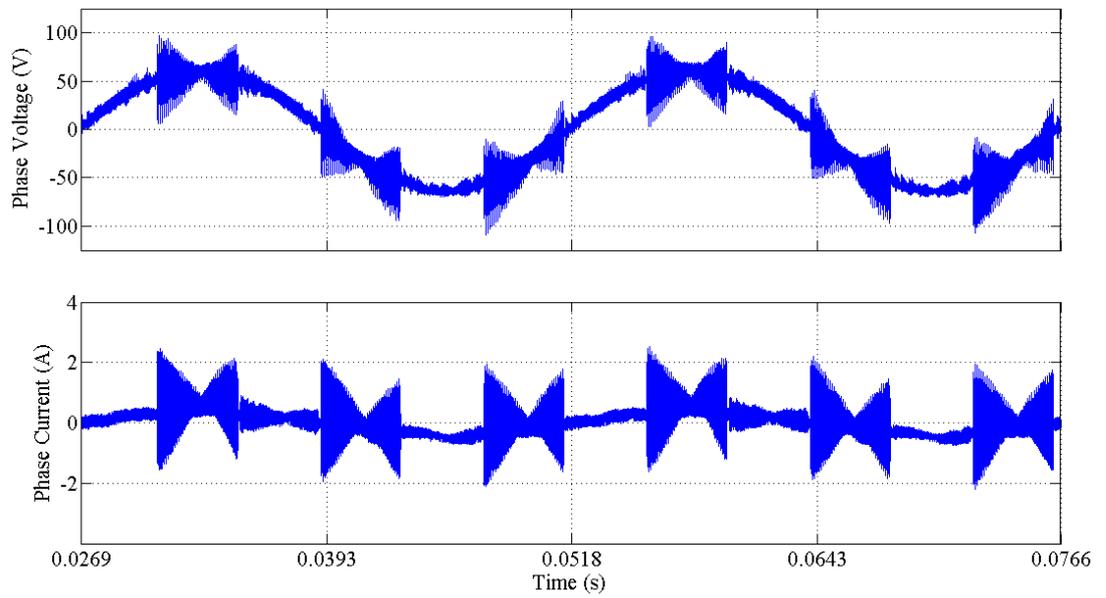
Table 5.7 summarises the test data and comparisons that are made for the DC values and power measurements in Figure 5.51 and 5.52 respectively. The DC link losses and DC-to-AC conversion losses show good correlation between analytic and simulated and this is probably due to similar assumptions in waveform shape being made in both cases. Overall the measured losses are higher by a factor of approximately two, indicating that more work is needed in this area to improve the correlation. However, it must be borne in mind that the quantities measured are low values and measurement sensitivity could have a major impact on the loss estimates. To address the measurement accuracy issue, power audits from DC supply to DC dissipated load are presented in Figure 5.53, which illustrates the power comparison between the VSI and CSI systems. The graphs show good correlation between DC generated power (i.e. the PMSM load), the estimated mechanical output power and the inverter input power, the DC input power is higher due to the increased losses in the CSI system, attributable to the link inductor and flyback circuitry.

Finally Table 5.8 summarises the results for Figure 5.53. Note, Table 5.7 the following abbreviations are used:

- P_{dc} is the DC power from the DC supply.
- P_{inv} is the DC power at the inverter terminals.
- P_{elec} is the three-phase electrical power as measured on the machine tails.
- P_{mech} is an estimation of the mechanical power based on the theoretical back-EMF and the instantaneous machine phase current.
- P_{gen} is the power generated into the load bank by the brushed DC machine.
- $P1Loss$ is equal to $(P_{dc} - P_{inv})$.
- $P2Loss$ is equal to $(P_{dc} - P_{elec})$.
- $P3Loss$ is equal to $(P_{inv} - P_{elec})$.
- $P4Loss$ is equal to $(P_{elec} - P_{mech})$.

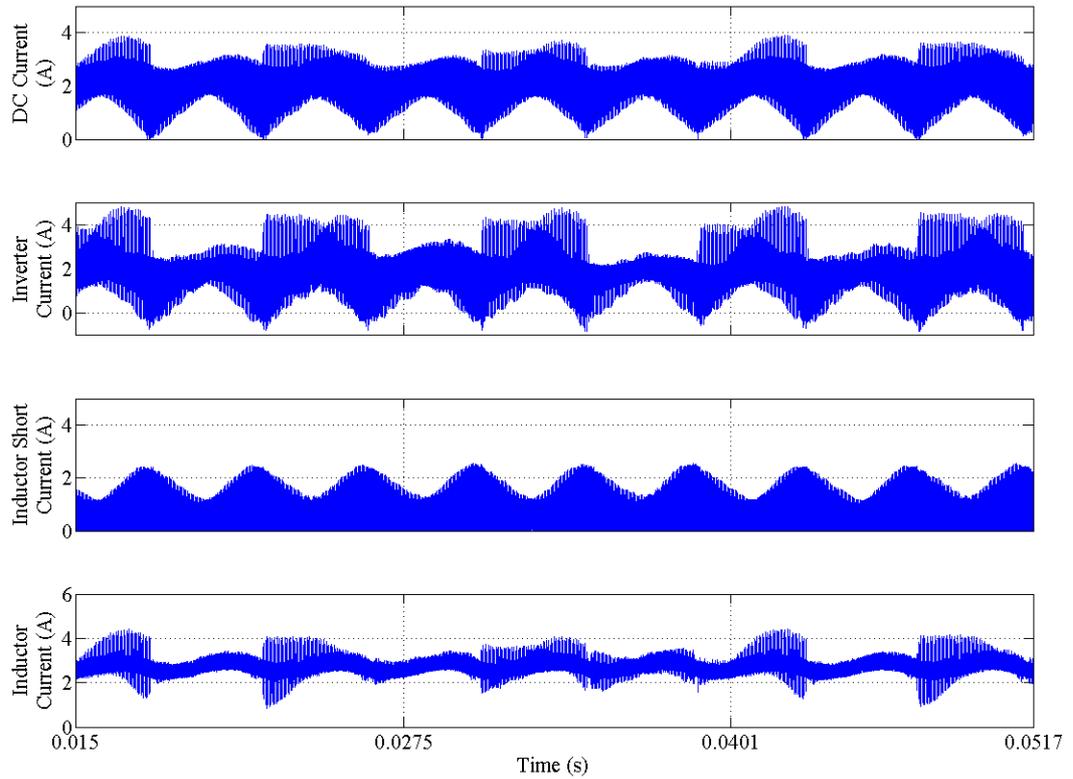


(b) DC link waveforms.

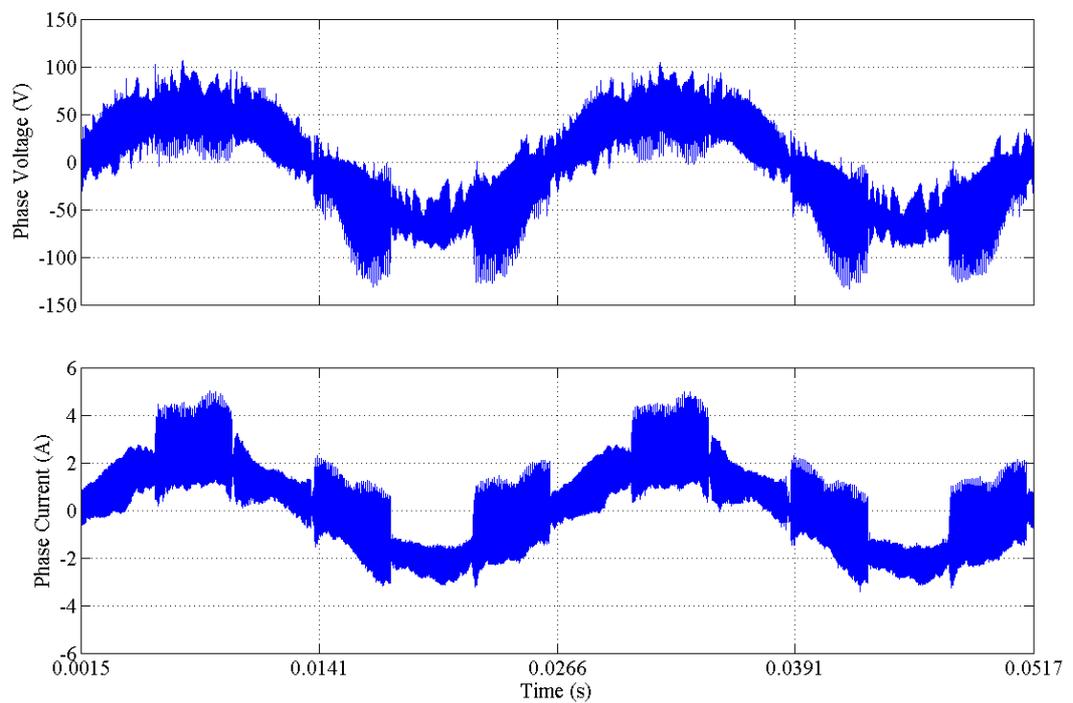


(c) PMSM phase voltage and current.

Fig. 5.36 CSI phase waveform overview;
2 cycles of the fundamental at no load point.

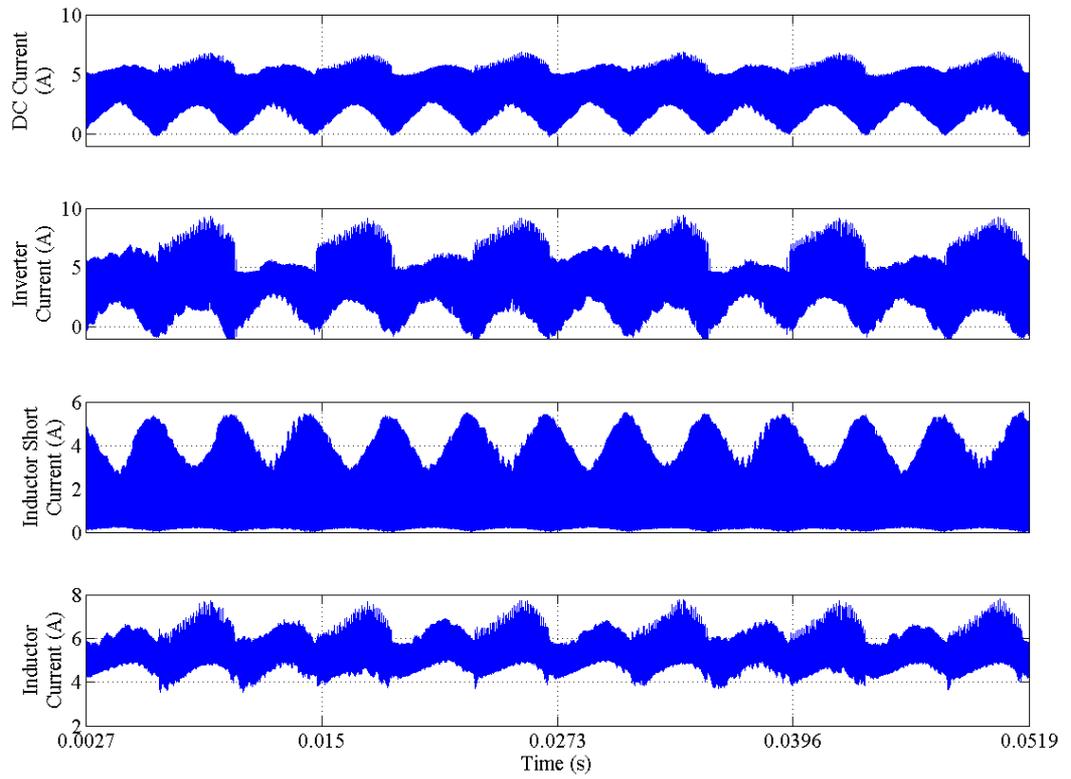


(a) DC link waveforms.

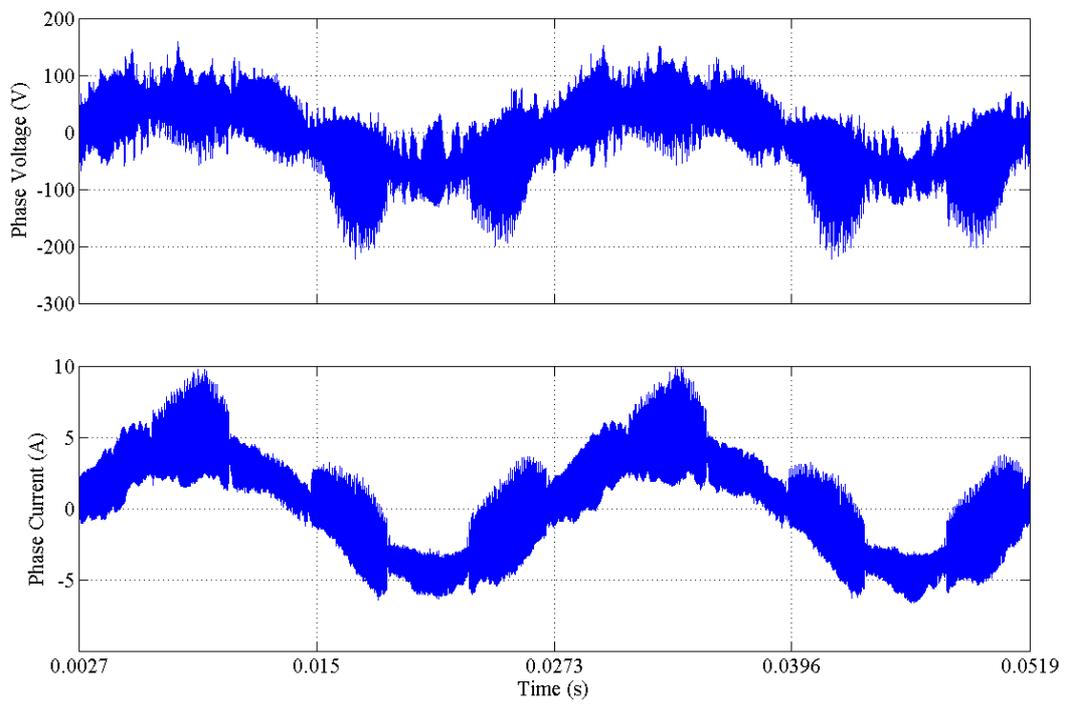


(b) PMSM phase voltage and current.

Fig. 5.37 CSI phase waveform overview;
 2 cycles of the fundamental at 0.25 p.u load point.

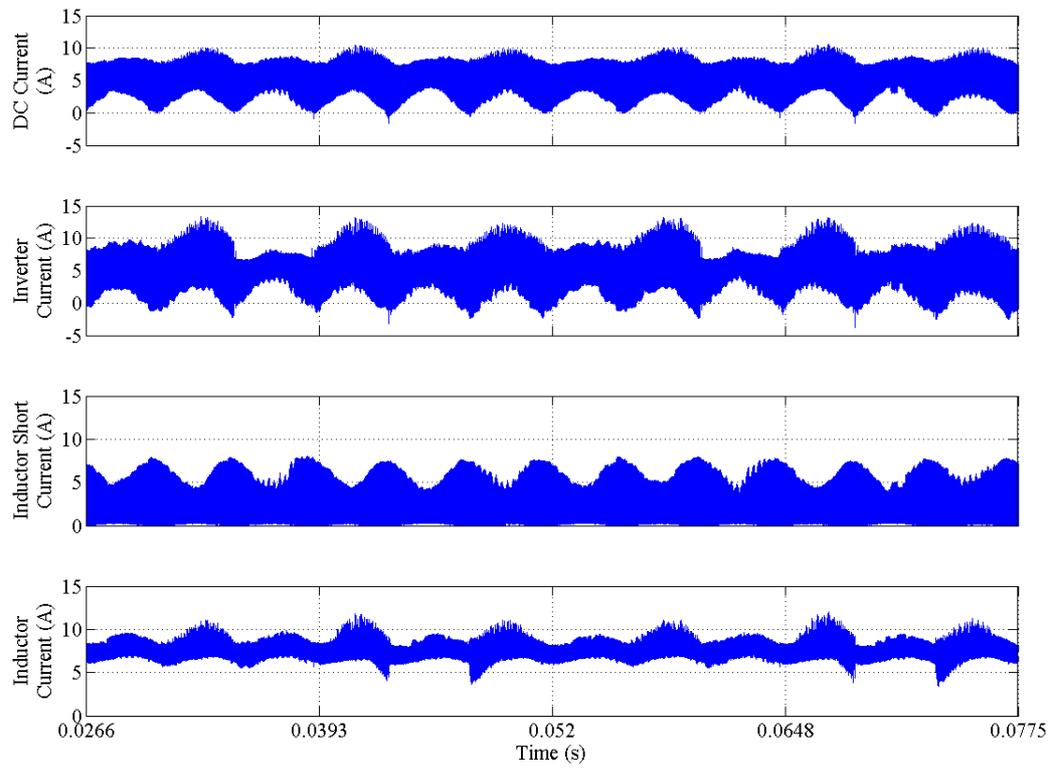


(a) DC link waveforms.

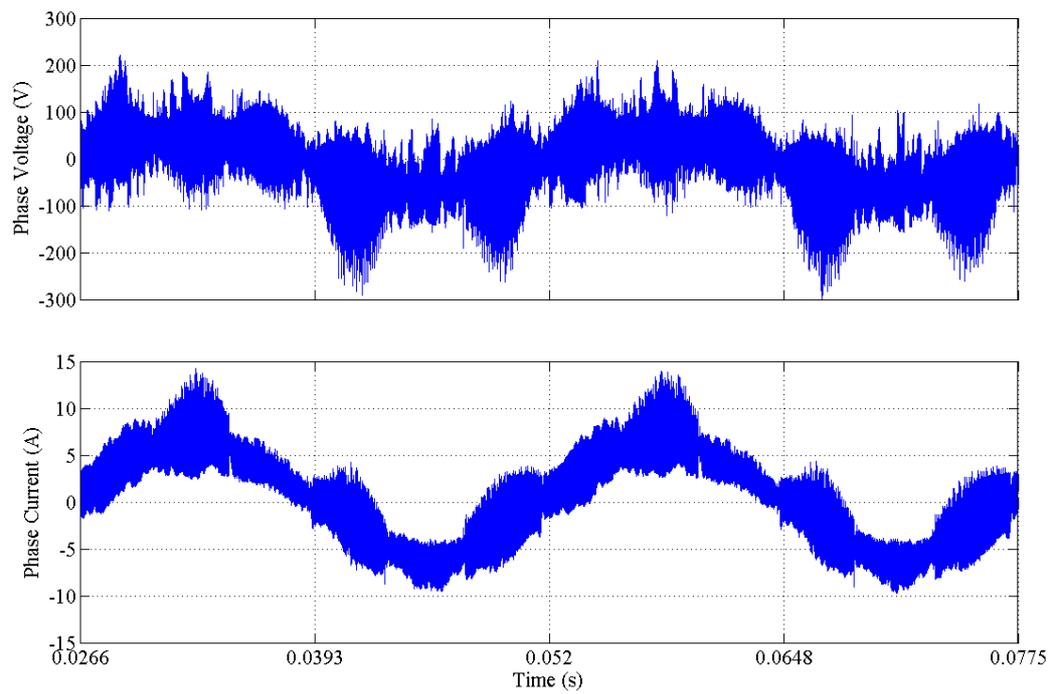


(b) PMSM phase voltage and current.

Fig. 5.38 CSI phase waveform overview;
 2 cycles of the fundamental at 0.5p.u load point.

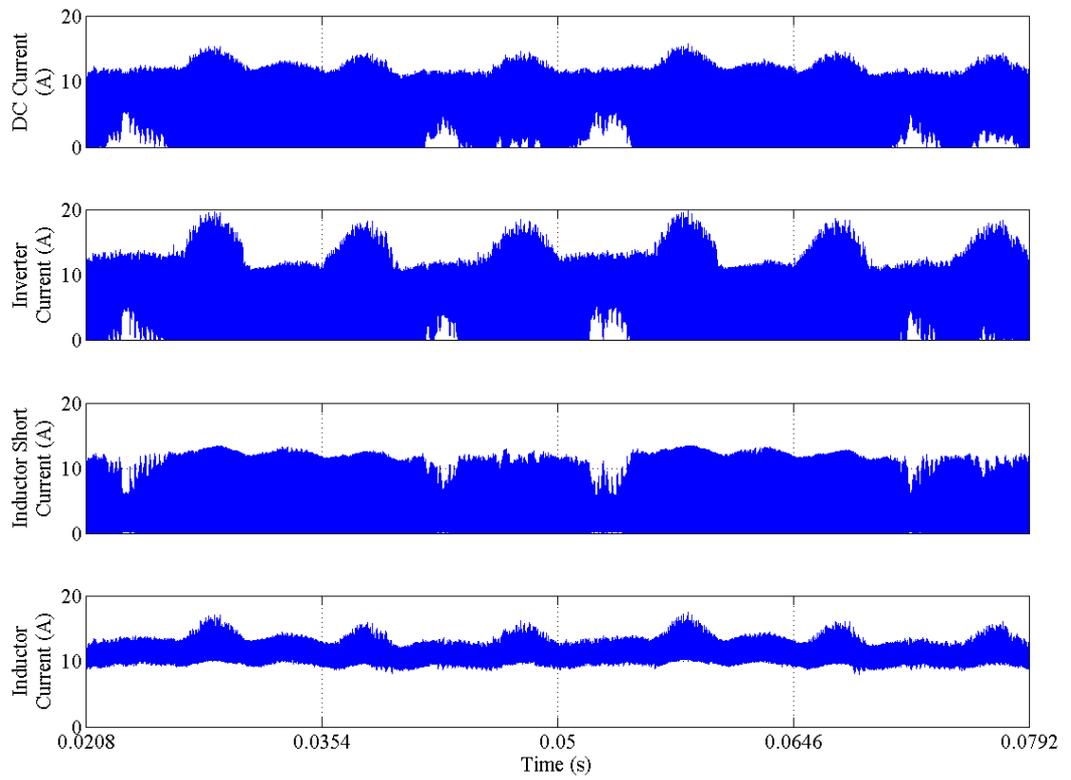


(a) DC link waveforms.

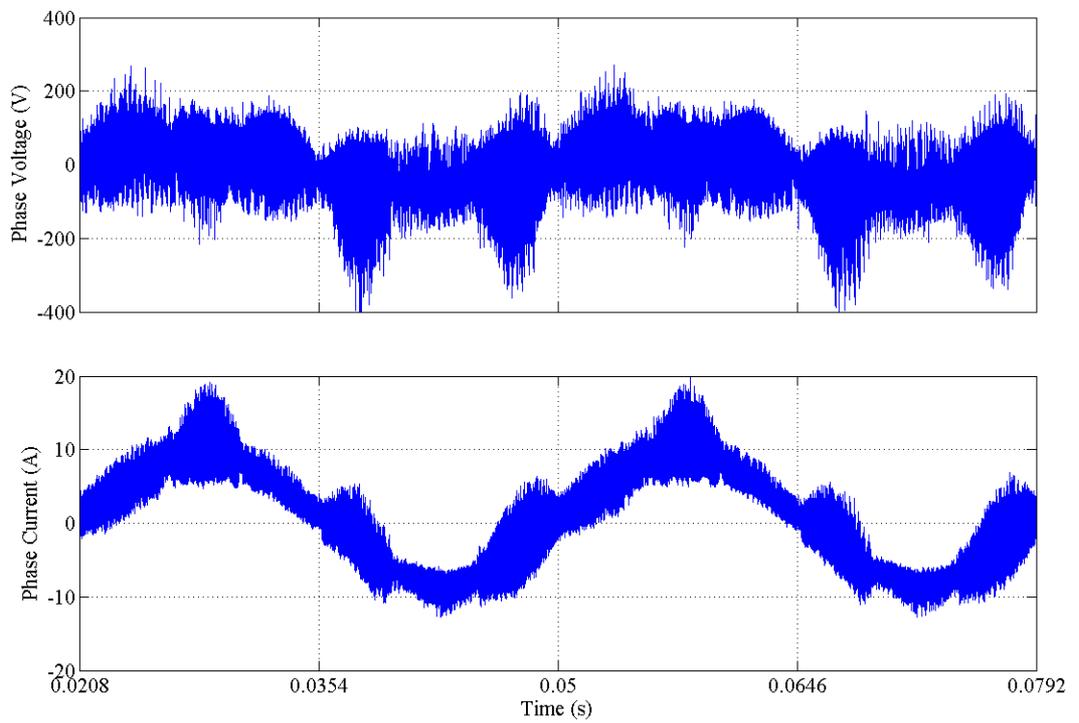


(b) PMSM phase voltage and current.

Fig. 5.39 CSI phase waveform overview;
2 cycles of the fundamental at 0.75p.u load point.

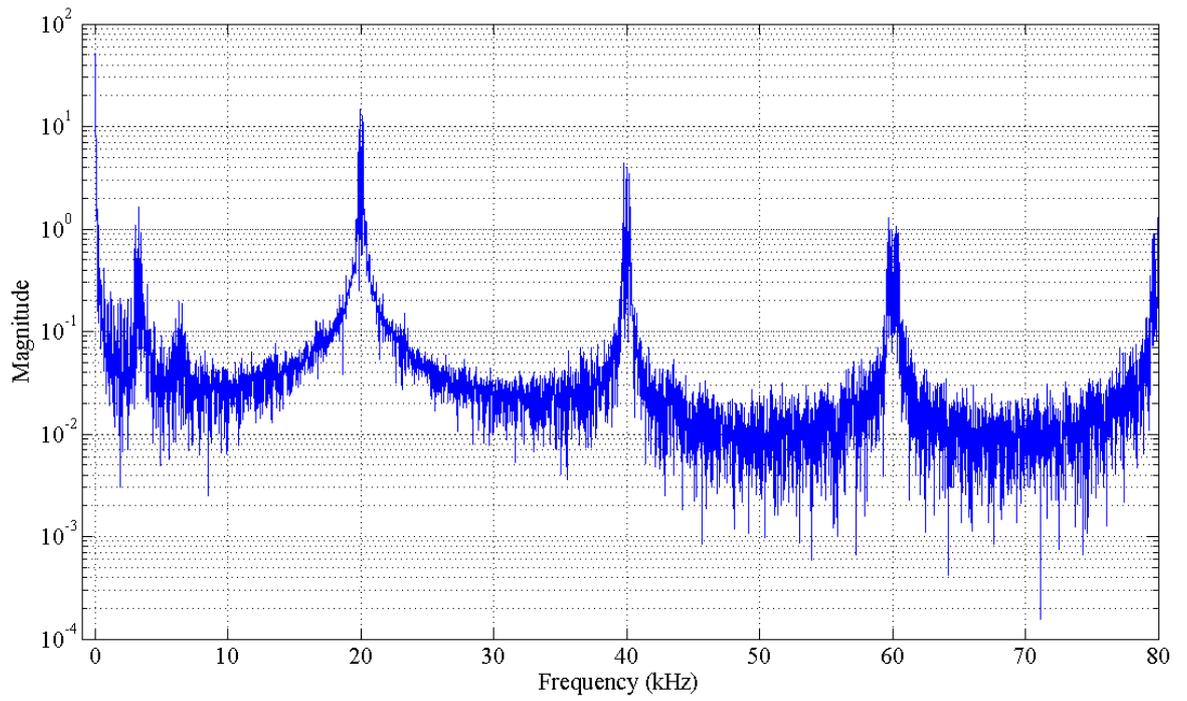


(a) DC link waveforms

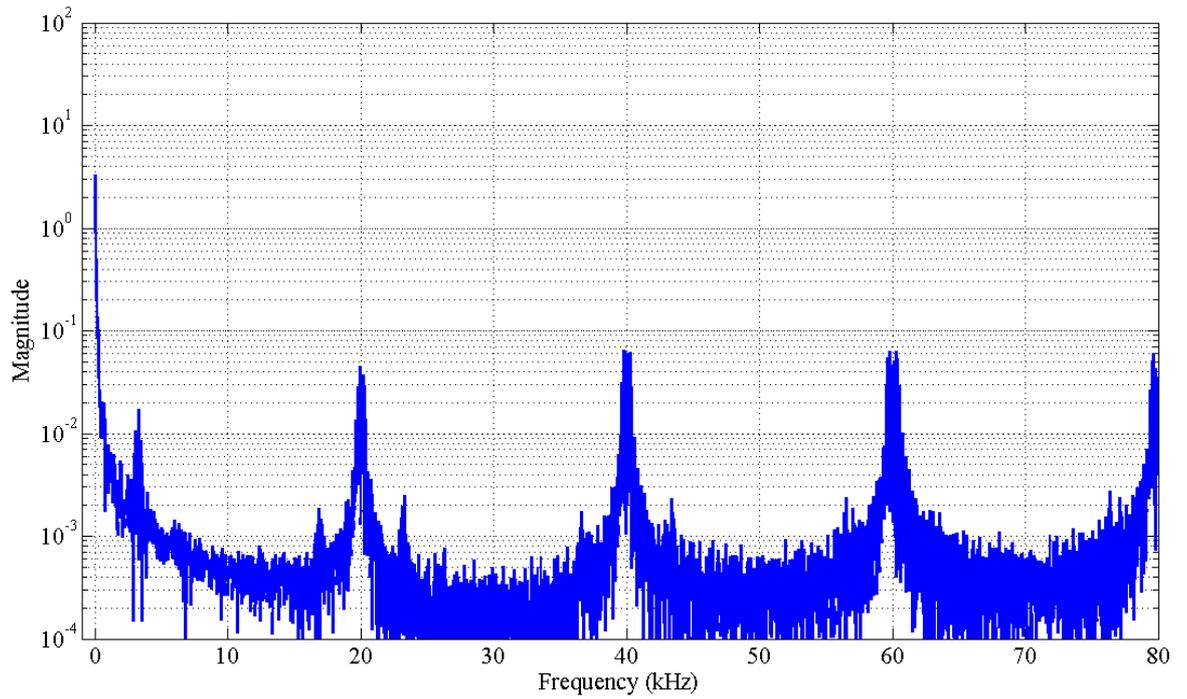


(b) PMSM phase voltage and current.

Fig. 5.40 CSI phase waveform overview;
2 cycles of the fundamental at 1 p.u. load point.

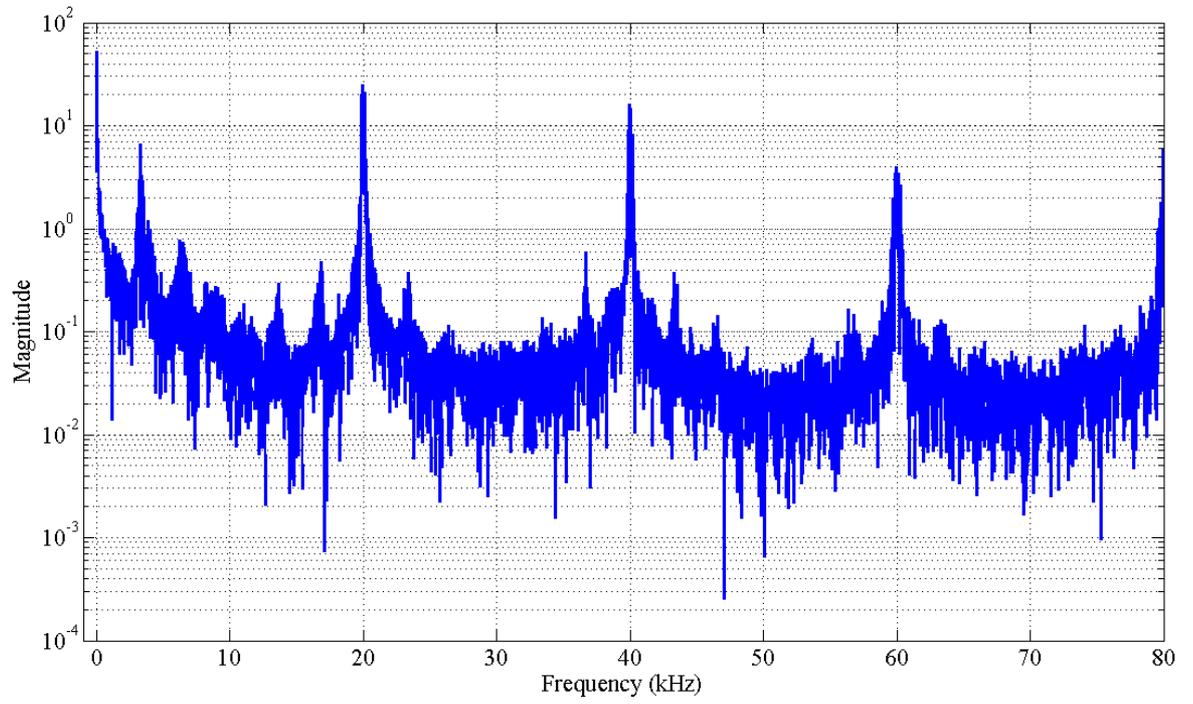


(a) Voltage waveform FFT result.

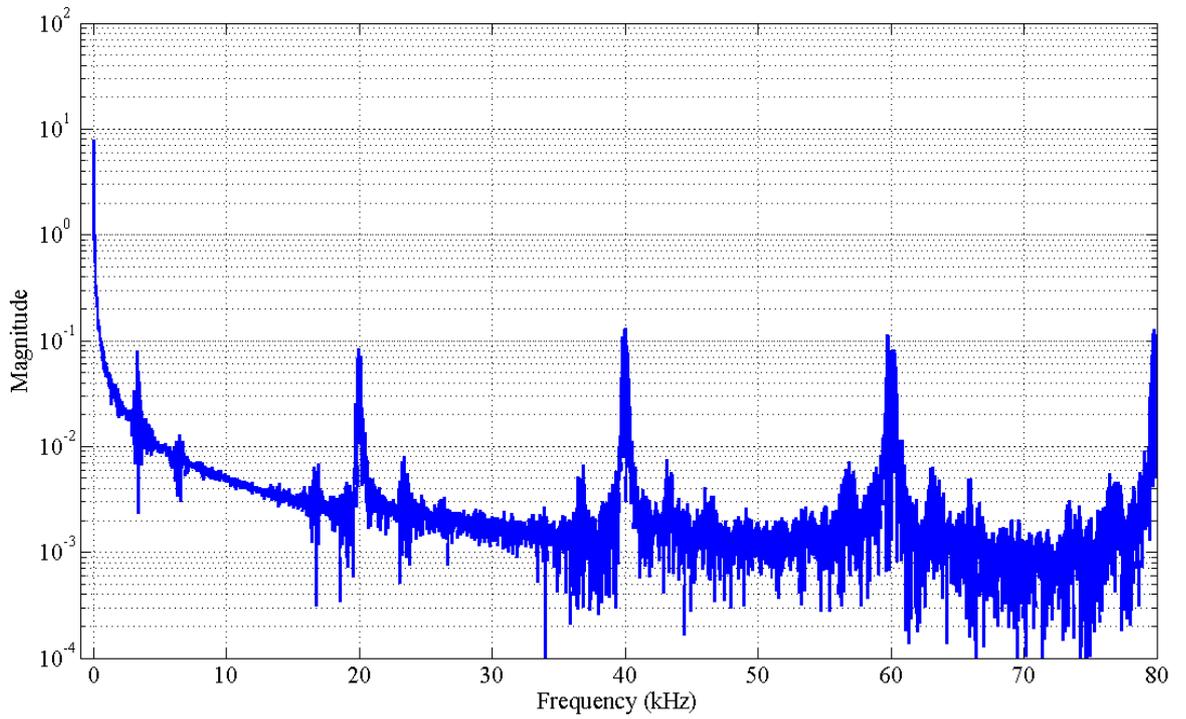


(b) Current waveform FFT result.

Fig. 5.41 CSI FFT analysis; 0.5 p.u. load point.

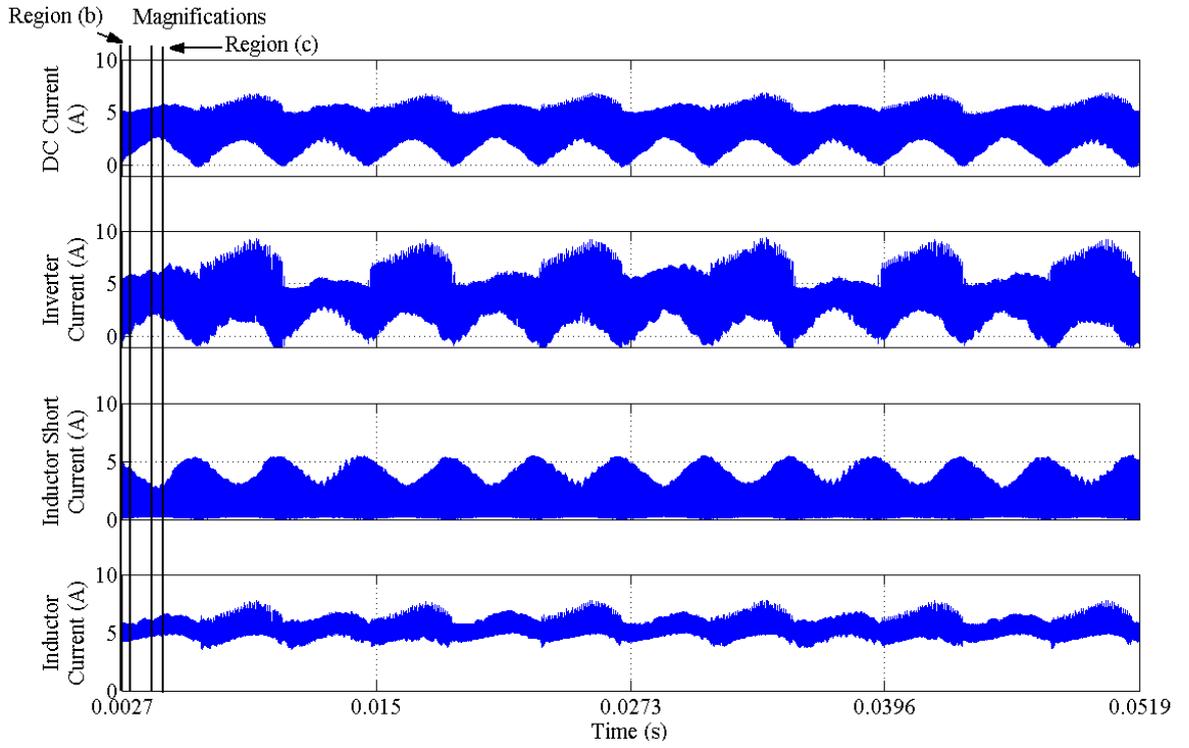


(a) Voltage waveform FFT result.

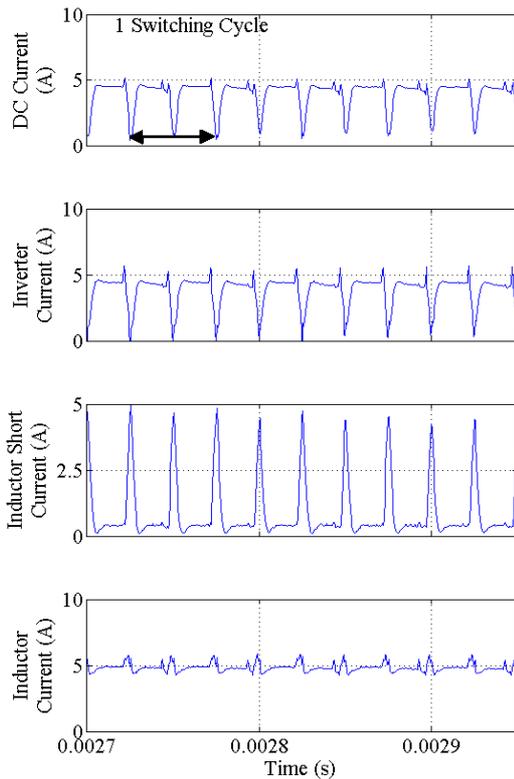


(b) Current waveform FFT result.

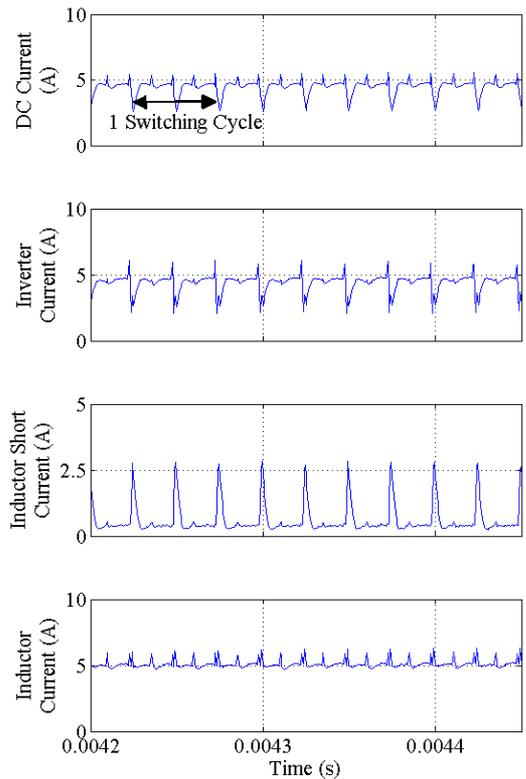
Fig. 5.42 CSI FFT analysis; 1 p.u. load point.



(a) Waveform envelopes.

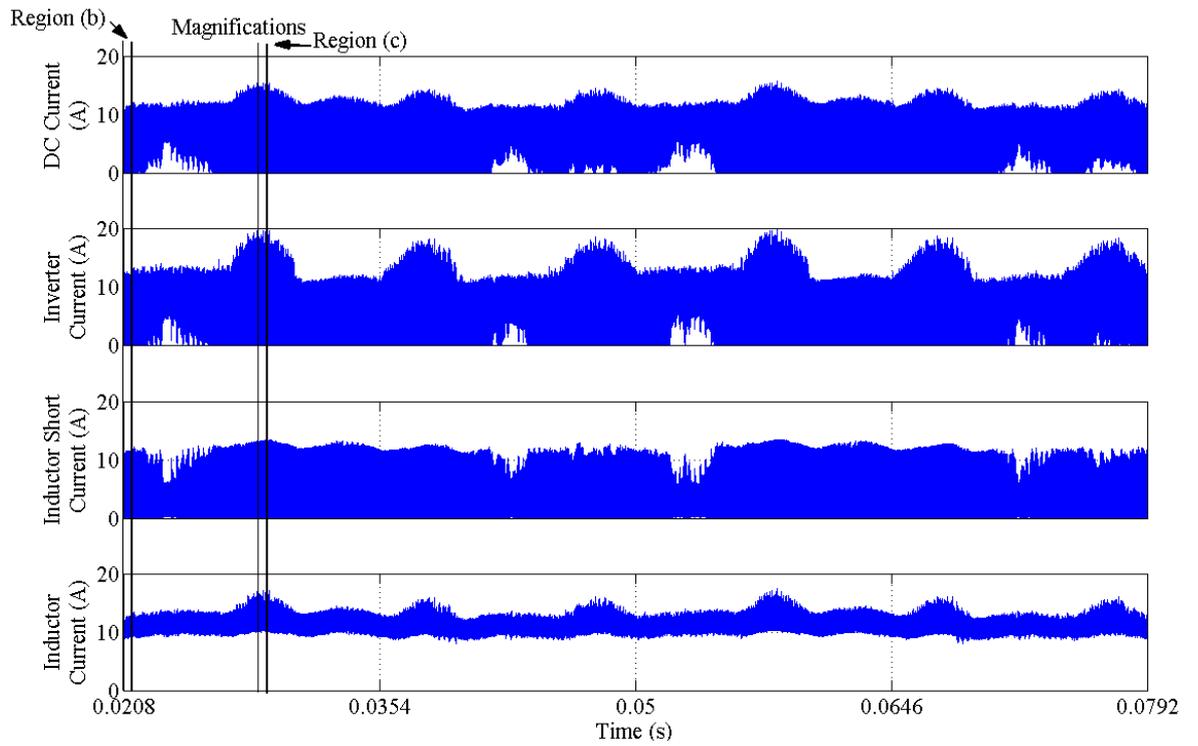


(b) Magnified region from (a)

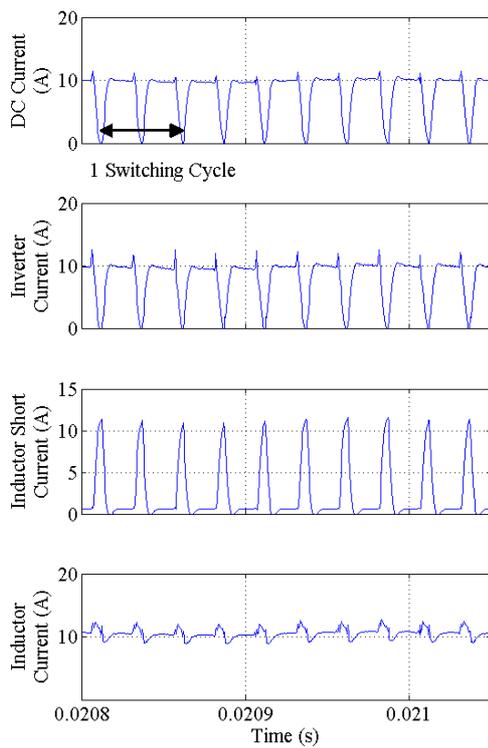


(c) Magnified region from (a)

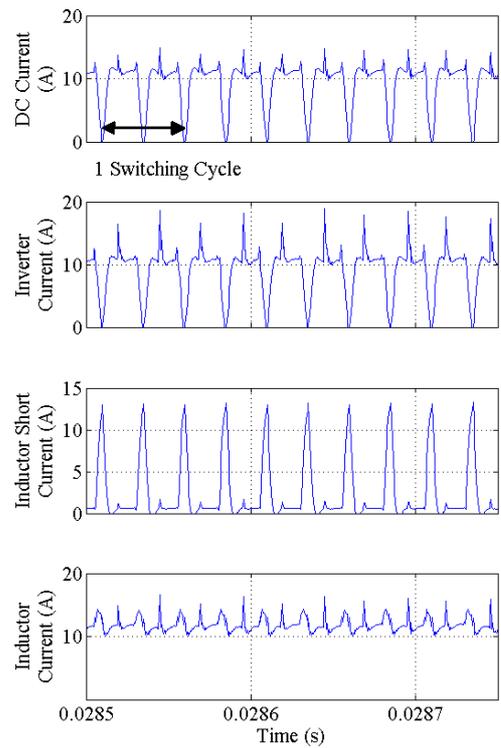
Fig. 5.43 CSI DC link waveforms; 0.5 p.u. load point.



(a) Waveform envelopes.

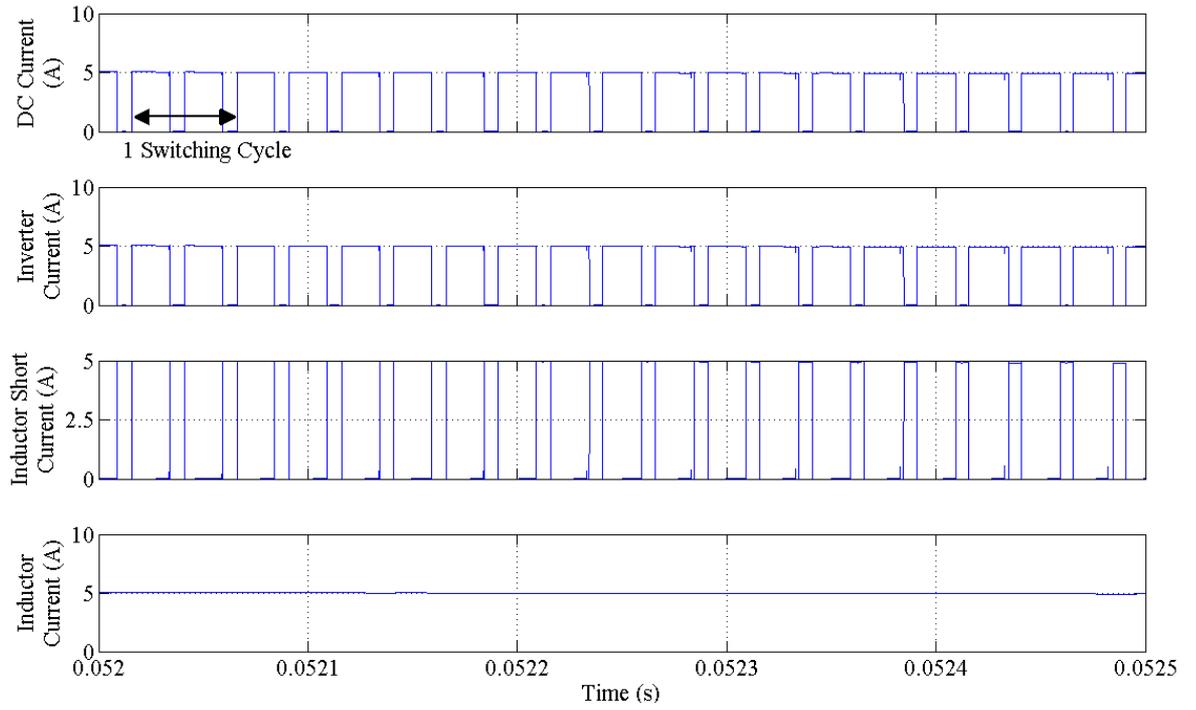


(b) Magnified region from (a)

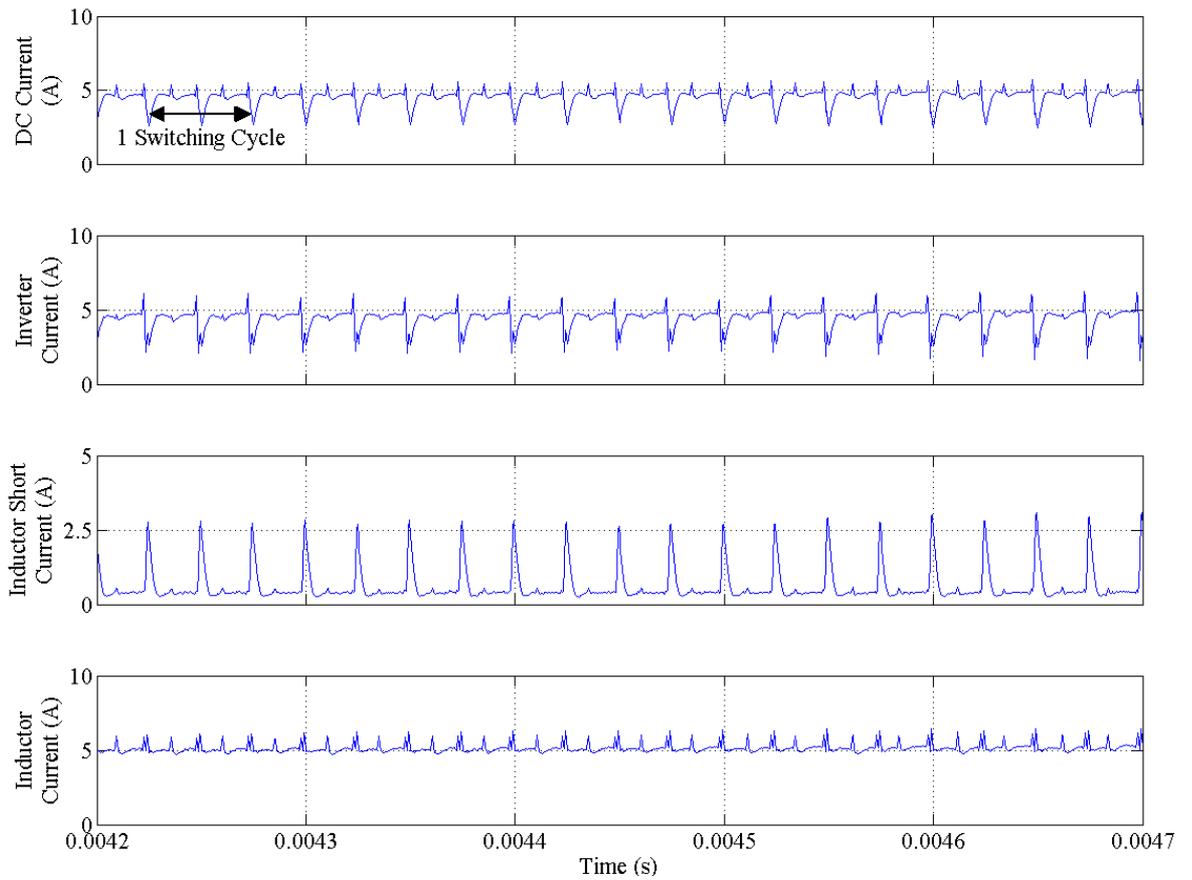


(c) Magnified region from (a)

Fig. 5.44 CSI DC link waveforms; 1 p.u. load point.

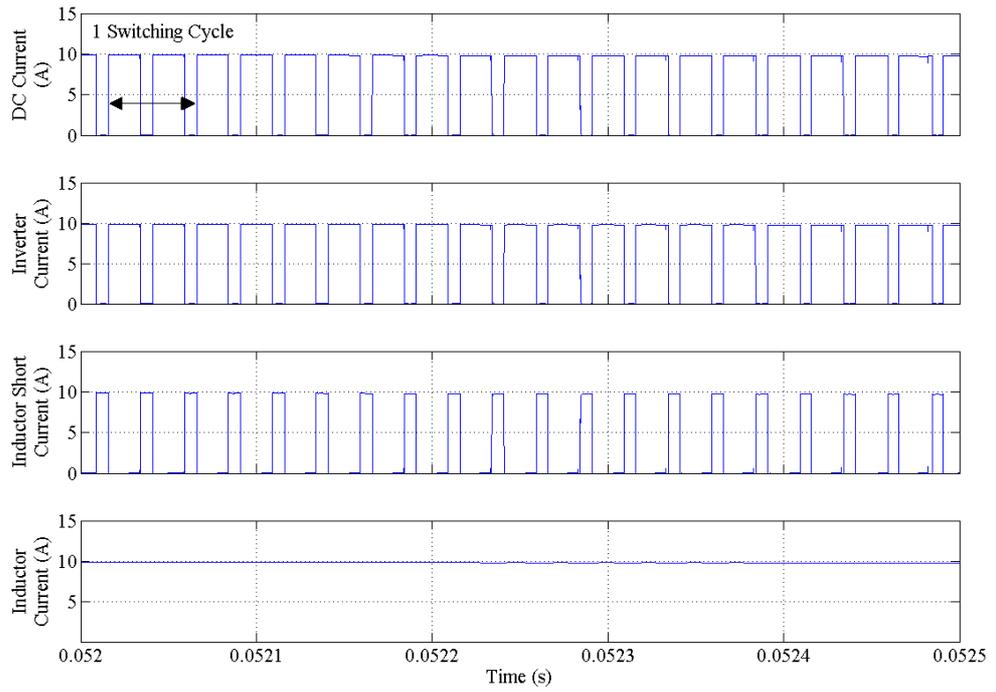


(a) Simulated waveforms (Fig 4.22 (b)).

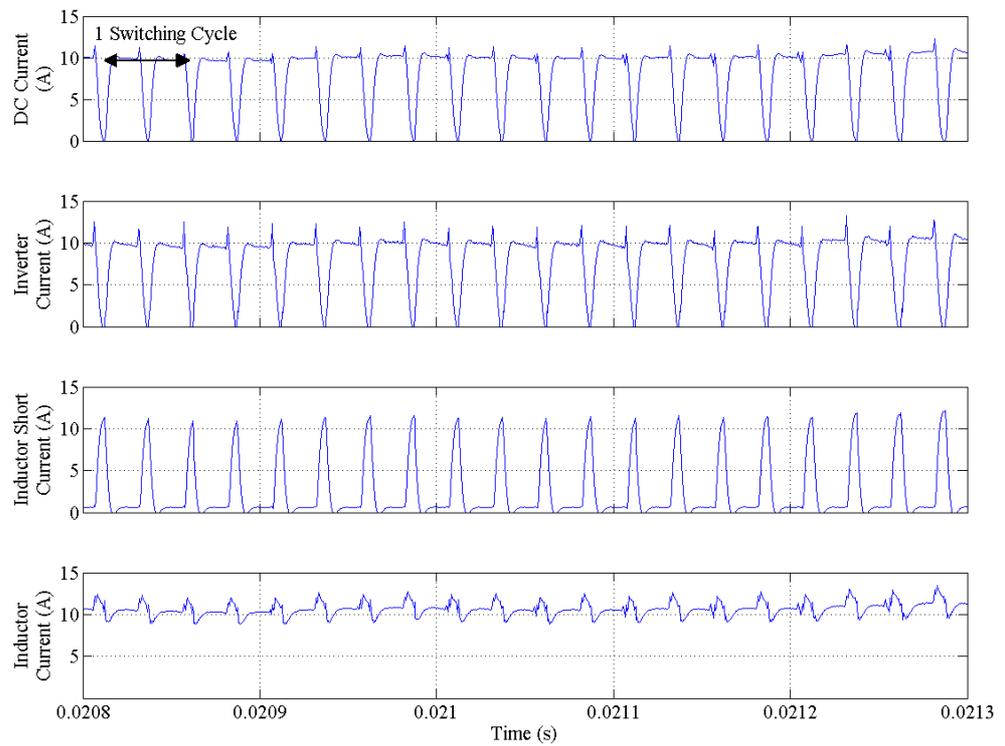


(b) Measured waveforms.

Fig. 5.45 Comparison of CSI DC link waveforms; 0.5 p.u. load point.

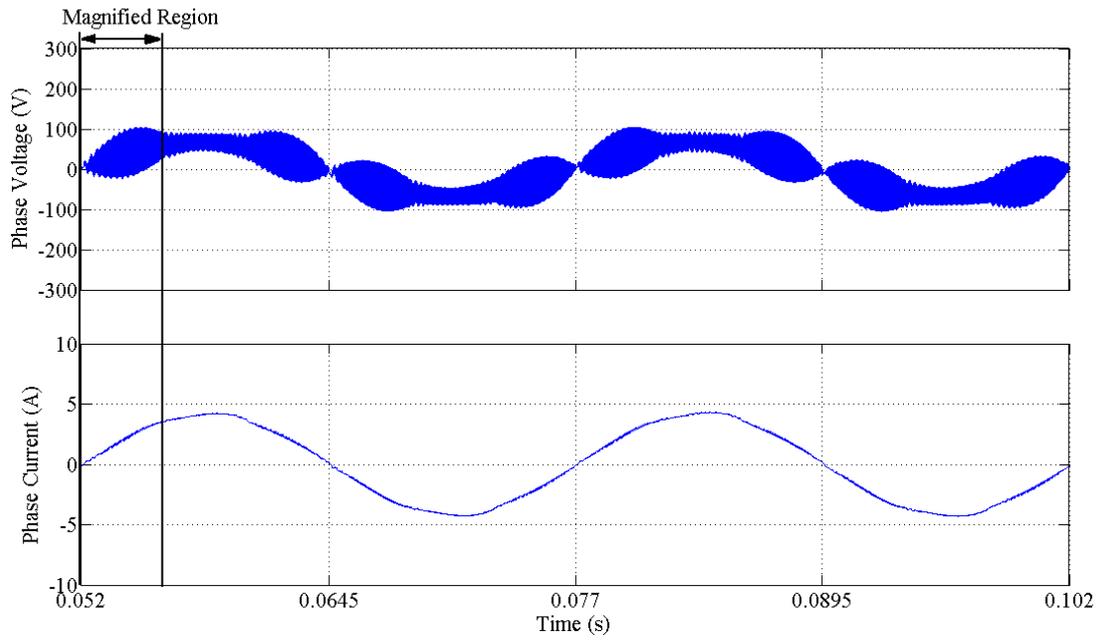


(a) Simulated waveforms (Fig 4.23 (b)).

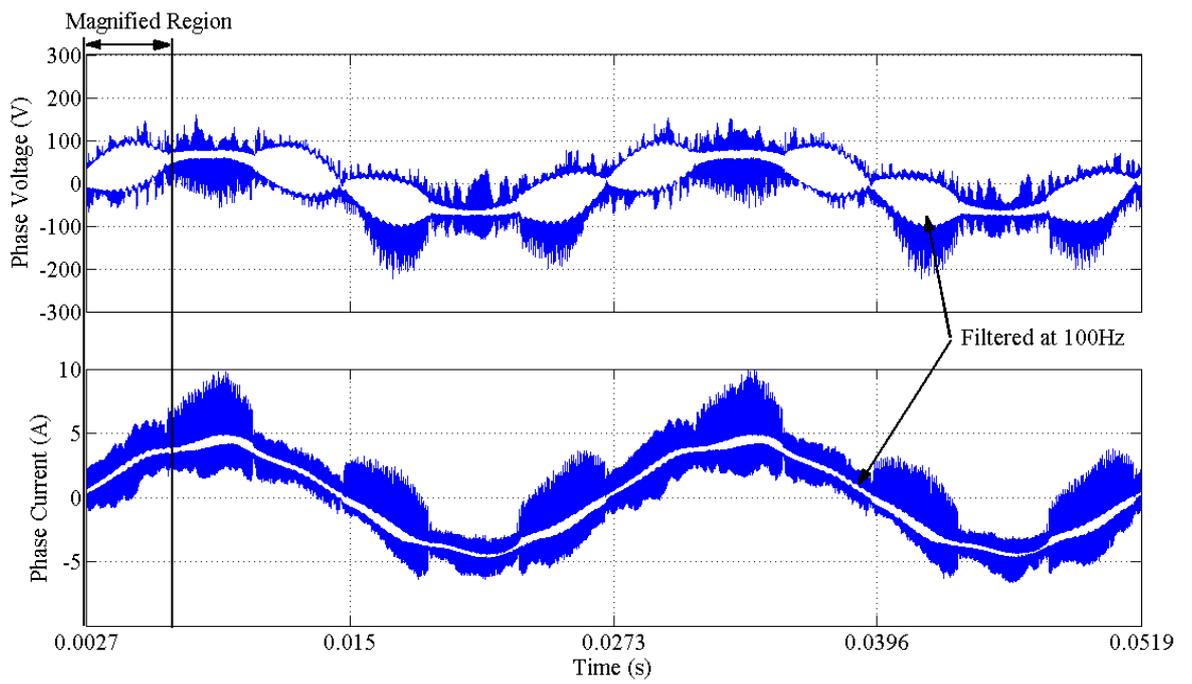


(b) Measured waveforms.

Fig. 5.46 Comparison of CSI DC link waveforms; 1 p.u. load point.

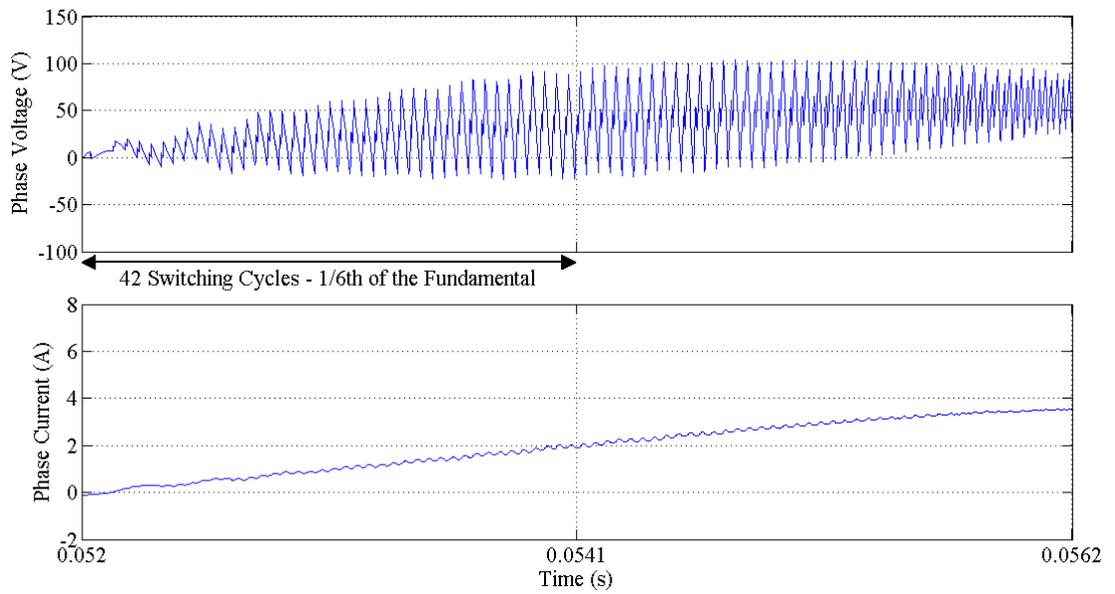


(a) Simulated waveforms.

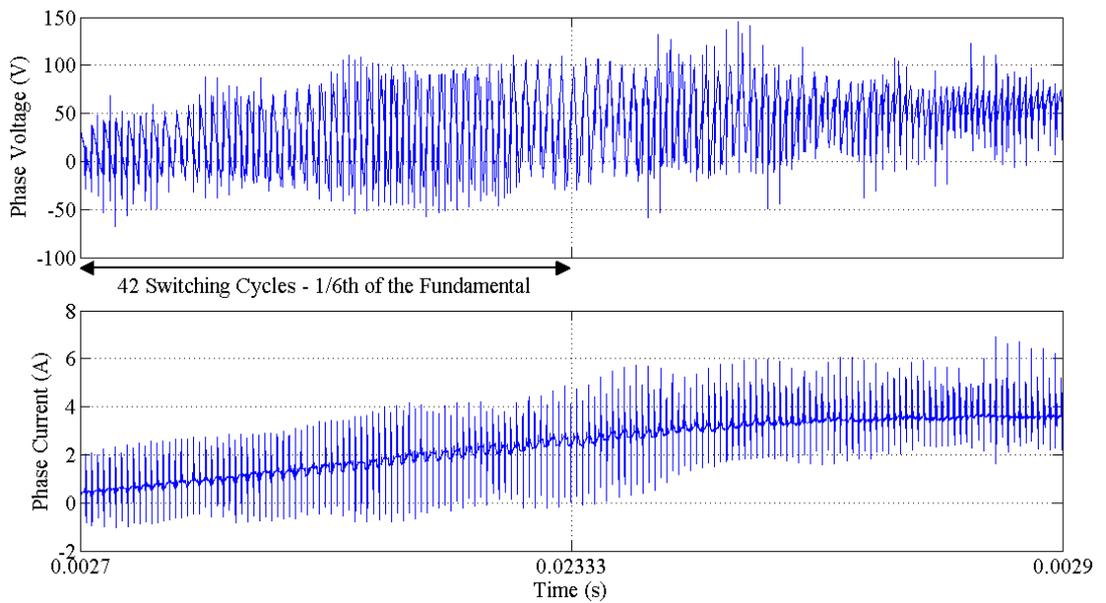


(b) Measured waveforms (white line superimposed on measured results).

Fig. 5.47 Comparison of CSI simulated and measured waveforms; 0.5 p.u. load point.

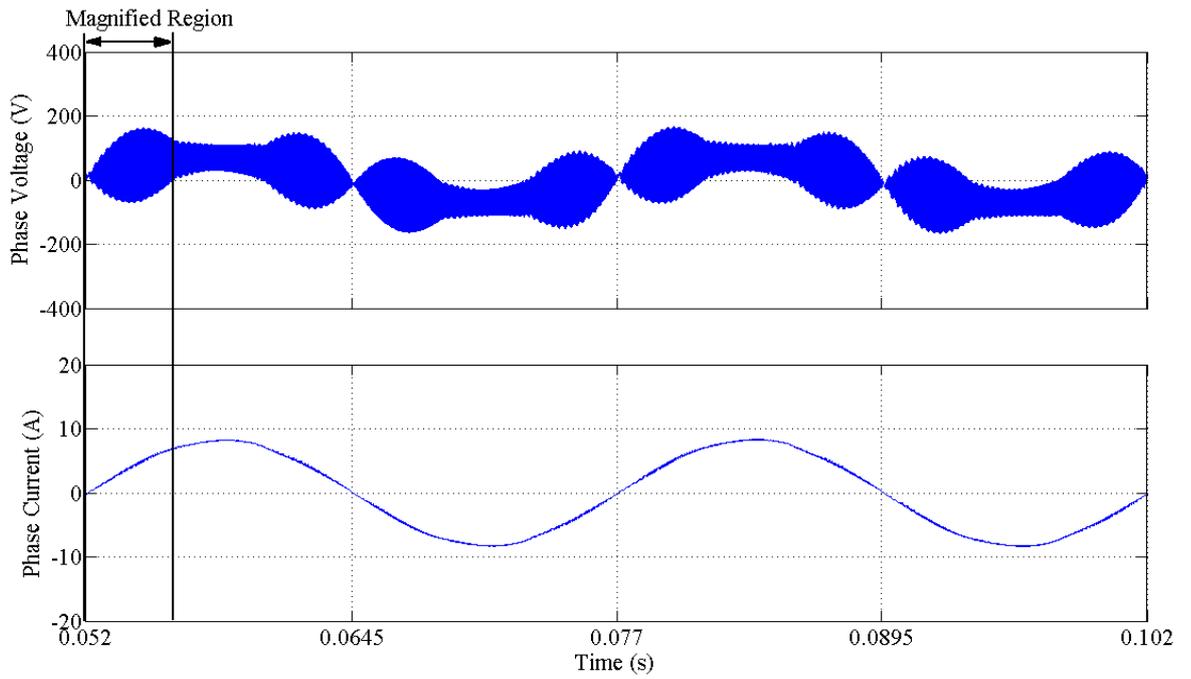


(a) Simulated waveforms.

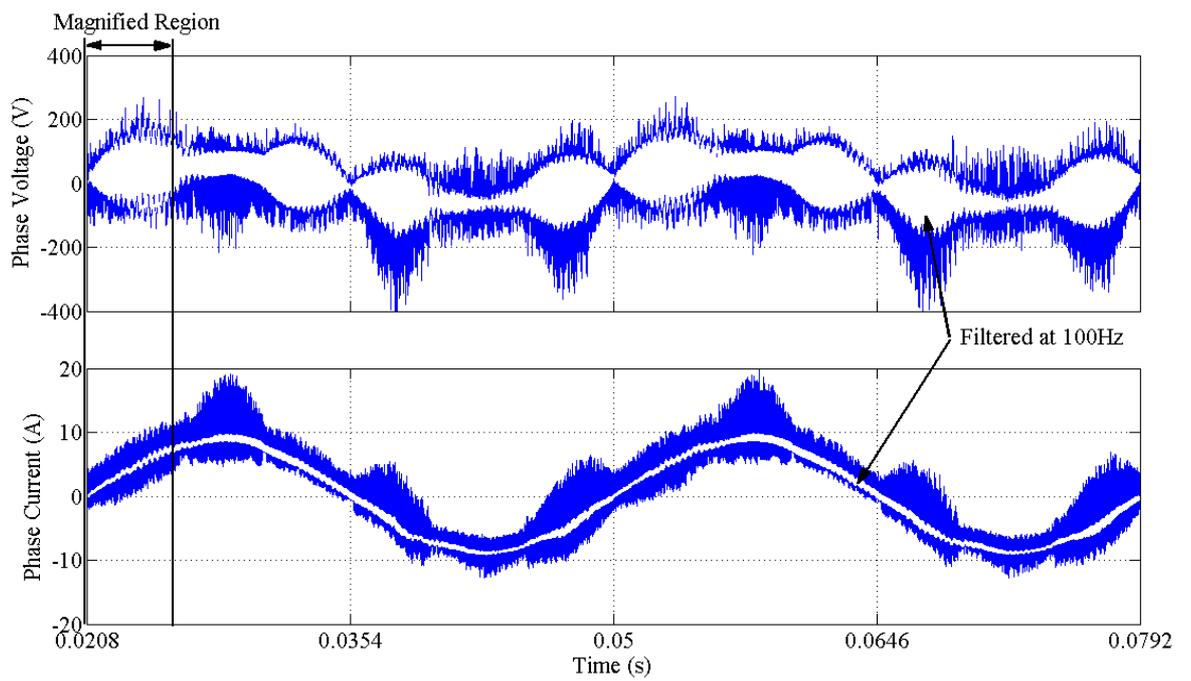


(b) Measured waveforms.

Fig. 5.48 Comparison of CSI simulated and measured waveforms; 0.5 p.u. load point, magnified region highlighted in Fig. 5.47.

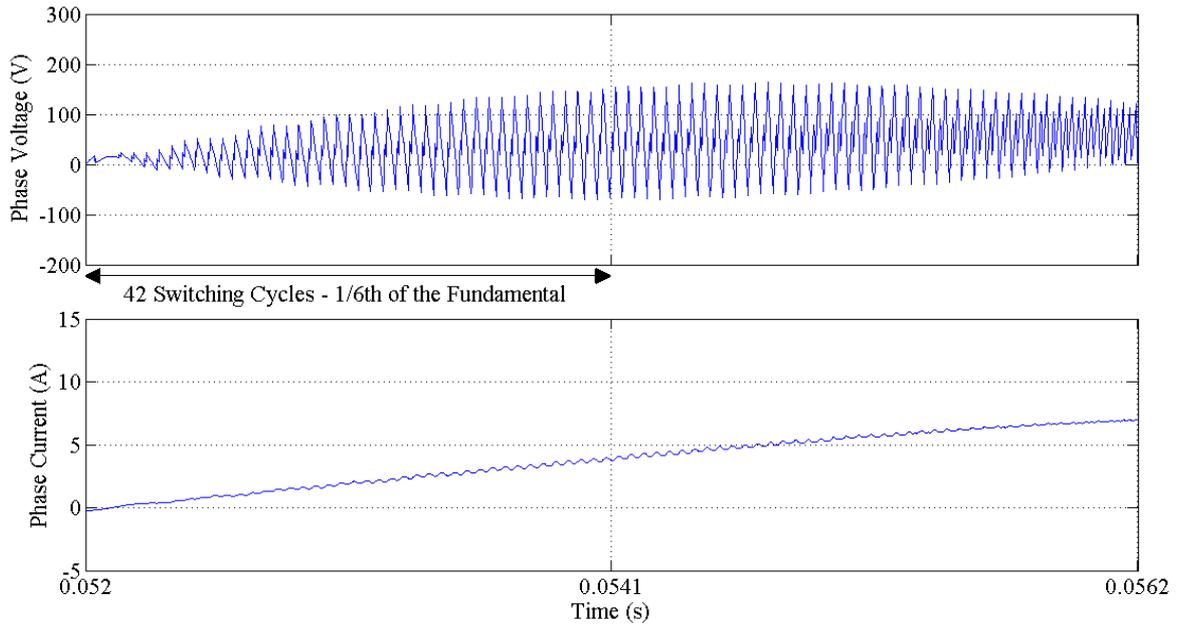


(a) Simulated waveforms.

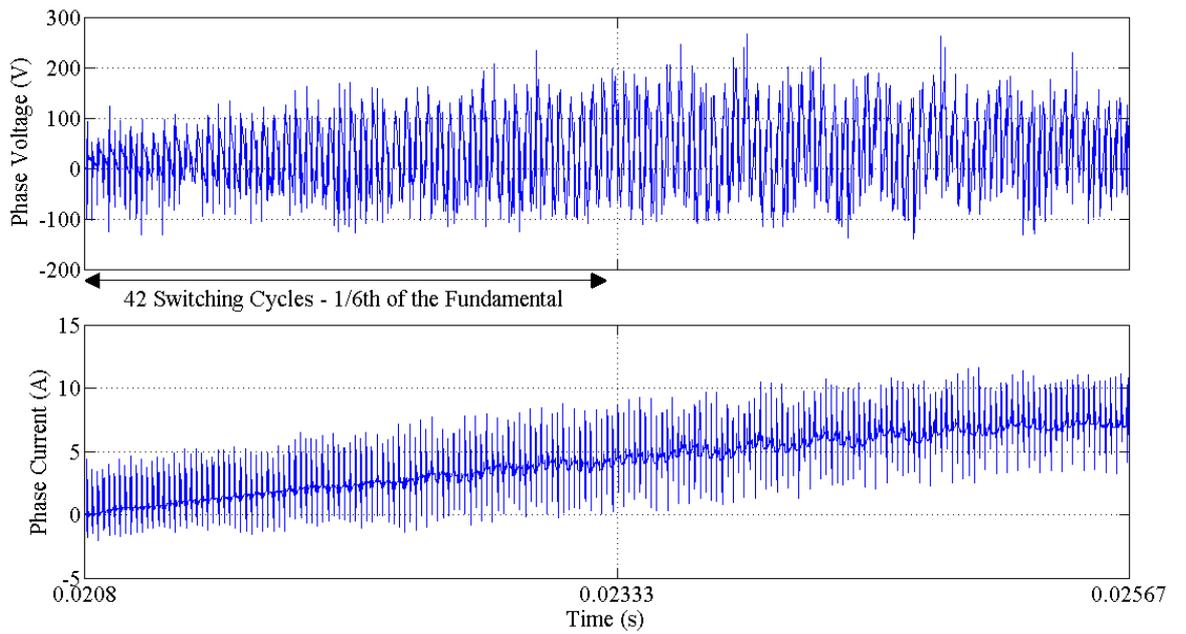


(b) Measured waveforms (white line superimposed on measured results).

Fig. 5.49 Comparison of CSI simulated and measured waveforms; 1 p.u. load point.

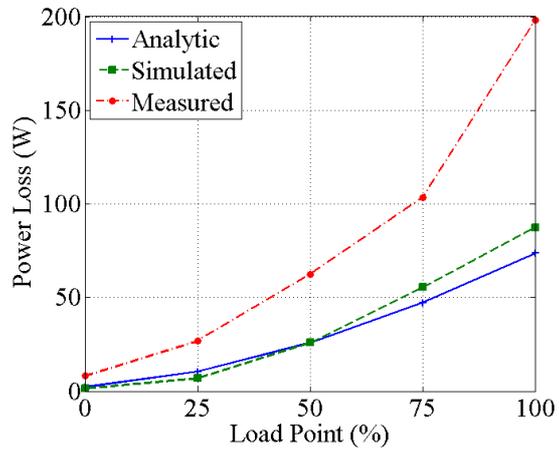


(a) Simulated waveforms.

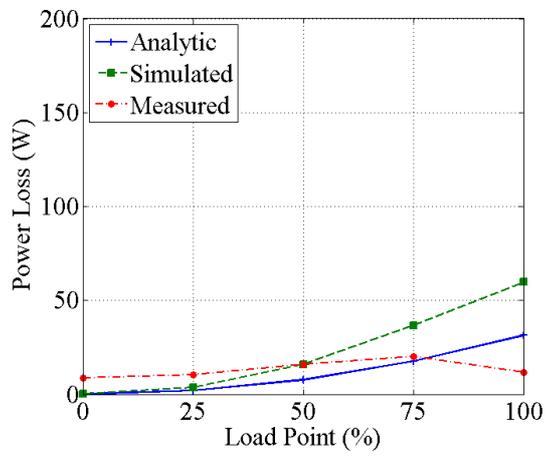


(b) Measured waveforms.

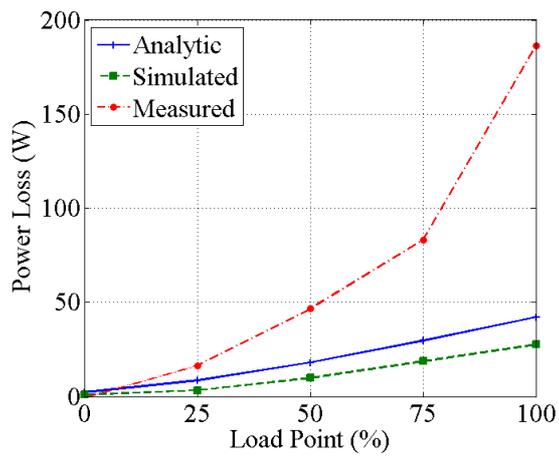
Fig. 5.50 Comparison of CSI simulated and measured waveforms; 1 p.u load point, magnified region highlighted in Fig. 5.49.



(a) DC input to electrical output loss.

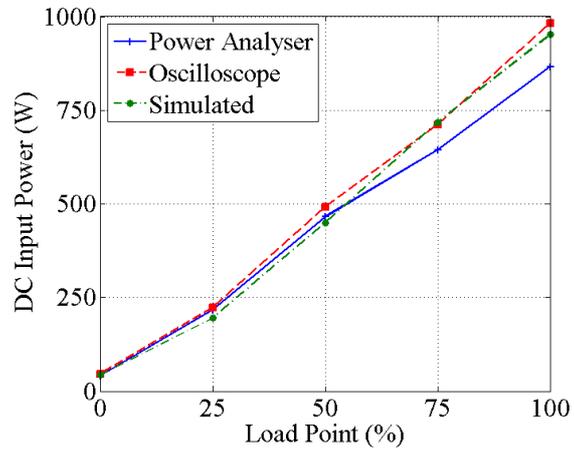


(b) DC link loss.

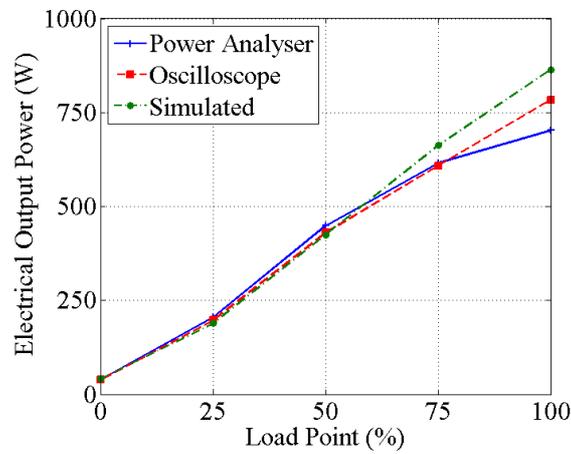


(c) Inverter loss.

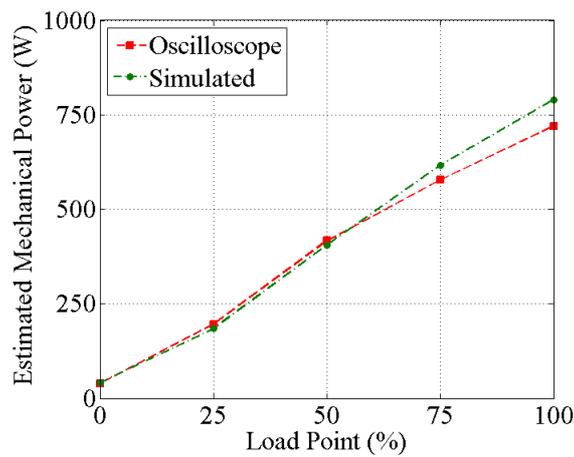
Fig. 5.51 CSI power loss comparison.



(a) DC input power.



(b) Electrical output power.



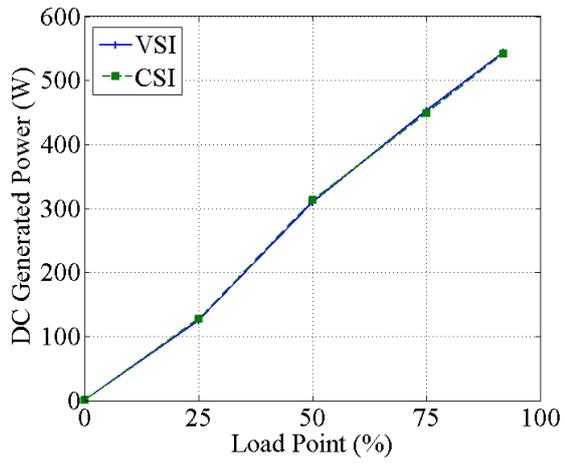
(c) Estimated mechanical power.

Fig. 5.52 CSI power audit.

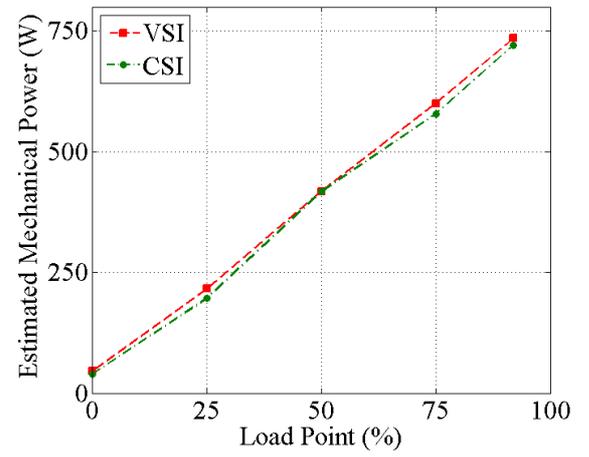
Analyser	Vdc	Idc	Pdc	Pinv	P1Loss	Vrms	Irms	Pelec	P2Loss	P3Loss	Pmech (est)	P4Loss	Pgen
0	103	0.396	40.84	NA	NA	45.336	0.349	39.78	1.06	NA	NA	39.78	0.17
25	107.92	2.013	216.79	NA	NA	47.202	1.728	205.11	11.68	NA	NA	205.11	127.36
50	112.14	4.177	465.54	NA	NA	53.487	3.588	448.77	16.77	NA	NA	448.77	312.65
75	109	5.962	644.38	NA	NA	56.828	5.142	615.99	28.39	NA	NA	615.99	448.81
92	104.83	8.503	866	NA	NA	61.287	7.624	702.75	163.25	NA	NA	702.75	541.73
Oscilloscope	Vdc	Idc	Pdc	Pinv	P1Loss	Vrms	Irms	Pelec	P2Loss	P3Loss	Pmech	P4Loss	Pgen
0	103.46	0.45	46.32	37.45	8.87	44.83	0.33	38.15	8.17	-0.70	38.93	-0.77	NA
25	107.71	2.08	223.95	213.45	10.50	46.69	1.49	197.12	26.83	16.33	196.27	0.84	NA
50	115.32	4.27	492.39	476.46	15.93	53.35	3.10	429.81	62.58	46.65	417.21	12.60	NA
75	117.07	6.07	712.18	691.91	20.27	58.95	4.43	608.69	103.48	83.21	578.15	30.55	NA
92	112.27	8.64	982.35	970.58	11.77	67.61	6.30	784.32	198.03	186.26	720.52	63.80	NA
SABER	Vdc	Idc	Pdc	Pinv	P1Loss	Vrms	Irms	Pelec	P2Loss	P3Loss	Pmech	P4Loss	Pgen
0	109.82	0.42	42.73	42.47	0.26	45.54	0.31	41.44	1.29	1.03	41.23	0.21	NA
25	114.56	1.84	195.56	191.92	3.64	47.42	1.36	188.7	6.86	3.22	184.7	4	NA
50	119.62	4.04	450.11	434.12	15.99	52.62	2.98	424.22	25.89	9.9	404.75	19.47	NA
75	124.94	6.15	717.85	681.16	36.69	59.66	4.55	662.45	55.4	18.71	617.14	45.31	NA
100	127.97	7.87	952.1	892.3	59.8	64.2	5.44	864.66	87.44	27.64	790.32	74.34	NA
Analytic	Vdc	Idc	Pdc	Pinv	Inductor	Vrms	Irms	Pelec	P2Loss	P3Loss	Pmech	P4Loss	Pgen
0	NA	NA	NA	NA	0.1	NA	NA	NA	2.25	2.15	NA	NA	NA
25	NA	NA	NA	NA	2	NA	NA	NA	10.53	8.53	NA	NA	NA
50	NA	NA	NA	NA	7.8	NA	NA	NA	25.83	18.03	NA	NA	NA
75	NA	NA	NA	NA	17.6	NA	NA	NA	47.34	29.74	NA	NA	NA
100	NA	NA	NA	NA	31.44	NA	NA	NA	73.68	42.24	NA	NA	NA

Note: P1Loss = (Pdc – Pinv); P2Loss = (Pdc – Pelec); P3Loss = (Pinv – Pelec); P4Loss = (Pelec – Pmech).

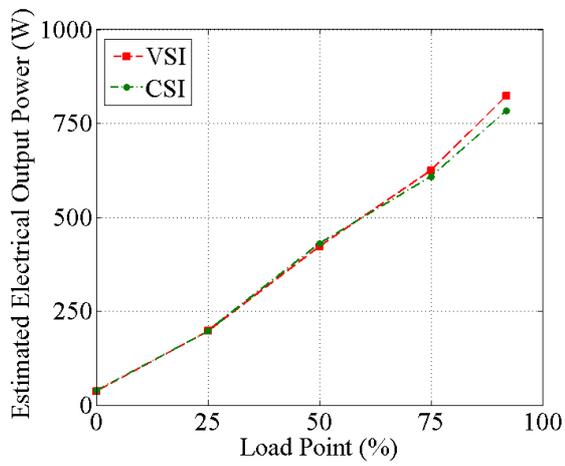
Table 5.7 CSI results comparison.



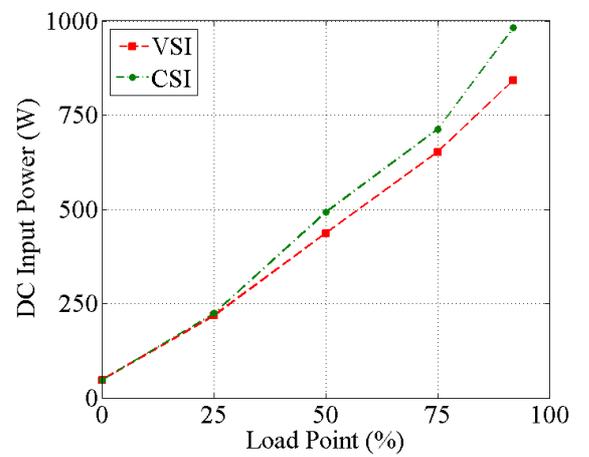
(a) DC generated power.



(b) Estimated mechanical power.



(c) Electrical input to inveter.



(d) DC electrical input.

Fig. 5.53 VSI and CSI power comparison.

Load	Pgen			Pmech		
	VSI	CSI	CSI / VSI	VSI	CSI	CSI / VSI
0	0.1	0.17	154.6	45.2	38.9	86.1
25	124.8	127.4	102.0	216.1	196.3	90.8
50	309.9	312.7	100.9	418.1	417.2	99.8
75	453.1	448.8	99.1	600.7	578.2	96.3
100	544.1	541.7	99.6	735.0	720.5	98.0
Load	Pelec			Pdc		
	VSI	CSI	CSI / VSI	VSI	CSI	CSI / VSI
0	37.5	38.2	1.01	47.2	46.3	97.8
25	197.4	197.1	0.99	218.1	224.0	102.7
50	421.9	429.8	1.02	436.7	492.4	112.8
75	624.4	608.7	0.98	651.6	712.2	109.3
100	824.1	784.3	0.95	842.8	982.4	116.6

Table 5.8 VSI and CSI power comparison results

5.7 Summary

A dual topology VSI and CSI, test facility has been designed and built to investigate the performance of PWM CSIs with PMSMs. The VSI results are typical of published drive system and there is good correlation between analytic, simulated and measured results, and thus forms a good benchmark for assessment of the CSI.

The CSI system shows a good correlation between simulated and measured waveforms. Analytic, simulated, measured results and power losses for the CSI system show the correct trends. However, there is a discrepancy between the analytic and simulated results when compared to the measured results, suggesting further work is required in this area.

DSP space vector control algorithms have been modified to convert standard VSI vector control algorithms to CSI vector control algorithms, when combined with the appropriate switching signal conversion system. Custom power electronic modules have been designed and built for both the VSI and CSI systems to facilitate the testing of a benchmark system and the study of a CSI system.

Comparisons have been made between the analytic, simulated and hardware system for the VSI and a close correlation has been found. DC link and PMSM phase voltage and current waveforms have been presented for the CSI system over a range of operating points. Harmonic analysis performed at the 0.5 p.u. and 1.0 p.u. operating points show that the PMSM phase voltage and currents are dominated by the fundamental frequency with switching frequency harmonics low in comparison. The CSI simulated and measured waveforms have been compared and show a good correlation. However, loss predictions from analytic and simulation methods have underestimated the losses by approximately one half, indicating that more work is required in this area. For the same loading conditions the losses within the PMSM are comparable, and within the limits of accuracy, thus the CSI does not appear to compromise PMSM performance. The electrical input-to and output-from the VSI and CSI inverter bridges are also comparable indicating that the additional conduction devices do not contribute significantly to the losses of the system. The greatest loss mechanism within the CSI system is the DC link inductor. Here, the use of a non-optimised inductor design, utilising industrial grade 50Hz E-core soft magnetic material, will increase the losses compared to an optimised design. Therefore this is an area of interest for further study.

CHAPTER 6

CONCLUSIONS

6.1 Review of Presented Work

Chapter 1 presented an overview of CSIs from their early use in the 1970's to the present date. With the advent of faster switching, higher rated power electronic devices, the development of CSIs was curtailed by the preferred VSI circuit topology. However, the CSI has potential drive system benefits as discussed in Chapter 1, and hence this research study.

Chapter 2 discusses evolution of standard VSI switch and control schemes for CSI applications. Consideration of pre-charge is presented and mapping of VSI to CSI logic discussed.

Chapter 3 develops analytic equations for the estimation of VSI and CSI losses and proposes a drive system specification that forms the basis of the VSI and CSI comparative study in Chapters 4 and 5.

Chapter 4 develops circuit simulation models for both the VSI and CSI topologies and presents simulation results that compare their relative performance.

Chapter 5 presents a circuit and test facility hardware design to validate the analysis of Chapter 3 and simulation study of Chapter 4.

Finally, Chapter 6 draws conclusions from all Chapters and suggests the scope for further research.

6.2 Conclusions and Recommendations for Further Work

Background theory on rotating machine control and associated power electronic switching has been presented for space vector modulation VSI convertors as a baseline reference for development of a CSI scheme. Detailed information, not commonly found in standard switching literature, has been presented, on the standard CSI switching scheme that is generally implemented via the use of a large DC link inductance. A modified CSI PWM switching scheme that allows the full benefits of PWM techniques to be achieved in CSI systems, i.e. allowing the inverter bridge to be switched in an all device-off mode, is presented in Chapter 2 and functionally demonstrated via tests reported in Chapter 5. This mode of switching allows a comparable strategy to VSI scheme to be realised. Methods for pre-charging the DC link inductor to allow for the safe start-up of CSI PWM systems, have been discussed and one procedure is presented that facilitates drive operation. Mapping of the VSI to CSI switching logic is presented in Chapter 2 again validated by the results of Chapter 5. This is a feature not previously published.

In chapter 3 a set of equations have been developed to allow analytic estimation of the losses in a CSI system. The analytic results show an increase in losses over the VSI, which is to be expected due to the additional semiconductor devices in the main power circuit conduction path. Previously studied CSI loss calculations used simplistic, generalised loss equations for the semiconductors and did not take account of the modified switching scheme used in the MCSI-SV-PWM scheme. No previous CSI semiconductor loss analysis have presented measured data to allow verify the validity of the analysis. Test data highlighted an underestimate of the simplified analytic and simulated results. This is an area for future study.

Simulation models of the VSI and CSI systems have been created using the SABER software package and demonstrated as suitable for the comparison of these inverters by the results presented in Chapter 5. Results for the VSI and CSI systems suggest that the inverter efficiency is slightly higher for the VSI system. However, the voltage and current waveforms in the PMSM and the predicted electrical-to-mechanical power conversion suggests that the two topologies are equitable in terms of machine performance.

A dual topology VSI and CSI, test facility has been designed and built to investigate the performance of PWM CSIs with PMSMs. The VSI results are typical of published drive system and there is good correlation between analytic, simulated and measured results, and thus forms a good benchmark for assessment of the CSI.

The CSI system shows a good correlation between simulated and measured waveforms. Analytic, simulated, measured results and power losses for the CSI system show the correct trends. However, there is a discrepancy between the analytic and simulated results when compared to the measured results, suggesting further work is required in this area.

Comparisons have been made between the analytic, simulated and hardware system for the VSI and a close correlation has been found. Harmonic analysis performed at the 0.5 p.u. and 1.0 p.u. operating points show that the PMSM phase voltage and currents are dominated by the fundamental frequency with switching frequency harmonics low in comparison. The CSI simulated and measured waveforms have been compared and show a good correlation. However, loss predictions from analytic and simulation methods have underestimated the losses by approximately one half, indicating that more work is required in this area. For the same loading conditions the losses within the PMSM are comparable, and within the limits of accuracy, thus the CSI does not appear to compromise PMSM performance. The electrical input-to and output-from the VSI and CSI inverter bridges are also comparable indicating that the additional conduction devices do not contribute significantly to the losses of the system. The greatest loss mechanism within the CSI system is the DC link inductor. Therefore this is an area of interest for further study.

6.3 Publications and Presentations Arising from this Study

The following publications have resulted from the work presented in this thesis, to-date:

- [1] CESAR update meeting: 3rd Task 4.1 Progress Meeting, at Jihlavan, Czech Republic, 12-13 November 2007.
- [2] CESAR update meeting: 5th Task 4.1 Progress Meeting, at the University of Manchester, UK, 20-21 January 2009.
- [3] Poster Presentation at The University of Manchester, School of Electrical and Electronic Engineering Postgraduate Research Poster Conference, Current Source Convertors for Vehicular Applications, 12th Nov 2008.
- [4] Woolaghan, S.; Schofield, N.; “Current Source Inverters for PM Machine Control,” *in the Proceedings of the IEEE International Conference on Electric Machines and Drives Conference (IEMDC '09)*, pp.702-708, 3-6 May 2009.

References

- [1] Holiday, S.; "Clerk Maxwell Lecture 2010," IET Clerk-Maxwell Lecture, 19th February 2009, London, UK and sub-reference "Energy Measures Report", Department for Business Enterprise and Regulatory Reform (BERR), website: <http://www.berr.gov.uk/files/file41260.pdf>, last accessed 20/09/2010.
- [2] Website: <http://www.cesarproject.eu/>, last accessed 20/09/2010.
- [3] Wheeler, P.W.; Rodriguez, J.C.; Clare, J.C.; Empringham, L.; Weinstein, A.; "Matrix converters: a technology review," in the *IEEE Transactions on Industrial Electronics*, Vol. 49, No. 2, pp. 267-288, Apr. 2002.
- [4] Wheeler, P.W.; Clare, J.C.; Apap, M.; Empringham, L.; Bradley, K.J.; Whitley, C.; Towers, G.; "A matrix converter based permanent magnet motor drive for an electro-hydrostatic aircraft actuator," in the *29th Annual Conference of the IEEE Industrial Electronics Society 2003 (IECON '03)*, Vol. 3, pp.2072-2077, 2003.
- [5] Bianchi, N.; Bolognani, S.; Zigliotto, M.; "Analysis of PM synchronous motor drive failures during flux weakening operation," in the *Record of the 27th Annual IEEE Power Electronics Specialists Conference 1996 (PESC '96)*, Vol. 2, pp.1542-1548, 1996.
- [6] Woolaghan, S.; Schofield, N.; "Current Source Inverters for PM Machine Control," in the *Proceedings of the IEEE International Conference on Electric Machines and Drives Conference 2009 (IEMDC '09)*, pp.702-708, 2009.
- [7] Delli Colli, V.; Cancelliere, P.; Marignetti, F.; Di Stefano, R.; "Influence of voltage and current source inverters on low-power induction motors," in the *IEE Proceedings on Electric Power Applications*, Vol. 152, pp.1311-1320, 2005.
- [8] Rivas, C.; Rufer, A.; "P.W.M Current converter for electric energy production systems from fuel-cells," in the *Record of the European Conference on Power Electronics and Applications*, 2001.
- [9] Hinrichsen, F.; Koch, I.; Candors, W.R.; "Current source IGBT-inverter for low inductive synchronous machines," in the *Record of the IEEE 35th Annual Power Electronics Specialists Conference 2004 (PESC 04)*, Vol. 4, pp.2849-2853, 2004.
- [10] Schofield, N.; Yap, H.T.; Bingham, C.M.; "Hybrid energy sources for electric and fuel cell vehicle propulsion," in the *Proceedings of the 2005 IEEE Conference Vehicle Power and Propulsion*, pp.522-529, 2005.

- [11] Bose, B.K.; "Power Electronics and AC Drives", published by Prentice-Hall, 1986, ISBN:0136868827.
- [12] Schofield, N.; "Brushless Permanent Magnet Traction Machines with Extended Speed Capability," Ph.D. Thesis, University of Sheffield, 1997.
- [13] Sen, P.C.; Namuduri, C.S.; Nandam, P.K.; "Evolution of control techniques for industrial drives," in the *Proceedings of the 1996 International Conference on Power Electronics, Drives and Energy Systems for Industrial Growth*, Vol. 2, pp.869-875, 1996.
- [14] Bose, B.K.; "Power Electronics and Motor Drives, advances and trends", published by Academic Elsevier Press, 2006, ISBN:0120884054.
- [15] Kerkman, R.J.; "Twenty years of PWM AC drives: when secondary issues become primary concerns," in the *Proceedings of the 22nd International Conference on Industrial Electronics, Control, and Instrumentation 1996*, Vol. 1, pp.LVII-LXIII, 1996.
- [16] Slemon, G.R.; Dewan, S.B.; Wilson, J.W.A.; "Synchronous Motor Drive with Current-Source Inverter," in the *IEEE Transactions on Industry Applications*, Vol. IA-10, No. 3, pp. 412-416, Mar. 1974.
- [17] Bose, B.K.; Lipo, T.A.; "Control and Simulation of a Current-Fed Linear Inductor Machine," in the *IEEE Transactions on Industry Applications*, Vol. IA-15, No. 6, pp. 591-600, Nov. 1979.
- [18] Phillips, K.P.; "Current-Source Converter for AC Motor Drives," in the *IEEE Transactions on Industry Applications*, Vol. IA-8, No. 6, pp. 679-683, Nov. 1972.
- [19] Lipo, T.A.; "Analysis and control of torque pulsations in current fed induction motor drives," in the *Record of the IEEE Power Electronics Specialist Conference*, pp. 89-96, 1978.
- [20] Hombu, M.; Ueda, S.; Ueda, A.; Matsuda, Y.; "A New Current Source GTO Inverter with Sinusoidal Output Voltage and Current," in the *IEEE Transactions on Industry Applications*, Vol. IA-21, No. 5, pp. 1192-1198, Sep. 1985.
- [21] Nonaka, S.; Nebu, Y.; "New GTO Current Source Inverter with Pulsewidth Modulation Control Techniques," in the *IEEE Transactions on Industry Applications*, Vol. IA-22, No. 4, pp. 666-672, July 1986.
- [22] Loh, P.C.; Blaabjerg, F.; Wong, C.P.; Tan, P.C.; "Tri-State Current Source Inverter With Improved Dynamic Performance," in the *IEEE Transactions on Power Electronics*, Vol. 23, No. 4, pp. 1631-1640, July 2008.

- [23] Halkosaari, .T.; Tuusa, H.; "Reduction of conducted emissions and motor bearing currents in current source PWM inverter drives," in the *Proceedings of the Power Electronics Specialists Conference*, Vol. 2, pp.959-964, 1999.
- [24] Cancelliere, P.; Delli Colli, V.D.; Di Stefano, R.; Marignetti, F.; "Voltage controlled modulation of a current source inverter," in the *Proceeding of the International Conference on Power Electronics, Machines and Drives*, pp.427-432, 2002.
- [25] Bendre, A.; Wallace, I.; Nord, J.; Venkataramanan, G.; "A current source PWM inverter with actively commutated SCRs," in the *Record of the IEEE 32nd Annual Power Electronics Specialists Conference 2001 (PESC 2001)*, Vol. 3, pp.1571-1576, 2001.
- [26] Sangshin, K.; Toliyat, H.A.; "A Current Source Inverter With Advanced External Circuit and Control Method,"in the *IEEE Transactions on Industry Applications*, Vol. 42, No. 6, pp. 1496-1507, Nov. 2006.
- [27] Trzynadlowski, A.M.; Patriciu, N.; Blaabjerg, F.; Pedersen, J.K.; "A hybrid, current-source/voltage-source power inverter circuit,"in the *IEEE Transactions on Power Electronics*, Vol. 16, No. 6, pp. 866-871, Nov. 2001.
- [28] Beig, A.R.; Ranganathan, V.T.; "A novel CSI-fed induction motor drive,"in the *IEEE Transactions on Power Electronics*, Vol. 21, No. 4, pp. 1073-1082, July 2006.
- [29] Klönne, A.; Fuchs, F.W.; "High Dynamic Performance of a PWM Current Source Converter Induction Machine Drive," in the *Record of the IEEE 32nd Annual European Conference on Power Electronics and Applications (EPE 2001)*, Vol. 3, pp.1571-1576, 2001.
- [30] Delli Colli, V.D.; Cancelliere, P.; Marignetti, F.; Di Stefano, R.; "Voltage control of current source inverters,"in the *IEEE Transaction on Energy Conversion*, Vol. 21, No. 2, pp. 451-458, June 2006.
- [31] Fuchs, F.W.; Klönne, A.; "DC link and dynamic performance features of PWM IGBT current source converter induction machine drives with respect to industrial requirements," in the *IEEE Proceeding for the Power Electronics and Motion Control Conference*, Vol. 3, pp.1393-1398, 2004.
- [32] Salo, M.; Tuusa, H.; "Vector-controlled PWM current-source-inverter-fed induction motor drive with a new stator current control method,"in the *IEEE Transactions on Industrial Electronics*, Vol. 52, No. 2, pp. 523-531, Apr. 2005.

- [33] Nikolic, A.; Jeftenic, B.; "Precise Vector Control of CSI Fed Induction Motor Drive," in the *European Transactions on Electrical Power (ETEP) published by John Wiley & Sons USA*, Vol. 16, No. 2, pp. 175-188, Mar. 2006.
- [34] Suh, Y.; Steinke, J.K.; Steimer, P.K.; "Efficiency Comparison of Voltage-Source and Current-Source Drive Systems for Medium-Voltage Applications," in the *IEEE Transactions on Industrial Electronics*, Vol. 54, No. 5, pp. 2521-2531, Oct. 2007.
- [35] Rees, S.; AmmannU.; Ammann, U.; "New stator voltage controller for high speed induction machines fed by current-source inverters," in the *Proceeding of the 35th Annual Power Electronics Specialists Conference 2004 (PESC '04)*, Vol. 1, pp.541-547, 2004.
- [36] Cancelliere, P.; Delli Colli, V.; Di Stefano, R.; Marignetti, F.; "Soft switching current source inverter with modified space vector modulation and active damping for an axial flux in-wheel motor with fractional slot winding," in the *Proceedings of the IEEE 35th Annual Power Electronics Specialists Conference 2004 (PESC '04)*, Vol. 2, pp.1190-1206, 2004.
- [37] Mohr, M.; Fuchs, F.W.; "Comparison of three phase current source inverters and voltage source inverters linked with DC to DC boost converters for fuel cell generation systems," in the *Proceedings of the Power Electronics and Applications European Conference, 2005*.
- [38] Adnanes, A.K.; Nilssen, R.; Rad, R.O.; "Power feed-back during controller failure in inverter fed permanent magnet synchronous motor drives with flux weakening," in the *Record of the IEEE 23rd Annual Power Electronics Specialists Conference, 1992 (PESC '92)*, Vol. 2, pp.958-963, 1992.
- [39] ABB Drives "GUIDE FOR CAPACITOR REFORMING IN ACS50, ACS55, ACS150, ACS310, ACS350, ACS355, ACS550, ACH550 and R1-R4 OINT-/SINT-boards.", available online at [http://www05.abb.com/global/scot/scot201.nsf/veritydisplay/cf2c9be9fc666ebbc1257729002bd7be/\\$File/Guide_for_capacitor_reforming_Rev_G.pdf](http://www05.abb.com/global/scot/scot201.nsf/veritydisplay/cf2c9be9fc666ebbc1257729002bd7be/$File/Guide_for_capacitor_reforming_Rev_G.pdf), last accessed 15/06/2010.
- [40] Gemmen, R.S.; "Analysis for the Effect of Ripple Current on Fuel Cell Operating Condition," in the *Journal of Fluids Engineering*, Vol. 125, pp. 576-585, 2003.
- [41] O'Kelly, D.; Simmons, S.; "Introduction to Generalized Electrical Machine Theory", published by McGraw Hill, 1969, ISBN:0070940509.

- [42] Smith, A.C.; "Design of Electrical Machines", Course Notes for EEEN60195, School of Electrical and Electronic Engineering, The University of Manchester, 2009.
- [43] Holmes, D.G.; Lipo, T.A.; "Pulse Width Modulation for Power Converters", published by IEEE Press/Wiley-Interscience, 2003, ISBN:0471208140.
- [44] Krishnan, R.; "Selection Criteria for Servo Motor Drives,"in the *IEEE Transactions on Industry Applications*, Vol. IA-23, No. 2, pp. 270-275, Mar. 1987.
- [45] Pillay, P.; Krishnan, R.; "Modelling, simulation, and analysis of permanent-magnet motor drives. I. The permanent-magnet synchronous motor drive,"in the *IEEE Transactions on Industry Applications*, Vol. 25, No. 2, pp. 265-273, Apr. 1989.
- [46] Bowes, S.R.; Clark, P.R.; "Regular-sampled harmonic-elimination PWM control of inverter drives,"in the *IEEE Transactions on Power Electronics*, Vol. 10, No. 5, pp. 521-531, Sep. 1995.
- [47] Moschopoulos, G.; Joos, G.; Ziogas, P.D.; "Input characteristics of variable modulation index controlled current source inverters,"in the *IEEE Transactions on Industrial Electronics*, Vol. 41, No. 2, pp. 216- 223, Apr. 1994.
- [48] Enjeti, P.N.; Ziogas, P.D.; Lindsay, J.F.; "A current source PWM inverter with instantaneous current control capability," in the *Conference Record of the 1988 IEEE Industry Applications Society Annual Meeting*, Vol. 10, pp.927-933, 1988.
- [49] Control Techniques Drives Ltd "Installation Guide - Unidrive Regen", available online at [http://www.controltechniques.com/CTcom/products/ac %20drives/unidrive%20classic/downloads.aspx](http://www.controltechniques.com/CTcom/products/ac%20drives/unidrive%20classic/downloads.aspx), last accessed 17/3/2009.
- [50] Pillay, P.; Ahmed, M.; Samudio, R.; "Modeling and Performance of a SRM Drive with Improved Ride-Through Capability,"in the *IEEE Transactions on Energy Conversion*, Vol. 16, No. 2, pp. 165-173, June 2001.
- [51] Mohan, N.; Underland, T.M.; Robbins, W.P.; "Power Electronics: Converters, Applications, and Design", published by Wiley, 2003, ISBN:0471429082.
- [52] Control Techniques Drives Ltd "Unimotor FM Product Data", available online at <http://www.controltechniques.com/CTcom/products/ac,%20dc%20and%20servo%20motors/servo%20motors.aspx>, last accessed 1/16/2010.
- [53] International Rectifier "IRGB4056dpbf Datasheet", available online at <http://www.irf.com/product-info/datasheets/data/irgb4056dpbf.pdf>, last accessed 18/8/2010.

- [54] STMicroelectronics "ST1210 Main Product Characteristics", available online at http://www.st.com/stonline/products/literature/ds/12164/sttth12_10.pdf, last accessed 18/8/2010.
- [55] Bierhoff, M.H.; Fuchs, F.W.; "Semiconductor losses in voltage source and current source IGBT converters based on analytical derivation," in the *Proceedings of the IEEE 35th Annual Power Electronics Specialists Conference 2004 (PESC 04)*, Vol. 4, pp.2836-2842, 2004.
- [56] Casanellas, F.; "Losses in PWM inverters using IGBTs," in the *IEE Proceedings of Electric Power Applications*, Vol. 142, p. 142, 1995.
- [57] Brown, A.J.; "An assessment of the efficiencies of soft and hard-switched inverters for application in power electric vehicles," Ph.D. Thesis, University of Sheffield, 2000.
- [58] Kolar, J.W.; Round, S.D.; "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," in the *IEE Proceedings Electric Power Applications*, Vol. 153, pp.535-543, 2006.
- [59] Cornell Dubilier Electronics Inc "Aluminium Electrolytic Capacitor Application Guide", available online at <http://www.cde.com/catalogs/AEappGUIDE.pdf>, last accessed 22/07/2010.
- [60] EPCOS AG "Metallized Polypropylene Film Capacitors Product Data", available online at http://www.epcos.com/inf/20/20/db/fc2009/MKPB326_51_656.pdf, last accessed 20/01/2010.
- [61] Lee, G.; Lee, D.; "Implementation of naturally sampled space vector modulation eliminating microprocessors," in the *Proceedings of the Power Electronics and Motion Control Conference 2000 (IPEMC 2000)*, Vol. 2, pp.803-807, 2000.
- [62] Synopsys Inc "SABER Sketch System Documentation", SABER Sketch version, B-2008.9-SP1, 2007.
- [63] Website: <http://www.ti.com/corp/docs/investor/dsp/dsp.htm>, last accessed 22/06/2010.
- [64] TI Inc "TMS320C28x DSP Workshop Student Guide", Training Course Documentation, Texas Instruments Inc, 2001.
- [65] Yu, Z.; "3.3V DSP for digital motor control", available online at <http://focus.ti.com/lit/an/spra550/spra550.pdf>, last accessed 20/3/2007.
- [66] Woolaghan, S.; "Dual Topolgy Test Rig Manual", Test Rig Operators Manual, University of Manchester, 2008.

- [67] EPCOS AG "NTC thermistors for temperature measurement datasheet", available online at http://www.epcos.com/inf/50/db/ntc_09/MiniSensor_s__B57861__S861.pdf, last accessed 22/7/2010.
- [68] TI Inc "TI Digital Motor Control Soution", available online at <http://focus.ti.com/lit/ml/sprb167a/sprb167a.pdf>, last accessed 22/5/2009.
- [69] Smith, S.W.; "Digital Signal Processing: A Practical Guide for Engineers and Scientists", published by Newnes, 2006, ISBN:075067444X.
- [70] TI Inc "IQmath Library: A Virtual Floating Point Engine", available online at http://focus.ti.com/docs/toolsw/folders/print/sprc_08_7.html, last accessed 22/7/2010.
- [71] Abu Khaizaran, M.S.; Rajamani, H.S.; Palmer, P.R.; "The high power IGBT current source inverter," in the *Conference Record of the Thirty-Sixth IAS Annual Meeting Industry Applications Conference*, Vol. 2, pp.879-885, 2001.
- [72] Seok-Hee, H.; Jahns, T.M.; Guven, M.K.; Aydin, M.; Soong, W.L.; "Impact of Maximum Back-EMF Limits on the Performance Characteristics of Interior Permanent Magnet Synchronous Machines," in the *Record of the 41st IEEE Industry Applications Conference*, Vol. 4, pp.1962-1969, 2006.

APPENDIX A. Summary of the “Dual Topology Test Rig Manual”

1. System Overview
2. DSP Information
 - 2.1 eZdsp Technical Reference Guide
 - 2.2 TI IQmath Library User Guide
 - 2.3 TI TMS320x281x DSP Analog-to-Digital Convertor (ADC) Reference Guide (SPRU060D)
 - 2.4 TI TMS320x281x DSP Event Manager (EV) Reference Guide (SPRU065E)
 - 2.5 TI PMSM3_4 System Documentation
 - 2.6 Main DSP code components for Dual Topology Test Rig
3. Circuit Details
 - 3.1 DSP Interface Board, schematics and PCB layout
 - 3.2 Multi-measurement Board, schematic and PCB layout
 - 3.3 CSI PWM Conversion Logic Board, schematic and PCB layout
 - 3.4 JGPL Gate Drive Board documentation
 - 3.5 PEM semiconductor data sheets
 - 3.6 Other component data sheets.

APPENDIX B. EPCOS Thermistor Details

Parameter	Value
Product number	B57861S -
Material type	F -
Accuracy	+/- 1 %
Resistance @ 25°C	5000 Ω
Max. temperature	155 °C

Table B.1 Thermistor parameters of interest.

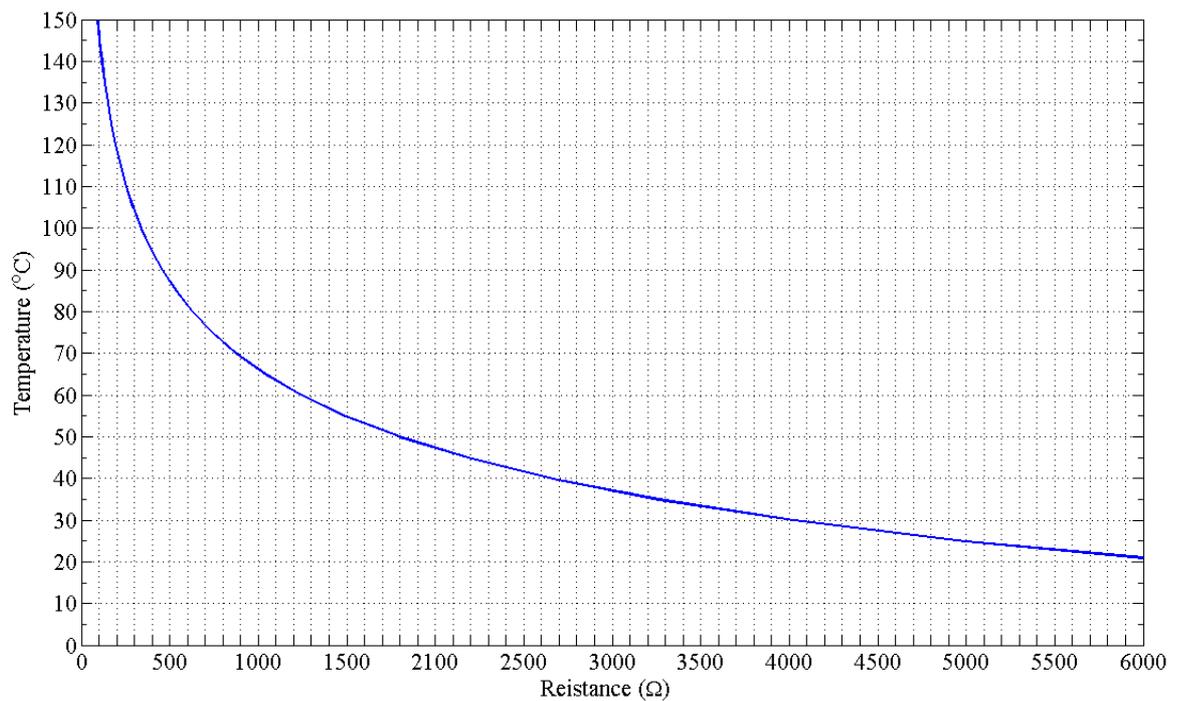


Fig. B.1 Resistance-Temperature chart for the EPCOS B57861S

APPENDIX C. DSP Software Code

C.1 Guide to Reading TI DSP Code

The DSP program code files include data for execute operations, programmer comments and compile time instructions, examples of each are detailed to aid understanding of the DSP code included in this appendix.

The commenting system allows programmer instructions and explanations to be included in the file. Comments can also be used to sections of code that are not needed but removal from the file is undesirable.

```
/* This is a comment for large section, ending the comment requires  
the characters in reverse, i.e. */  
// This is a line comment, comments end at the end of the line
```

Compile instructions are always prefixed by the ‘#’ symbol and instruct the compiler program to include files or define symbols for future use, etc.

```
#include "pmsm3_4.h"          // this includes the header file pmsm3_4.h  
#define PI 3.14159265358979 // this defines symbol PI for use in calcs
```

Program instructions always end with a semi-colon; instructions can only span lines with the use of a back slash \.

```
int16 DlogCh1 = 0;    /* The variable DlogCh1 is defined as a 16-bit  
integer of value zero */  
  
PIDREG3 pid1_id = PIDREG3_DEFAULTS;    /* Create an object, pid1_id,  
of type PIDREG3 with starting values of PIDREG3_DEFAULTS */  
  
InitSysCtrl();    /* call the sub-function InitSysCtrl, do not send  
any variables to the sub-function */
```

C.2 CSI Main Execution Code

```
/*=====
System Name:  PMSM34

File Name:  PMSM3_4.C

Description:      Primary system file for the Real Implementation of
                  Position Control Based Sensored Field Orientation
                  Control for a Three Phase Permanent-Magnet
                  Synchronous Motor (PMSM) using QEP sensor

Originator:      Digital control systems Group - Texas Instruments
Modified by S Woolaghan, University of Manchester

=====
History:
-----
04-15-2005  Version 3.20: Support both F280x and F281x targets
04-25-2005  Version 3.21: Move EINT and ERTM down to ensure that all
initialization is completed before interrupts are allowed.
2008: Modified for CSI operation at UoM - Do not use on standard
inverter
=====*/

// Include header files used in the main function
#include "target.h"
#include "DSP281x_Device.h"
#include "IQmathLib.h"
#include "pmsm3_4.h"
#include "parameter.h"
#include "build.h"
#include <math.h>

// Prototype statements for functions found within this file.
interrupt void MainISR(void);
interrupt void QepISR(void);

// Global variables used in this system
float32 VdTesting = 0;           // Vd testing (pu)
float32 VqTesting = 0.25;       // Vq testing (pu)
float32 IdRef = 0;              // Id reference (pu)
float32 IqRef = 0.1;           // Iq reference (pu)
float32 SpeedCur = 0;
float32 T = 0.001/ISR_FREQUENCY; /* Sampling period (sec), see
Parameter.h */

Uint16 IsrTicker = 0;
Uint16 BackTicker = 0;
Uint16 SpeedLock = 0;

int16 DlogCh1 = 0;
int16 DlogCh2 = 0;
int16 DlogCh3 = 0;
int16 DlogCh4 = 0;

volatile Uint16 EnableFlag = FALSE;

Uint16 SpeedLoopPrescaler = 10; // Speed loop prescaler
Uint16 SpeedLoopCount = 1;     // Speed loop counter

int16 SpeedRef = 0;
```

```

int16 Direction = 1;

// Instance a few transform objects
CLARKE clarkel = CLARKE_DEFAULTS;
PARK park1 = PARK_DEFAULTS;
IPARK ipark1 = IPARK_DEFAULTS;

// Instance PID regulators to regulate the d and q synchronous axis
// currents, speed and position
PIDREG3 pid1_id = PIDREG3_DEFAULTS;
PIDREG3 pid1_iq = PIDREG3_DEFAULTS;
PIDREG3 pid1_pos = PIDREG3_DEFAULTS;
PIDREG3 pid1_spd = PIDREG3_DEFAULTS;

// Instance a PWM driver
PWMGEN pwm1 = PWMGEN_DEFAULTS;

/* Instance a Space Vector PWM modulator. This modulator generates
a, b and c phases based on the d and q stationery reference frame
inputs */
SVGENDQ svgen_dq1 = SVGENDQ_DEFAULTS;

// Instance a QEP interface driver
QEP qep1 = QEP_DEFAULTS;

// Instance a speed calculator based on QEP
SPEED_MEAS_QEP speed1 = SPEED_MEAS_QEP_DEFAULTS;

// Instance a enable PWM drive driver (only for DMC1500)
DRIVE drv1 = DRIVE_DEFAULTS;

// Instance a ramp controller to smoothly ramp the frequency
RMPCNTL rc1 = RMPCNTL_DEFAULTS;

// Instance a ramp generator to simulate an Angle
RAMPGEN rg1 = RAMPGEN_DEFAULTS;

// Create an instance of the current/dc-bus voltage measurement
// driver
ILEG2DCBUSMEAS ilg2_vdc1 = ILEG2DCBUSMEAS_DEFAULTS;

// Create instance of averaging array
MEAS_ARRAY meas1 = MEAS_ARRAY_DEFAULTS;

// Create an instance of DATALOG Module
DLOG_4CH dlog = DLOG_4CH_DEFAULTS;

void main(void)
{
/* Initialize System Control registers, PLL, WatchDog, Clocks to
default state: This function is found in the DSP281x_SysCtrl.c
file.*/
    InitSysCtrl();

// HISPCP prescale register settings, normally it will be set to
// default values
    EALLOW; // This is needed to write to EALLOW protected
// registers
    SysCtrlRegs.HISPCP.all = 0x0000; // SYSCLKOUT/1
    EDIS; // This is needed to disable write to EALLOW protected
// registers

// Disable and clear all CPU interrupts:
    DINT;

```

```

        IER = 0x0000;
        IFR = 0x0000;

// Initialize Pie Control Registers To Default State:
// This function is found in the DSP281x_PieCtrl.c file.
    InitPieCtrl();

// Initialize the PIE Vector Table To a Known State:
// This function is found in DSP281x_PieVect.c.
// This function populates the PIE vector table with pointers
// to the shell ISR functions found in DSP281x_DefaultIsr.c.
    InitPieVectTable();
    spi_fifo_init();           //Enable SPI FIFO
    spi_init();               //Enable SPI

// User specific functions, Reassign vectors (optional), Enable
Interrupts:

// Set I/O pins to off to ensure safe start-up of inverter
    EALLOW;                  // Enable EALLOW
    GpioMuxRegs.GPAMUX.all = 0x0000; // Disable PWM1-6
    GpioMuxRegs.GPADIR.all = 0x003F; // Pins 0 5 as O/P
    GpioMuxRegs.GPFMUX.all = 0x0007; // Select GPIOs to be SPI
// pins except LOADDACS
    GpioMuxRegs.GPFDIR.all = 0x0E08; // Set LOADDACS as GPIO
Output
    EDIS;                    // Disable EALLOW
    GpioDataRegs.GPADAT.all = 0x0000; // Zero outputs
    GpioDataRegs.GPFDAT.all = 0x0000; // Zero outputs

// Waiting for enable flag set
    while (EnableFlag==FALSE)
    {
        BackTicker++;
        EnableFlag = !GpioDataRegs.GPFDAT.bit.GPIOF5;
// Set pushbutton as enable
    }

// Initialize EVA Timer 1:
// Setup Timer 1 Registers (EV A)
    EvaRegs.GPTCONA.all = 0;

// Enable Underflow interrupt bits for GP timer 1
    EvaRegs.EVAIMRA.bit.T1UFINT = 1;
    EvaRegs.EVAIFRA.bit.T1UFINT = 1;

// Enable CAP3 interrupt bits for GP timer 2
    EvaRegs.EVAIMRC.bit.CAP3INT = 1;
    EvaRegs.EVAIFRC.bit.CAP3INT = 1;

// Reassign ISRs.
// Reassign the PIE vector for T1UFINT and CAP3INT to point to a
// different ISR then the shell routine found in
// DSP281x_DefaultIsr.c. This is done if the user does not want to
// use the shell ISR routine but instead wants to use their own ISR.

    EALLOW; // This is needed to write to EALLOW protected
// registers
    PieVectTable.T1UFINT = &MainISR;
    PieVectTable.CAPINT3 = &QepISR;
    EDIS; // This is needed to disable write to EALLOW protected
// registers

// Enable PIE group 2 interrupt 6 for T1UFINT

```

```

PieCtrlRegs.PIEIER2.all = M_INT6;

// Enable PIE group 3 interrupt 7 for CAP3INT
PieCtrlRegs.PIEIER3.all = M_INT7;

// Enable CPU INT2 for T1UFINT and INT3 for CAP3INT:
IER |= (M_INT2 | M_INT3);

// Initialize PWM module
pwm1.PeriodMax = SYSTEM_FREQUENCY*1000000*T/2; // Perscaler
// X1 T1), ISR period = T x 1
pwm1.init(&pwm1);

// Initialize DATALOG module
dlog.iptr1 = &DlogCh1;
dlog.iptr2 = &DlogCh2;
dlog.iptr3 = &DlogCh3;
dlog.iptr4 = &DlogCh4;
dlog.trig_value = 0x1;
dlog.prescaler = 1;
dlog.init(&dlog);

// Initialize QEP module
qep1.LineEncoder = 4096;
qep1.MechScaler = _IQ30(0.25/qep1.LineEncoder);
qep1.PolePairs = P/2;
qep1.CalibratedAngle = 2800;
qep1.CsiOffset = 0x0AAB;
qep1.init(&qep1);

// Initialize the Speed module for QEP based speed calculation
speed1.K1 = _IQ21(1/(BASE_FREQ*T));
speed1.K2 = _IQ(1/(1+T*2*PI*30)); // Low-pass cut-off
frequency
speed1.K3 = _IQ(1)-speed1.K2;
speed1.BaseRpm = 120*(BASE_FREQ/P);

// Initialize enable drive module (FOR DMC1500 ONLY)
drv1.init(&drv1);
GpioDataRegs.GPFDAT.all = 0x0000;

// Initialize ADC module
ilg2_vdc1.init(&ilg2_vdc1);

// Initialize average filter
meas1.init(&meas1);

// Initialize the RAMPGEN module
rg1.StepAngleMax = _IQ(BASE_FREQ*T);

// Initialize the RAMPGEN module
rcl.RampDelayMax = 5;

// Initialize the RAMPCNTL module
// scl.RampDelayMax = 5;

// Initialize the PID_REG3 module for Id
pid1_id.Kp = _IQ(0.1);
pid1_id.Ki = _IQ(T/0.02);
pid1_id.Kd = _IQ(0/T);
pid1_id.Kc = _IQ(0.5);
pid1_id.OutMax = _IQ(0.30);
pid1_id.OutMin = _IQ(-0.30);

```

```

// Initialize the PID_REG3 module for Iq
pid1_iq.Kp = _IQ(0.1);
pid1_iq.Ki = _IQ(T/0.02);
pid1_iq.Kd = _IQ(0/T);
pid1_iq.Kc = _IQ(0.5);
pid1_iq.OutMax = _IQ(0.95);
pid1_iq.OutMin = _IQ(-0.95);

// Initialize the PID_REG3 module for speed control
pid1_spd.Kp = _IQ(1);
pid1_spd.Ki = _IQ(T*SpeedLoopPrescaler/0.3);
pid1_spd.Kd = _IQ(0/(T*SpeedLoopPrescaler));
pid1_spd.Kc = _IQ(0.2);
pid1_spd.OutMax = _IQ(1);
pid1_spd.OutMin = _IQ(-1);
SpeedCur = SpeedRef;

// Enable global Interrupts and higher priority real-time debug
events:
    EINT;          // Enable Global interrupt INTM
    ERTM;          // Enable Global realtime interrupt DBGM

// IDLE loop. Just sit and loop forever:
    for(;;) BackTicker++; // Holding loop until enable button
// activated
    }
    interrupt void MainISR(void) // Run main
    {

// Verifying the ISR
    IsrTicker++;

// ***** LEVEL1 *****
#if (BUILDLEVEL==LEVEL1)
// Volt/Hertz with internal position ref
//
// -----
// Set the direction
// -----
    if (Direction == 1)
    {
        SpeedRef = ilg2_vdc1.POT1;          // Potentiometer for
SpeedRef
    }
    else if (Direction == -1)
    {
        SpeedRef = ilg2_vdc1.POT1;
        SpeedRef *= -1;
    }

// -----
// Connect inputs of the RMP module and call the Ramp control
// calculation function.
// -----
    rc1.TargetValue = _IQ15toIQ(SpeedRef);
    rc1.calc(&rc1);

// -----
// Connect inputs of the RAMP GEN module and call the Ramp
// generator calculation function.
// -----
    rg1.Freq = rc1.SetpointValue;
    rg1.calc(&rg1);

```

```

// -----
// Call the ILEG2_VDC read function.
// -----
    ilg2_vdc1.read(&ilg2_vdc1);                // Read ADC

//-----
// Perform measurement averaging.
//-----
    meas1.Meas_A = ilg2_vdc1.ImeasA;    // Average phase A
    meas1.Meas_B = ilg2_vdc1.ImeasB;    // Average phase B
    meas1.calc(&meas1);

// -----
// Connect inputs of the INV_PARK module and call the inverse park
// transformation calculation function.
// -----
    ipark1.Ds = _IQ(VdTesting);          // D component setpoint
    ipark1.Qs = _IQ15toIQ(ilg2_vdc1.POT2); // Pot2 for voltage ref
    ipark1.Angle = rg1.CSI;              // CSI compensated angle
    ipark1.calc(&ipark1);

// -----
// Connect inputs of the SVGEN_DQ module and call the space-
// vector gen. calculation function.
// -----
    svgen_dq1.Ualpha = ipark1.Alpha;
    svgen_dq1.Ubeta = ipark1.Beta;
    svgen_dq1.calc(&svgen_dq1);

// -----
// Connect inputs of the PWM_DRV module and call the PWM signal
// generation update function.
// -----
    pwm1.MfuncC1 = (int16)_IQtoIQ15(svgen_dq1.Ta);
    pwm1.MfuncC2 = (int16)_IQtoIQ15(svgen_dq1.Tb);
    pwm1.MfuncC3 = (int16)_IQtoIQ15(svgen_dq1.Tc);
    pwm1.update(&pwm1);

// -----
// Connect inputs of the DATALOG module
// -----
    DlogCh1 = (int16)_IQtoIQ15(rg1.Out);    // Generated angle
    DlogCh2 = (int16)_IQtoIQ15(rg1.CSI);    // CSI angle
    DlogCh3 = (int16)_IQtoIQ15(svgen_dq1.Ta); // Phase A ref
    DlogCh4 = (int16)(ilg2_vdc1.ImeasA);

//-----
// SPI DAC Output
//-----
    spi_xmit_A((Uint16)_IQtoIQ15(rg1.CSI)); // Position signal
    spi_xmit_B((Uint16)_IQtoIQ15(svgen_dq1.Ta) + 0x8000); // Phase
A // output ref (+DC offset)
    //spi_xmit_C();
    //spi_xmit_d();

#endif // (BUILDLEVEL==LEVEL1)

// ***** LEVEL2 *****
// Volt/Hertz with encoder feedback
//
#if (BUILDLEVEL==LEVEL2)

```

```

// -----
// Call the ILEG2_VDC read function.
// -----
    ilg2_vdc1.read(&ilg2_vdc1);           // Read ADC

//-----
// Perform measurement averaging.
//-----
    meas1.Meas_A = ilg2_vdc1.ImeasA;
    meas1.Meas_B = ilg2_vdc1.ImeasB;
    meas1.calc(&meas1);

// -----
// Connect inputs of the INV_PARK module and call the inverse
// park transformation calculation function.
// -----
    ipark1.Ds = _IQ(VdTesting);
    ipark1.Qs = _IQ15toIQ(ilg2_vdc1.POT2);
    ipark1.Angle = speed1.CsiTheta; // CSI compensated rotor angle
    ipark1.calc(&ipark1);

// -----
// Connect inputs of the SVGEN_DQ module and call the space-
// vector gen. calculation function.
// -----
    svgen_dq1.Ualpha = ipark1.Alpha;
    svgen_dq1.Ubeta = ipark1.Beta;
    svgen_dq1.calc(&svgen_dq1);

// -----
// Connect inputs of the PWM_DRV module and call the PWM signal
// generation update function.
// -----
    pwm1.MfuncC1 = (int16)_IQtoIQ15(svgen_dq1.Ta);
    pwm1.MfuncC2 = (int16)_IQtoIQ15(svgen_dq1.Tb);
    pwm1.MfuncC3 = (int16)_IQtoIQ15(svgen_dq1.Tc);
    pwm1.update(&pwm1);

// -----
// Connect inputs of the DATALOG module
// -----
    DlogCh1 = (int16)_IQtoIQ15(speed1.ElecTheta); // Actual
// motor angle
    DlogCh2 = (int16)_IQtoIQ15(speed1.CsiTheta); // CSI
// compensated angle
    DlogCh3 = (int16)(meas1.Ave_A);
    DlogCh4 = (int16)(meas1.Ave_B);

//-----
// SPI DAC Output
//-----
    spi_xmit_A((Uint16)_IQtoIQ15(speed1.CsiTheta));
    spi_xmit_B((Uint16)_IQtoIQ15(speed1.ElecTheta));
    spi_xmit_C((Uint16)_IQtoIQ15(svgen_dq1.Ta) + 0x8000);
    //spi_xmit_d();

// -----
// Call the QEP_DRV calculation function.
// -----
    qep1.calc(&qep1);

// -----
// Connect inputs of the SPEED_FR module and call the speed
// calculation function

```

```

// -----
speed1.ElecTheta = _IQ15toIQ((int32)qep1.ElecTheta);
speed1.CsiTheta = _IQ15toIQ((int32)qep1.CsiTheta);
speed1.DirectionQep = (int32)(qep1.DirectionQep);
speed1.calc(&speed1);

#endif // (BUILDLEVEL==LEVEL2)

// ***** LEVEL3 *****
#if (BUILDLEVEL==LEVEL3)
// Current control with artificial position ref
// -----
// Set the direction
// -----
if (Direction == 1)
{
    SpeedRef = ilg2_vdc1.POT1; // Potentiometer for SpeedRef
}
else if (Direction == -1)
{
    SpeedRef = ilg2_vdc1.POT1;
    SpeedRef *= -1;
}

// -----
// Connect inputs of the RMP module and call the Ramp control
// calculation function.
// -----
rc1.TargetValue = _IQ15toIQ(SpeedRef);
rc1.calc(&rc1);

// -----
// Connect inputs of the RAMP GEN module and call the Ramp
// generator calculation function.
// -----
rg1.Freq = rc1.SetpointValue;
rg1.calc(&rg1);

// -----
// Call the ILEG2_VDC read function.
// -----
ilg2_vdc1.read(&ilg2_vdc1);

//-----
// Perform measurement averaging.
//-----
meas1.Meas_A = ilg2_vdc1.ImeasA;
meas1.Meas_B = ilg2_vdc1.ImeasB;
meas1.calc(&meas1);

// -----
// Connect inputs of the CLARKE module and call the clarke
// transformation calculation function.
// -----
clarke1.As = _IQ15toIQ((int32)meas1.Ave_A);
clarke1.Bs = _IQ15toIQ((int32)meas1.Ave_B);
clarke1.calc(&clarke1);

// -----
// Connect inputs of the PARK module and call the park
// transformation calculation function.
// -----
park1.Alpha = clarke1.Alpha;

```

```

    park1.Beta = clarkel.Beta;
    park1.Angle = rg1.CSI;
    park1.calc(&park1);

// -----
//   Connect inputs of the PID_REG3 module and call the PID IQ
//   controller calculation function.
// -----
    pid1_iq.Ref = _IQ(IqRef);
    pid1_iq.Fdb = park1.Qs;
    pid1_iq.calc(&pid1_iq);

// -----
//   Connect inputs of the PID_REG3 module and call the PID ID
//   controller calculation function.
// -----
    pid1_id.Ref = _IQ(IdRef);
    pid1_id.Fdb = park1.Ds;
    pid1_id.calc(&pid1_id);

// -----
//   Connect inputs of the INV_PARK module and call the inverse
//   park transformation calculation function.
// -----
    ipark1.Ds = pid1_id.Out;
    ipark1.Qs = pid1_iq.Out;
    ipark1.Angle = rg1.CSI;
    ipark1.calc(&ipark1);

// -----
//   Connect inputs of the SVGEN_DQ module and call the space-
//   vector gen. calculation function.
// -----
    svgen_dq1.Ualpha = ipark1.Alpha;
    svgen_dq1.Ubeta = ipark1.Beta;
    svgen_dq1.calc(&svgen_dq1);

// -----
//   Connect inputs of the PWM_DRV module and call the PWM signal
//   generation update function.
// -----
    pwm1.MfuncC1 = (int16)_IQtoIQ15(svgen_dq1.Ta);
    pwm1.MfuncC2 = (int16)_IQtoIQ15(svgen_dq1.Tb);
    pwm1.MfuncC3 = (int16)_IQtoIQ15(svgen_dq1.Tc);
    pwm1.update(&pwm1);

// -----
//   Connect inputs of the DATALOG module
// -----
    DlogCh1 = (int16)_IQtoIQ15(rg1.CSI);
    DlogCh2 = (int16)_IQtoIQ15(park1.Qs);
    DlogCh3 = (int16)(meas1.Ave_A);
    DlogCh4 = (int16)(meas1.Ave_B);

//-----
//   SPI DAC Output
//-----
    spi_xmit_A((Uint16)_IQtoIQ15(rg1.CSI));
    spi_xmit_B((Uint16)_IQtoIQ15(park1.Qs));
    spi_xmit_C((Uint16)_IQtoIQ15(svgen_dq1.Ta) + 0x8000);
    //spi_xmit_D();

#endif // (BUILDLEVEL==LEVEL3)

```

```

// ***** LEVEL4 *****
#if (BUILDLEVEL==LEVEL4)
// Current control with encoder feedback
// -----
// Call the ILEG2_VDC read function.
// -----
    ilg2_vdc1.read(&ilg2_vdc1);

//-----
// Perform measurement averaging.
//-----
    meas1.Meas_A = ilg2_vdc1.ImeasA;
    meas1.Meas_B = ilg2_vdc1.ImeasB;
    meas1.calc(&meas1);

// -----
// Connect inputs of the CLARKE module and call the clarke
// transformation calculation function.
// -----
    clarkel.As = _IQ15toIQ((int32)meas1.Ave_A);
    clarkel.Bs = _IQ15toIQ((int32)meas1.Ave_B);
    clarkel.calc(&clarkel);

// -----
// Connect inputs of the PARK module and call the park
// transformation calculation function.
// -----
    park1.Alpha = clarkel.Alpha;
    park1.Beta = clarkel.Beta;
    park1.Angle = speed1.ElecTheta;
    park1.calc(&park1);

// -----
// Connect inputs of the PID_REG3 module and call the PID IQ
// controller calculation function.
// -----
    pid1_iq.Ref = _IQ15toIQ(ilg2_vdc1.POT2); // Potentiometer as
// Iq ref
    pid1_iq.Fdb = park1.Qs;
    pid1_iq.calc(&pid1_iq);

// -----
// Connect inputs of the PID_REG3 module and call the PID ID
// controller calculation function.
// -----
    pid1_id.Ref = _IQ(IdRef);
    pid1_id.Fdb = park1.Ds;
    pid1_id.calc(&pid1_id);

// -----
// Connect inputs of the INV_PARK module and call the inverse
// park transformation calculation function.
// -----
    ipark1.Ds = pid1_id.Out;
    ipark1.Qs = pid1_iq.Out;
    ipark1.Angle = speed1.CsiTheta;
    ipark1.calc(&ipark1);

// -----
// Connect inputs of the SVGEN_DQ module and call the space-
// vector gen. calculation function.
// -----
    svgen_dq1.Ualpha = ipark1.Alpha;
    svgen_dq1.Ubeta = ipark1.Beta;

```

```

        svgen_dq1.calc(&svgen_dq1);

// -----
//   Connect inputs of the PWM_DRV module and call the PWM signal
//   generation update function.
// -----
    pwm1.MfuncC1 = (int16)_IQtoIQ15(svgen_dq1.Ta);
    pwm1.MfuncC2 = (int16)_IQtoIQ15(svgen_dq1.Tb);
    pwm1.MfuncC3 = (int16)_IQtoIQ15(svgen_dq1.Tc);
    pwm1.update(&pwm1);

// -----
//   Connect inputs of the DATALOG module
// -----
    DlogCh1 = (int16)_IQtoIQ15(speed1.ElecTheta);
    DlogCh2 = (int16)_IQtoIQ15(park1.Qs);
    DlogCh3 = (int16)(meas1.Ave_A);
    DlogCh4 = (int16)(meas1.Ave_B);

//-----
//   SPI DAC Output
//-----
    spi_xmit_A((Uint16)_IQtoIQ15(speed1.ElecTheta));
    spi_xmit_B((Uint16)_IQtoIQ15(svgen_dq1.Ta) + 0x8000);
    //spi_xmit_C();
    //spi_xmit_D();

// -----
//   Call the QEP_DRV calculation function.
// -----
    qep1.calc(&qep1);

// -----
//   Connect inputs of the SPEED_FR module and call the speed
//   calculation function
// -----
    speed1.ElecTheta = _IQ15toIQ((int32)qep1.ElecTheta);
    speed1.CsiTheta = _IQ15toIQ((int32)qep1.CsiTheta);
    speed1.DirectionQep = (int32)(qep1.DirectionQep);
    speed1.calc(&speed1);

#endif    // (BUILDLEVEL==LEVEL4)

// ***** LEVEL5 *****
#if (BUILDLEVEL==LEVEL5)
// Speed control
// -----
//   Call the ILEG2_VDC read function.
// -----
    ilg2_vdc1.read(&ilg2_vdc1);

// -----
//   Set the direction
// -----
    SpeedRef = ilg2_vdc1.POT1;
    if (Direction == -1)
    {
        SpeedRef *= -1;
    }

//-----

```

```

// Perform measurement averaging.
//-----
meas1.Meas_A = ilg2_vdc1.ImeasA;
meas1.Meas_B = ilg2_vdc1.ImeasB;
meas1.calc(&meas1);

//-----
// Connect inputs of the CLARKE module and call the clarke
// transformation calculation function.
//-----
clarke1.As = _IQ15toIQ((int32)meas1.Ave_A);
clarke1.Bs = _IQ15toIQ((int32)meas1.Ave_B);
clarke1.calc(&clarke1);

//-----
// Connect inputs of the PARK module and call the park
// transformation calculation function.
//-----
park1.Alpha = clarke1.Alpha;
park1.Beta = clarke1.Beta;
park1.Angle = speed1.ElecTheta;
park1.calc(&park1);

//-----
// Connect SpeedRefRamp and call the calculation function
//-----
rc1.TargetValue = _IQ15toIQ(SpeedRef); //Ramp limit the ref
rc1.calc(&rc1);

//-----
// Connect inputs of the PID_REG3 module and call the PID speed
// controller calculation function.
//-----
if (SpeedLoopCount==SpeedLoopPrescaler) // Execute speed
// loop every 1 in X loops
{
    pid1_spd.Ref = rc1.SetpointValue;
    pid1_spd.Fdb = speed1.Speed;
    pid1_spd.calc(&pid1_spd);
    SpeedLoopCount=1;
}
else SpeedLoopCount++;

//-----
// Connect inputs of the PID_REG3 module and call the PID IQ
// controller calculation function.
//-----
pid1_iq.Ref = pid1_spd.Out;
pid1_iq.Fdb = park1.Qs;
pid1_iq.calc(&pid1_iq);

//-----
// Connect inputs of the PID_REG3 module and call the PID ID
// controller calculation function.
//-----
pid1_id.Ref = _IQ(IdRef);
pid1_id.Fdb = park1.Ds;
pid1_id.calc(&pid1_id);

//-----
// Connect inputs of the INV_PARK module and call the inverse
// park transformation calculation function.
//-----
ipark1.Ds = pid1_id.Out;

```

```

    ipark1.Qs = pid1_iq.Out;
    ipark1.Angle = speed1.CsiTheta;
    ipark1.calc(&ipark1);

// -----
//   Connect inputs of the SVGEN_DQ module and call the space-
//   vector gen. calculation function.
// -----
    svgen_dq1.Ualpha = ipark1.Alpha;
    svgen_dq1.Ubeta = ipark1.Beta;
    svgen_dq1.calc(&svgen_dq1);

// -----
//   Connect inputs of the PWM_DRV module and call the PWM signal
//   generation update function.
// -----
    pwm1.MfuncC1 = (int16)_IQtoIQ15(svgen_dq1.Ta);
    pwm1.MfuncC2 = (int16)_IQtoIQ15(svgen_dq1.Tb);
    pwm1.MfuncC3 = (int16)_IQtoIQ15(svgen_dq1.Tc);
    pwm1.update(&pwm1);

// -----
//   Connect inputs of the DATALOG module
// -----
    DlogCh1 = (int16)_IQtoIQ15(speed1.ElecTheta);
    DlogCh2 = (int16)_IQtoIQ15(park1.Qs);
    DlogCh3 = (int16)meas1.Ave_A;
    DlogCh4 = (int16)_IQtoIQ15(pid1_spd.Err);

//-----
//   SPI DAC Output
//-----
    spi_xmit_A((Uint16)_IQtoIQ15(speed1.ElecTheta));
    spi_xmit_B((Uint16)_IQtoIQ15(svgen_dq1.Ta) + 0x8000);
    //spi_xmit_C();
    //spi_xmit_D();

// -----
//   Call the QEP_DRV calculation function.
// -----
    qep1.calc(&qep1);

// -----
//   Connect inputs of the SPEED_FR module and call the speed
//   calculation function
// -----
    speed1.ElecTheta = _IQ15toIQ((int32)qep1.ElecTheta);
    speed1.CsiTheta = _IQ15toIQ((int32)qep1.CsiTheta);
    speed1.DirectionQep = (int32)(qep1.DirectionQep);
    speed1.calc(&speed1);

#endif    // (BUILDLEVEL==LEVEL5)

// -----
//   Call the DATALOG update function.
// -----
    dlog.update(&dlog);

// Enable more interrupts from this timer
    EvaRegs.EVAIMRA.bit.T1UFINT = 1;

// Note: To be safe, use a mask value to write to the entire
// EVAIFRA register. Writing to one bit will cause a read-modify-

```

```

// write operation that may have the result of writing 1's to clear
// bits other than those intended.
    EvaRegs.EVAIFRA.all = BIT9;

// Acknowledge interrupt to receive more interrupts from PIE group 2
    PieCtrlRegs.PIEACK.all |= PIEACK_GROUP2;

// -----
//   Connect inputs of the EN_DRV module and call the
//   enable/disable PWM signal
// -----
    EnableFlag = !GpioDataRegs.GPFDAT.bit.GPIOF5;
    drv1.EnableFlag = EnableFlag;
    drv1.update(&drv1);
}

interrupt void QepISR(void)
{
// -----
//   Call the QEP_DRV isr function.
// -----
    qep1.isr(&qep1);

// Enable more interrupts from this timer
    EvaRegs.EVAIMRC.bit.CAP3INT = 1;

// Note: To be safe, use a mask value to write to the entire
// EVAIFRC register. Writing to one bit will cause a read-modify-
// write operation that may have the result of writing 1's to clear
// bits other than those intended.
    EvaRegs.EVAIFRC.all = BIT2;

// Acknowledge interrupt to receive more interrupts from PIE group 3
    PieCtrlRegs.PIEACK.all |= PIEACK_GROUP3;
}

//=====
// No more.
//=====

```

C.3 CSI Offset

```

/*=====
File name:          F281XQEP.C

Description:       This file contains source for the QEP drivers for the
                  F281X

Originator:       Digital Control Systems Group Texas Instruments

Target:           TMS320F281x family
=====

```

History:

04-15-2005 Version 3.20: Using DSP281x v. 1.00 or higher
2008: Modified for CSI operation at UoM - Do not use on standard inverter
-----*/

```
#include "DSP281x_Device.h"
#include "f281xqep.h"

void F281X_EV1_QEP_Init(QEP *p)
{
    EvaRegs.CAPCONA.all = QEP_CAP_INIT_STATE; // Set up capture units
    EvaRegs.T2CON.all = QEP_TIMER_INIT_STATE; // Set up capture timer
    EvaRegs.T2PR = 4*p->LineEncoder; // Init Timer 1 period Register
    EvaRegs.EVAIFRC.bit.CAP3INT = 1; // Clear CAP3 flag
    EvaRegs.EVAIMRC.bit.CAP3INT = 1; // Enable CAP3 Interrupt

    EALLOW; // Enable EALLOW
    GpioMuxRegs.GPAMUX.all |= 0x0700; // Set up the capture pins to
// primary functions
    EDIS; // Disable EALLOW
}

void F281X_EV1_QEP_Calc(QEP *p)
{
    int32 Tmp;

    // Check the rotational direction
    p->DirectionQep = 0x4000&EvaRegs.GPTCONA.all;
    p->DirectionQep = p->DirectionQep>>14;

    // Check the timer 2 counter for QEP
    p->RawTheta = EvaRegs.T2CNT + p->CalibratedAngle;

    // Compute the mechanical angle in Q15
    Tmp = __qmpy32by16(p->MechScaler,p->RawTheta,31); // Q15 = Q30*Q0
    p->MechTheta = (int16)(Tmp); // Q15 -> Q15
    p->MechTheta &= 0x7FFF; // Wrap around 0x07FFF

    // Compute the electrical angle in Q15
    p->ElecTheta = p->PolePairs*p->MechTheta; // Q0*Q15 = Q15
    p->ElecTheta &= 0x7FFF; // Wrap around 0x07FFF

    // Compute electrical offset in Q15
    p->CsiTheta = p->ElecTheta + p->CsiOffset;
    p->CsiTheta &= 0x7FFF;
}

void F281X_EV1_QEP_Isr(QEP *p)
{
    p->QepCountIndex = EvaRegs.T2CNT; // Get the timer 2 counter for
// one mechanical revolution
    EvaRegs.T2CNT = 0; // Reset the timer 2 counter
    p->IndexSyncFlag = 0x00F0; // Set the index flag
}
```

C.4 Measurement Filter

```
/*=====
File name:      mov_av.C

Description:    This file contains source for a moving average filter

Originator:    S Woolaghan, UoM

Target:        TMS320F281x family

=====
History:
-----
DEC-2007 Version 1.0: Original version for window of 8 values
-----*/

#include "DSP281x_Device.h"
#include "mov_av.h"

void mov_av_init(MEAS_ARRAY *p)
{
    p->n_ptr = 0;
}

void mov_av_calc(MEAS_ARRAY *p)
{
    p->Meas_A_array[p->n_ptr] = (p->Meas_A >> 3);
    p->Ave_A = p->Meas_A_array[0] + p->Meas_A_array[1] + \
        p->Meas_A_array[2] + p->Meas_A_array[3] + \
        p->Meas_A_array[4] + p->Meas_A_array[5] + \
        p->Meas_A_array[6] + p->Meas_A_array[7];
    p->Meas_B_array[p->n_ptr] = (p->Meas_B >> 3);
    p->Ave_B = p->Meas_B_array[0] + p->Meas_B_array[1] + \
        p->Meas_B_array[2] + p->Meas_B_array[3] + \
        p->Meas_B_array[4] + p->Meas_B_array[5] + \
        p->Meas_B_array[6] + p->Meas_B_array[7];
    p->n_ptr = (p->n_ptr + 1) % 8;
}
}
```